FIR Filter HAS

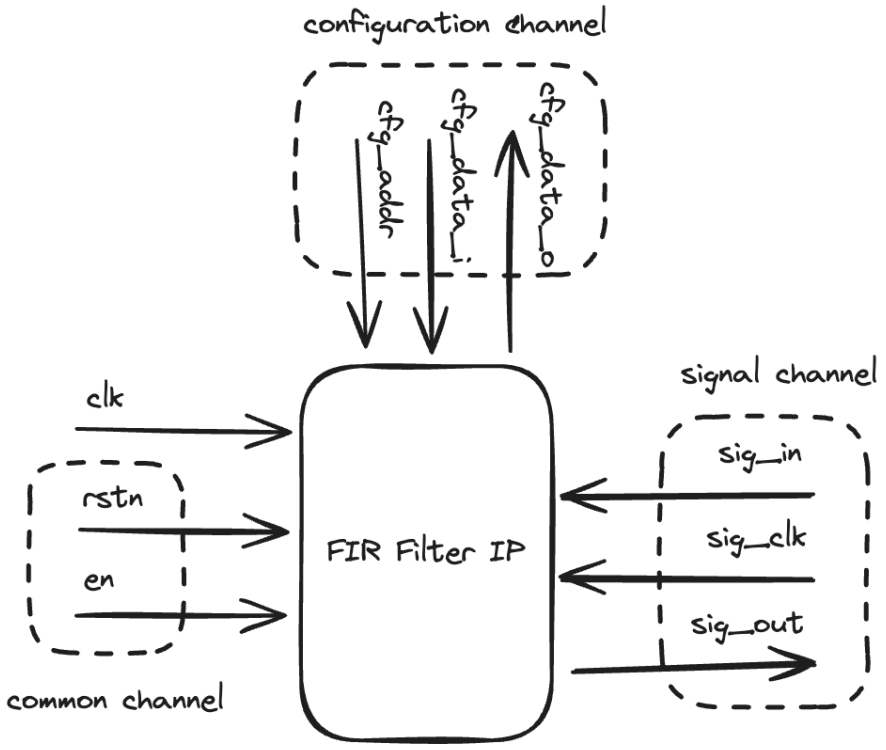
Overview

This IP core is a 4-tap Finite Impulse Response (FIR) filter, designed to process digital input signals with a fixed set of coefficients. It includes a UART (Universal Asynchronous Receiver-Transmitter) interface for debugging and monitoring purposes, enabling real-time adjustment and inspection of the filter parameters.

Features

1. 4-Tap FIR Filter: A fixed-length filter that processes input data with 4 filter coefficients.
2. Encoding: 8-bit signed fixed point encoding with 6 fractional bits
3. Coefficient Interface: Enables loading of filter coefficients dynamically through the UART interface.
4. Data Width: Fixed data width of 8 bits for both input and output.
5. Clocking: Operates based on a single input clock.
6. Supports reset signal to initialize the filter state.
7. Debugging: UART debug interface allows for input signal injection, access to internal state, and output signal dumping

Block Diagram



Interface Signals

Name	Dimension	Description
clk	1-bit	Clock signal for the IP’s control
en	1-bit	Enable signal, active high
rstn	1-bit	Global reset signal, active low
cfg_addr	8-bit	Address line to access the IP’s registers
cfg_data_i	32-bit	Data input line for the IP’s registers
cfg_data_o	32-bit	Data output line for the IP’s registers
sig_clk	1-bit	Clock signal for sampling the input signal
sig_in	8-bit	Input signal for the filter
sig_out	8-bit	Output signal of the filter

IP Registers

Control and Status Register (CSR, address 0x0)

Name	Position	Access	Description
FEN	[0:0]	R/W	Filter enable, when disabled, input signal will not get filtered 0: disabled 1: enabled
C0EN	[1:1]	R/W	Coefficient 0 enable. When disabled, coefficient 0 will not be used in the filter 0 : disabled 1: enabled
C1EN	[2:2]	R/W	Coefficient 1 enable. When disabled, coefficient 0 will not be used in the filter 0 : disabled 1: enabled
C2EN	[3:3]	R/W	Coefficient 2 enable. When disabled, coefficient 0 will not be used in the filter 0 : disabled 1: enabled
C3EN	[4:4]	R/W	Coefficient 3 enable. When disabled, coefficient 0 will not be used in the filter

			0 : disabled 1: enabled
HALT	[5:5]	R/W	Halt, will halt the filter if enabled. Any incoming data will be stored in the filter's input buffer. Input signal data will be discarded if the filter overflows.
STS	[7:6]	R/W	Filter state: 0 : IDLE 1 : HALTED 2 : FILTERING 3 : RSVD
IBCNT	[15:8]	RO	Input buffer count. Shows how many entry are in the input signal buffer
IBOVF	[16:16]	RO	Input buffer overflow. Shall be set to 1 if the input buffer ever overflows. Will reset upon the assertion of the global reset signal or input buffer clear field.
IBCLR	[17:17]	R/W1C	Input buffer clear. Will clear the input buffer when 1 is written to it.
TCLR	[18:18]	R/W1C	Tap clear. Will clear the filter taps when 1 is written to it.
RND	[20:19]	R/W	Rounding mechanism. 0 : Round down 1: Round up 2: Round 3: RSVD
ICOEF	[21:21]	RO	Invalid coefficient flag. Will be set to 1 if the sum of enabled coefficients are > 1.
ICAP	[22:22]	RO	Invalid cap flag. Will be set to 1 if the COEF.HCAP < COEF.LCAP
RSVD	[31:23]	RO	Reserved

Coefficients Register (COEF, address 0x4)

Name	Position	Access	Description
C0	[7:0]	RW	Coefficient 0 value
C1	[15:8]	RW	Coefficient 1 value
C2	[23:16]	RW	Coefficient 2 value
C3	[31:24]	RW	Coefficient 3 value

Output Capping Register (OUTCAP, address 0x8)

Name	Position	Access	Description
HCAP	[7:0]	RW	High output value cap
LCAP	[15:8]	RW	Low output value cap
RSVD	[31:16]	RO	Reserved

Usage Guide

Power on Reset (POR)

The registers in the IP will be set to a predefined value upon power-on as shown by the table below. **Note: use the below table as the source of truth for the POR register values, the latest golden model may not represent this state**.

Register	Name	Position	POR Value
CSR	FEN	[0:0]	0x1
CSR	C0EN	[1:1]	0x1
CSR	C1EN	[2:2]	0x1
CSR	C2EN	[3:3]	0x1
CSR	C3EN	[4:4]	0x0
CSR	HALT	[5:5]	0x0
CSR	STS	[7:6]	0x0
CSR	IBCNT	[15:8]	0x00
CSR	IBOVF	[16:16]	0x0
CSR	IBCLR	[17:17]	N/A
CSR	TCLR	[18:18]	N/A
CSR	RND	[20:19]	0x2
CSR	ICOEF	[21:21]	0x0
CSR	ICAP	[22:22]	0x0
CSR	RSVD	[31:23]	N/A

COEF	C0	[7:0]	0x00
COEF	C1	[15:8]	0x40
COEF	C2	[23:16]	0x00
COEF	C3	[31:24]	0x00
OUTCAP	HCAP	[7:0]	0x40
OUTCAP	LCAP	[15:8]	0xC0
OUTCAP	RSVD	[31:16]	N/A

IP Configuration

To ensure predictable behaviour, any configuration to the IP must be done when it is in the HALTED state. This can be done by setting the CSR.HALT field to 1. The software can then verify the state of the IP by checking the CSR.STS field is equal to 3. Any configuration (ex: filter coefficients, high and low caps, coefficient enable, etc.) can then be done safely. To further ensure predictable behaviour, the software may also clear the input signal buffer and the filter taps by setting the appropriate registers.

Note that there is a requirement for the filter coefficients which is not enforced by the hardware. The sum of all enabled filter coefficients must be less than or equal to 1. It is up to the software to enforce this rule in order to avoid overflow within the IP’s processing elements.

Running the Filter

Digital signal filtering with this IP can only be done when it is not in the HALTED state and when FEN is enabled. It is recommended to clear the filter taps after reconfiguring the filter coefficients by setting the TCLR field. If the IP is not in HALTED and FEN is disabled, the IP will bypass filtering and output of the signal channel will be an identical copy of its input signal. If signals are driven when the IP is in the halted state, the IP will not return a valid output on its signal channel. Input signals that are sampled when the IP is in the HALTED state will be stored in its internal buffer.