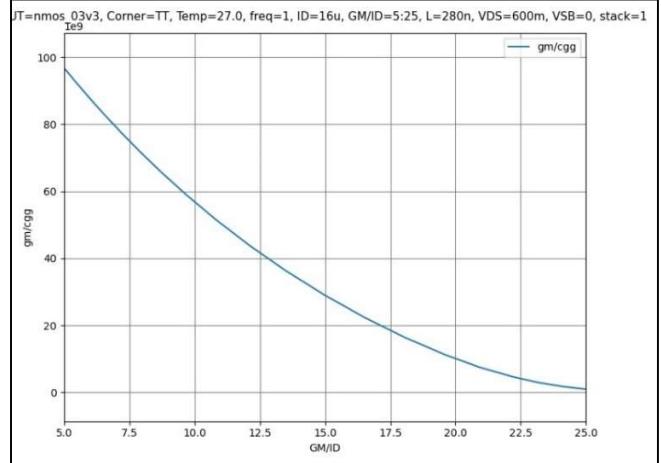
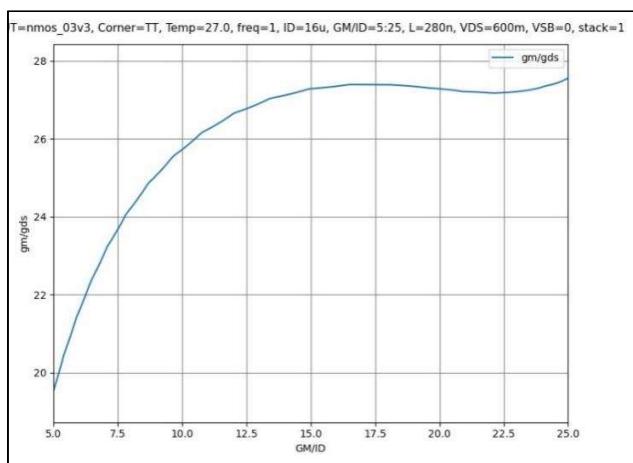
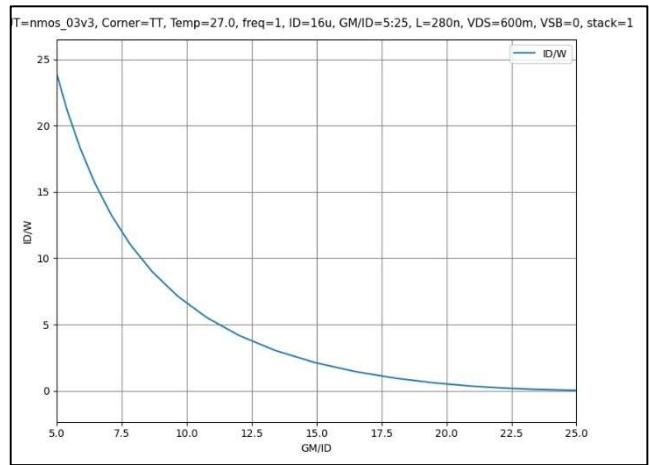
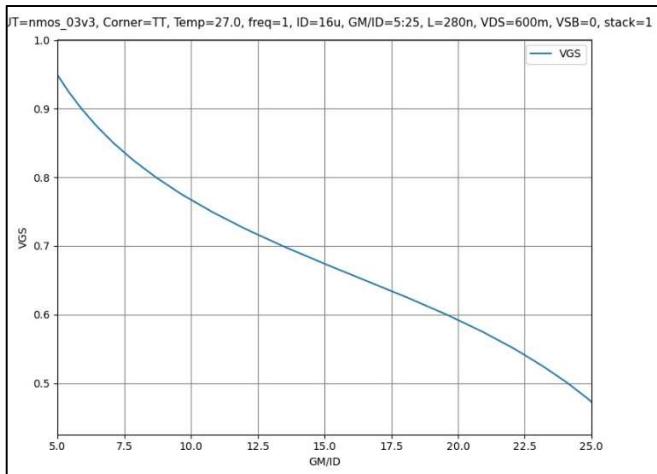


Mini Project 2_(Lab 11)

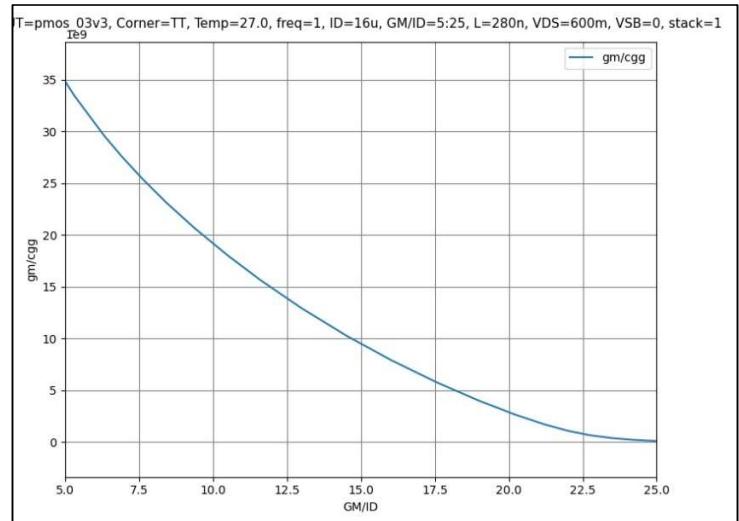
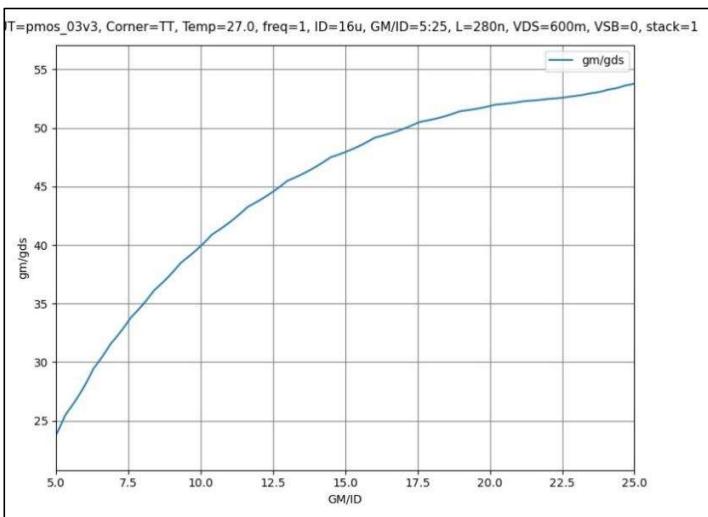
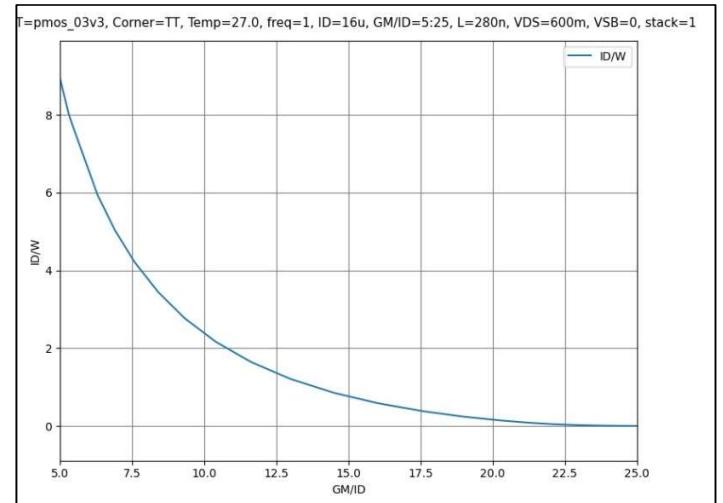
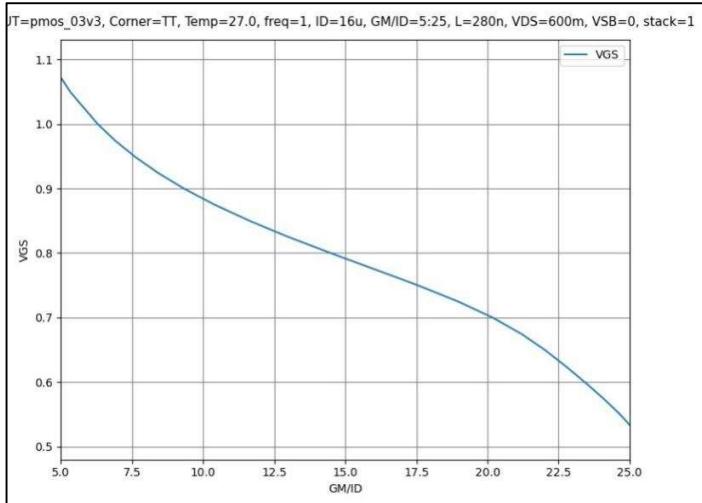
Fully-Differential Folded Cascode OTA

PART 1: gm/ID Design Charts

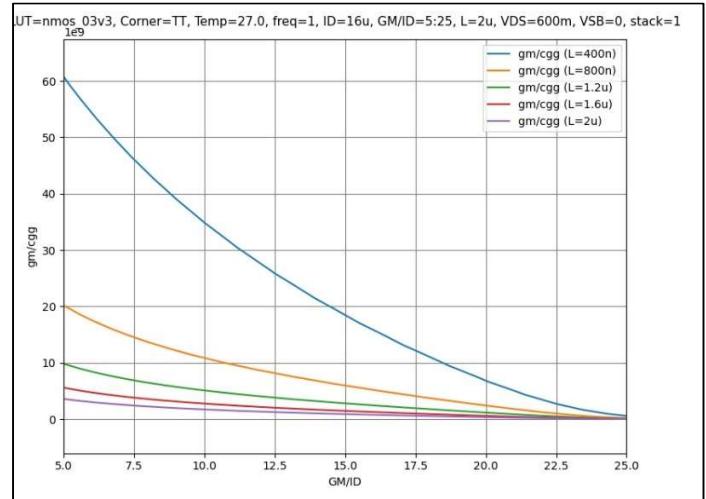
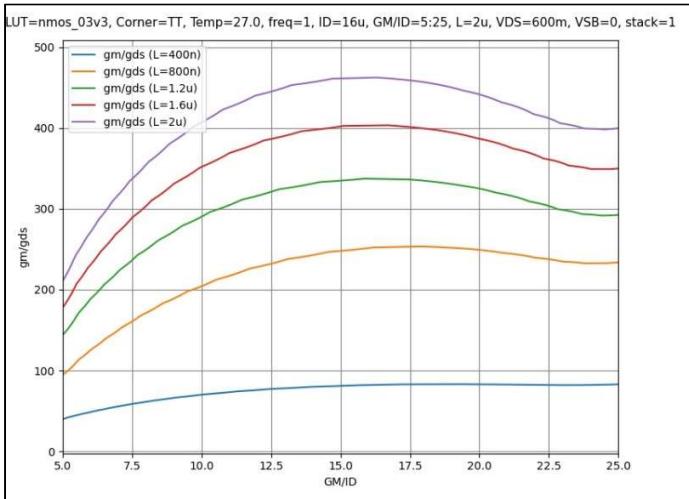
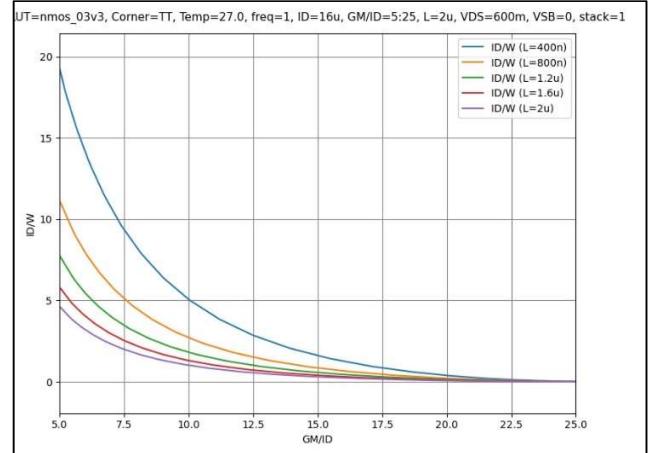
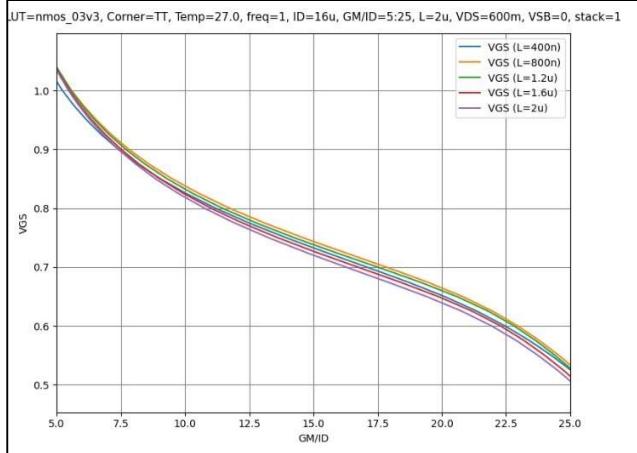
NMOS at L = min (0.28u)



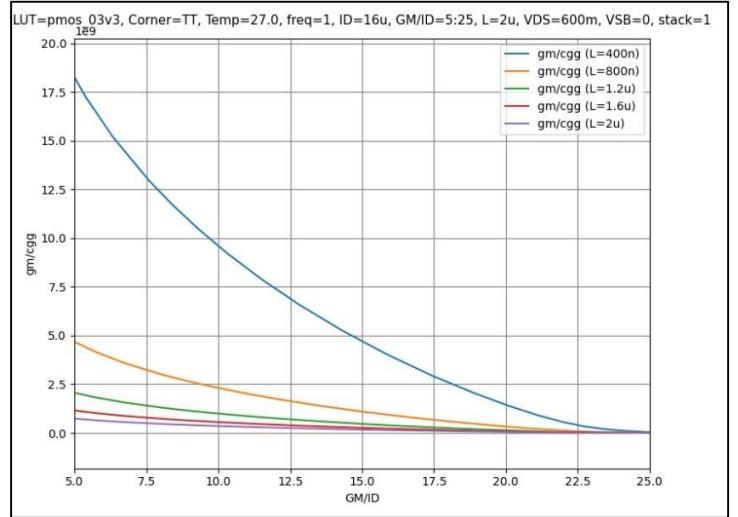
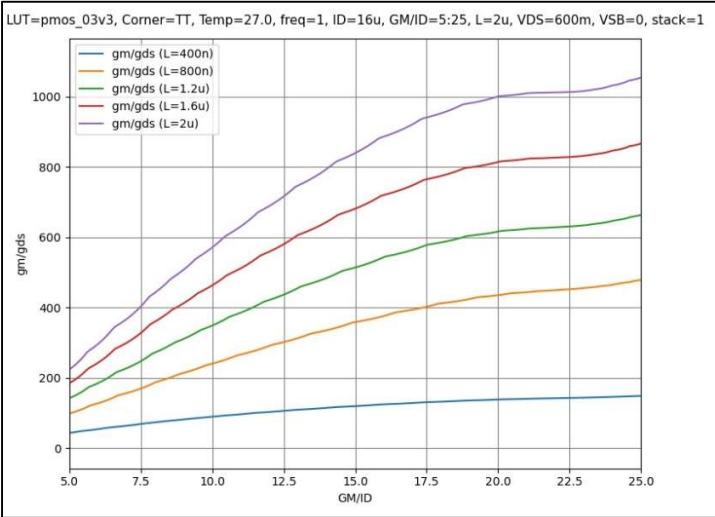
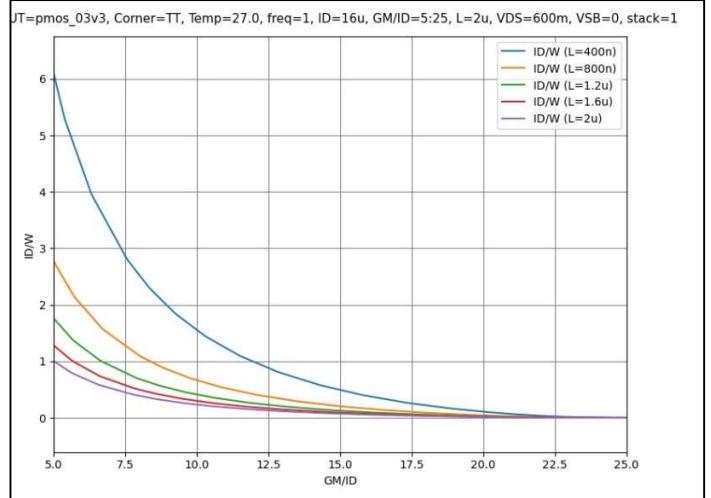
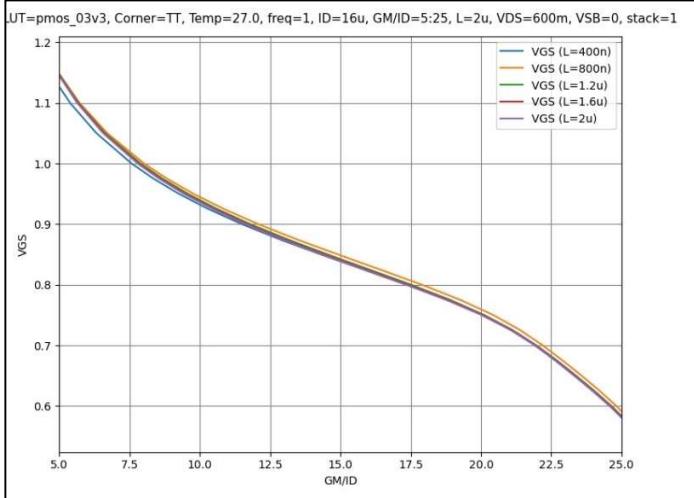
PMOS at L = min (0.28u)



NMOS at L= 1u:1u:5u



PMOS at L= 1u:1u:5u



PART 2: Design

(1)OTA Design

We want to design a fully differential folded cascode OTA with the following specs:

- **Supply voltage:** 2.5V
- **Closed loop gain:** 2
- **Phase margin at required ACL** ≥ 70 deg
- **CMIR – high** ≥ 1 V
- **CMIR – low** ≤ 0 V
- **Differential output swing:** 1.2 V pk to pk
- **Load:** 500fF
- **DC loop gain:** 60 dB
- **Settling time for 1% error:** 100 ns

1) PMOS Input Pair(M6,M7)

$$STcl = \ln\left(\frac{0.99}{0.01}\right) \tau cl = 4.6 \tau cl = 100n \rightarrow \tau cl = 21.76ns$$

$$BWcl = \frac{1}{2\pi\tau cl} = 7.3MHz \quad (Cf = 1pF \text{ and } Cin = 2pF , Cl = 0.5pF)$$

$$\beta = \frac{Cf}{Cf + Cin + CQTAin} = \frac{1}{3} \text{ (neglecting COTA, in which frequency dependent)}$$

$$LG = 60dB = 1000 \rightarrow AOL = \frac{LG}{\beta} = 3000 , BWol = \frac{BWcl}{1 + LG} = 7.3KHz$$

$$GBW = AOL * BWol = 21.9MHz$$

$$Cout = Cl + (Cf||Cin) = 1.2pF$$

$$GBW = \frac{gm, ip}{2\pi C_{out}} \rightarrow gm, ip \geq 165u \rightarrow gm, ip = 185uS \text{ (some margin to increase BW)}$$

$$\text{use } \frac{gm}{ID} = 18.5 \rightarrow ID = 10uA$$

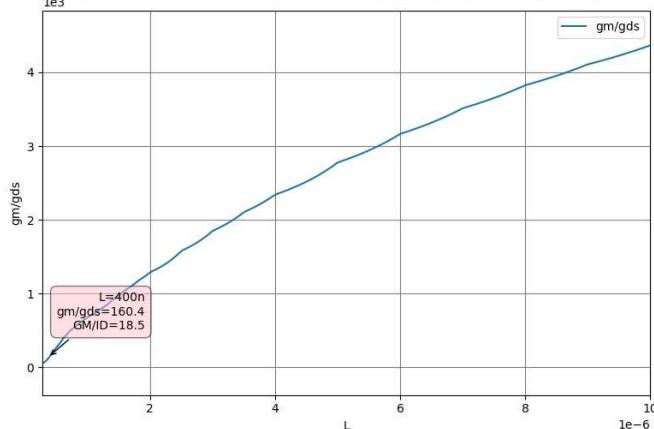
$$AOL = gm, ip * Rout \rightarrow Rout = 16.2Mohms$$

We'll make a rough estimate that CG PMOS and CG NMOS have same gm = 150uS

(because will use $\frac{gm}{ID} = 15$ and ID = 10uA) and all of them have same ro

$$Rout = \frac{gm \cdot C_{out} \cdot ro^2}{4} \rightarrow ro = 657.6Kohms \rightarrow gm \cdot ro \geq 122$$

T=pmos_03v3, Corner=TT, Temp=27.0, freq=1, ID=10u, GM/ID=18.5, L=min:max, VDS=1, VSB=0, stack=1



ID	10u
gm/ID	18.5
L	400n
VDS	1
VSB	0
Stack	1

Results:

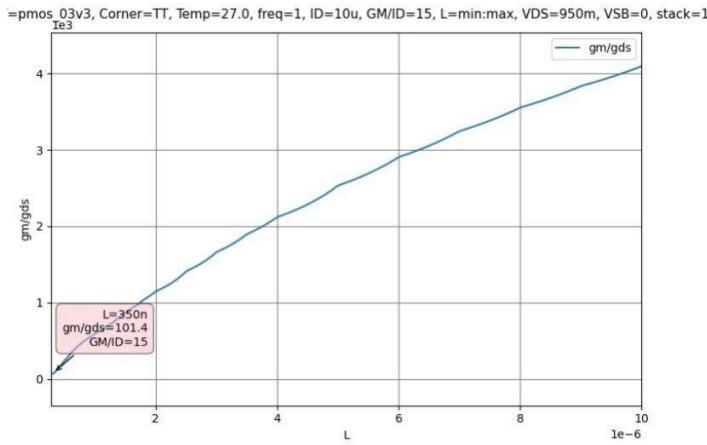
	Name	TT-27.0
1	ID	10u
2	IG	N/A
3	L	400n
4	W	52.82u
5	VGS	780.1m
6	VDS	1
7	VSB	0

L = 400n

W = 52.8u

2) PMOS CG(M13,M14)

We said above we'll use $gm/ID = 15$, $ID = 10\mu$ and $gm/gds \geq 98$



LUT Settings

ID	10u
gm/ID	15
L	350n
VDS	0.95
VSB	0
Stack	1

Results:

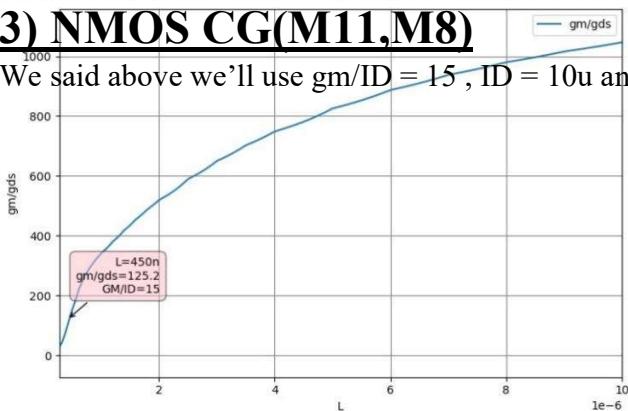
	Name	TT-27.0
1	ID	10u
2	IG	N/A
3	L	350n
4	W	17.01u
5	VGS	824.6m
6	VDS	950m
7	VSB	0

L = 350n
W = 17u

JT=nmos_03v3, Corner=TT, Temp=27.0, freq=1, ID=10u, GM/ID=15, L=min:max, VDS=950m, VSB=0, stack=1

3) NMOS CG(M11,M8)

We said above we'll use $gm/ID = 15$, $ID = 10\mu$ and $gm/gds \geq 98$



LUT Settings

ID	10u
gm/ID	15
L	450n
VDS	0.95
VSB	0.3
Stack	1

Results:

	Name	TT-27.0
1	ID	10u
2	IG	N/A
3	L	450n
4	W	6.8u
5	VGS	836.5m
6	VDS	950m
7	VSB	300m

L = 450n

W = 6.8u

4) PMOS CM

We 'll use gm/ID = 10 and L=1.2u (because we want to reduce mirroring mismatch), ID = 10uA

Diode Connected(M5)

L = 1.2u

W= 12.33 with m = 2

We'll do 1:1 mirroring, so other PMOS CM(M2,M3,M4),ID=10uA

L = 1.2u

W= 12.33u with m = 2

LUT Settings	
ID	10u
gm/ID	10
L	1.2u
VDS	0.3
VSB	0
Stack	1
Results:	
Name	TT-27.0
1 ID	10u
2 IG	N/A
3 L	1.2u
4 W	24.67u
5 VGS	940.8m
6 VDS	300m
7 VSB	0

5) NMOS CM

We 'll use gm/ID = 10 and L=1.2u (because we want to reduce mirroring mismatch), ID = 10uA

Diode Connected(M12)

L = 1.2u

W= 5.57u with m = 1

We'll do 1:2 mirroring, so other NMOS CM(M9,M10),ID=20uA

L = 1.2u

W= 5.57u with m = 2

LUT Settings	
ID	10u
gm/ID	10
L	1.2u
VDS	0.3
VSB	0
Stack	1
Results:	
Name	TT-27.0
1 ID	10u
2 IG	N/A
3 L	1.2u
4 W	5.57u
5 VGS	833.6m
6 VDS	300m
7 VSB	0

5) PMOS Tail Current Source(M1)

We 'll use $gm/ID = 10$ and $L=1.2\mu$ (because we want to reduce mirroring mismatch), $ID = 20\mu A$

$L = 1.2\mu$

$W= 11.6\mu$ with $m = 4$

LUT Settings

ID	20 μ
gm/ID	10
L	1.2 μ
VDS	1.2
VSB	0
Stack	1

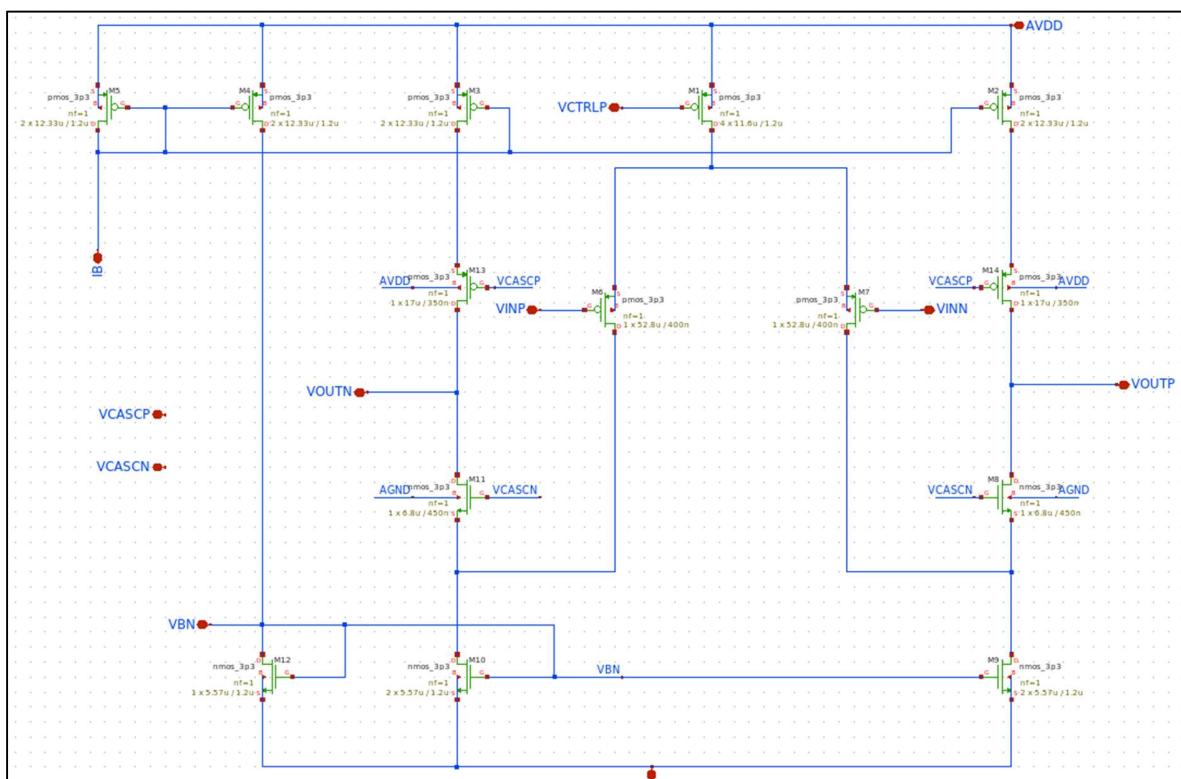
Results:

	Name	TT-27.0
1	ID	20 μ
2	IG	N/A
3	L	1.2 μ
4	W	47.82 μ
5	VGS	941.3m
6	VDS	1.2
7	VSB	0

$$VCASN = VGSN_{cg} + V^* = 836.5m + 300m = 1.1365 \approx 1.14$$

$$VCASP = VDD - VGSP_{cg} - V^* = 2.5 - 824.6m - 300m = 1.13754 \approx 1.375$$

OTA Sizing



(2)CMFB Design

Current Budget of CMBF is half of OTA, I'll use 5uA in each branch

1)Error Amplifier

1-PMOS Diode connected load(M1,M2)

same L and gm/ID of OTA PMOS Tail Current Source

ID=5uA which is quarter current , which means we'll use quarter width

L = 1.2u

W= 11.96 with m = 1

LUT Settings	
ID	5u
gm/ID	10
VDS	0.95
VSB	0
Stack	1
Results:	
Name	TT-27.0
1 ID	5u
2 IG	N/A
3 L	1.2u
4 W	2.73u
5 VGS	833.1m
6 VDS	950m
7 VSB	0

2-NMOS Input pair(M3,M4)

We'll use gm/ID = 10 , L=1.2u , I = 5uA

L = 1.2u

W= 2.73u with m = 1

3-NMOS CM(M5)

same L and gm/ID of OTA NMOS Diode connected CM

ID=10uA which is half current , which means we'll half width

L = 1.2u

W= 5.57u with m = 1, W is fine tuned to 5.8u to reduce error

2) PMOS Buffer stage

1-PMOS Load(M6,M7)

same L and gm/ID of OTA PMOS Diode connected CM

ID=5uA which is half current , which means we'll use half width

LUT Settings	
ID	5u
gm/ID	15
L	1.2u
VDS	0.95
VSB	0
Stack	1

Results:

Name	TT-27.0
1 ID	5u
2 IG	N/A
3 L	1.2u
4 W	39.78u
5 VGS	844.1m
6 VDS	950m
7 VSB	0

L = 1.2u

W= 12.33 with m = 1

2-CD PMOS(M8,M9)

We'll use gm/ID = 15 , L=1.2u , I = 5uA

L = 1.2u

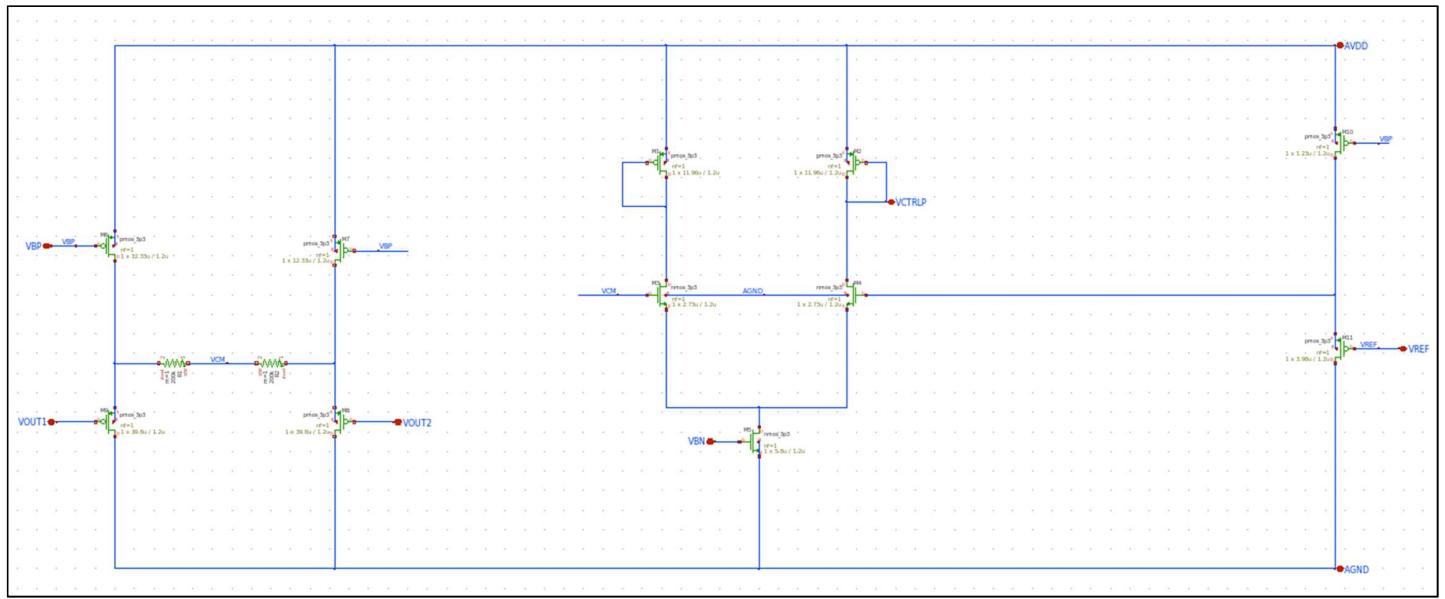
W= 39.8u with m = 1

3-Sesing Resistance

We'll use 200k not 50k

I also added an identical CD to that used to buffer VOUTP and VOUTN to shift the VREF instead of doing it manually. This allows tracking of VREF with VOUTP and VOUTN across PVT and hence keeping the VOUT,CM constant.

CMFB Sizing



(3) Biasing Circuit Design

as we calculated above that

$$VCASN = 1.14$$

$$VCASP = 1.375$$

To avoid high power consumption, we'll use $I = 1\text{uA}$ instead of 10uA , so mirroring is done 10:1

1) VCASN Circuit

1-PMOS CM(M13)

$$L = 1.2\mu$$

$$W = 1.23 \text{ with } m = 2$$

2-NMOS Diode Connected(M11)

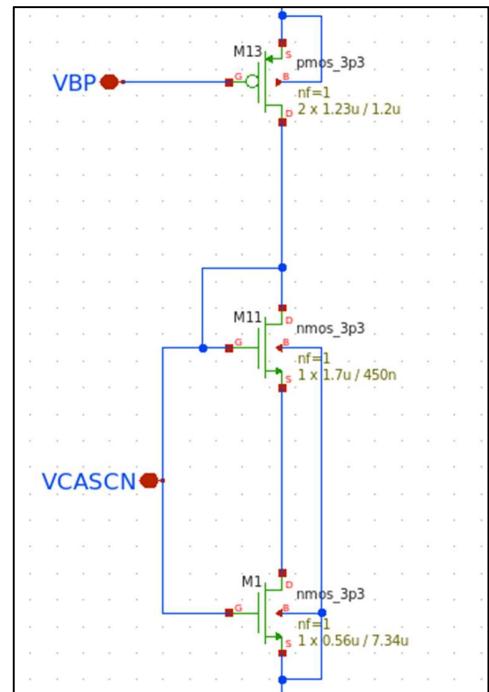
$$L = 450\text{n}$$

$$W = 1.7\mu \text{ with } m = 1$$

3-NMOS Stack(M1)

$$L = 7.34\mu$$

$$W = 0.56\mu \text{ with } m = 1$$



We finely tuned L (because it's more effective than W) until we reached our desired VCASNC

2) VCASP Circuit

1-NMOS CM(M4)

L = 1.2u

W= 0.56u with m = 1

2-PMOS Diode Connected(M3)

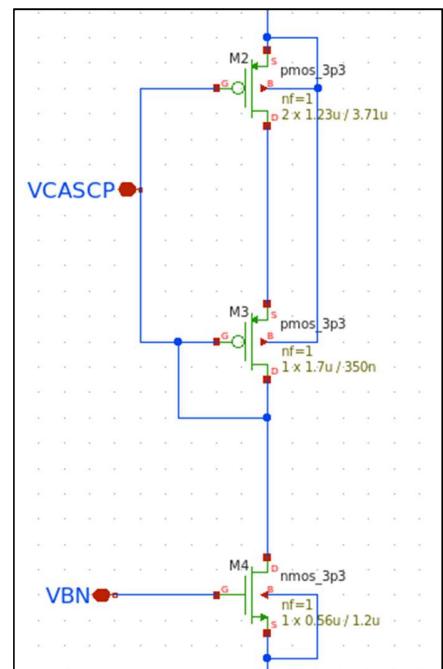
L = 350n

W= 1.7u with m = 1

3-PMOS Stack(M2)

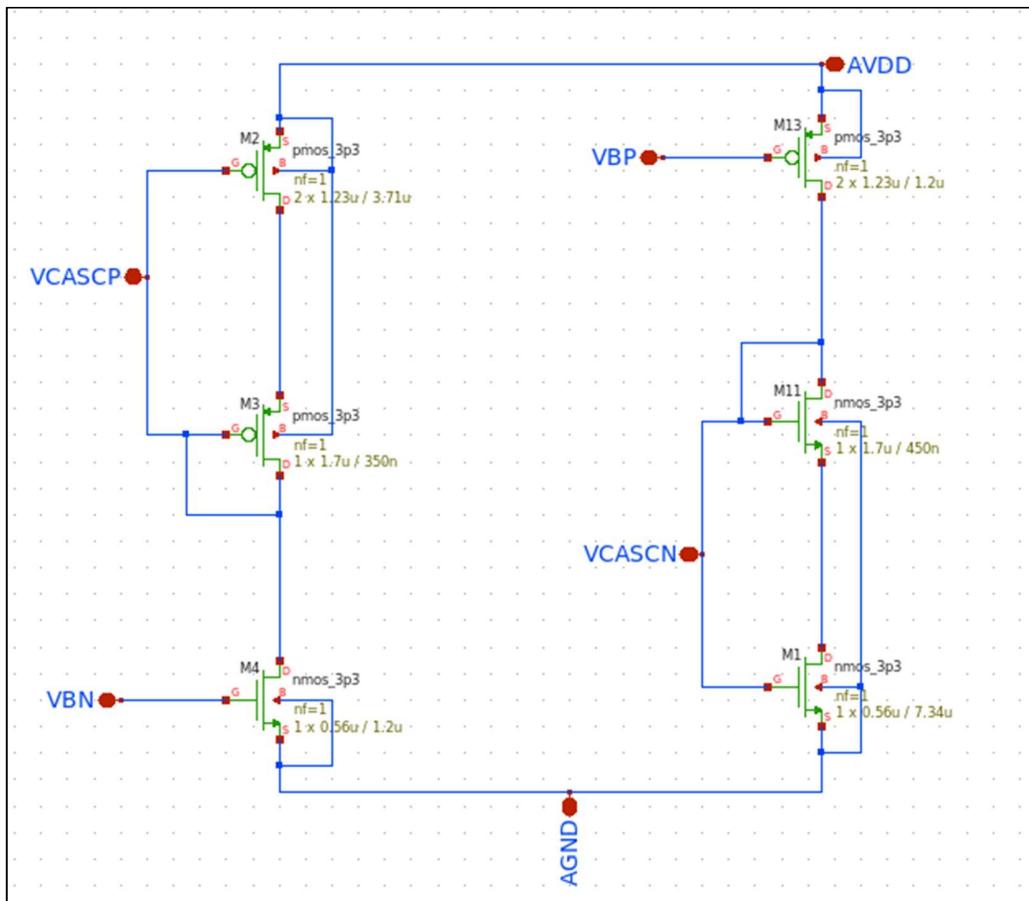
L = 3.71u

W= 1.23u with m = 2



We finely tuned L (because it's more effective than W) until we reached our desired VCASNP

Magic Battery Sizing



Tables Showing DC OP for all transistors

OTA

	M6,7	M13,14	M11,8	M2,3,4,5	M12	M9,10	M1
W (m)	52.8u	17u	6.8u	2*12.33u	5.57u	2*5.57u	4*11.6u
L (m)	400n	350n	450n	1.2u	1.2u	1.2u	1.2u
ID (uA)	10	10	10	10	10	10	20
gm/ID (S/A)	18.5	15	15	10	10	10	10

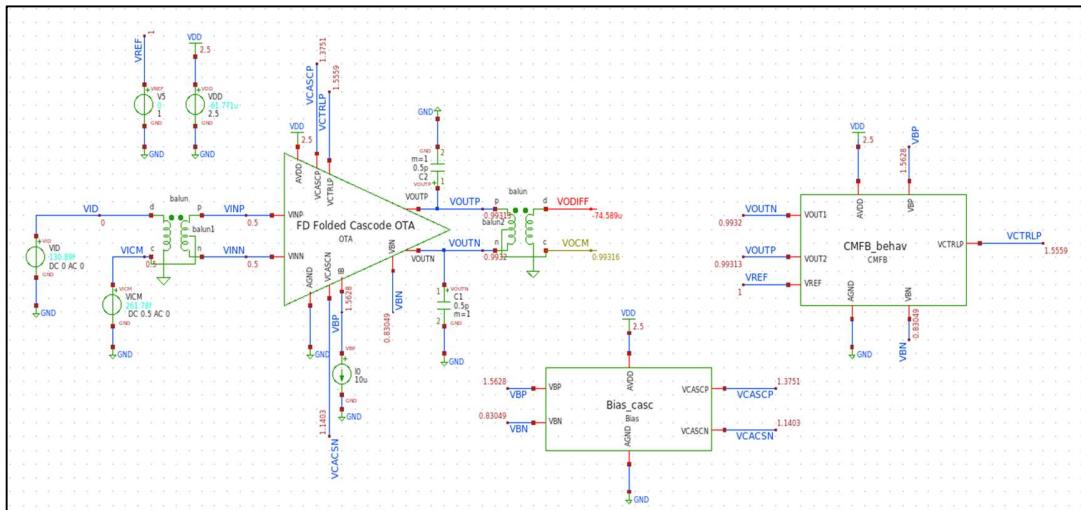
CMFB

	M1,2	M3,4	M5	M6,7,10	M8,9,11
W (m)	11.96u	2.73u	5.8u	12.33u	39.8u
L (m)	1.2u	1.2u	1.2u	1.2u	1.2u
ID (uA)	5	5	5	5	5
gm/ID (S/A)	9.768	9.897	10.09	9.876	14.8

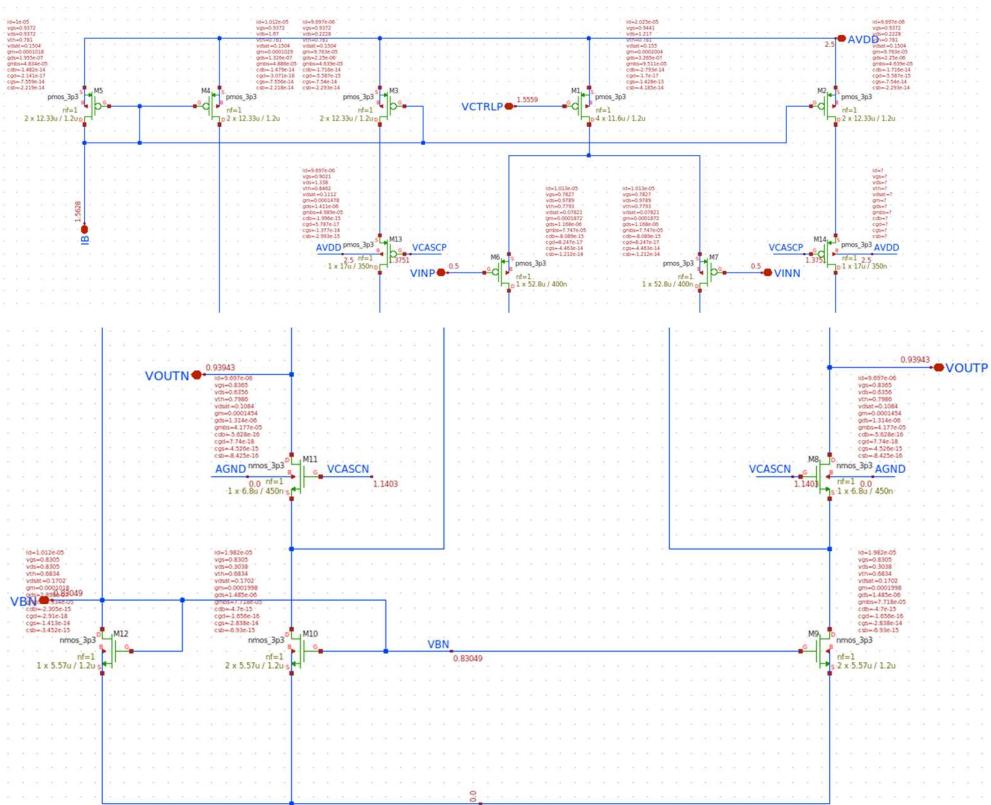
PART 3: Open Loop OTA simulation (Behavioral CMFB)

1) DC op

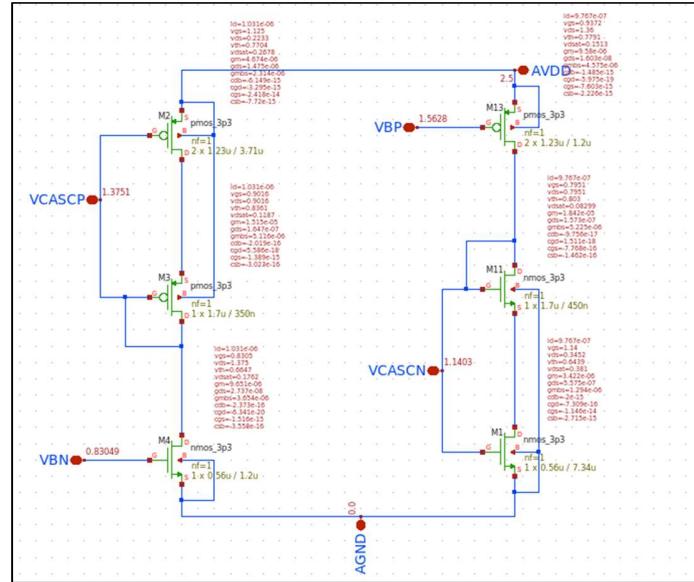
Testbench annotated



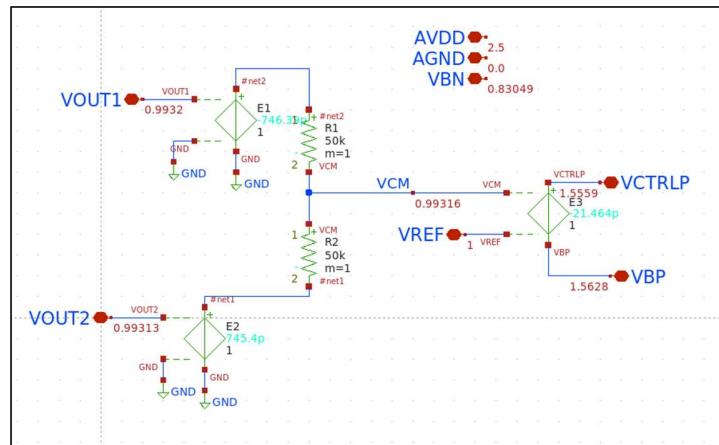
OTA Schematic annotated



Bias circuit annotated



CMFB annotated



We set Vref at a value close to VDD/2 to maximize output swing , **Vref = 1**

Vcm = 0.99316, which is very close to Vref but not equal because CMFB AOL is finite

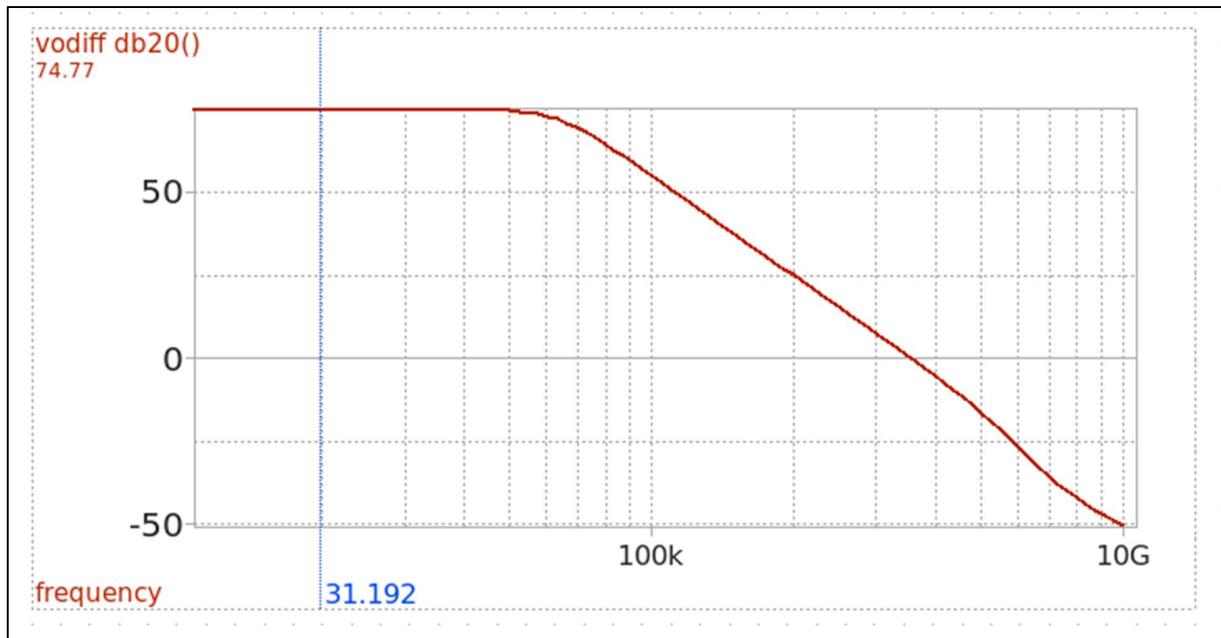
Differential input of the error amplifier is $V_{cm} - V_{ref} = 0.99315 - 1 = -6.85mV$

Differential output of the error amplifier is $V_{ctrlp} - V_{bp} = 1.5559 - 1.5628 = -6.9mV$

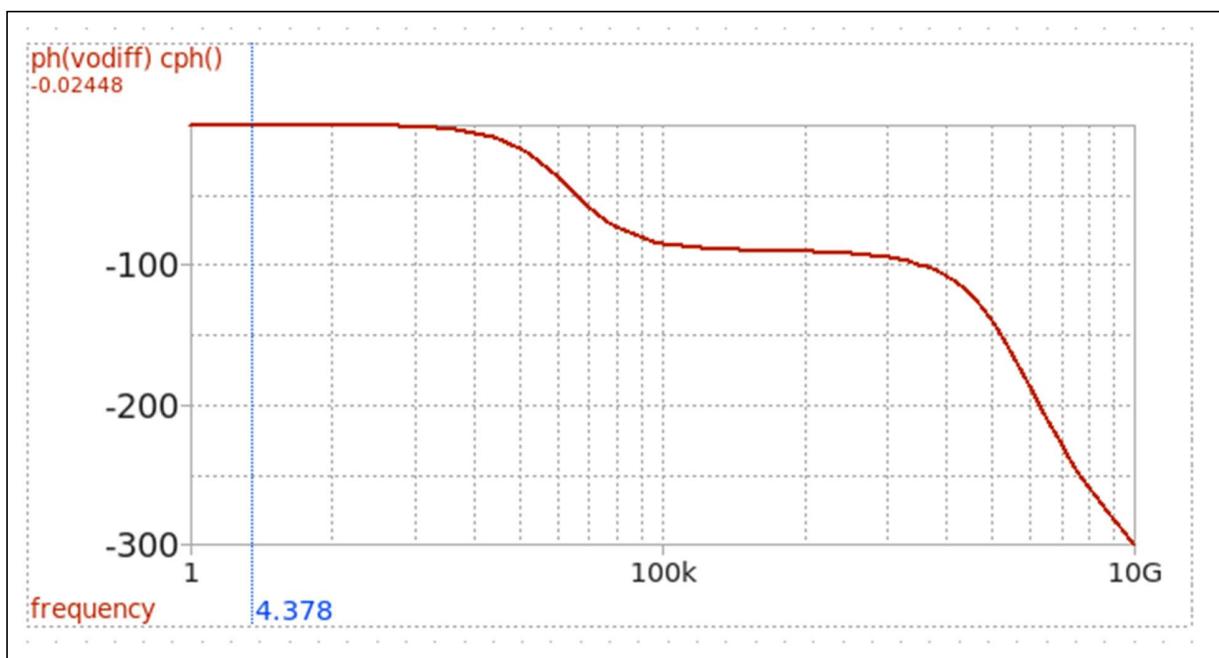
Differential Gain = $V_{out}/V_{in} = 1.007$, so this error amplifier works as a buffer

2) Diff Small Signal

Diff gain in dB vs frequency



Diff gain phase vs frequency



Circuit Parameters

```

dc_gain          = 5.474206e+03 at= 1.000000e+00
dc_gain_db      = 7.476642e+01 at= 1.000000e+00
bw               = 1.033426e+04
gbw              = 5.657187e+07 at= 1.000000e+00
ugf              = 5.686888e+07
phase            = -1.749707e+00
pm               = 7.974917e+01 at= 1.000000e+00
binary raw file "ac_behav.raw"

```

Hand Analysis

$$R_{out} = R_{up} R_{down} = 29.65 \text{ Mohms}$$

$$R_{up} = rocasp(1 + (gmcasp + gmbcasp)rocspl) + rocspl = 62.35 \text{ Mohms}$$

$$R_{down} = rocasn(1 + (gmcasn + gmbcasn)(rocsn||roinpl)) + (rocsn||roinpl) = 56.54 \text{ Mohms}$$

$$Av = gmpin \quad Rout = 5550 = 74.88 \text{ dB}$$

$$Cl = 0.5 \text{ pF}$$

$$BW = \frac{1}{2\pi R_{out} Cl} = 10.73 \text{ KHz}$$

$$GBW = UGF = Av \quad BW = 59.58 \text{ MHz}$$

From pz analysis, wp, nd = 600M

$$PM = 90 - \tan^{-1} \left(\frac{UGF}{wp,nd} \right) = 84.33^\circ$$

```

pole(1) = -6.00251e+08, 0.000000e+00
pole(2) = -1.29049e+08, 0.000000e+00
pole(3) = -1.29049e+08, 1.000000e+08
pole(4) = -1.29049e+08, -1.000000e+08
pole(5) = -2.82206e+05, 0.000000e+00
pole(6) = -5.30231e+00, 0.000000e+00
pole(7) = 0.000000e+00, 0.000000e+00
zero(1) = -1.03127e+08, 0.000000e+00
zero(2) = -2.30578e+01, 0.000000e+00
zero(3) = 0.000000e+00, 0.000000e+00

```

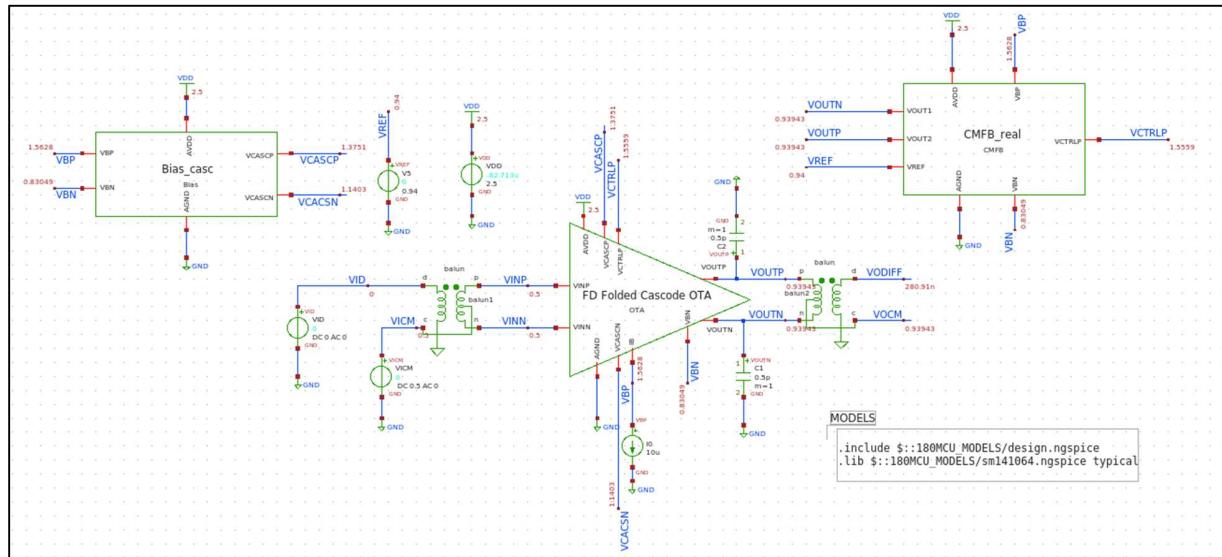
Comparing Results of Simulation and Hand Analysis

	Simulation	Hand Analysis
Av(dB)	74.76	74.88
BW(Hz)	10.33K	10.73K
GBW(Hz)	56.57M	59.58M
UGF	56.86M	59.58M
PM(deg)	79.74	84.33

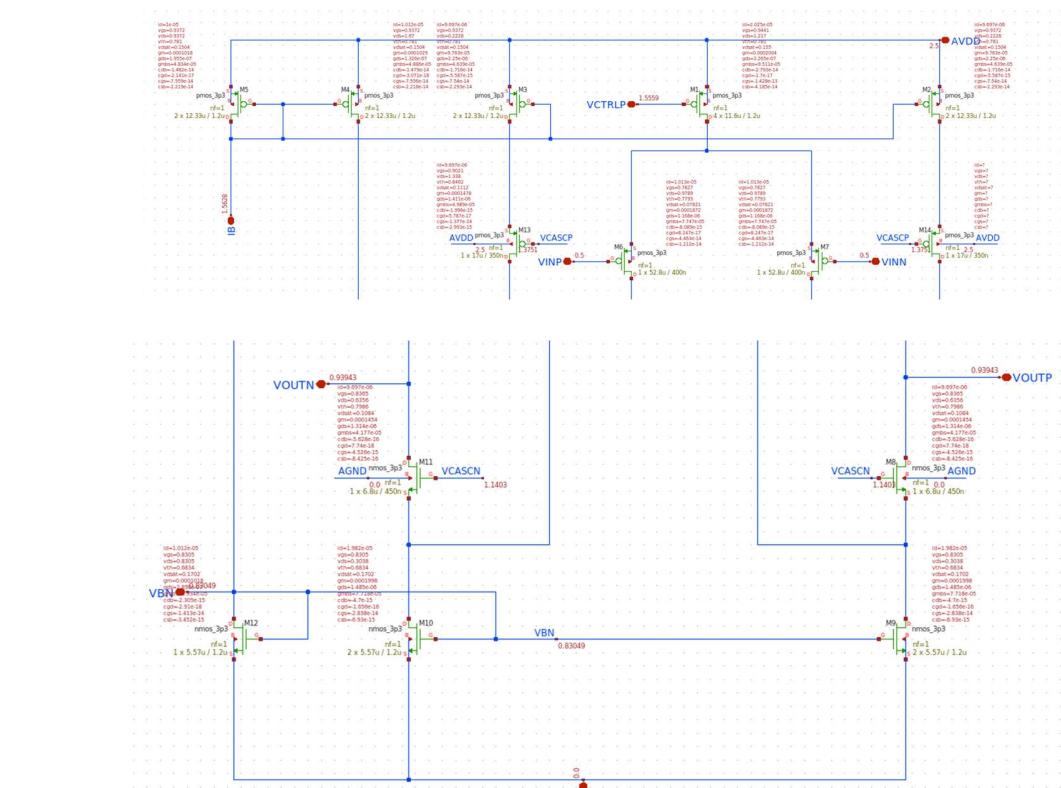
PART 4: Open Loop OTA simulation (Real CMFB)

1) DC op

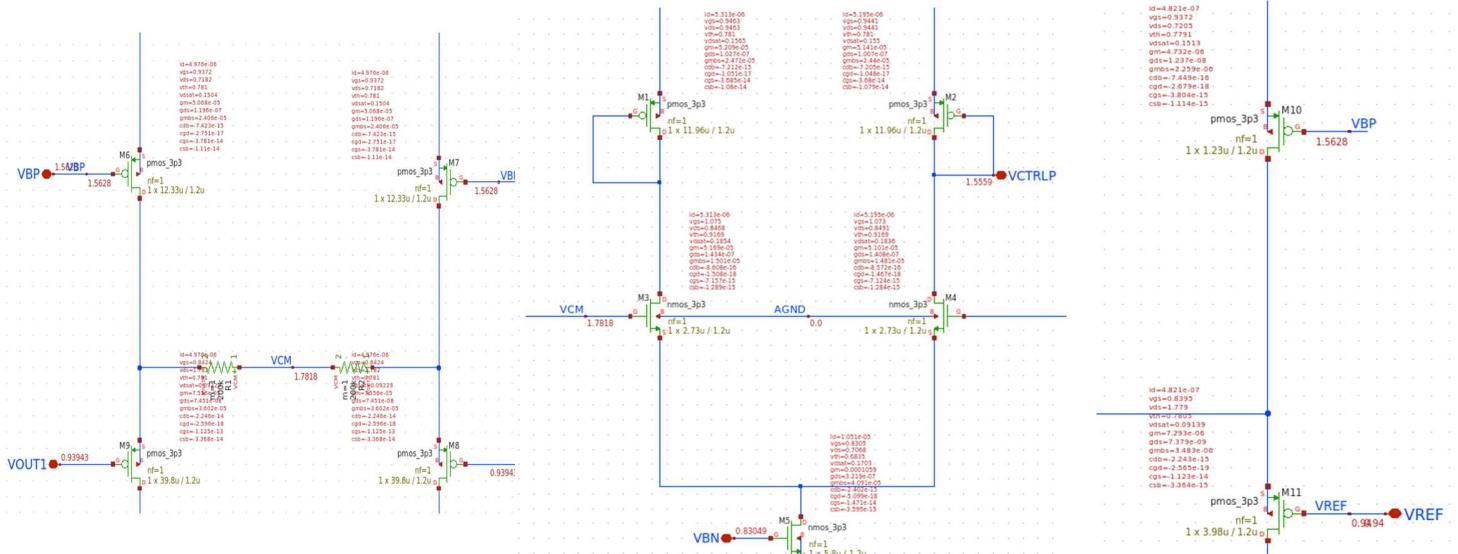
Testbench annotated



OTA Schematic annotated



CMFB annotated



$$V_{outmin} = 2V^* = 0.4v$$

$$V_{outmax} = VDD - VGScd - V^* = 2.5 - 0.82 - 0.2 = 1.48v$$

$$V_{ref} = (V_{outmin} + V_{outmax})/2 = 0.94v \text{ to be in the middle of the swing, } \underline{V_{ref}= 0.94}$$

V_{ocm} = 0.9394, which is very close to V_{ref} but not equal because CMFB AOL is finite

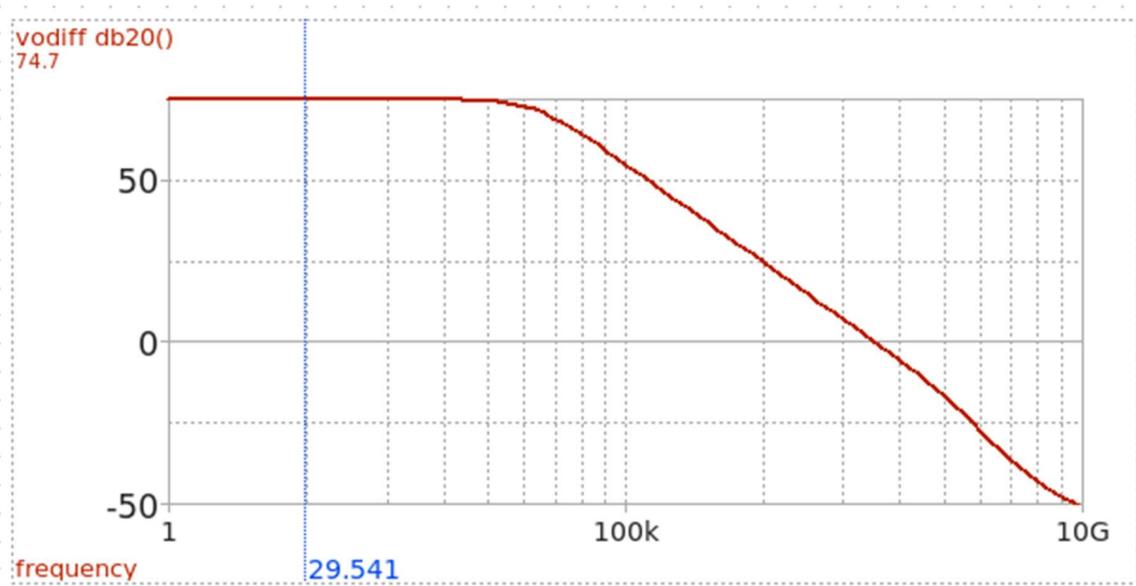
Differential input of the error amplifier is $VGS3 - VGS4 = 1.075 - 1.073 = -2m$

Differential output of the error amplifier is $VGS2 - VGS1 = 0.9441 - 0.9463 = -2.2mv$

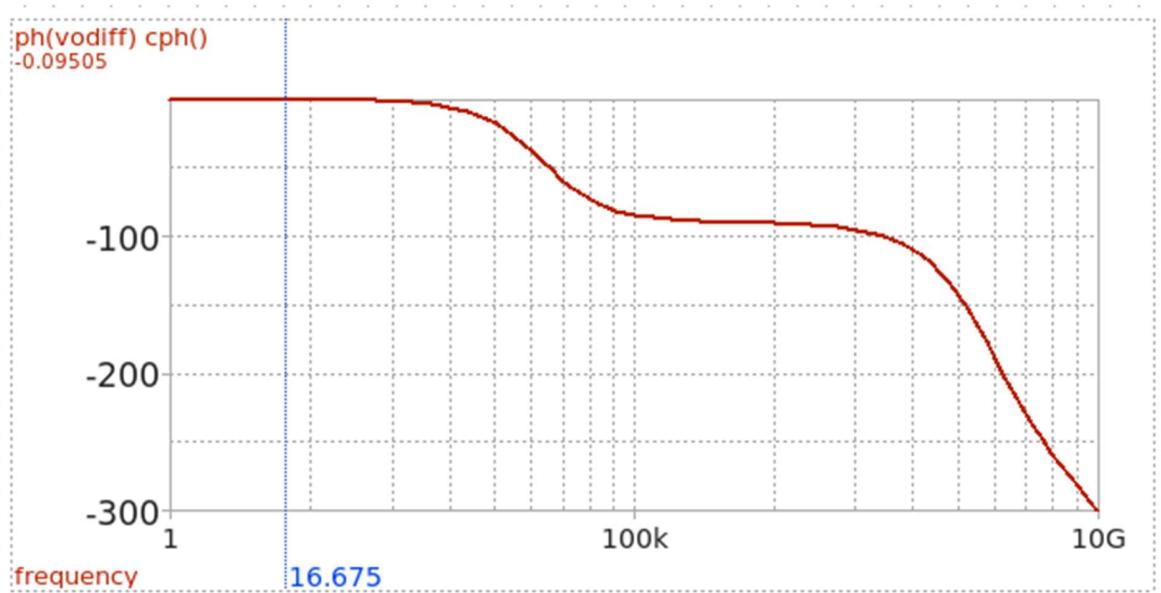
Differential Gain = $V_{out}/V_{in} = 1.1$

2) Diff Small Signal

Diff gain in dB vs frequency



Diff gain phase vs frequency



Circuit Parameters

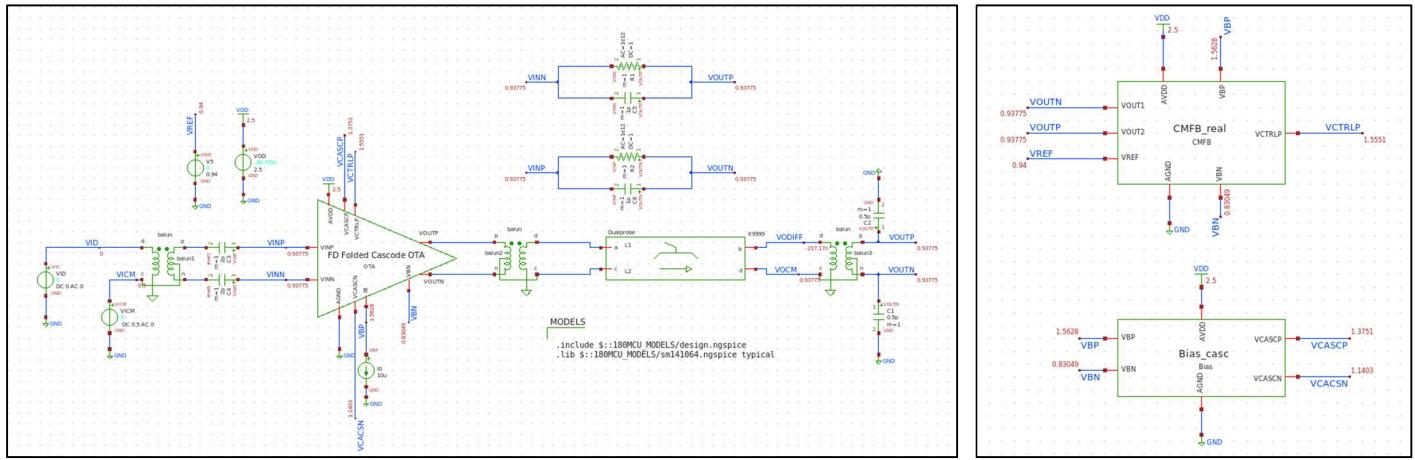
```
dc_gain          = 5.430779e+03 at= 1.000000e+00
dc_gain_db      = 7.469724e+01 at= 1.000000e+00
bw               = 1.010649e+04
gbw              = 5.488611e+07 at= 1.000000e+00
ugf              = 5.443989e+07
phase            = -1.764732e+00
pm               = 7.888830e+01 at= 1.000000e+00
```

These values are close to what's calculated in behavioral model

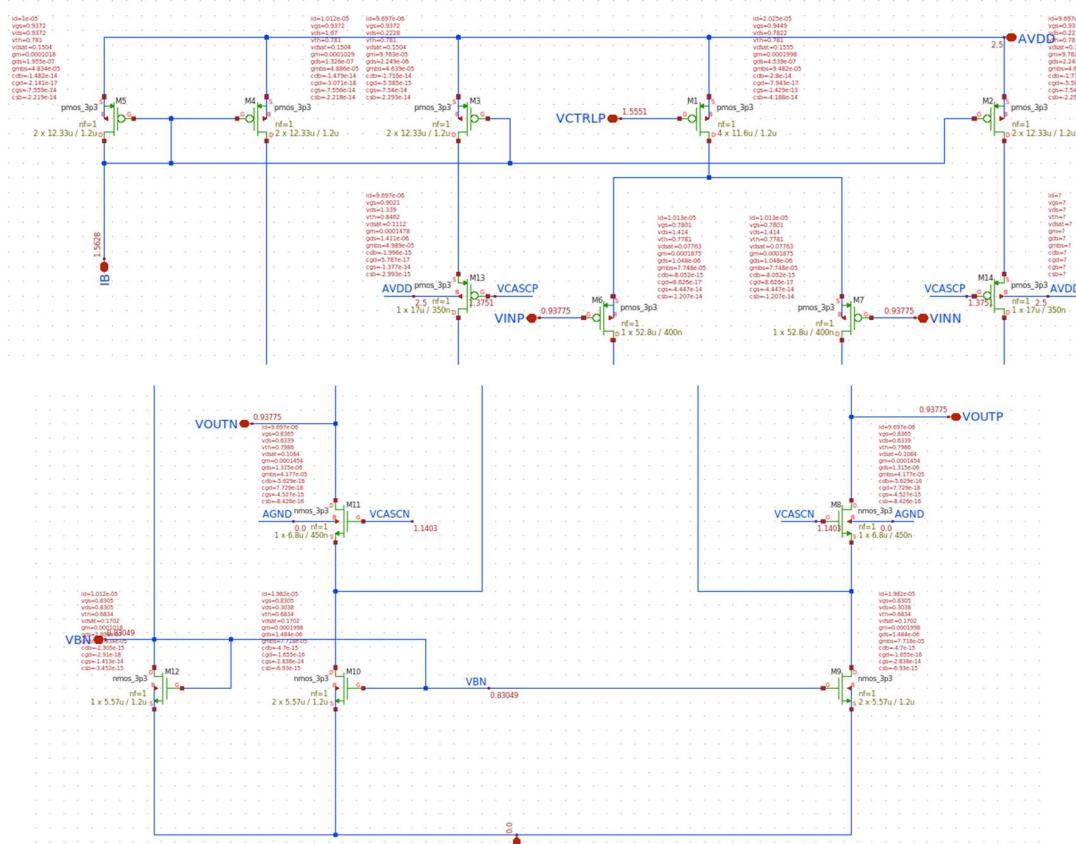
PART 5: Closed Loop OTA simulation (STB & AC)

1) DC op

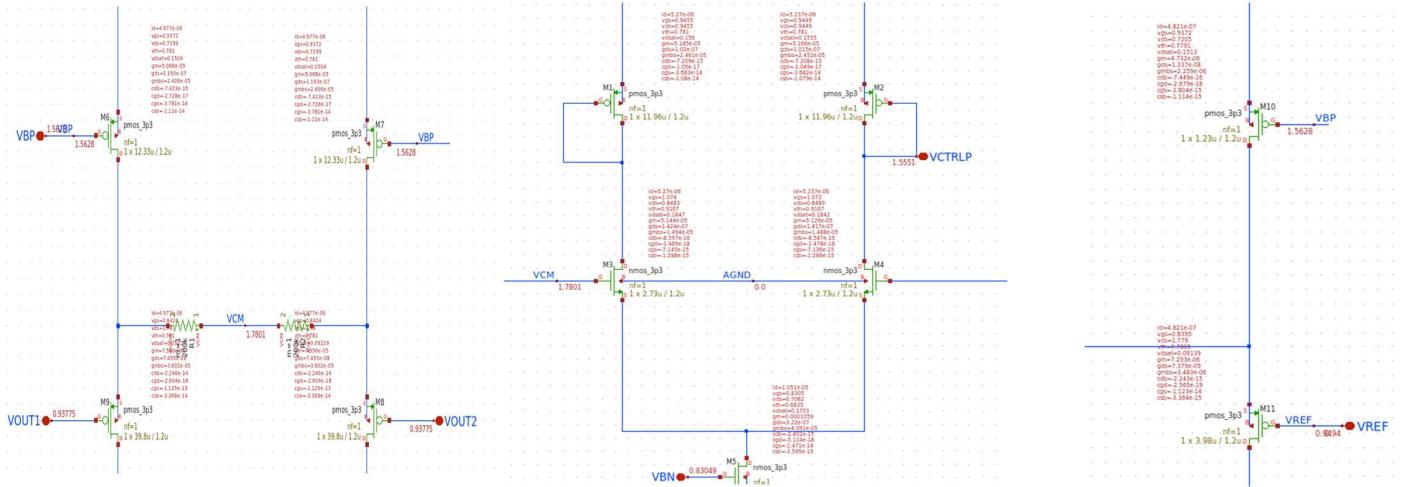
Testbench annotated



OTA Schematic annotated



CMFB annotated

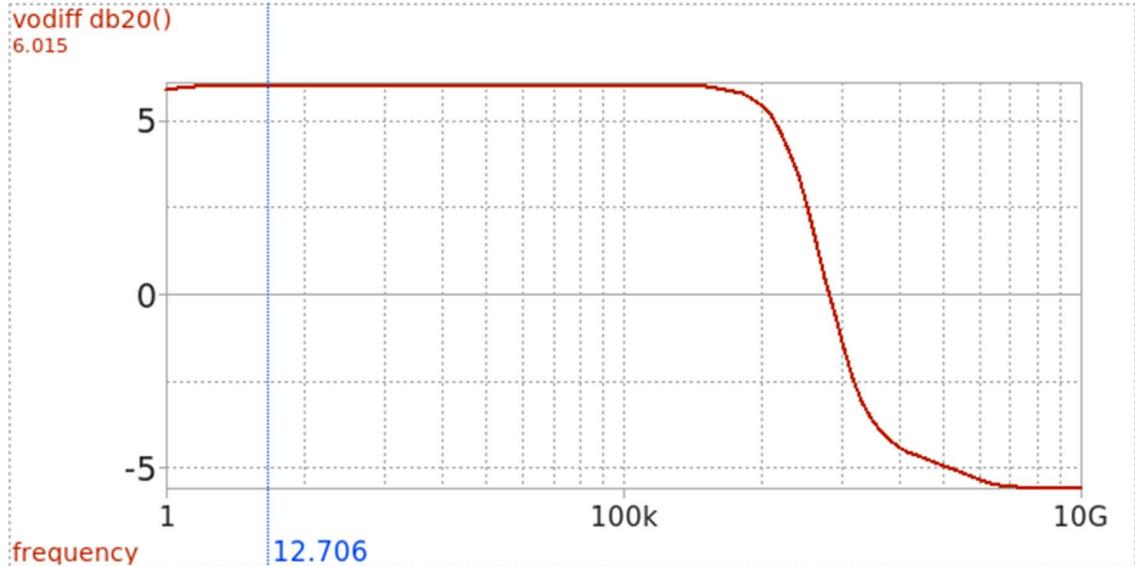


CM level at output node = 0.93775v which is approximately equal to Vref (0.94v) of CMFB to be in the middle of the swing as calculated before

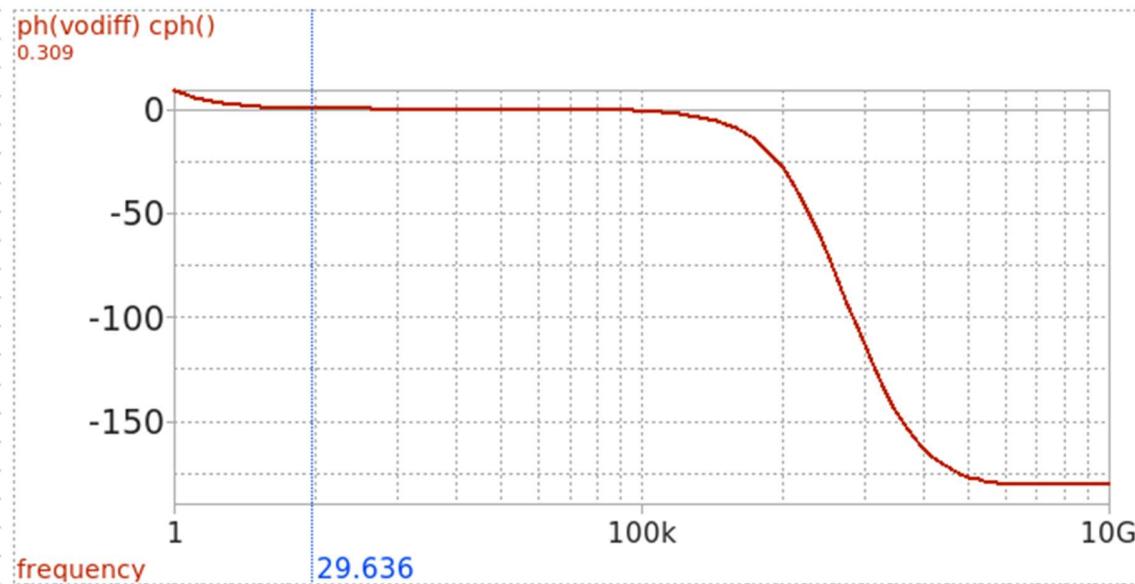
CM level at input node = 0.93775v which is equal to CM level at output node due to negative feedback in which they are both connected with parallel cap and resistor (cap becomes oc , and dc res is too small)

2) Differential closed loop

Diff gain in dB vs frequency



Diff gain phase vs frequency

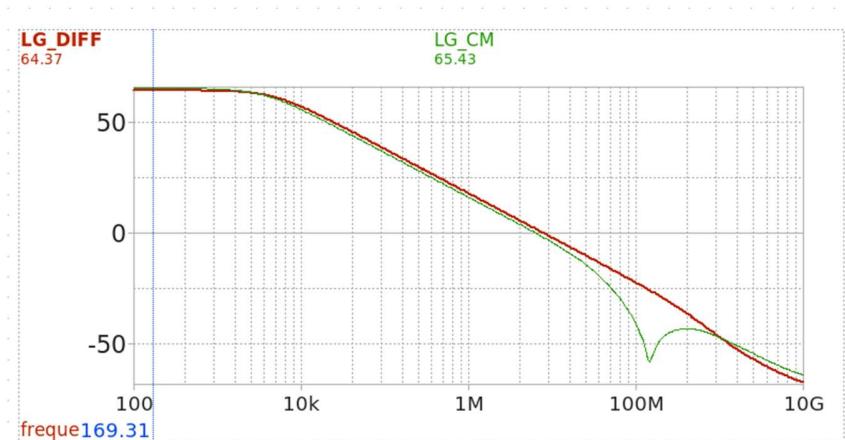


Circuit Parameters

```
dc_gain          = 1.998791e+00 at= 1.258925e+03
dc_gain_db      = 6.015350e+00 at= 1.258925e+03
bw               = 8.973849e+06
gbw              = 1.793685e+07 at= 1.000000e+00
ugf              = 1.763805e+07
phase            = -1.719457e+00
pm               = 8.148237e+01 at= 1.000000e+00
```

3) Differential and CMFB loops stability

appended LG in dB



appended LG Phase



Circuit Results (1 is Diff and 2 is CM)

```
gain_1          = 1.653794e+03 at= 1.000000e+02
l1_gain_crossover_freq= 7.875158e+06
l1_phaseatzerogain = 8.853679e+01
gain_2          = 1.870890e+03 at= 1.000000e+02
l2_gain_crossover_freq= 6.335305e+06
l2_phaseatzerogain = 7.373220e+01
-----
loop1_lg = 6.436963e+01
loop1_gx = 7.875158e+06
loop1_pm = 8.853679e+01
-----
loop2_lg = 6.544097e+01
loop2_gx = 6.335305e+06
loop2_pm = 7.373220e+01
```

Diff

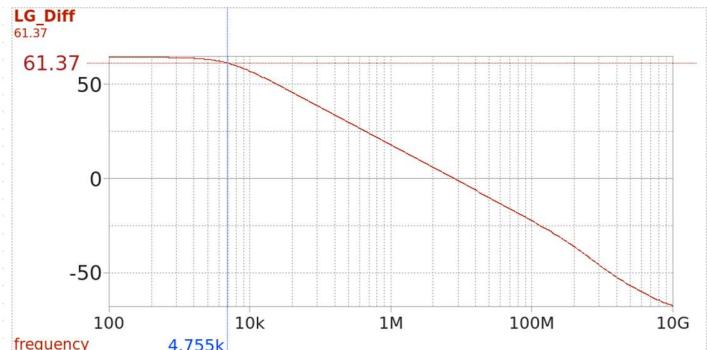
Gain = 64.37dB = 1653.8

BW(-3dB) = 4.755kHz at 61.37dB

GBW = Gain*BW = 7.76MHz

GX = 7.875MHz

PM = 88.53



CM

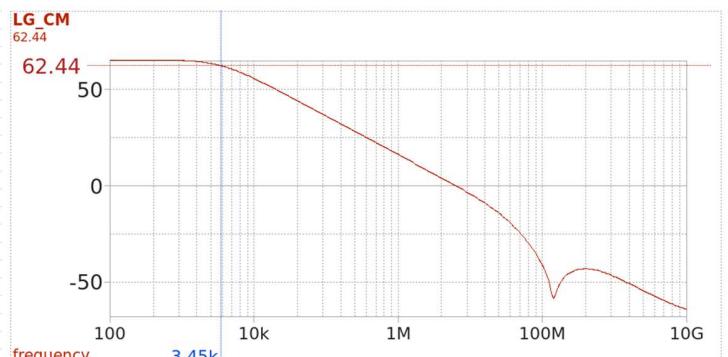
Gain = 65.44dB = 1870.9

BW(-3dB) = 3.45kHz at 62.44dB

GBW = Gain*BW = 6.45MHz

GX = 6.33MHz

PM = 73.73



	Differential	CM
PM(deg)	88.53	73.73
GBW(Hz)	7.76M	6.33M

PM of CM is lower than PM of Diff because CM passes in CMFB which introduces many poles to the CM that causes lower PM, but PM of Diff is close to 90.

LG of CM is higher than LG of Diff because CM passes in CMFB which has a gain higher than unity a bit which makes this difference.

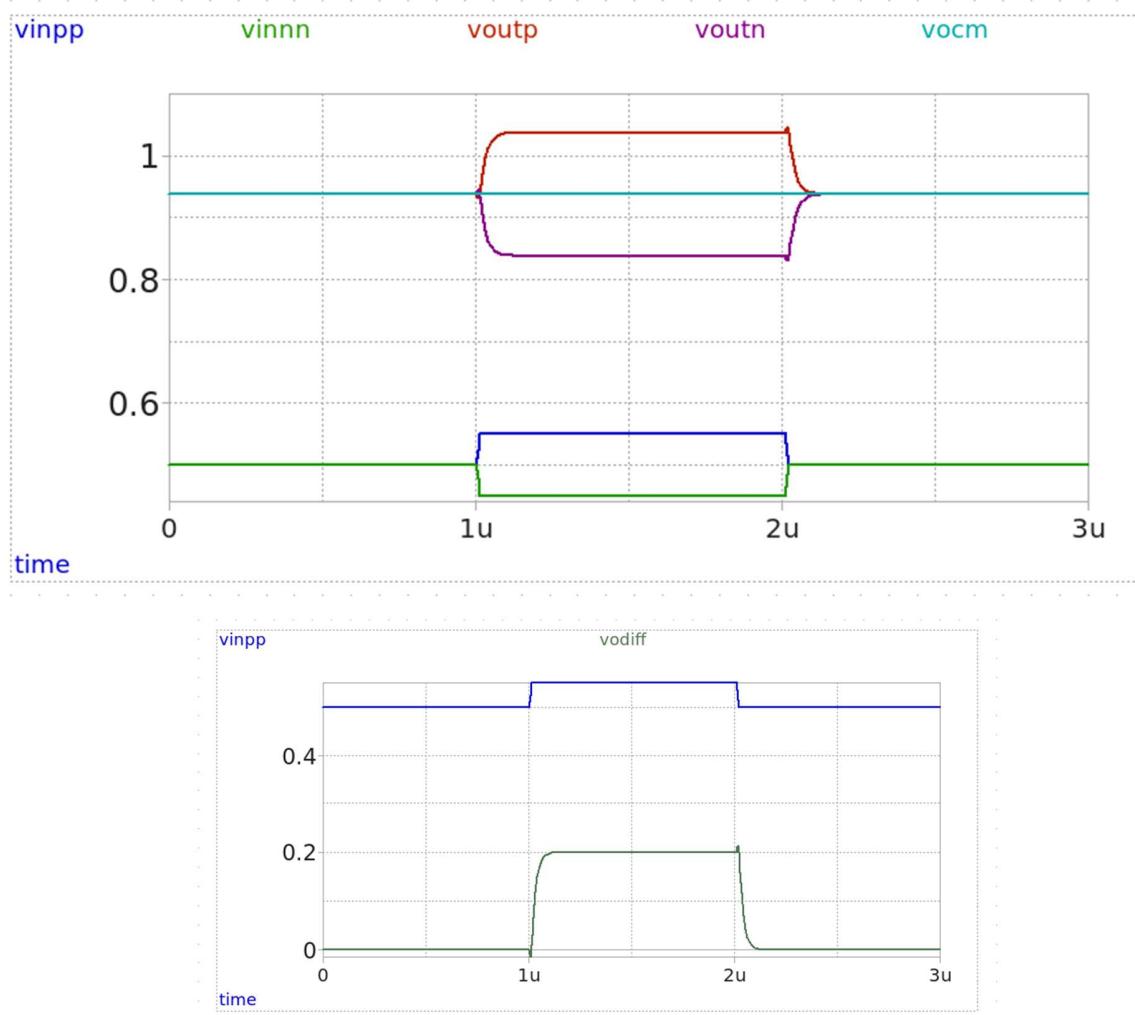
	Open Loop	Closed Loop
LG(dB)	74.7	64.37
GBW(Hz)	56.57M	7.76M

LG is lower in Closed loop due to feedback which turns it into a voltage-current amplifier and it's multiplied by Beta factor which is 1/3 (could be lower if we didn't neglect C_{in})

GBW is also lower in Closed loop due to feedback loading effect which results in increasing Cap leading to decrease in BW therefore GBW.

PART 6: Closed Loop OTA simulation (Transient)

1) Differential Input Pulse

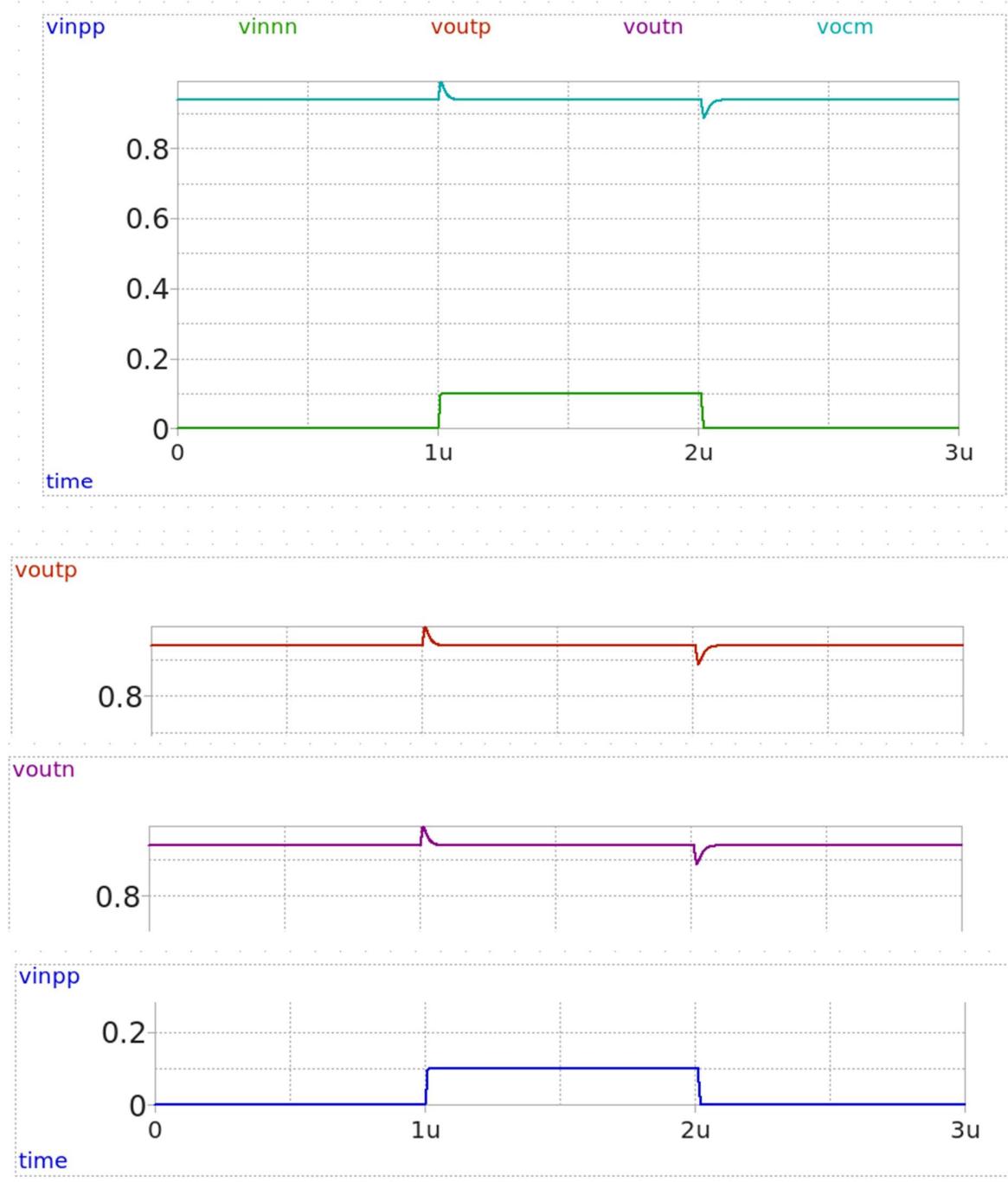


There is no ringing observed because PM of differential loop = 88.53 which is stable (>76)
(but there is a very small overshoot)

```
initial_val          = -6.476912e-07
final_val           = 1.998811e-01
sett_time           = 1.100926e-06
t_sett              = 1.009260e-07 at= 0.000000e+00
```

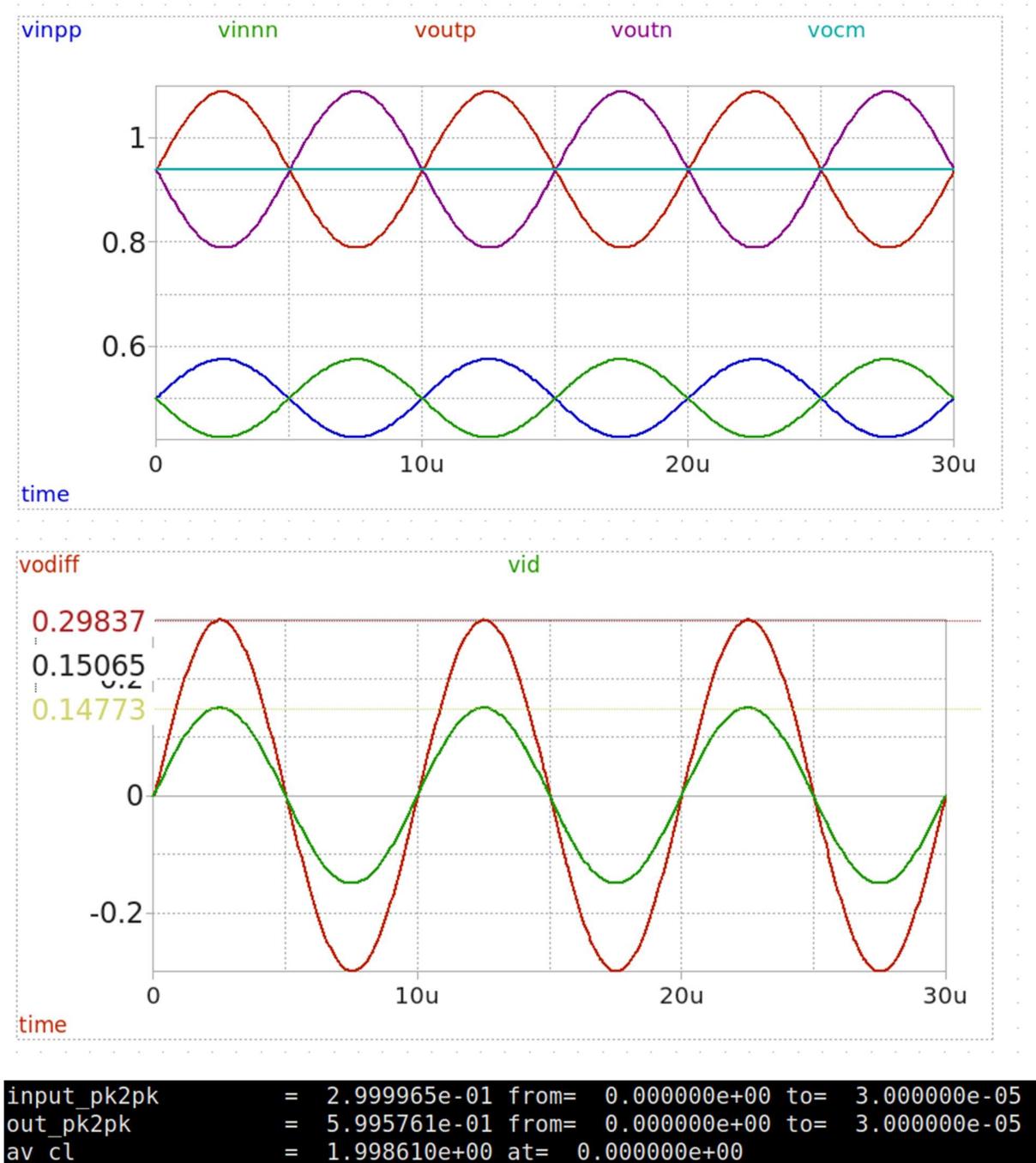
Settling time = 100.926ns, it meets the required specification

2) Common Mode Input Pulse



There is no ringing observed because PM of CM loop = 73.73 which is very close to (PM=73 that suffers from a very slight overshoot, but no peaking and fastest settling)

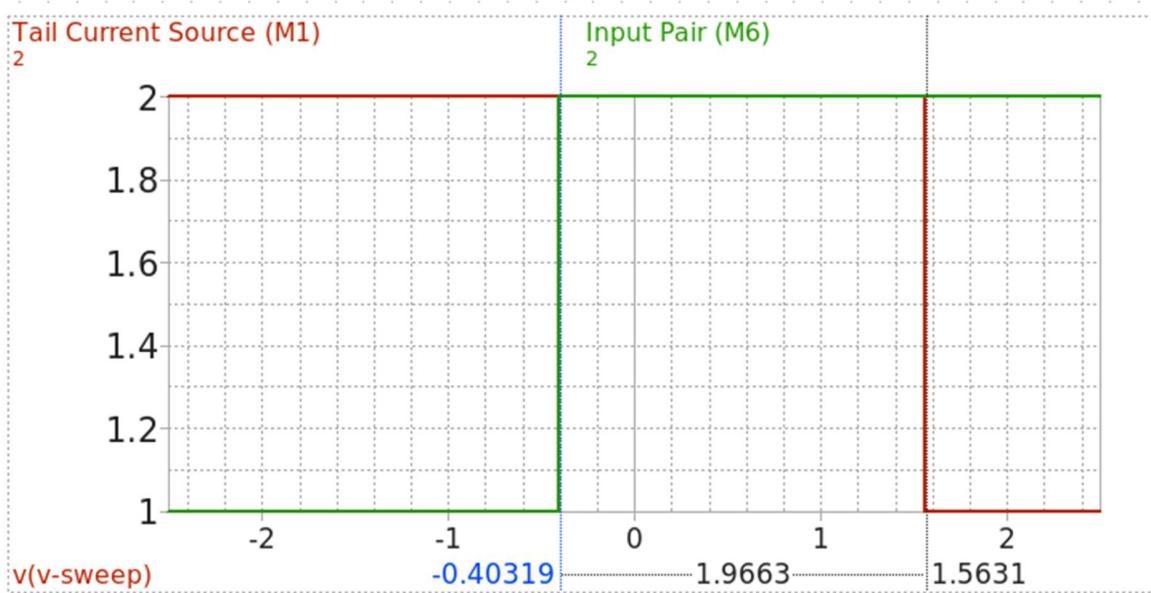
3) Output Swing



Vinpk2pk = 299mV

Voutpk2pk = 599mV , so Voutpk2pk-diff = 2*Voutpk2pk = 1.199V

Extra - CMIR



CMIR-low = -0.4

CMIR-high = 1.56

Summary of Specs achieved

	Required	Achieved
Supply Voltage	2.5v	2.5v
Load	0.5pF	0.5pF
Closed Loop Gain	2dB	1.9987dBz
Phase Margin at Acl=2dB	$\geq 70^\circ$	88.53°
CMIR – low	$\leq 0V$	-0.4v
CMIR – high	$\geq 0.6V$	1.5v
Diff output swing(pk-to-pk)	1.2V	1.199V
DC Loop gain	60dB	64.37dB
CL settling time for 1% error	100ns	100.926ns

Appendix

You will find ngspice codes I used to run these simulations.

https://github.com/ymsayedh/Lab11_Codes