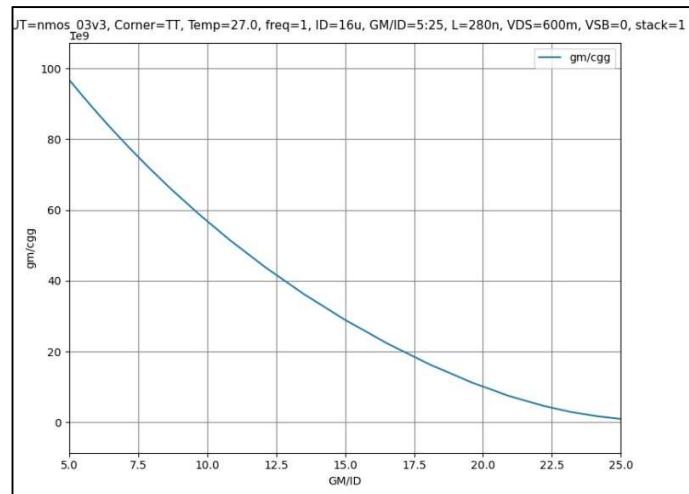
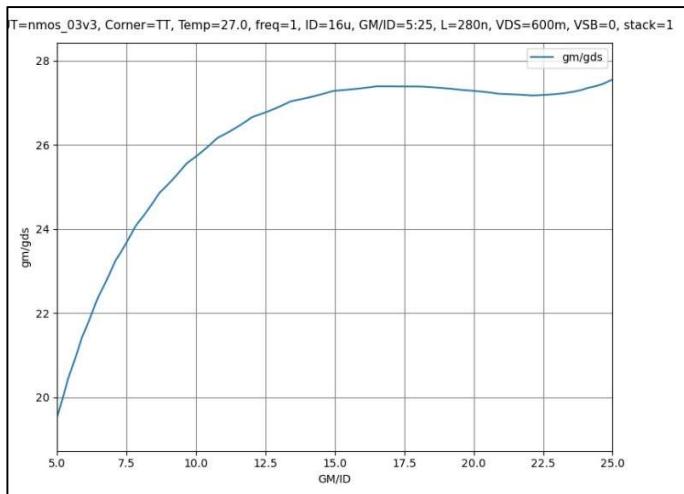
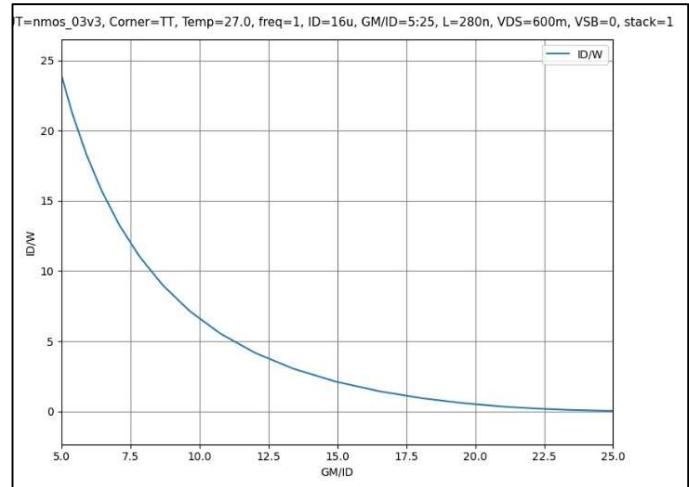
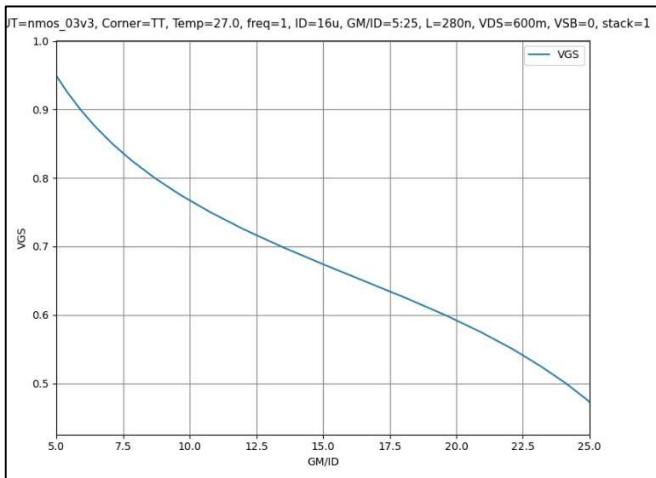


Mini Project 1 (Lab 09)

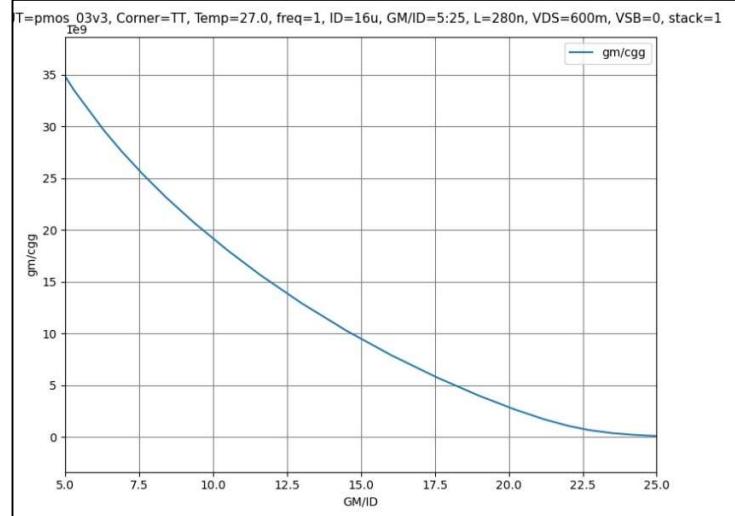
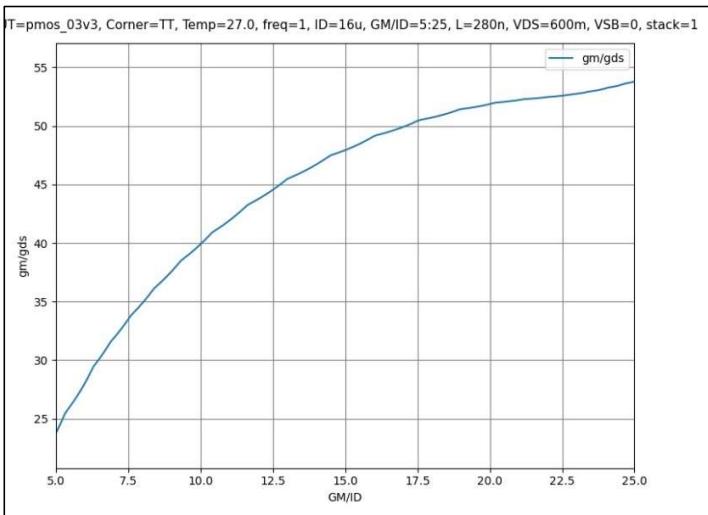
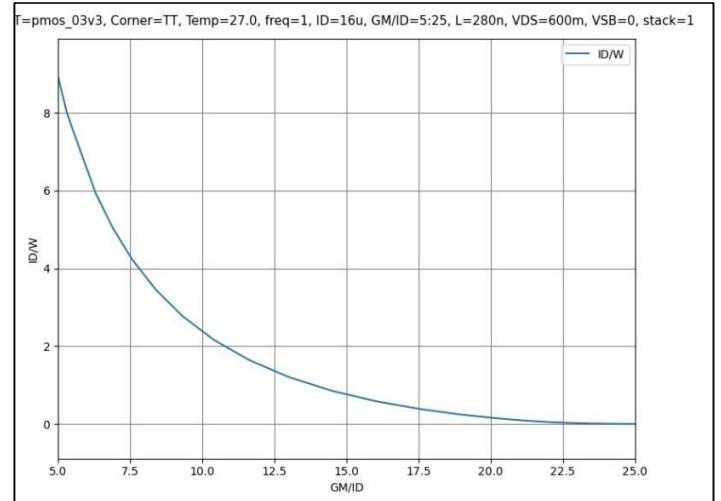
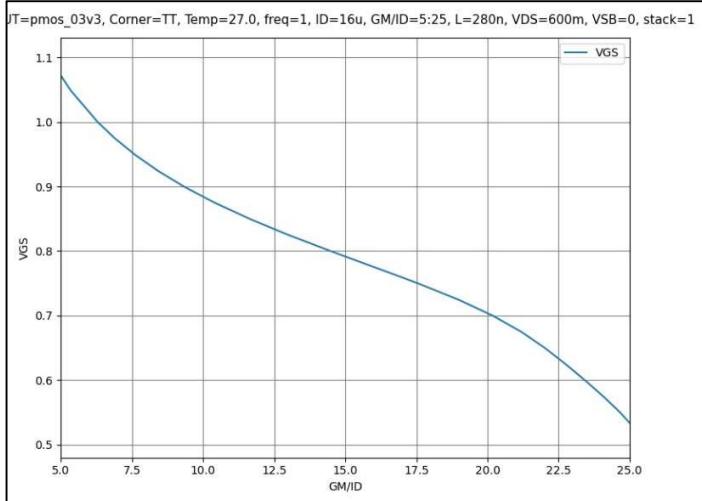
Two-Stage Miller OTA

PART 1: gm/ID Design Charts

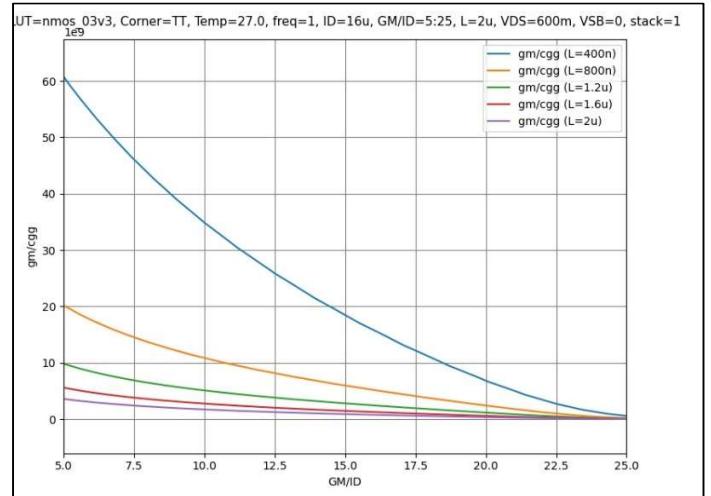
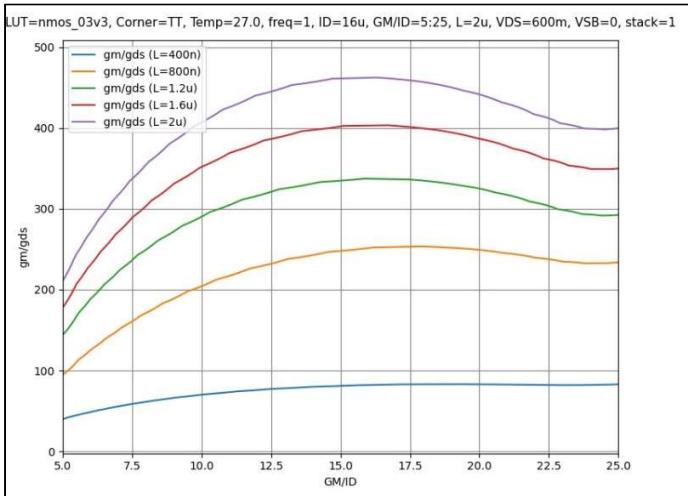
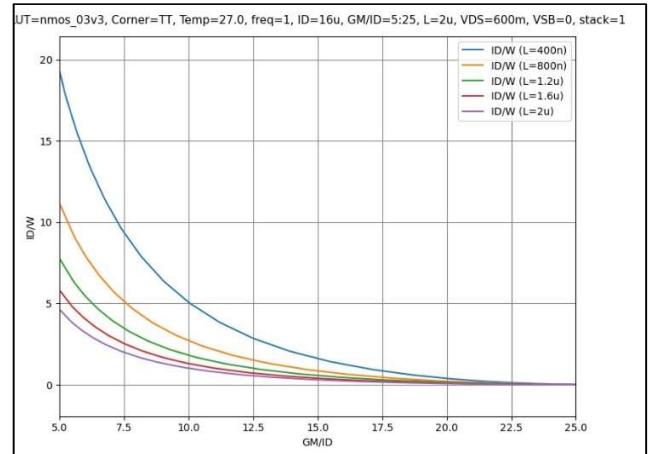
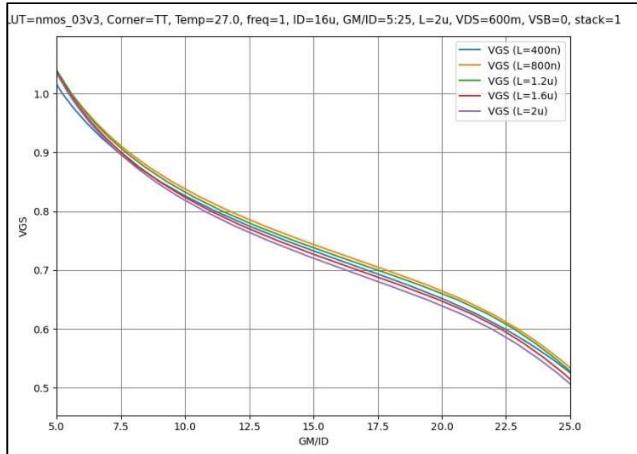
NMOS at L = 0.18u



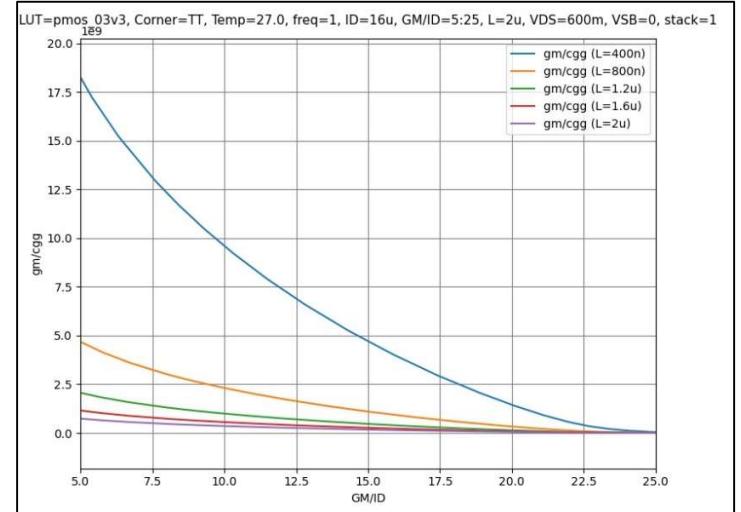
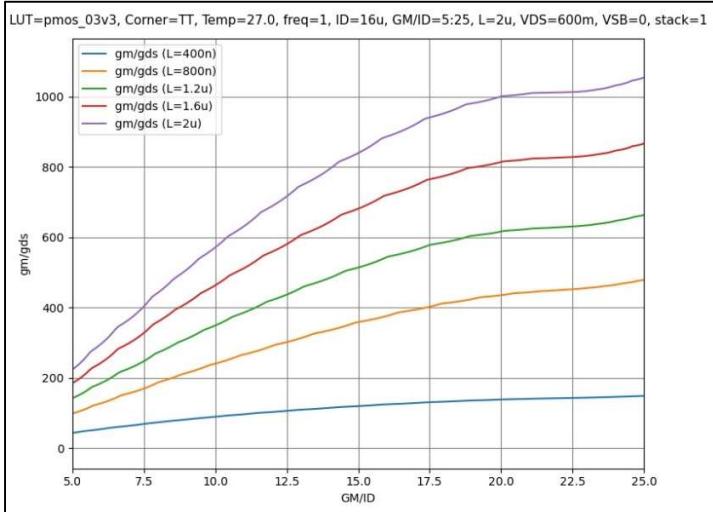
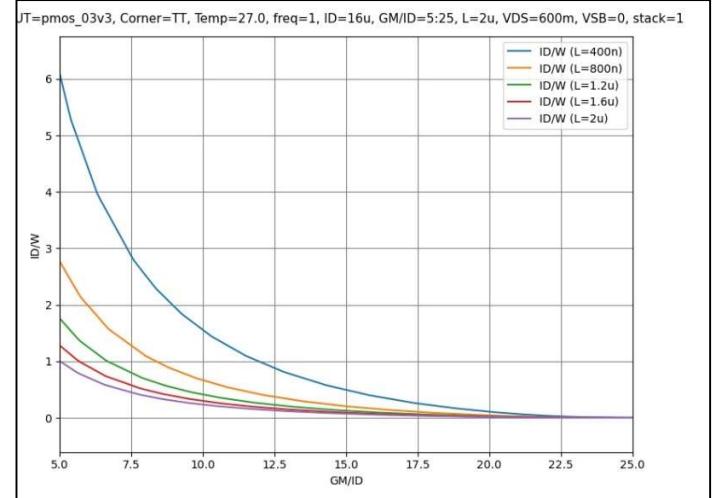
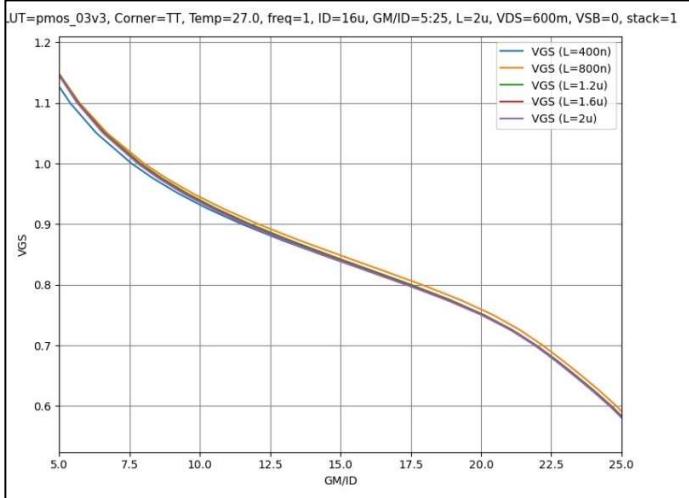
PMOS at L = 0.18u



NMOS at L=0.5u:0.5u:2u



PMOS at L=0.5u:05u:2u



PART 2: OTA Design

We want to design a Two Stage Compensated Miller OTA with the following specs:

Supply voltage: 1.8V
Static gain error <= 0.05%
CMRR @ DC >= 74dB
Phase margin (avoid pole-zero doublets) >= 70 deg
OTA current consumption <= 60uA
CMIR – high >= 0.8 V
CMIR – low <= 0.2V
Output swing: 0.2 – 1.6V
Load: 5pF
Buffer closed loop rise time (10% to 90%) <= 70ns
Slew rate (SR): 5V/ μ s

We implemented a two-stage Miller OTA with a PMOS differential input pair, an NMOS current mirror active load, an NMOS tail current source, and a common-source NMOS second stage

PMOS input pair is chosen to achieve a low-voltage CMIR requirement (close to GND rail)

Two-stage topology is chosen because the required open-loop DC gain (≥ 74 dB) is too high to be achieved reliably with a single-stage OTA.

NMOS current mirror load's (first stage) sizing is chosen to match VGS with the second-stage input device to minimize systematic offset.

Miller compensation (C_c & R_z) is used between the output of the first stage and the input of the second stage to make this node a dominant pole, ensuring phase margin $\geq 70^\circ$ in addition to forcing zero at infinity to avoid closely spaced pole-zero pairs.

In first stage, VDD is divided equally on tail current source, cm load and input pair (VDD/3)

In second stage, VDD is divided equally on load and input (VDD/2)

PMOS input pair don't suffer from any body effect because we are using CMOS technology

First: PMOS Input Pair

We are using Bias current of 10uA

I want to use 1:1 mirroring which makes **Iss = 10uA**

Slew rate = $\text{Iss}/\text{Cc} = 5\text{V/uS}$, which makes $\text{Cc} = 2\text{pF}$ but I'll use lower Cc because I am considering parasitic capacitors and some Slew rate margin, so **Cc = 1.76pF**

Closed Loop Rise Time $\leq 70\text{ns}$, $\text{TRcl} = 2.2\tau_{\text{cl}}$, $\tau_{\text{cl}} = \frac{1}{BW_{\text{cl}}}$, $BW_{\text{cl}} = \frac{2.2}{\text{TRcl}} \geq 31.43\text{Mrad/sec}$
 $BW_{\text{cl}} = \frac{GBW}{A_{\text{cl}}} = GBW$, $GBW = \frac{gm}{Cc} \geq 31.43\text{Mrad/sec} \rightarrow \underline{\text{gm} \geq 55.3\text{uS}}$

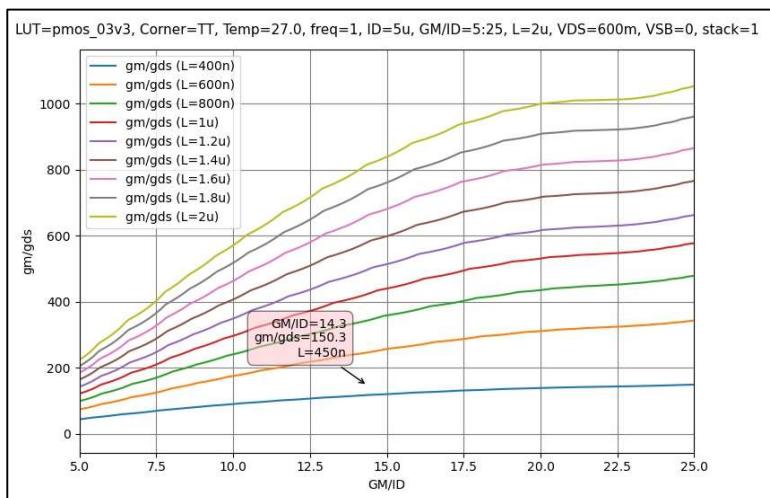
We'll design identical input pair, so Iss is divided equally therefore **ID = 5uA**

We'll have a $\text{gm}/\text{ID} = 11.06$ but we'll use a higher **gm/ID = 14.3** to get a higher gm achieving higher GBW

Static gain error $\leq 0.05\%$, Static gain error = $1/\text{LG} = 1/\beta \text{Aol} = 1\text{Aol}$, $\text{Aol} \geq 2000 = 66\text{dB}$

Assuming gain of 1st stage is double gain of 2nd stage
(1st stage gain = 63.25, 2nd stage gain = 31.62)

Assuming ro of input pair = ro of cm load, 1st stage gain = $\frac{gmro}{2} \geq 63.25$, **gmro ≥ 126.5**



LUT Settings	
ID	5u
gm/ID	14.3
L	450n
VDS	0.6
VSB	0
Stack	1
Results:	
Name	TT-27.0
1 ID	5u
2 IG	N/A
3 L	450n
4 W	9.87u
5 VGS	858.3m
6 VDS	600m
7 VSB	0
22 VDSAT	117m

Input Pair Sizing

L = 450nm

W = 10um

VGS = 858.3mv

Vdsat = 117mv

Second: NMOS Current Mirror Load

$$r_{on} = r_o = \frac{126.5}{g_{mp}} \geq 2.28M \rightarrow VA = ID * r_o \geq 11.4 \rightarrow \underline{\underline{VA = 11.5}}$$

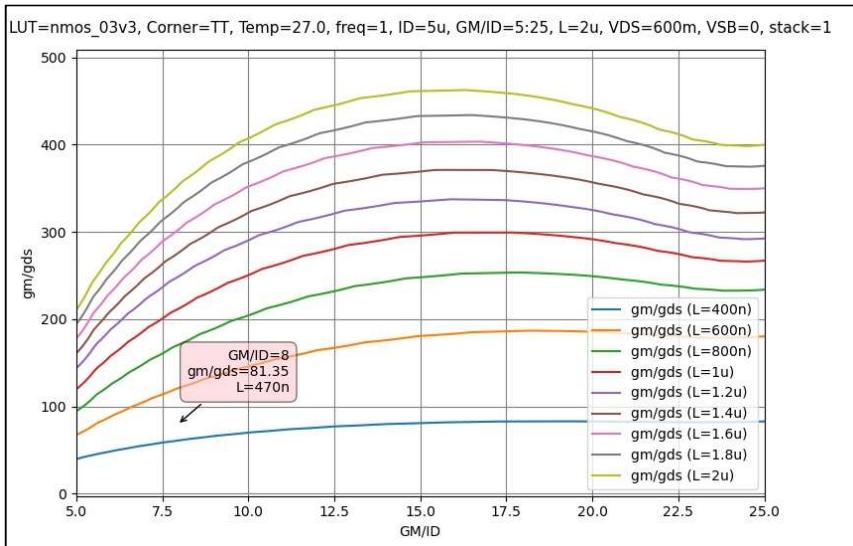
$$V_{inCM(min)} = -|VGS_p| + |Vdsatp| + VGS_n \text{ (VGSp and VDsatp of input pair)}$$

Since max value for $V_{inCM(max)} = 0.2$, so we can get max value for $VGS_n \leq 941.3mV \rightarrow 900mV$

using SA to get gm/ID using VGS and VA

gm/ID = 8, ID = 5uA, gmn = 40 uS, gmro ≥ 91

LUT Settings	
ID	5u
VGS	900m
VA	11.5
VDS	0.6
VSB	0
Stack	1
Results:	
Name	TT-27.0
7 VSB	0
8 gm/ID	8.007
9 Vstar	249.8m



LUT Settings	
ID	5u
gm/ID	8
L	470n
VDS	0.6
VSB	0
Stack	1
Results:	
Name	TT-27.0
1 ID	5u
2 IG	N/A
3 L	470n
4 W	680n
5 VGS	896.7m
6 VDS	600m
7 VSB	0
Y-Expr gm/ID*fT	

CM load Sizing

L = 470nm

W = 680nm

We used another sizing downwards to minimize systematic offset

Third: Tail Current Source

$$CMRR = \frac{Av}{AvCM} \rightarrow AvCM(1st) = \frac{Av}{CMRR} = Av(1st) - CMRR \text{ (in dB)} = 36 - 74 = -38dB$$

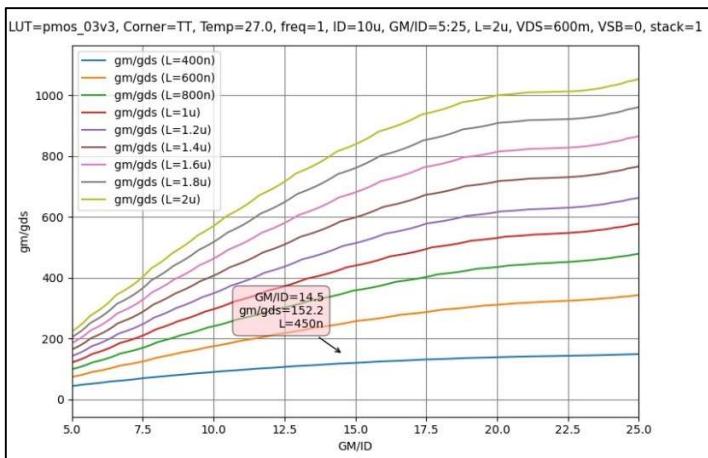
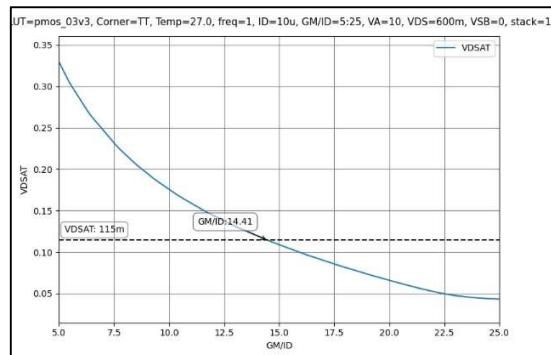
$$AvCM \leq 0.0126, AvCM = \frac{1}{2 * gmn * Rss} \text{ (assume } Rss = roCS) \rightarrow roCS = 992k \rightarrow \underline{\text{VA = 11.5}}$$

$$VinCM(max) = VDD - |VGSp| - |VdsatCS|$$

Since min value for VinCM(max) = 0.8, so we can get max value for VDsatCS
 $V_{Dsat} \leq 142m \rightarrow 115m$

Plotting Vdsat to get gm/ID = 14.5

gm = 145uS, gmro ≥ 144



LUT Settings

ID	10u
gm/ID	14.5
L	450n
VDS	0.6
VSB	0
Stack	1

Results:

Name	TT-27.0
1 ID	10u
2 IG	N/A
3 L	450n
4 W	20.78u
5 VGS	854.2m
6 VDS	600m
7 VSB	0

Y-Expr gm/ID*fT

CS Sizing

L = 450nm

W = 21um

We'll use 1:1 mirroring in the first stage, so same sizing

Fourth: Second Stage

We'll use PMOS load to make it mirror current and NMOS input stage to be biased with output of 1st stage (VGS of Diode connected NMOS load)

$wp_2 = 4wu$ to get $PM = 76$ which makes our system critically damped and achieving our spec

$$wu = GBW \geq 31.43 \text{Mrad}, wp_2 = \frac{gmn}{CL} \rightarrow gmn = 4 * CL * GBW \rightarrow gmn \geq 628.6 \mu\text{s}$$

2nd Stage Gain = $gmn (ron||rop)$, and by comparing with 1st stage
gain 2nd = gain 1st / 2

$gm_{2^{nd}} = 10 gm_{1^{st}}$ (not to violate max current cons and we also used a higher gm in 1st stage than min)

, so $rop_{2^{nd}} = rop_{1^{st}} / 5$ and $ro = VA/ID$ (L is constant, so VA is constant)
therefore $ID_{2^{nd}} = 5 ID_{1^{st}} = 50 \mu\text{A}$ (We assumed $ron = rop$ to get ID of this stage, that's not true)

ID = 50uA , rop2 = rop1/5 = 198k

PMOS Load Sizing

We'll use 1:5 mirroring to achieve that ID , so

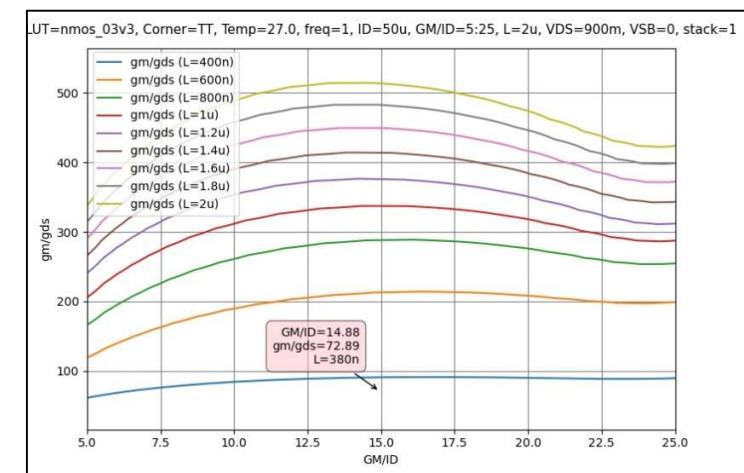
L = 450nm

W = 5*21 = 105um

Since we know both of gm and ID

, so we'll use gm/ID = 14.88 to get higher gm

2nd Stage Gain = $gmn (ron||rop) \geq 31.62 \rightarrow ron_2 = 67k$
 $\rightarrow gmro \geq 42$



LUT Settings		
ID	50u	
W	29.97u	
L	380n	
VDS	0.9	
VSB	0	
Stack	1	
Results:		
TT-27.0		
2	IG	N/A
3	L	380n
4	W	29.97u
5	VGS	721.4m
6	VDS	900m
7	VSB	0
8	gm/ID	14.88
Y-Expr gm/ID*fT		

NMOS Input Sizing

L= 380nm

W= 29.97um

Fifth: NMOS Current Mirror Load Resizing

It's important to do that to minimize systematic offset by making VGS of CM load in 1st stage to be equal to VGS of input of 2nd stage. (I mentioned that above).

We have four parameters for MOSFET. ID , W , L , Bias point(V*,VGS,gm/ID)
We'll change Bias point(VGS) while keeping ID and L constant, so W will change.

When I did the simulation using this sizing, it didn't go well
so I managed to reduce W until it worked well.

CM load Sizing

L= 470nm

W=4.98um

After we run dc analysis to see DC OP, we calculated suitable Rz to make zero at infinity

$$R_z = \frac{1}{gm8} = 1333k$$

LUT Settings

ID	5u
VGS	721.2m
L	470n
VDS	0.6
VSB	0
Stack	1

Results:

Name	TT-27.0
1 ID	4.997u
2 IG	N/A
3 L	470n
4 W	5.27u
5 VGS	721.2m
6 VDS	600m
7 VSB	0

Y-Expr gm/ID*fT

Table Showing DC OP for all transistors using SA

(These values will change when simulating)

M1 is CM load NMOS on diode connected side

M2 is CM load PMOS on output side

M3 is input PMOS on diode connected side (V_{in-})

M4 is input PMOS on output side (V_{in+})

M5 is reference current PMOS

M6 is mirrored current PMOS for 1st stage

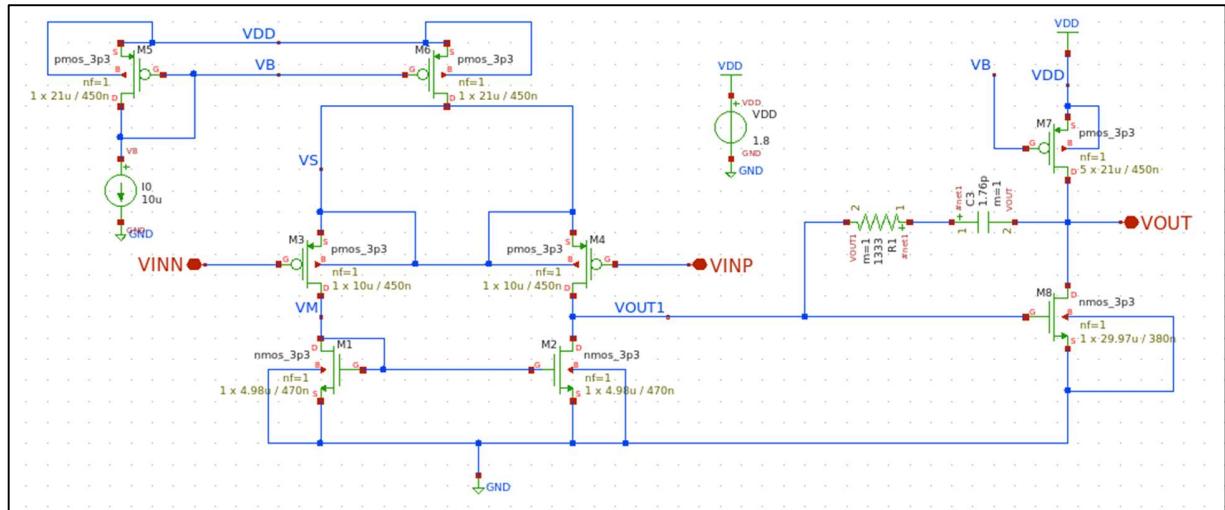
M7 is mirrored current PMOS for 2nd stage

M8 is input NMOS for 2nd stage

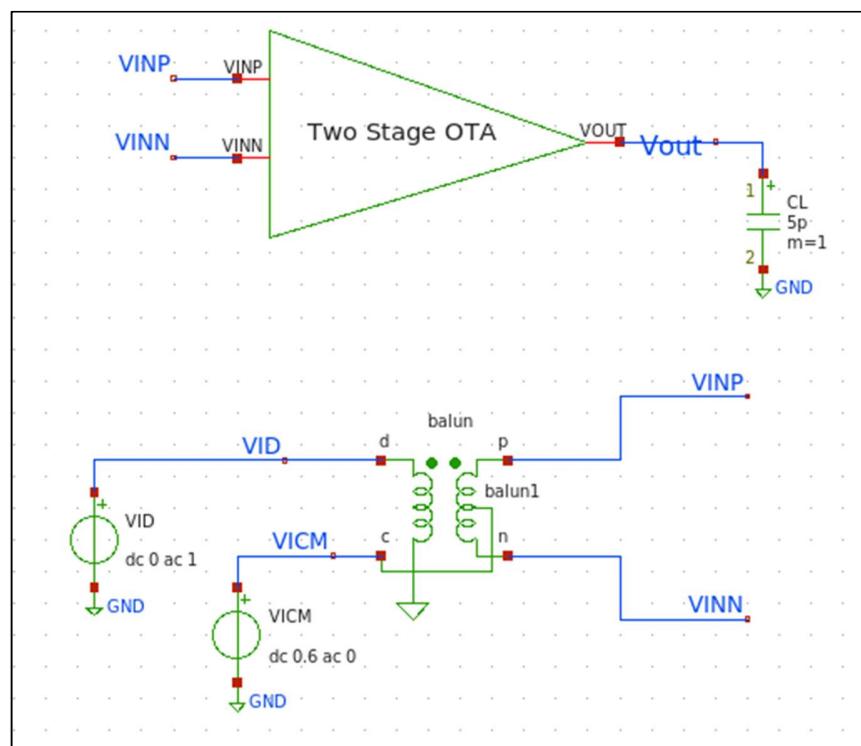
	M1 & M2	M3 & M4	M5	M6	M7	M8
W (um)	4.98	10	21	21	105	29.97
L (nm)	470	450	450	450	450	380
gm (uS)	81.74	70.7	144.2	144.2	720.8	743.8
ID (uA)	5	5	10	10	50	50
gm/ID (S/A)	16.35	14.14	14.42	14.42	14.42	14.88
VDsat	156.7m	116.4m	113.8m	113.8m	113.8m	104.3
Vov(VGS-VTH)	18.92m	74.5m	70.61m	70.61m	70.61m	34.17m
V*(2ID/gm)	122.3m	141.4m	138.7m	138.7m	138.7m	134.4m

PART 3: Open Loop OTA simulation

Schematic



Testbench



1) DC Operating point

```
==== Calculated Parameters ====
M1: gm/id = 16.5283 S/A, Vstar = 0.121004 V, ro = 1.64186E+06 ohms
M2: gm/id = 16.5283 S/A, Vstar = 0.121004 V, ro = 1.64186E+06 ohms
M3: gm/id = 14.6214 S/A, Vstar = 0.136785 V, ro = 2.46264E+06 ohms
M4: gm/id = 14.6214 S/A, Vstar = 0.136785 V, ro = 2.46264E+06 ohms
M5: gm/id = 14.6378 S/A, Vstar = 0.136633 V, ro = 1.26309E+06 ohms
M6: gm/id = 14.6913 S/A, Vstar = 0.136135 V, ro = 784857 ohms
M7: gm/id = 14.6315 S/A, Vstar = 0.136691 V, ro = 257941 ohms
M8: gm/id = 14.9551 S/A, Vstar = 0.133734 V, ro = 104529 ohms
```

BSIM4v5: Berkeley Short Channel IGFET Model-4			
device	m.xm8.m0	m.xm7.m0	m.xm5.m0
model	nmos_3p3.12	pmos_3p3.12	pmos_3p3.12
id	5.01725e-05	5.01725e-05	1e-05
gm	0.000750334	0.000734101	0.000146378
gds	9.56672e-06	3.87685e-06	7.9171e-07
gmbs	0.000228313	0.000316561	6.31275e-05
vgs	0.721769	0.853343	0.853343
vth	0.689539	0.785449	0.78552
vds	0.902619	0.897376	0.853342
vdsat	0.103731	0.111621	0.111576

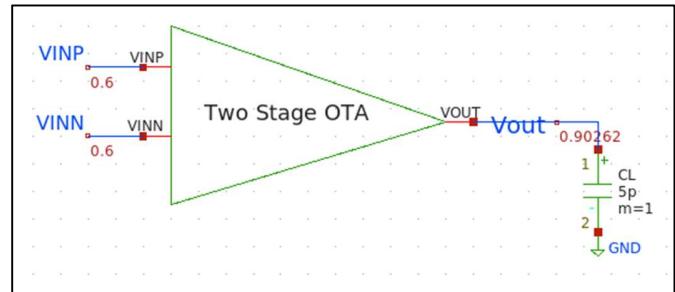
BSIM4v5: Berkeley Short Channel IGFET Model-4			
device	m.xm6.m0	m.xm1.m0	m.xm2.m0
model	pmos_3p3.12	nmos_3p3.8	nmos_3p3.8
id	9.51403e-06	4.75702e-06	4.75702e-06
gm	0.000139774	7.86255e-05	7.86255e-05
gds	1.27412e-06	6.09066e-07	6.09066e-07
gmbs	6.03397e-05	2.72441e-05	2.72441e-05
vgs	0.853343	0.72177	0.72177
vth	0.786334	0.707302	0.707302
vds	0.346117	0.721769	0.721769
vdsat	0.111066	0.094248	0.094248

BSIM4v5: Berkeley Short Channel IGFET Model-4			
device	m.xm3.m0	m.xm4.m0	m.xm2.m0
model	pmos_3p3.8	pmos_3p3.8	pmos_3p3.8
id	4.75702e-06	4.75702e-06	4.75702e-06
gm	6.95544e-05	6.95544e-05	6.95544e-05
gds	4.06068e-07	4.06068e-07	4.06068e-07
gmbs	3.00039e-05	3.00039e-05	3.00039e-05
vgs	0.853881	0.853881	0.853881
vth	0.785714	0.785714	0.785714
vds	0.73211	0.73211	0.73211
vdsat	0.111793	0.111793	0.111793

```

vout = 9.026231e-01
vinn = 6.000000e-01
vinp = 6.000000e-01
vout1 = 7.217712e-01
vm = 7.217712e-01

```

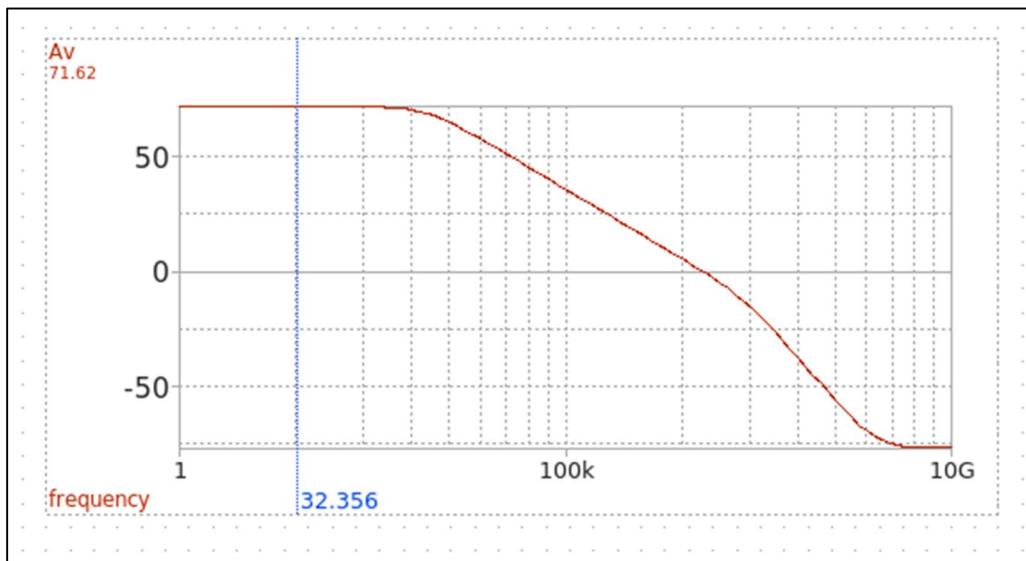


Yes, Current and gm of input pair (M3,M4) are equal because they are matched and have same bias point and there is no differential input.

The output voltage of the first stage = 721.8mv because it follows the mirror node (VGS of diode connected current mirror load (M1))

The output of the second stage = 902.6mv because there is no systematic offset between cm load nmos and second stage input nmos, so we designed it to be VDD/2 to be in the middle of output swing.

2) Diff small signal ccs



Hand Analysis

$$Avd = gm4(ro2||ro4) * gm8(ro7||ro8) = 3824 = 71.65dB$$

Comparing Avd from Simulation and Hand Analysis

	Simulation	Hand Analysis
Avd(dB)	71.62	71.65

```

==== AC Results ====
Av Diff: 71.6172 dB, BW: 1595.3 Hz
UGF: 5.94447E+06 Hz
GBW: 6.07714E+06 Hz
Av CM: -7.08954 dB, BW: 1595.3 Hz
CMRR: 78.7067 dB

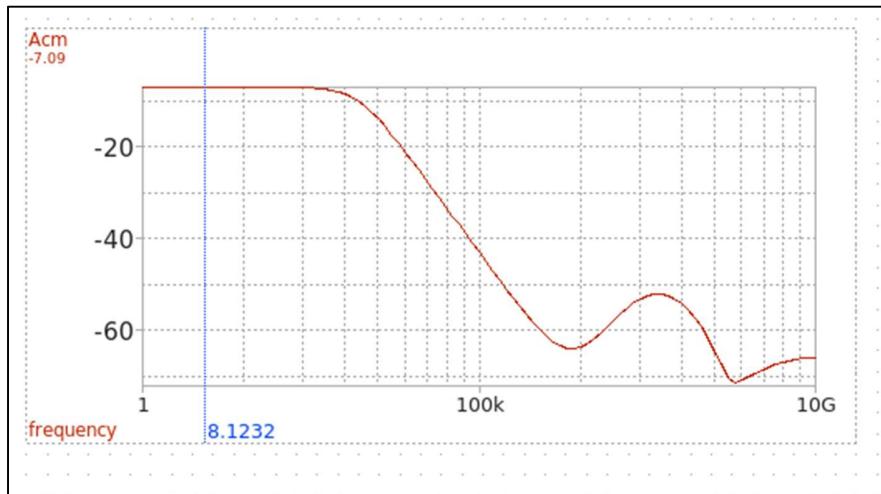
```

Hand Analysis

$$BW = wp1 = \frac{1}{2\pi(r_o2||r_o4) C_c(1 + gm8(r_o7||r_o8))} = 1625 \text{ Hz}, GBW = Av * BW = 6.2 \text{ MHz}$$

	Simulation	Hand Analysis
BW(Hz)	1595.3	1625
GBW(Hz)	6M	6.2M

3) CM small signal ccs



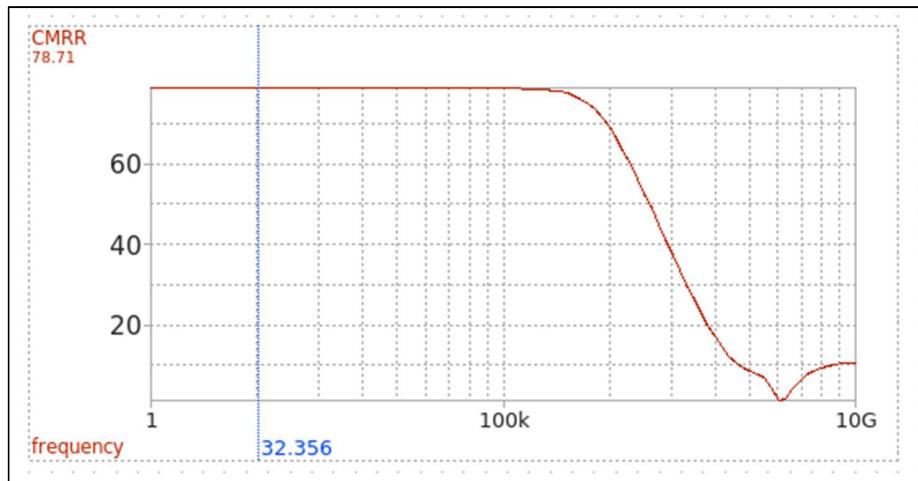
Hand Analysis

$$Acm = \frac{1}{2*gm2*r_o6} * gm8(r_o7||r_o8) = 0.452 = -6.89 \text{ dB}$$

Comparing Acm from Simulation and Hand Analysis

	Simulation	Hand Analysis
Acm(dB)	-7.09	-6.89

4) CMRR (Optional)



Hand Analysis

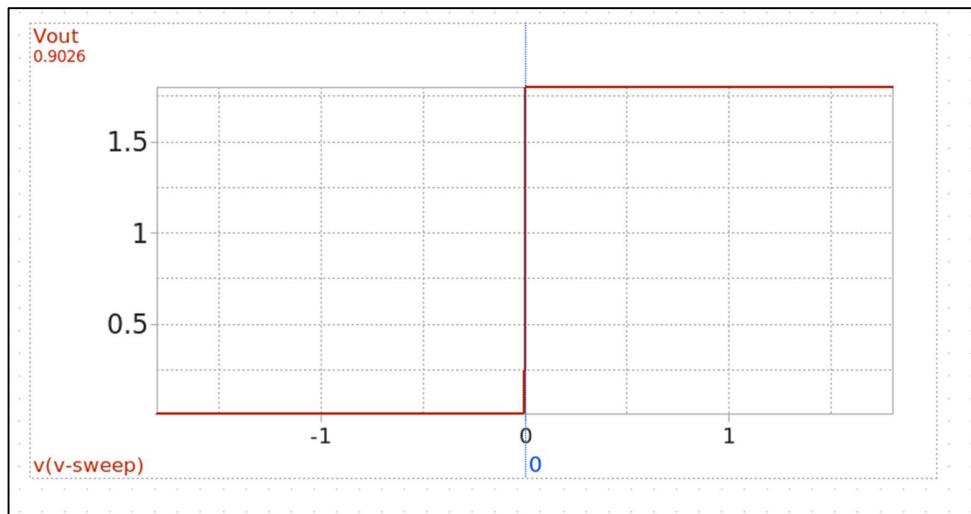
$$CMRR = Avd - Acm = 71.65 - (-6.89) = 78.54 \text{ dB}$$

Comparing CMRR from Simulation and Hand Analysis

	Simulation	Hand Analysis
CMRR(dB)	78.71	78.54

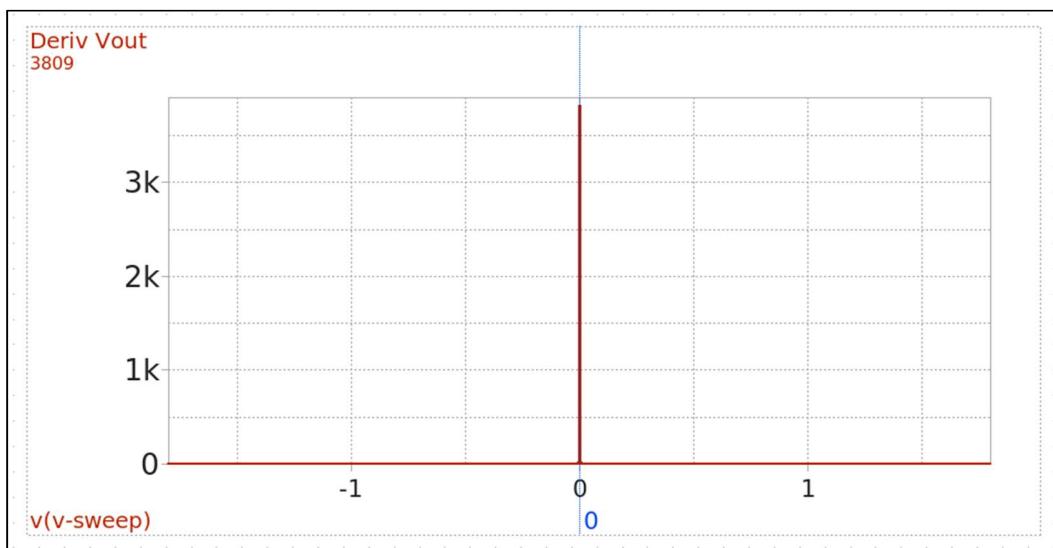
5) Diff large signal ccs (Optional)

Vout vs Vid



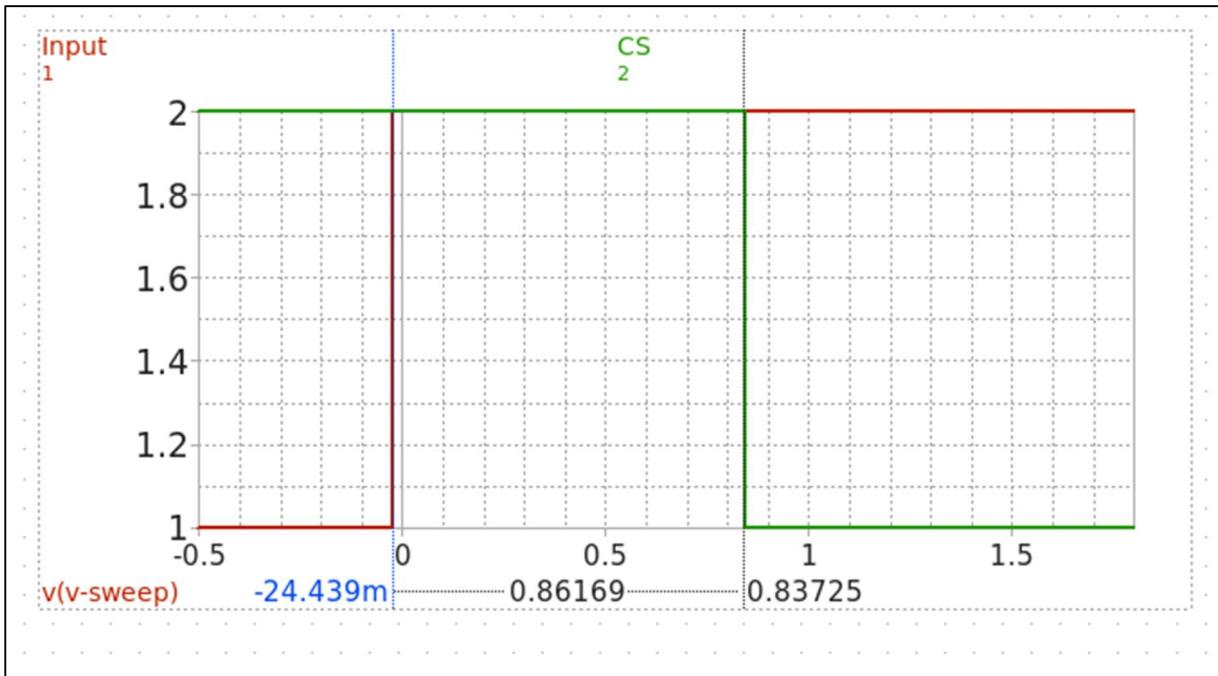
when $V_{in} = 0$, $V_{out} = 0.9026$, the reason stated in answer of a question above in DC OP.

Vout derivative vs Vid



when $V_{in}=0$, $V_{out}\ derivative = 3809 = 71.6\text{dB}$ which equals the value of Avd at the bias point of the circuit. (I used a smaller step to achieve it)

6) CM large signal ccs (region vs VICM):



Hand Analysis

$$CMIR - low = -|VGS3| + |Vdsat3| + VGS1 = -20mv$$

In case of lower input, Input pair(M3) gets out of saturation.

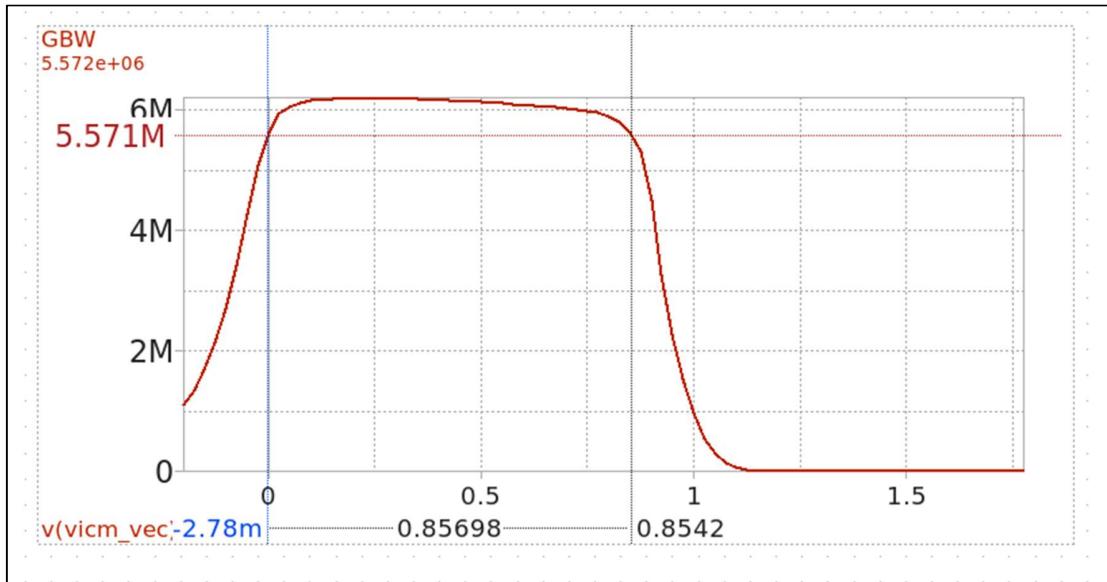
$$CMIR - high = VDD - |VGS3| - |Vdsat6| = 0.835v$$

In case of higher input, Current Source(M6) gets out of saturation.

Comparing CMIR from Simulation and Hand Analysis

	Simulation	Hand Analysis
CMIR-low(V)	-24.4m	-20m
CMIR-high(V)	0.83725	0.835

6) CM large signal ccs (GBW vs VICM) (Optional)



$$90\% * \text{max_gbw} = 90\% * 6.19\text{M} = 5.571\text{M}$$

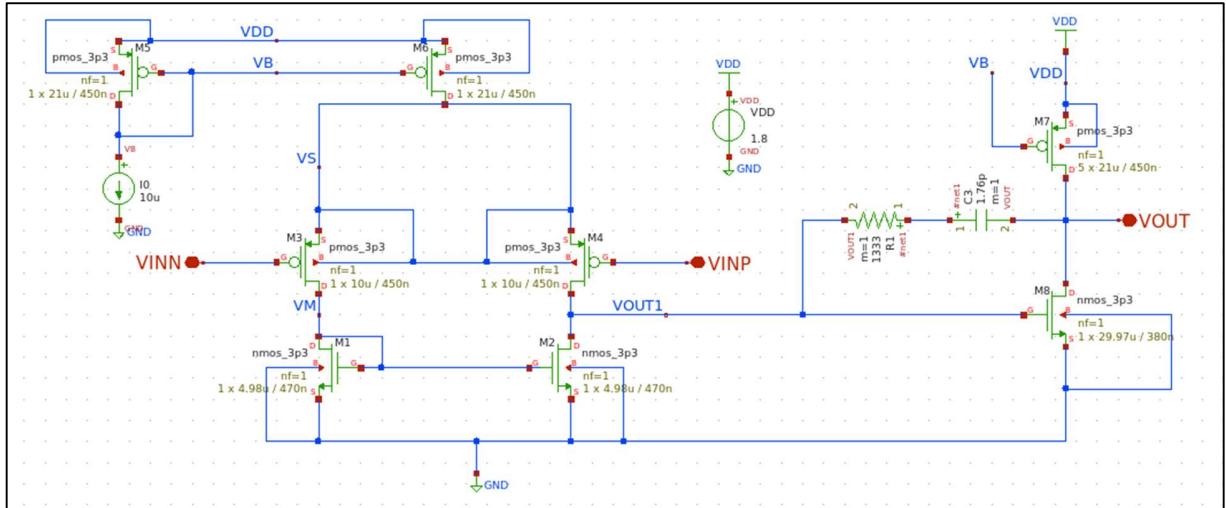
Calculated CMIR and GBW using code

```
max_gbw          =  6.190969e+06 at=  7.943282e+01
min_vinCM       =  -2.782325e-03
max_vinCM       =   8.542861e-01
min_vinCM = -2.78233e-03
max_vinCM = 8.542861e-01
cmir = 8.570684e-01
```

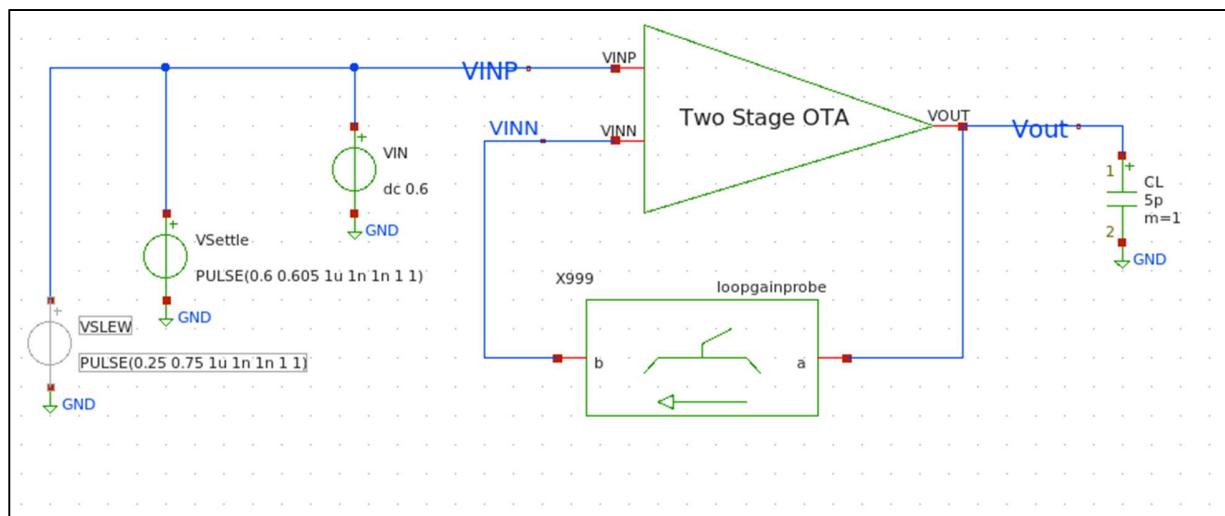
Same CMIR-high = 0.854v, but lower CMIR-low = 2mv (comparing to regions)
if we calculated them from GBW ,so CMIR = 0.857v.

PART 4: Closed Loop OTA simulation

Schematic



Testbench



1) DC Operating point

```
==== Calculated Parameters ====
M1: gm/id = 16.6111 S/A, Vstar = 0.120401 V, ro = 1.66893E+06 ohms
M2: gm/id = 16.6081 S/A, Vstar = 0.120423 V, ro = 1.67248E+06 ohms
M3: gm/id = 14.6824 S/A, Vstar = 0.136218 V, ro = 2.49559E+06 ohms
M4: gm/id = 14.6789 S/A, Vstar = 0.13625 V, ro = 2.48333E+06 ohms
M5: gm/id = 14.6363 S/A, Vstar = 0.136646 V, ro = 1.26272E+06 ohms
M6: gm/id = 14.6899 S/A, Vstar = 0.136148 V, ro = 786151 ohms
M7: gm/id = 14.5856 S/A, Vstar = 0.137122 V, ro = 288361 ohms
M8: gm/id = 14.8579 S/A, Vstar = 0.134609 V, ro = 93829.1 ohms
```

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.xm8.m0	m.xm7.m0	m.xm5.m0
model	nmos_3p3.12	pmos_3p3.12	pmos_3p3.12
id	5.10916e-05	5.12957e-05	1.00035e-05
gm	0.000759114	0.000748178	0.000146414
gds	1.06577e-05	3.46788e-06	7.91943e-07
gmbs	0.000231379	0.000322418	6.31432e-05
vgs	0.727008	0.853367	0.853367
vth	0.691246	0.784963	0.78552
vds	0.600068	1.19993	0.853366
vdsat	0.105658	0.111941	0.111591

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.xm6.m0	m.xm1.m0	m.xm2.m0
model	pmos_3p3.12	nmos_3p3.8	nmos_3p3.8
id	9.51853e-06	4.65566e-06	4.65957e-06
gm	0.000139826	7.73359e-05	7.73868e-05
gds	1.27202e-06	5.99186e-07	5.97915e-07
gmbs	6.03621e-05	2.67966e-05	2.68142e-05
vgs	0.853367	0.72048	0.72048
vth	0.786333	0.707304	0.707293
vds	0.347043	0.720479	0.727008
vdsat	0.111082	0.0935915	0.0935974

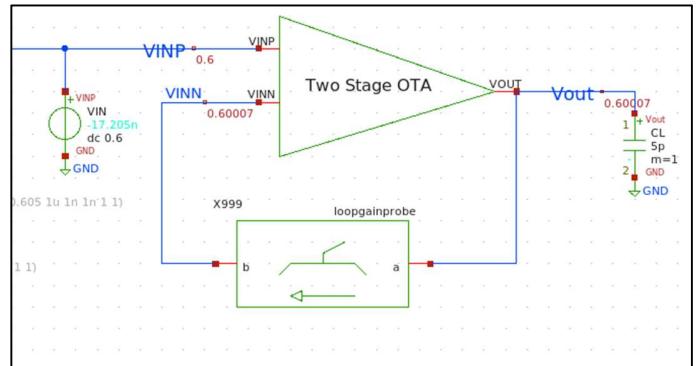
BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.xm3.m0	m.xm4.m0
model	pmos_3p3.8	pmos_3p3.8
id	4.68811e-06	4.69043e-06
gm	6.88325e-05	6.88502e-05
gds	4.00707e-07	4.02685e-07
gmbs	2.96927e-05	2.97007e-05
vgs	0.852883	0.852955
vth	0.785714	0.785724
vds	0.732473	0.725945
vdsat	0.111166	0.111205

```

vout = 6.000719e-01
vinn = 6.000719e-01
vinp = 6.000000e-01
vout1 = 7.270101e-01
vm = 7.204814e-01

```



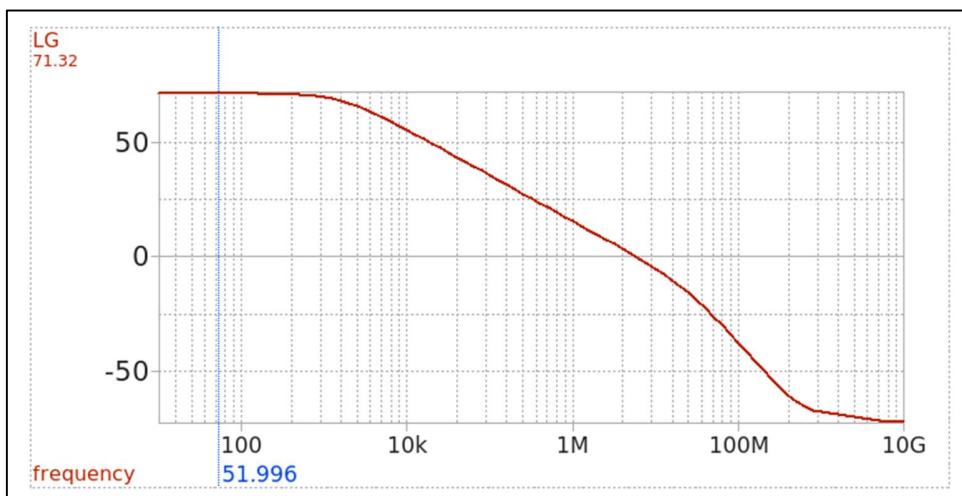
No, Vout of CL isn't equal Vout in OL
because Vout follows Vinn in this way it becomes defined

Vinp is different from Vinn as there must be a finite differential input because gain is finite
In the second stage as Vout is defined, making PMOS controls I in the branch setting VGS of the NMOS, therefore setting Vout1 that's Why Vout1 doesn't follow VM anymore

No, Current and gm of input pair (M3,M4) aren't equal because there is a small differential input which causes difference in their VGS.

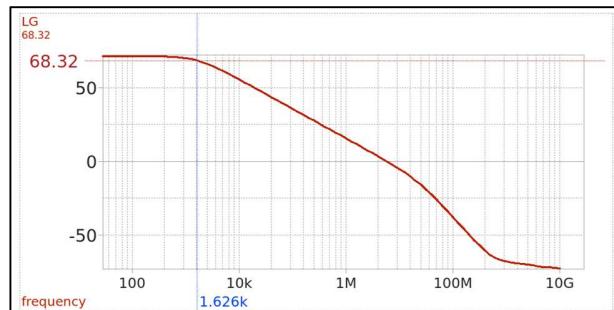
2) Loop Gain

Magnitude in dB

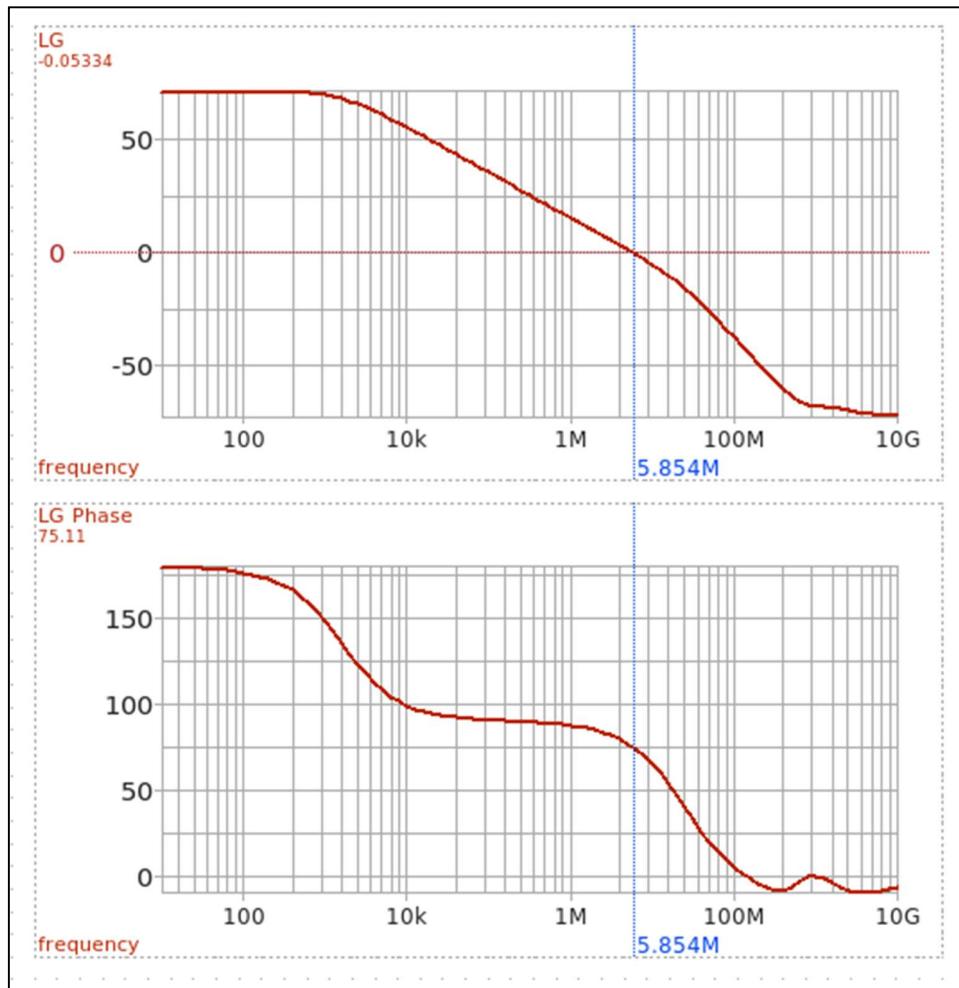


$$71.32 \text{dB} - 3 \text{dB} = 68.32 \text{dB}$$

to get BW



Phase



Simulation Results

```
dc_loop_gain      =  7.132590e+01
gain_crossover_freq =  5.854596e+06
pm = 7.519049e+01
```

BW, LG (from plot) = 1626 Hz

*GBW, LG = LG * BW, LG = 3681.29 * 1626 = 5.98MHz*

Comparing Open loop and Loop Gain

	Open Loop	Loop gain
DC gain(dB)	71.6	71.32
UGF(Hz)	5.944M	5.85M
GBW(Hz)	6.07M	5.98M

Hand Analysis

$$GX = GBW, ol = 6.2MHz \rightarrow 38.95 \text{ Mrad/sec}$$

$$wp2 = \frac{gm8}{Cl} = 151.8\text{M}, PM = 90 - \tan^{-1}\left(\frac{GX}{wp1}\right) = 75.6^\circ$$

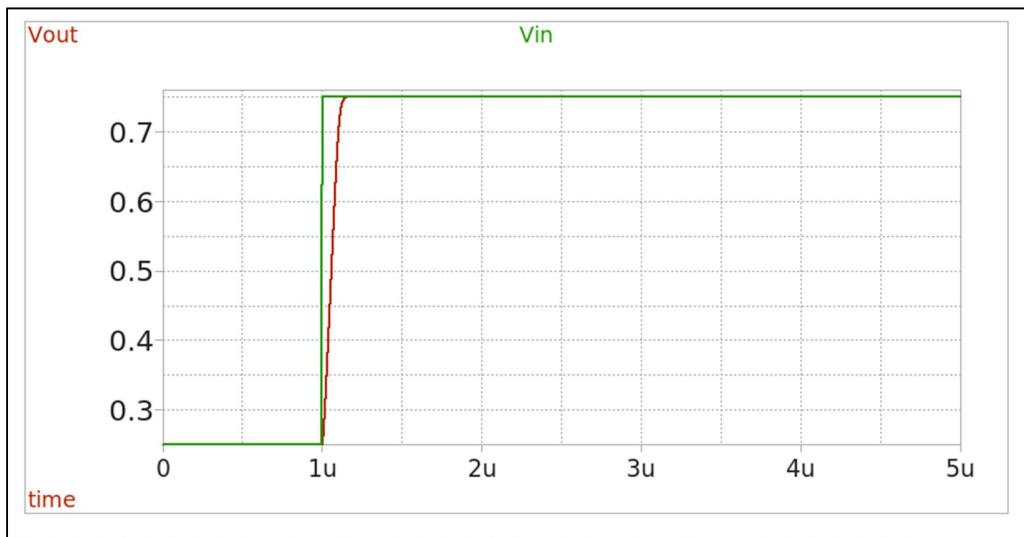
$$LG = \beta Aol = 3824 = 71.65dB$$

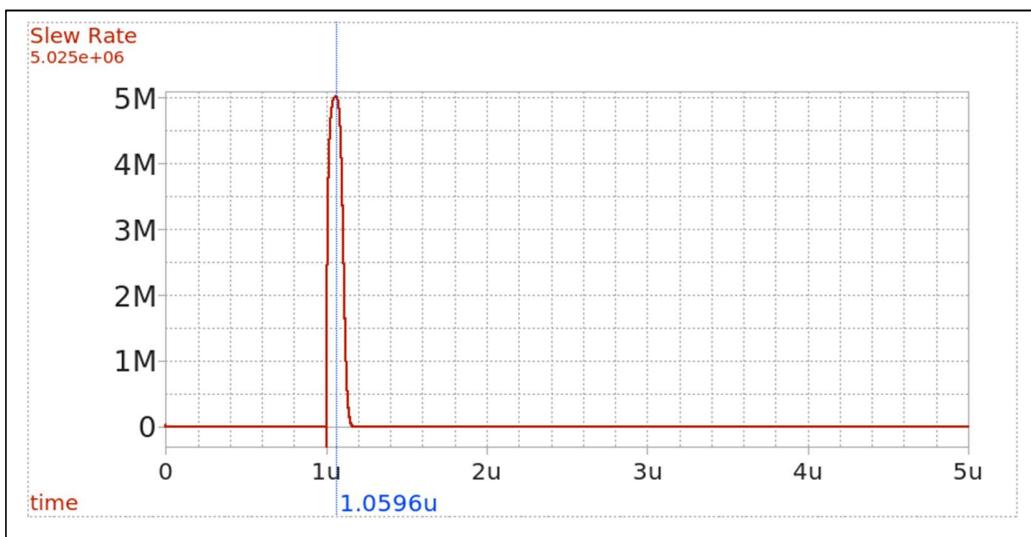
$$GBW = Aol * BWol = GBW, ol = 6.2\text{M}$$

Comparing Results of Simulation and Hand Analysis

	Simulation	Hand Analysis
LG(dB)	71.32	71.65
GBW(Hz)	5.98M	6.2M
GX(Hz)	5.85M	6.2M
PM(deg)	75.2	75.6

Slew Rate is maximum value in $\text{der}(V_{out})/\text{time}$





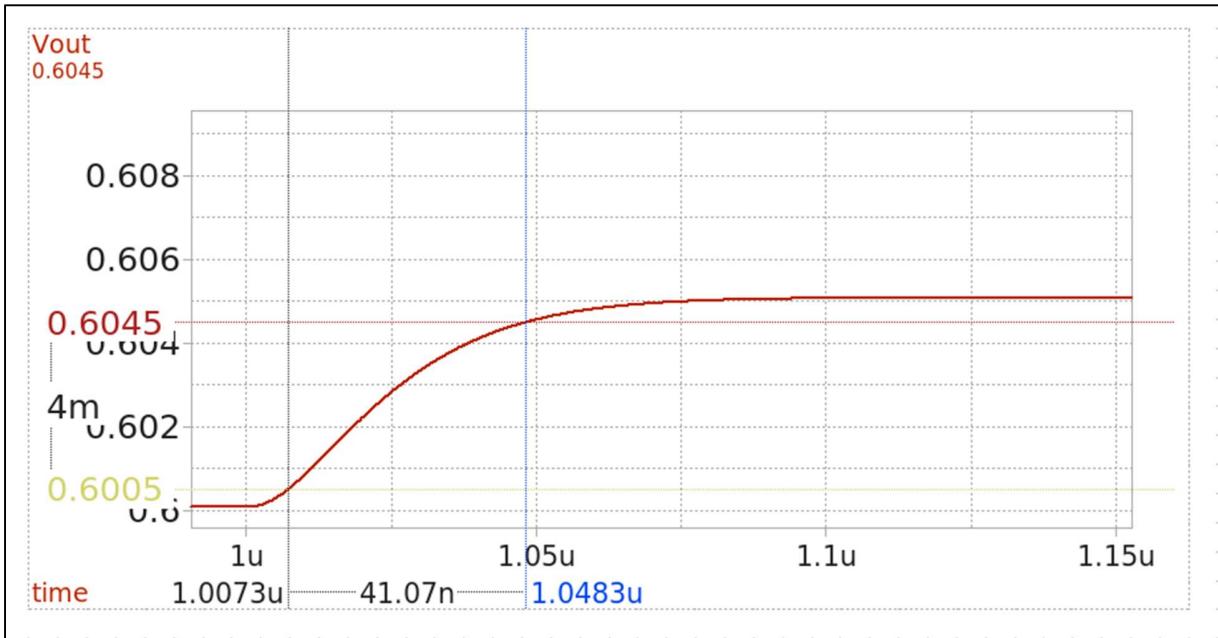
Hand Analysis

$$\text{Slew rate} = \frac{I_{SS}}{C_C} = 5.68\text{M}$$

Comparing Slew Rate from Simulation and Hand Analysis

	Simulation	Hand Analysis
Slew Rate	5.025M	5.68M

Settling time



Hand Analysis

$$Rise\ time = 2.2 \tau_{cl} = \frac{2.2}{BW, cl} = \frac{2.2}{2\pi GBW, Hz} = 56ns$$

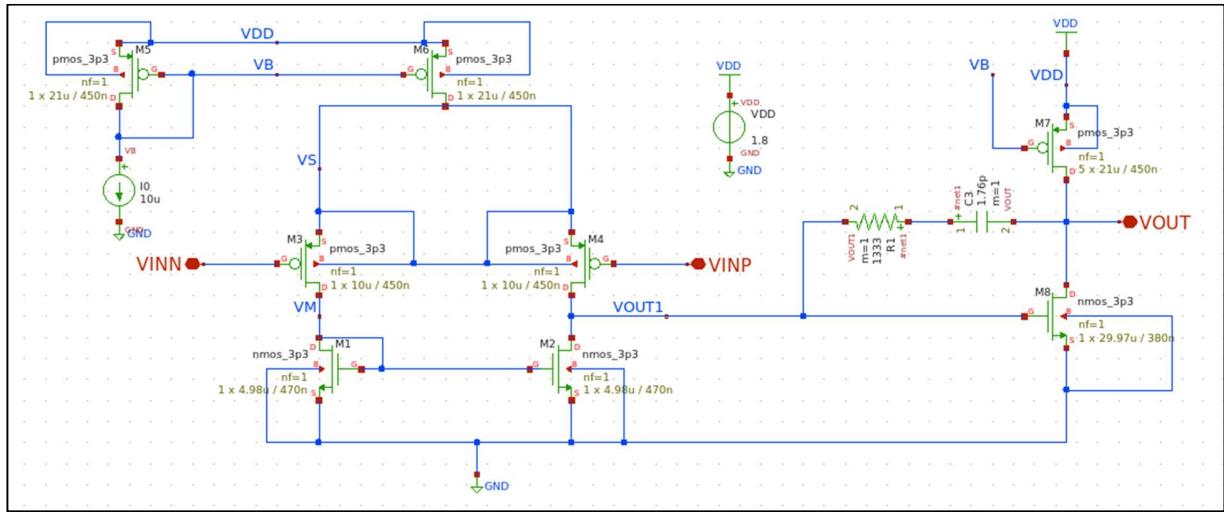
Comparing Rise time from Simulation and Hand Analysis

	Simulation	Hand Analysis
Rise time(sec)	41.07n	56n

There is a difference between simulation results and hand analysis results because we are using first order system approximation to calculate rise time, but our amplifier is second order system

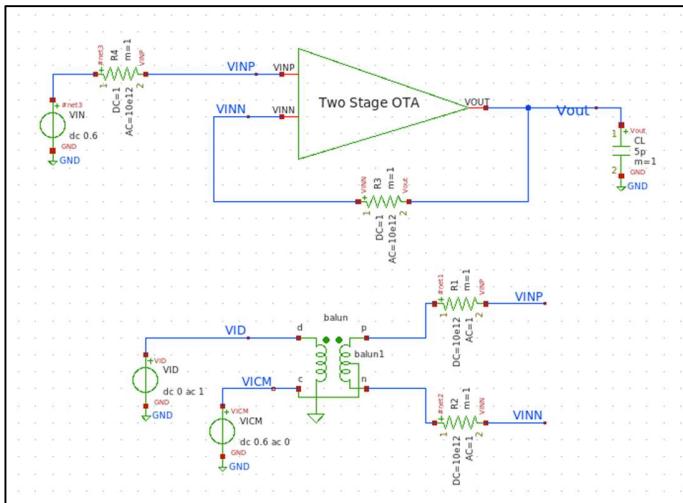
PART 5: DC Closed Loop AC Open-Loop OTA simulation (Optional)

Schematic



Testbench

I used DC,AC resistances instead of switches due to xschem limitations



1) DC Operating point

```
==== Calculated Parameters ====
M1: gm/id = 16.5297 S/A, Vstar = 0.120994 V, ro = 1.64231E+06 ohms
M2: gm/id = 16.5272 S/A, Vstar = 0.121013 V, ro = 1.64527E+06 ohms
M3: gm/id = 14.623 S/A, Vstar = 0.136771 V, ro = 2.46356E+06 ohms
M4: gm/id = 14.6188 S/A, Vstar = 0.13681 V, ro = 2.45271E+06 ohms
M5: gm/id = 14.6378 S/A, Vstar = 0.136633 V, ro = 1.26309E+06 ohms
M6: gm/id = 14.6913 S/A, Vstar = 0.136135 V, ro = 784763 ohms
M7: gm/id = 14.587 S/A, Vstar = 0.137108 V, ro = 288445 ohms
M8: gm/id = 14.8429 S/A, Vstar = 0.134745 V, ro = 93567.9 ohms
```

BSIM4v5: Berkeley Short Channel IGFET Model-4			
device	m.x1.xm8.m0	m.x1.xm7.m0	m.x1.xm5.m0
model	nmos_3p3.12	pmos_3p3.12	pmos_3p3.12
id	5.12779e-05	5.12779e-05	1e-05
gm	0.00076111	0.000747993	0.000146378
gds	1.06874e-05	3.46687e-06	7.9171e-07
gmbs	0.00023199	0.000322338	6.31275e-05
vgs	0.727253	0.853343	0.853343
vth	0.691246	0.784963	0.78552
vds	0.600076	1.19992	0.853342
vdsat	0.105793	0.111926	0.111576

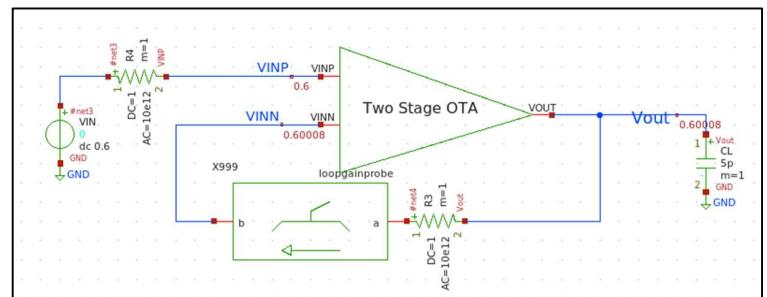
BSIM4v5: Berkeley Short Channel IGFET Model-4			
device	m.x1.xm6.m0	m.x1.xm1.m0	m.x1.xm2.m0
model	pmos_3p3.12	nmos_3p3.8	nmos_3p3.8
id	9.51396e-06	4.75531e-06	4.75866e-06
gm	0.000139773	7.86038e-05	7.86473e-05
gds	1.27427e-06	6.089e-07	6.07803e-07
gmbs	6.03392e-05	2.72366e-05	2.72516e-05
vgs	0.853343	0.721748	0.721748
vth	0.786334	0.707302	0.707293
vds	0.346061	0.721747	0.727253
vdsat	0.111066	0.094237	0.094242

BSIM4v5: Berkeley Short Channel IGFET Model-4			
device	m.x1.xm3.m0	m.x1.xm4.m0	m.x1.xm2.m0
model	pmos_3p3.8	pmos_3p3.8	nmos_3p3.8
id	4.75531e-06	4.75866e-06	4.75866e-06
gm	6.95366e-05	6.95657e-05	6.95657e-05
gds	4.05916e-07	4.07713e-07	4.07713e-07
gmbs	2.99963e-05	3.00091e-05	3.00091e-05
vgs	0.853856	0.853937	0.853937
vth	0.785714	0.785723	0.785723
vds	0.732187	0.726681	0.726681
vdsat	0.111777	0.111822	0.111822

```

vout = 6.000804e-01
vinn = 6.000804e-01
vinp = 6.000000e-01
vout1 = 7.272550e-01
vm = 7.217496e-01

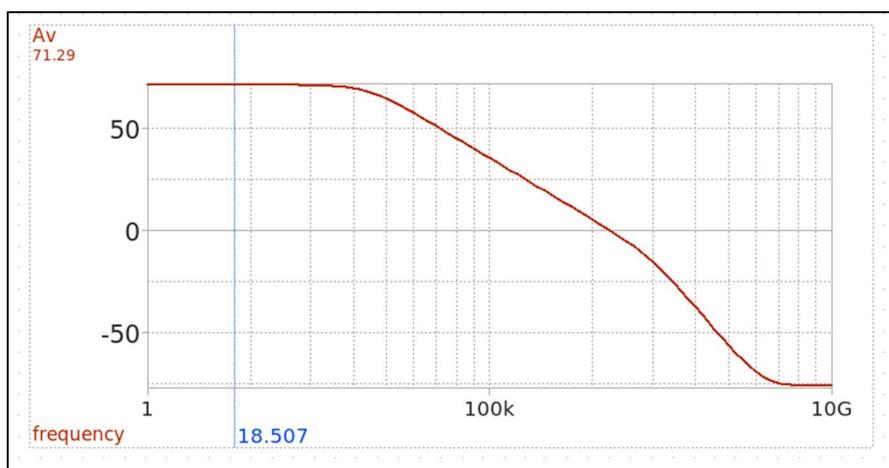
```



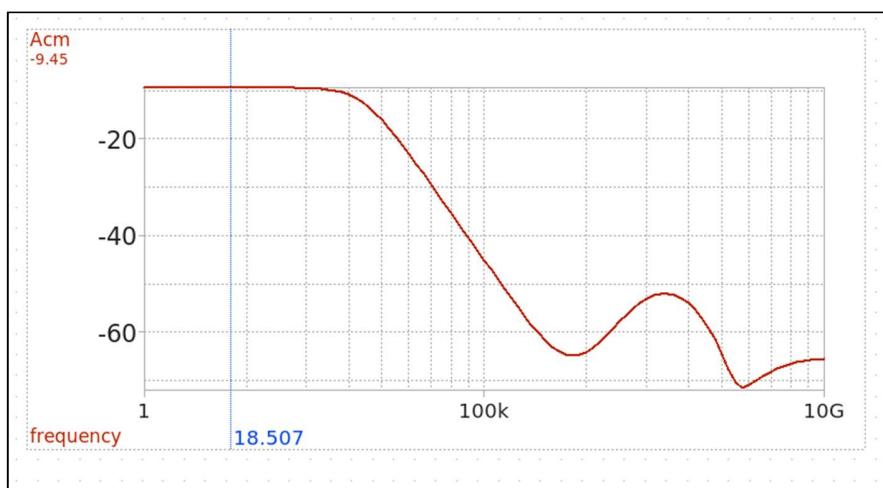
DC op results are very close to Closed loop DC op results.

2) Small Signal Analysis

Differential Gain



Common Mode Gain



```
Av Diff: 71.2922 dB, BW: 1658.05 Hz
UGF: 5.94562E+06 Hz
GBW: 6.08423E+06 Hz
Av CM: -9.44991 dB, BW: 1658.05 Hz
CMRR: 80.7421 dB
```

AC results are close to Open loop AC op results, so this technique helped us to achieve that. (not exactly due to mismatch in input pair)

Implementation of Rz by a MOSFET (Bonus)

MOSFET can work as a voltage controlled resistance if it's biased in Deep Triode (Linear) Region where VDS is too small close to zero. Value of R is controlled by VGS linearly.

We'll use NMOS and bias it with $VDD = 1.8v$.

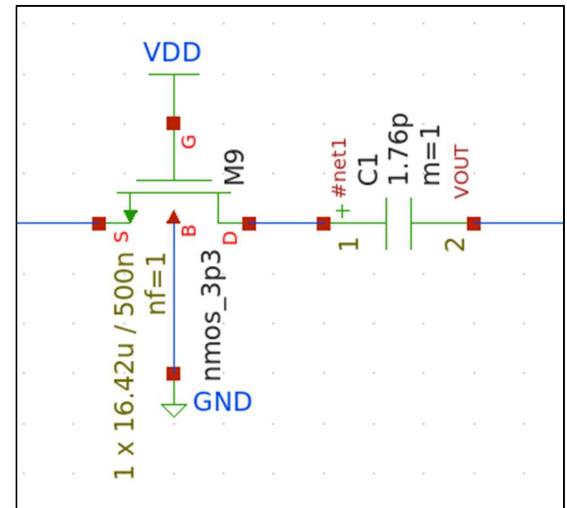
$VG = 1.8v$

$VS = vout1 = 721.7mV$ (obtained from DC op), so $VGS = 1.078$

$VSB = 721.7mV$

$VDS = 10m$ (very small to operate in Linear Region)

$$Rz = \frac{1}{gm8} = 1333k$$



using ADT to obtain its sizing

assuming $L=500nm$

L=500nm

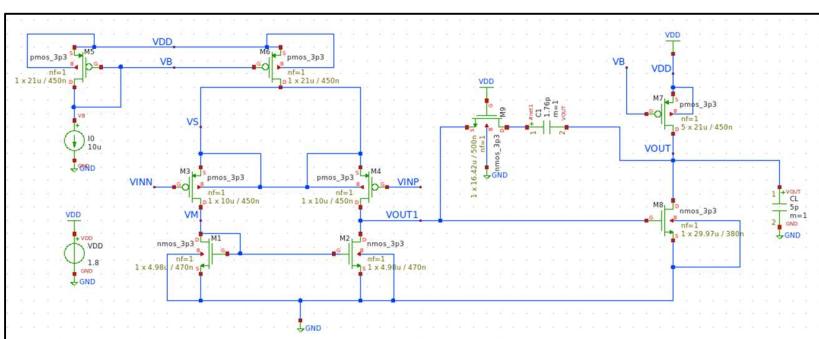
W=16.42um

LUT Settings

LUT	nmos_03v3
Corner	TT
Temp (°C)	27.0
Frequency	1
Ron	1333
VGS	1.0782288
L	500n
VDS	1m
VSB	0.7217712
Stack	1

Results:

Name	TT-27.0
3 L	500n
4 W	16.42u



device	m.xm9.m0
model	nmos_3p3.12
id	7.21139e-13
gm	4.14462e-12
gds	0.000765184
gmbs	1.09354e-12
vgs	1.07823
vth	0.927099
vds	-9.42439e-10
vdsat	0.188117

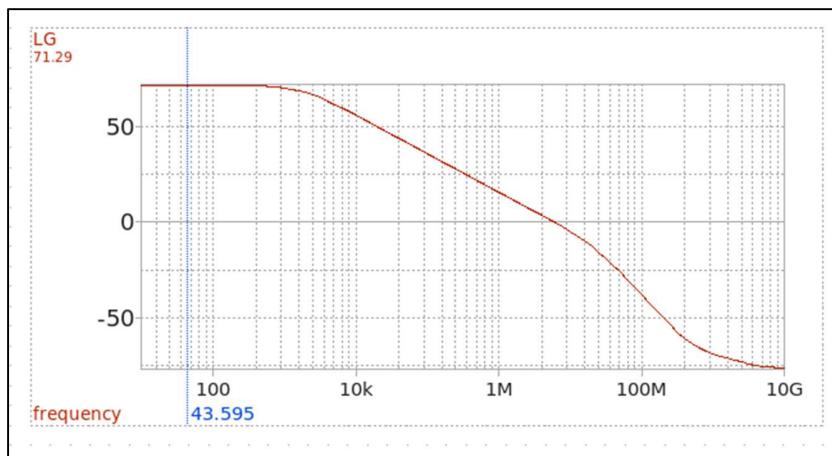
We ran DC analysis on OL

To make sure that our sizing is right and Zero is cancelled

We ran AC analysis on OL

```
==== AC Results ====
Av Diff: 71.6171 dB, BW: 1594.19 Hz
UGF: 5.9274E+06 Hz
GBW: 6.07293E+06 Hz
Av CM: -7.08896 dB, BW: 1594.19 Hz
CMRR: 78.7061 dB
```

We ran STB analysis on CL



```
dc_loop_gain      = 7.129483e+01
gain_crossover_freq = 5.983765e+06
pm = 7.454052e+01
```

Our sizing is right! zero is cancelled and also close results to our previous simulations

Summary of Specs achieved

	Required	Achieved
Supply Voltage	1.8V	1.8V
Load	5pF	5pF
Static gain error	$\leq 0.05\%$	0.027 %
CMRR @ DC	$\geq 74dB$	78.71
Phase Margin	$\geq 70^\circ$	75.2°
OTA Current Consumption	$\leq 60\mu A$	60 uA
CMIR – low	$\leq 0.2V$	-2.78m
CMIR – high	$\geq 0.8V$	0.8542m
Output Swing	0.2v – 1.6v	0.1v – 1.69v
Buffer closed loop rise time	$\leq 70ns$	41.07ns
Slew rate (SR)	5V/ μs	5.025V/ μs

$$\text{Static gain error} = 100\%/\text{LG} = 100\%/3681.3 = 0.027 \%$$

$$V_{out}(\text{max}) = V_{DD} - V_{Dsat7} = 1.8 - 0.111621 = 1.69v$$

$$V_{out}(\text{min}) = V_{Dsat8} = 0.1$$

all specs are achieved.