Bilkent University

EE-202 Circuit Theory

Lab 4

Waveform Generator

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Section 02

Introduction

This lab aims to design a circuit that generates the voltage waveform shown in Figure 1. The design should be based on OPAMPs and RC circuits. The specifications are given in Figure 2.

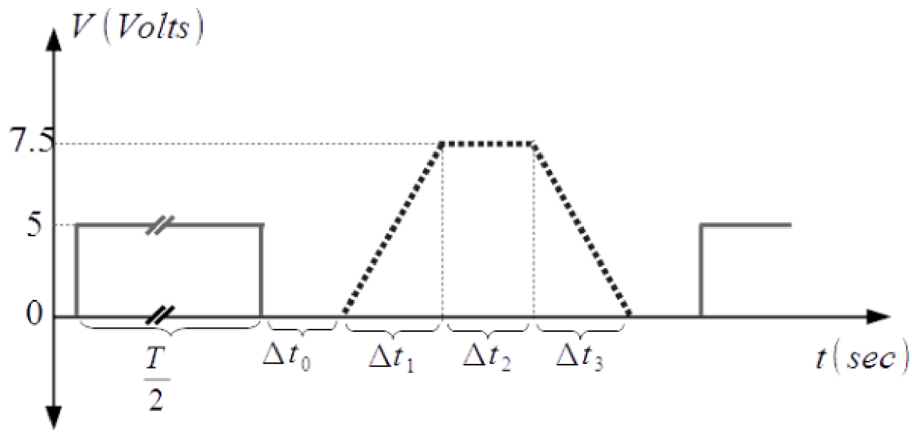

Figure 1: Required waveform

$$\Delta t_0 = 3ms, \quad \Delta t_1 = 2ms, \quad \Delta t_2 = 3ms, \quad \Delta t_3 = 2ms$$

Input peak voltage: $5V$

Output peak voltage: $7.5V$

Input frequency: $f < 50Hz, \quad T = \frac{1}{f}$

Figure 2: Specifications for Δt's and frequencies

For this experiment, f is chosen as 20 Hz. Therefore, the input is a square wave with a 5V peak value and 20 Hz frequency.

Analysis

There are three steps to generate a delayed trapezoid waveform:

1. Creating 3 ms (Δt_0) and 10 ms (sum of all Δt's) delays, in other words, shifting the wave
2. Integrating both waveforms to create the required shape (skew-lines)
3. Subtracting one waveform from another.

In the design, LM324 model OPAMP is used. The Vcc inputs for the OPAMPs are Vcc+ = 9V, Vcc- = 0V.

Step 1: Delay Circuit

To achieve 3 ms and 10 ms delays, a comparator OPAMP can be used. A reference voltage is added to the V- input of the OPAMP. This voltage is Vcomp = 2.5V. To the V+ input, an RC circuit is added. The comparator circuit's function is caused by the OPAMP's operating region:

- When V+ is greater than Vcomp (reference voltage at V-) the OPAMP is in the positive saturation region, where Vout=Vcc+.
- When V+ is smaller than Vcomp (reference voltage at V-) the OPAMP is in the negative saturation region, where Vout=Vcc-.

Figures 3 shows the delay circuits on LTSpice.

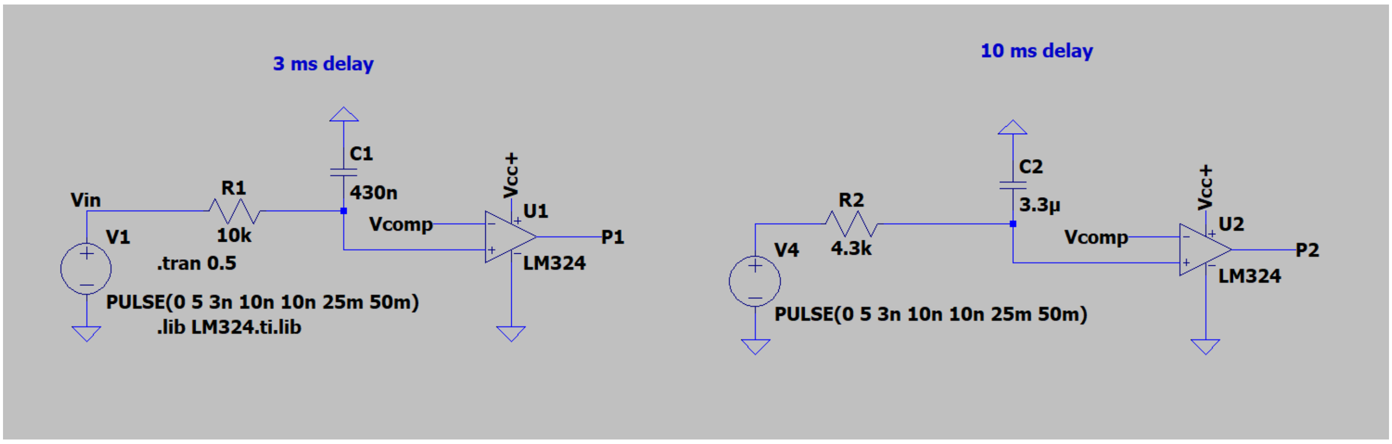

Figure 3: Delay circuits using comparator OPAMPs

To find the values of R and C, firstly KCL at the + input is considered:

$$\frac{dV_c}{dt} * C + \frac{V_c - V_{in}}{R} = 0 \quad \Rightarrow \quad \frac{dV_c}{dt} + \frac{V_c}{RC} = \frac{V_{in}}{RC} \tag{1}$$

To solve (1), a differential equation, the characteristic equation should be found as:

$$\lambda + \frac{1}{RC} = 0 \Rightarrow \lambda = -\frac{1}{RC}$$

Therefore, the natural response is:

$$V_{c,nat} = c_1 * e^{-\frac{t}{RC}}$$

and the forced response, caused by the input, is found as:

$$V_{c,forced} = V_{in}$$

To determine c_1, the fact that at t=0, V_c=0 (initial condition) is used, therefore c_1= -5. Putting all together, the solution for V_c is obtained as:

$$V_c = V_{c,nat} + V_{c,forced} = -5e^{-\frac{t}{RC}} + 5$$

Using this, the value of V_c should be equal to Vcomp = 2.5V at t = 3ms and t = 10ms to achieve delays. For t = 3ms:

$$2.5 = -5e^{-\frac{3ms}{R_1C_1}} + 5 \Rightarrow e^{-\frac{3ms}{R_1C_1}} = \frac{1}{2}$$

$$R_1 * C_1 = 0.0043$$

and for t = 10ms:

$$2.5 = -5e^{-\frac{10ms}{R_2C_2}} + 5 \Rightarrow e^{-\frac{10ms}{R_2C_2}} = \frac{1}{2}$$

$$R_2 * C_2 = 0.0144$$

After some trial and error, the chosen values that satisfy the conditions are:

$$R_1 = 10k\Omega \,, C_1 = 430nF$$

$$R_2 = 4.3k\Omega \,, C_2 = 3.3\mu F$$

The output voltage Vout is E_{sat} (slightly lower than Vcc+ = 9V) when the OPAMP is positively saturated, and Vout= Vcc- = 0V when the OPAMP is negatively saturated, since the OPAMP is operating in the non-linear region.

Step 2: Integrator Circuit

Second step is to integrate the waveforms to generate skew lines as in the required output. By using an integrator circuit, shown in Figure 4, and integrating a step function, the skew line can be obtained. The outputs of the delay circuits P1 and P2, which are essentially step functions, are connected to the circuit.

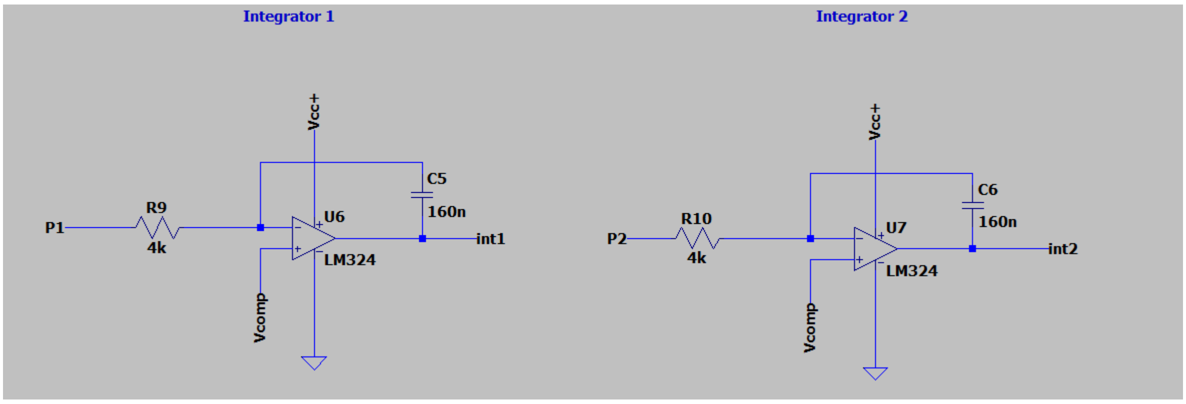

Figure 4: Integrator circuits

To derive the output equation, first KCL at V- is considered:

$$\frac{dV_c}{dt} * C + \frac{V_- - V_{in}}{R} = 0 \xrightarrow[\substack{OPAMP \\ is\ in\ the\ linear \\ region,\ \ V+ = V-}]{} dV_c = \frac{V_{in} - V_+}{RC} dt$$

Integrating both sides;

$$\int \frac{V_{in} - V_+}{RC} dt = V_c \quad \Rightarrow V_c = \frac{V_{in} - V_+}{RC} * t + K$$

To determine K, the fact that at t=0, V_c=0 (initial condition) is used, therefore K=0. Putting all together, the solution for V_c is obtained as:

$$V_c = \frac{V_{in} - V_+}{RC} * t \Rightarrow V_c = \frac{2.5}{RC} * t$$

At t=2ms (since Δt_1 = 2ms), V_C should be equal to V_{max}=7.5V as required:

$$7.5 = \frac{2.5}{RC} * 2ms \Rightarrow \ R * C = 6.67 * 10^{-4}$$

After some trial and error, the following values are chosen:

$$R = 4k\Omega, C = 160nF$$

The values for 3 ms and 10 ms circuits are the same since the skew lines are the same for them.

Step 3: Subtractor Circuit

The final step is to subtract two waveforms from one another to obtain the required shape. The subtractor circuit can again be constructed using an OPAMP, shown in Figure 5.

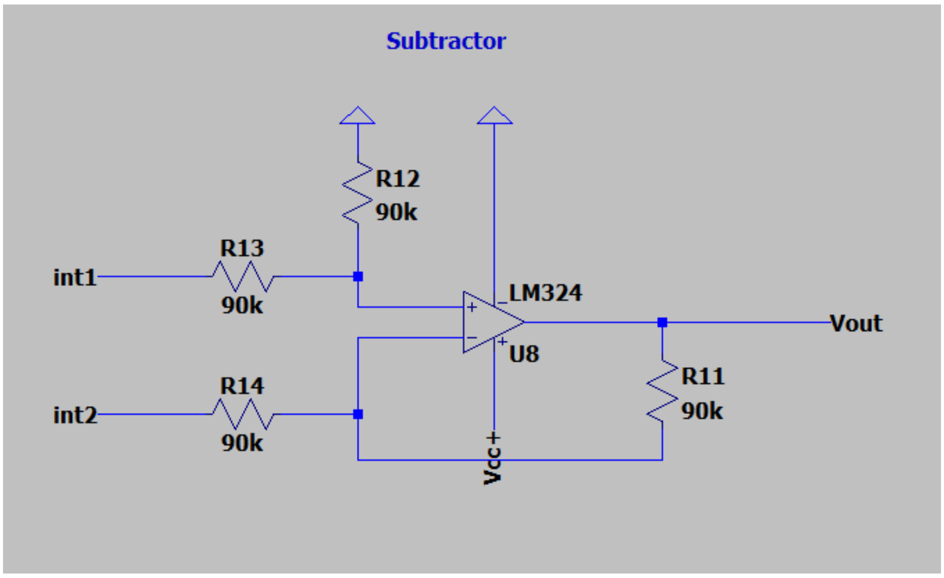

Figure 5: Subtractor circuit

KCL at V-:

$$\frac{V_{int,2} - V_-}{R_{14}} = \frac{V_- - V_{out}}{R_{11}} \quad \Rightarrow \quad V_- = \left(\frac{V_{int,2}}{R_{14}} + \frac{V_{out}}{R_{11}}\right) * \frac{1}{\left(\frac{1}{R_{11}} + \frac{1}{R_{14}}\right)}$$

KCL at V+:

$$\frac{V_{int,1} - V_+}{R_{13}} = \frac{V_+}{R_{12}} \quad \Rightarrow \quad V_+ = \frac{V_{int,1}}{R_{13}\left(\frac{1}{R_{12}} + \frac{1}{R_{13}}\right)}$$

Assuming the OPAMP is operating in the linear region:

$$V_- = V_+ \quad \Rightarrow \quad \left(\frac{V_{int,2}}{R_{14}} + \frac{V_{out}}{R_{11}}\right) * \frac{1}{\left(\frac{1}{R_{11}} + \frac{1}{R_{14}}\right)} = \frac{V_{int,1}}{R_{13}\left(\frac{1}{R_{12}} + \frac{1}{R_{13}}\right)}$$

It can be seen that choosing $R_{11} = R_{12} = R_{13} = R_{14}$, the equation reduces to:

$$V_{out} = V_{int,1} - V_{int,2}$$

For this case, all resistors are chosen as 90kΩ.

Simulations

The circuit is implemented on LTSpice with the calculated values as seen in Figure 6.

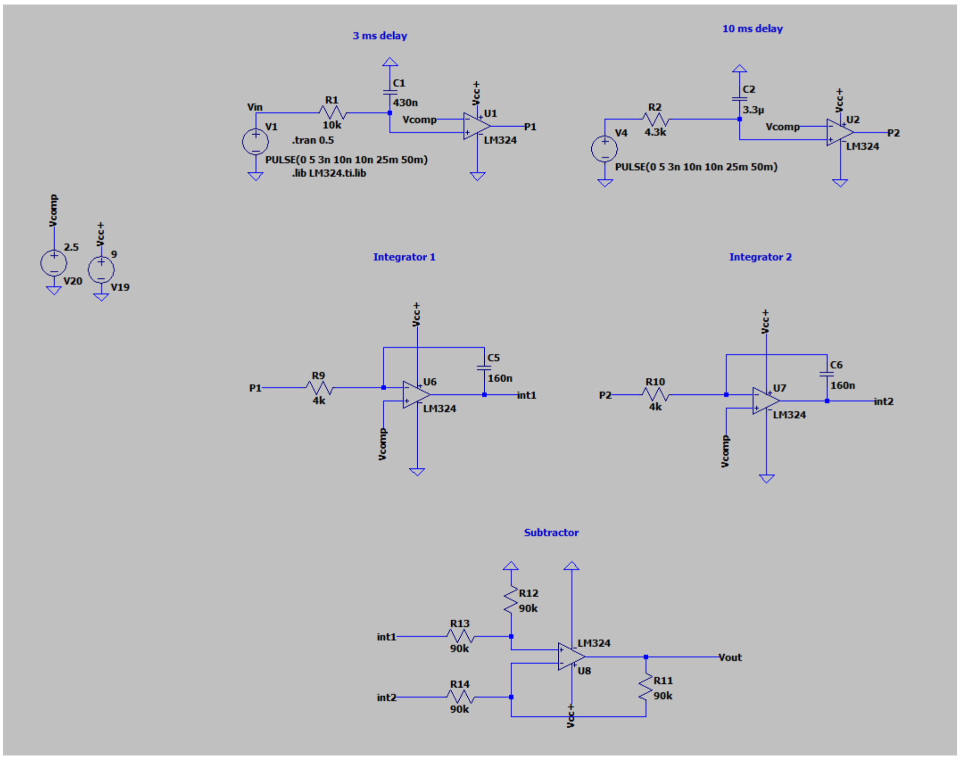

Figure 6: Software circuit

Figures 7-15 show the measurements on the plots.

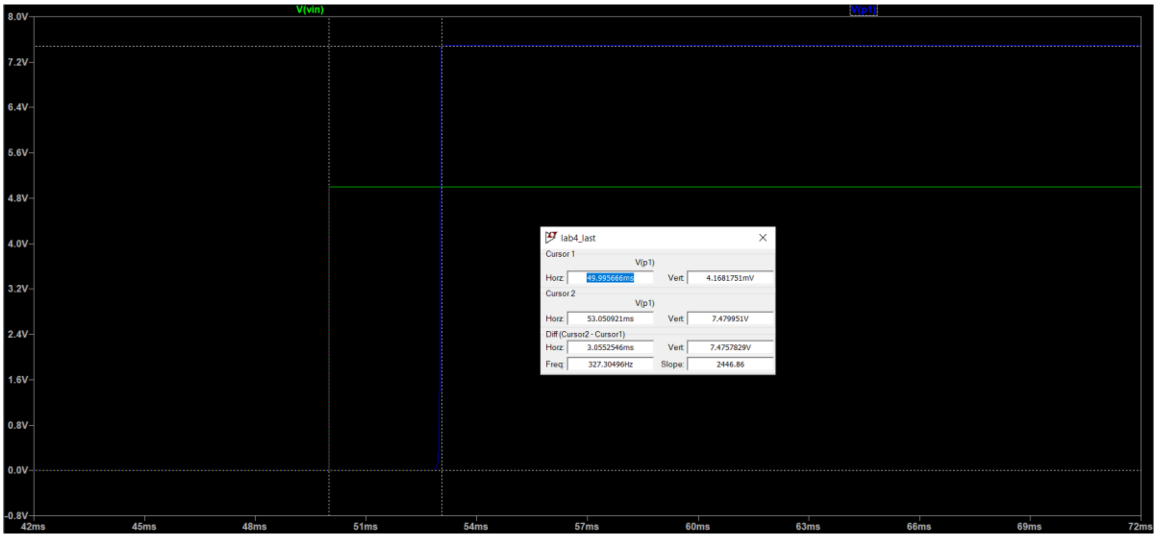

Figure 7: Delay from the first delay circuit is 3.055 ms

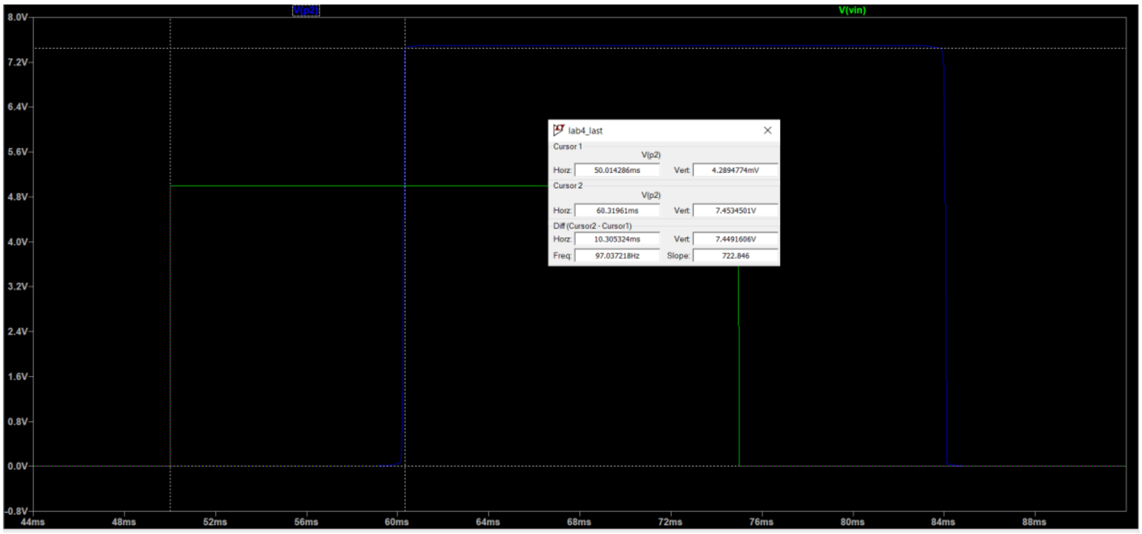

Figure 8: Delay from the second delay circuit is 10.3 ms

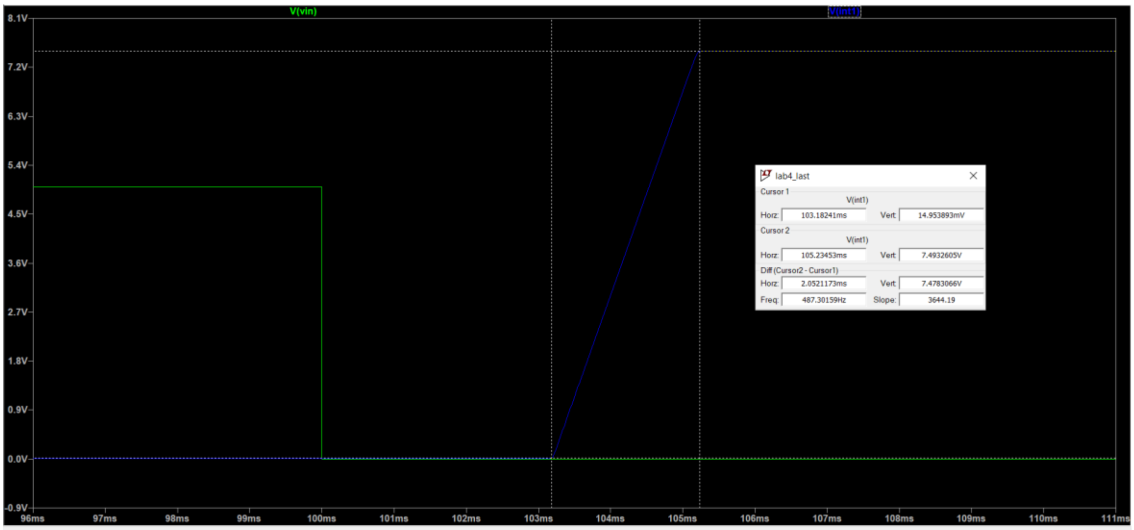

Figure 9: First integrator circuit's output, Δt_1 = 2.05ms

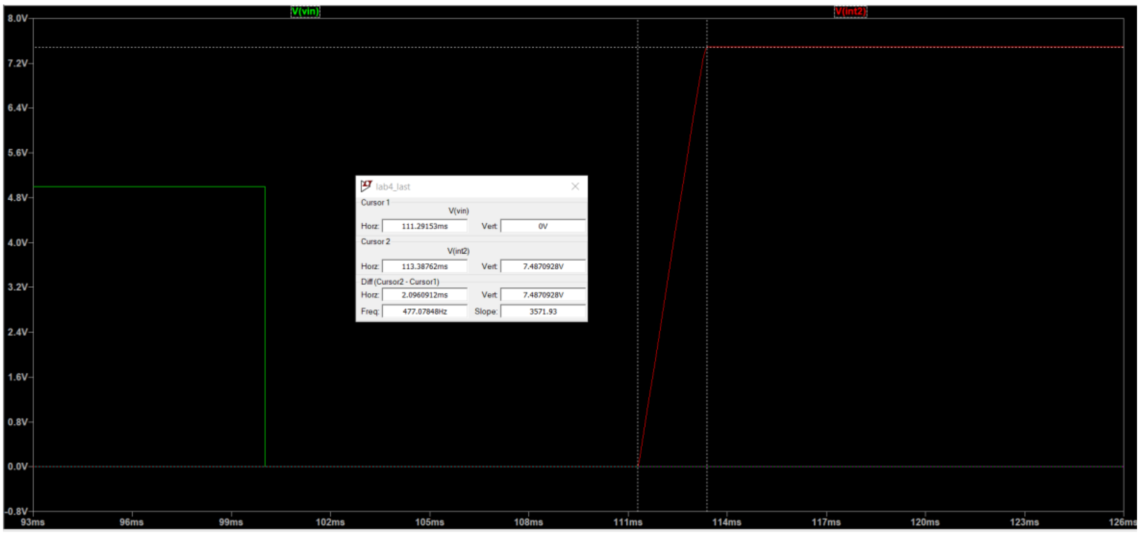

Figure 10: Second integrator circuit's output, Δt_1 = 2.1ms

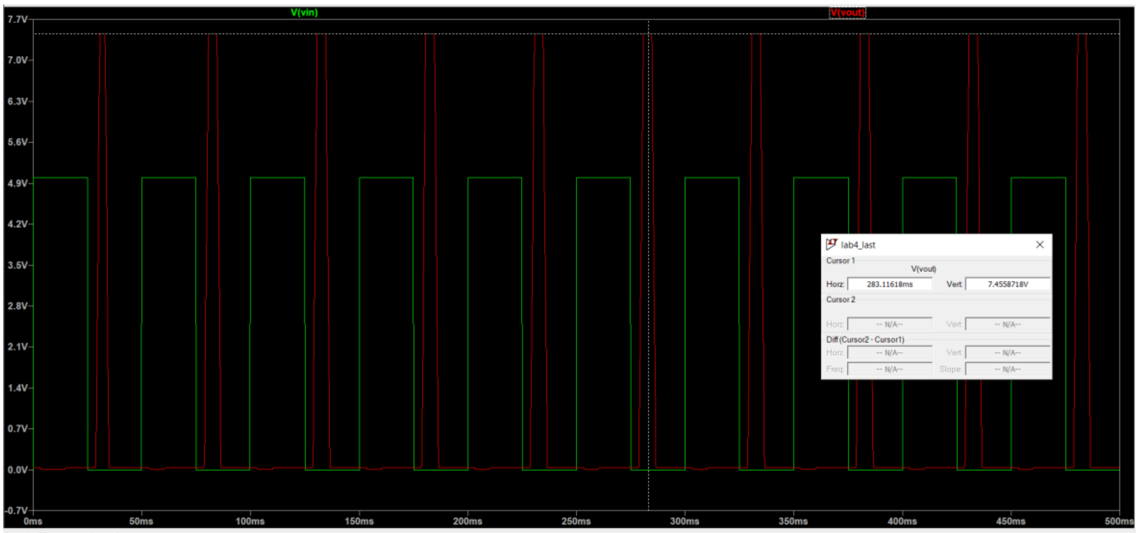

Figure 11: Output voltage is shown in red, Vmax=7.46V

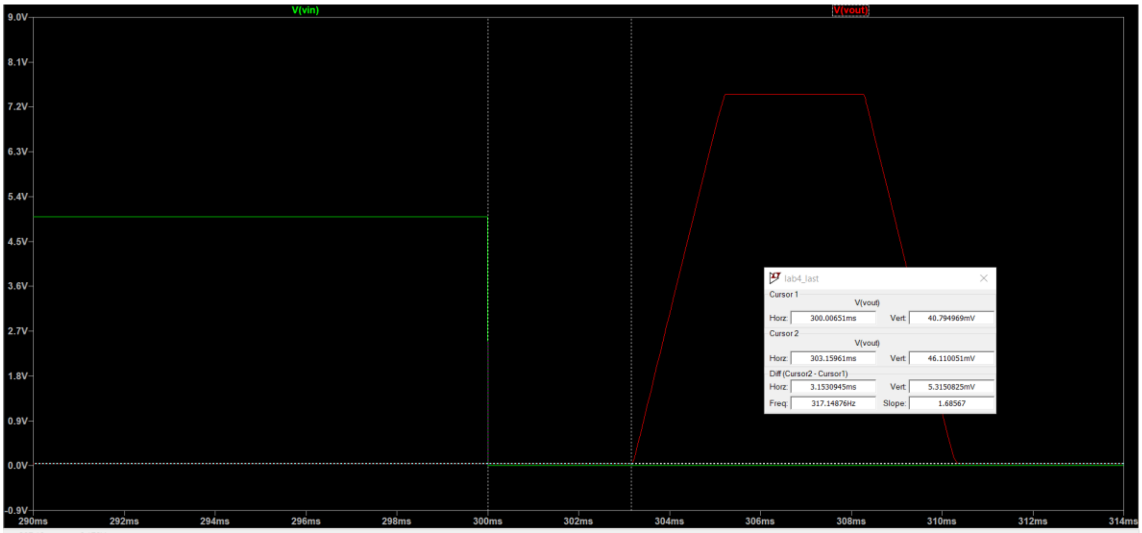

Figure 12: Δt_0=3.15ms

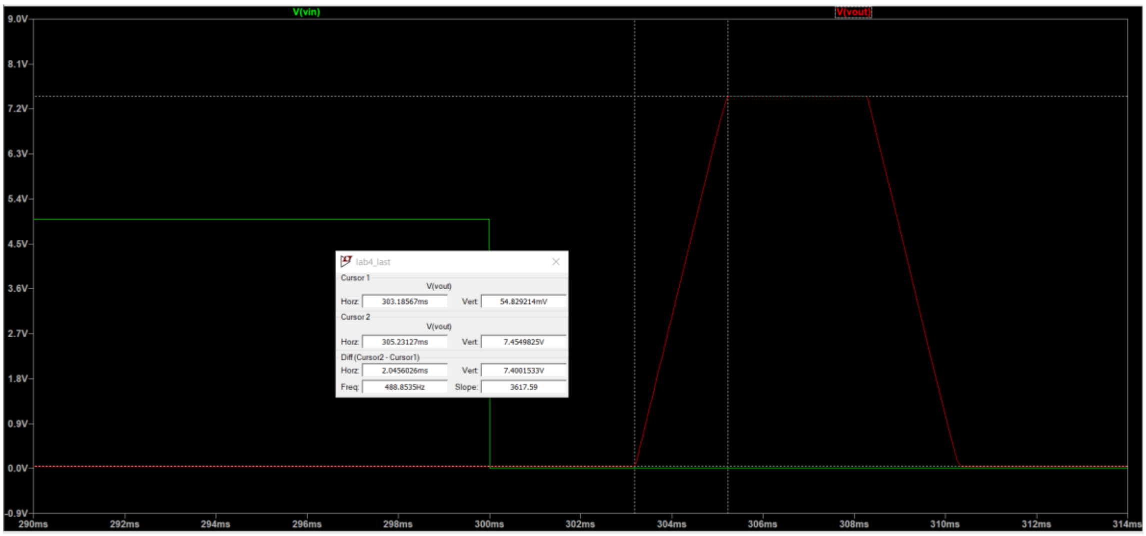

Figure 13: Δt_1=2.05ms

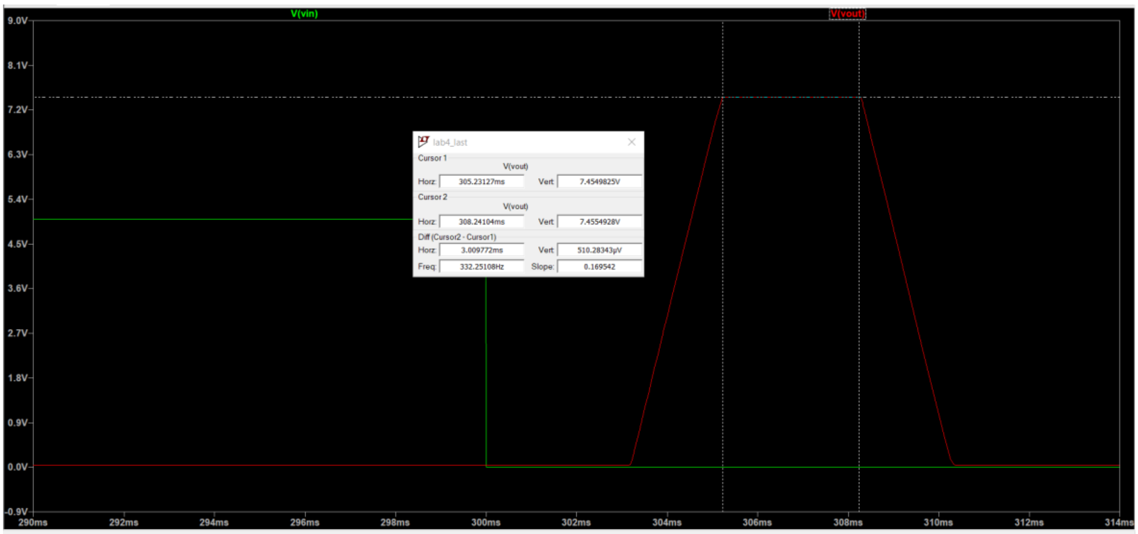

Figure 14: Δt_2=3.01ms

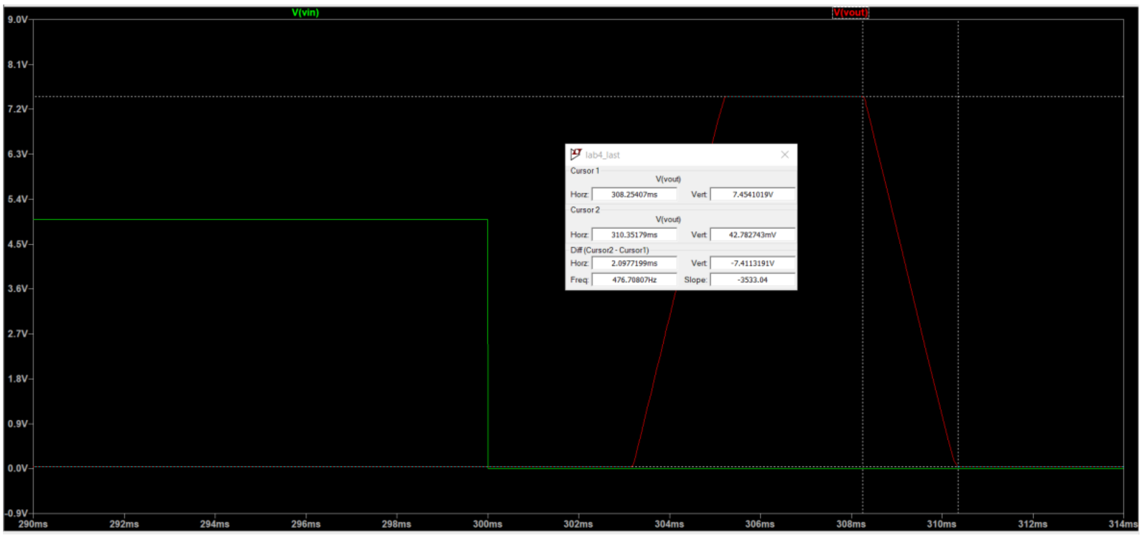

Figure 15: Δt_3=2.1ms

The software results and errors are presented in Table 1.

	Δt_0	Δt_1	Δt_2	Δt_3	V_{max}
Expected value	3 ms	2 ms	3 ms	2 ms	7.5V
Simulation value	3.15 ms	2.05 ms	3.01 ms	2.1 ms	7.46V
Error	5%	2.5%	0.33%	5%	0.53%

Table 1: Simulation results

As seen in Table 1, all the errors are within the ±10% bound as required.

Hardware Implementation

In the hardware part, two LM324 Quad OPAMP ICs are used. Figure 16 shows the pin diagram. As in the simulation part, the Vcc+ input is 9V, and Vcc- is grounded. This is achieved by using the DC voltage source in the lab. Then the circuit is implemented on the breadboard, as shown in Figure 17.

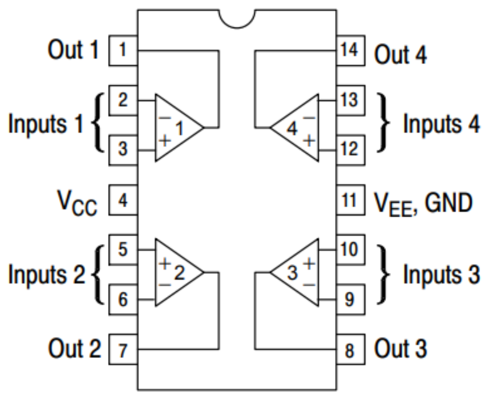

Figure 16: LM324 diagram

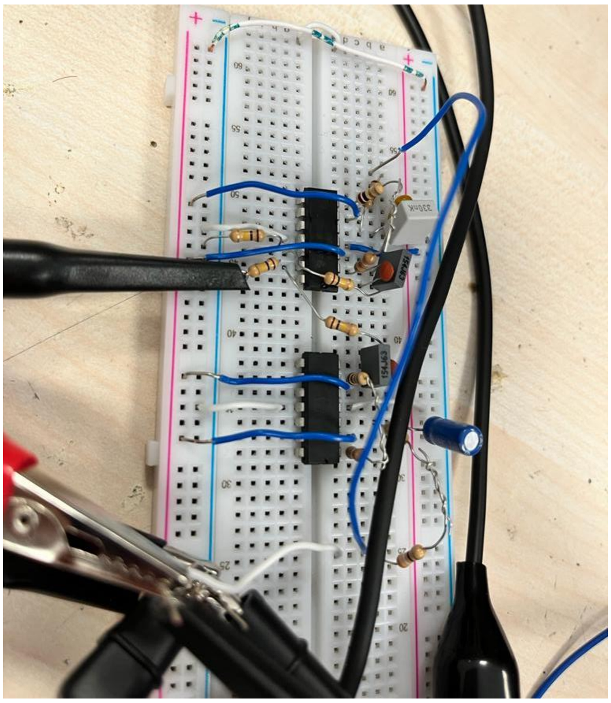

Figure 17: Circuit is implemented

The input voltage is a square wave with 2.5V peak-to-peak value and 20 Hz frequency, and the Vcomp input is given 2.5 V using the DC voltage source. The input is also given a 1.25V offset to carry the voltage to the positive side. The adjustments are shown in Figure 18.

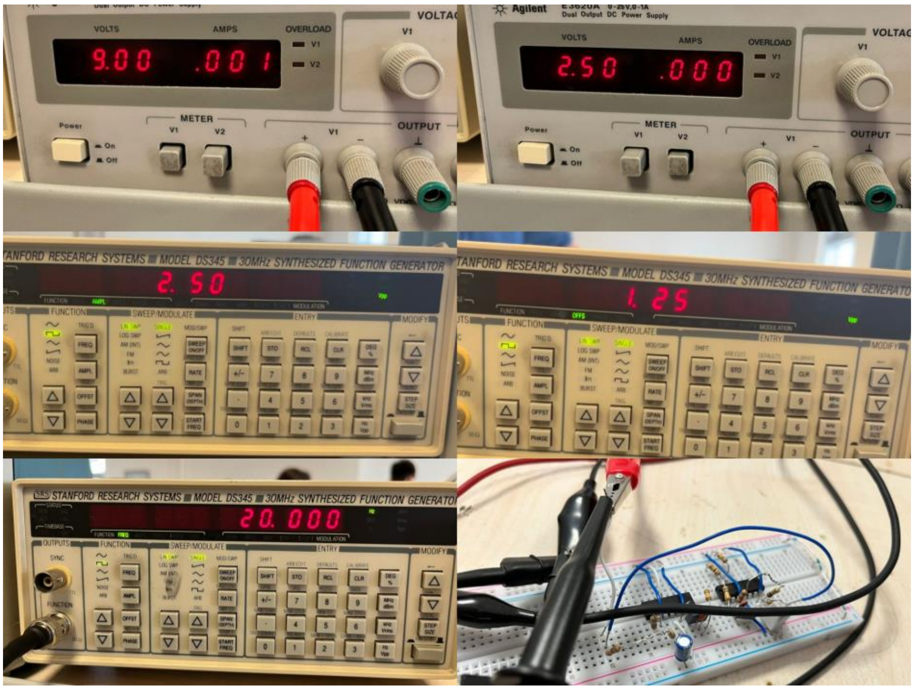

Figure 18: Hardware configurations

Then the measurements are made using the oscilloscope, shown in Figures 19-27, and the results are presented in Table 2.

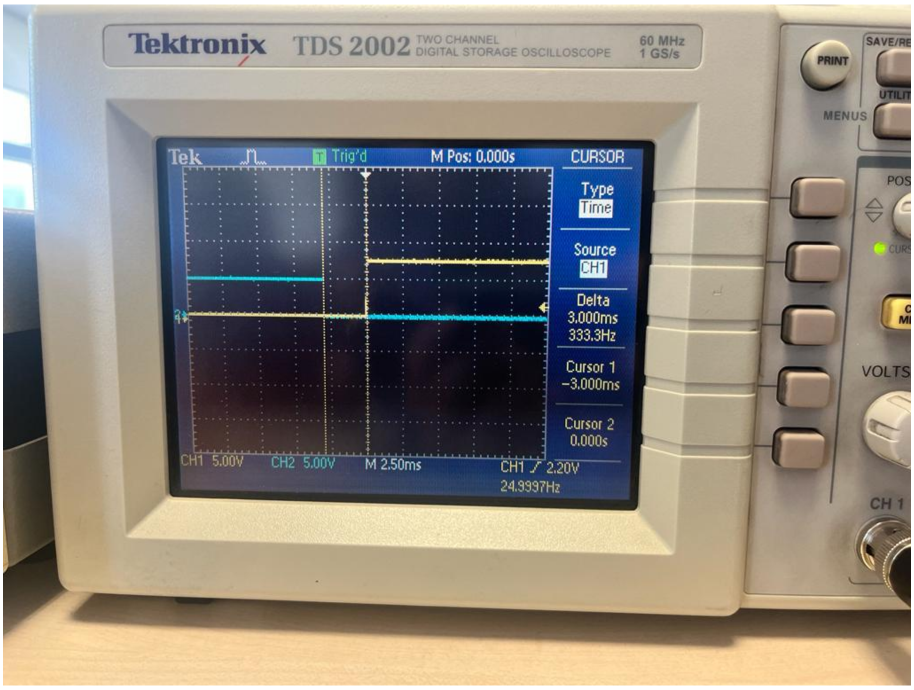

Figure 19: First delay circuit's output (shown in yellow) vs input voltage (shown in blue), delay is 3 ms

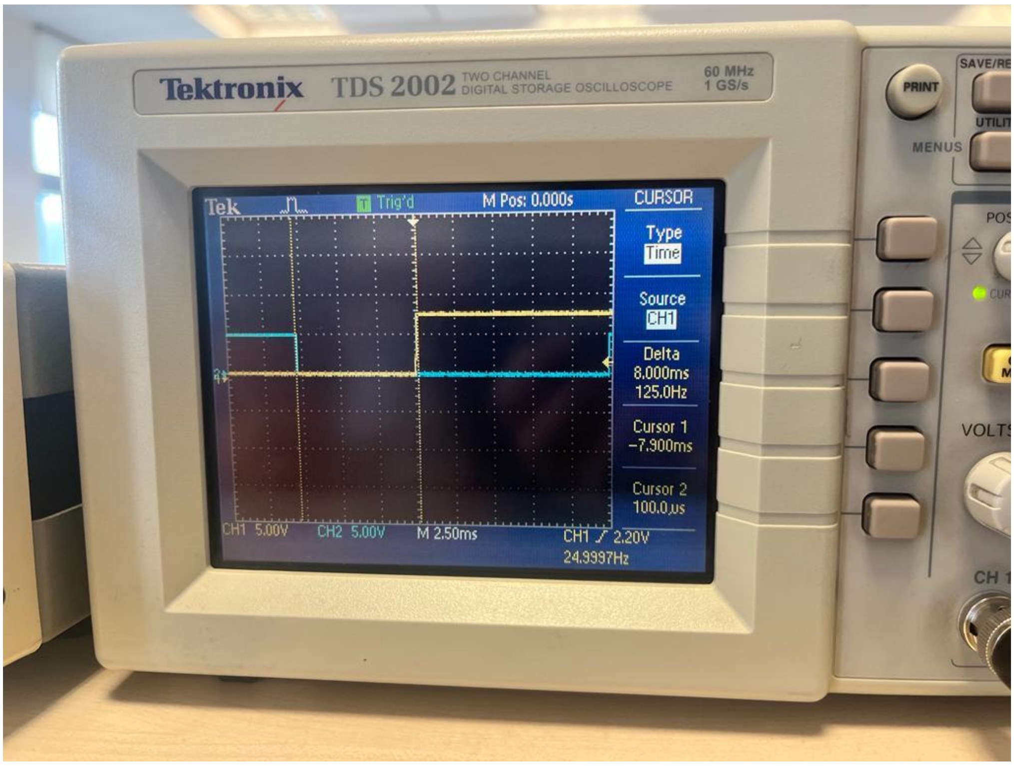

Figure 20: Second delay circuit's output, delay is 8 ms

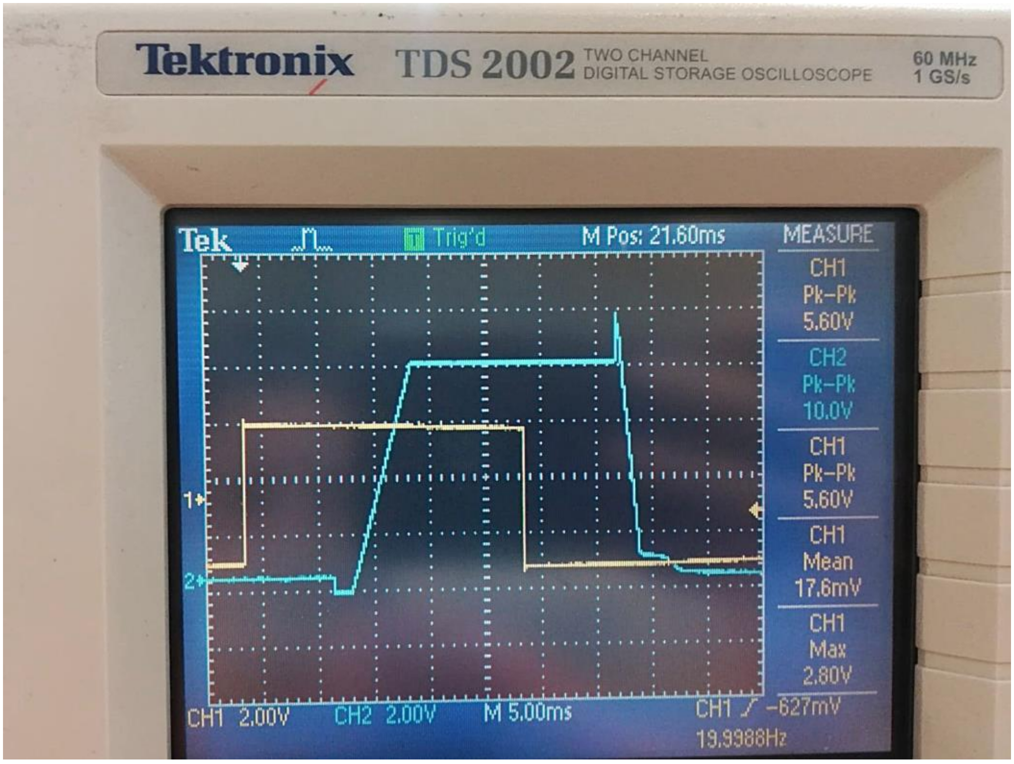

Figure 21: First integrator circuit's output

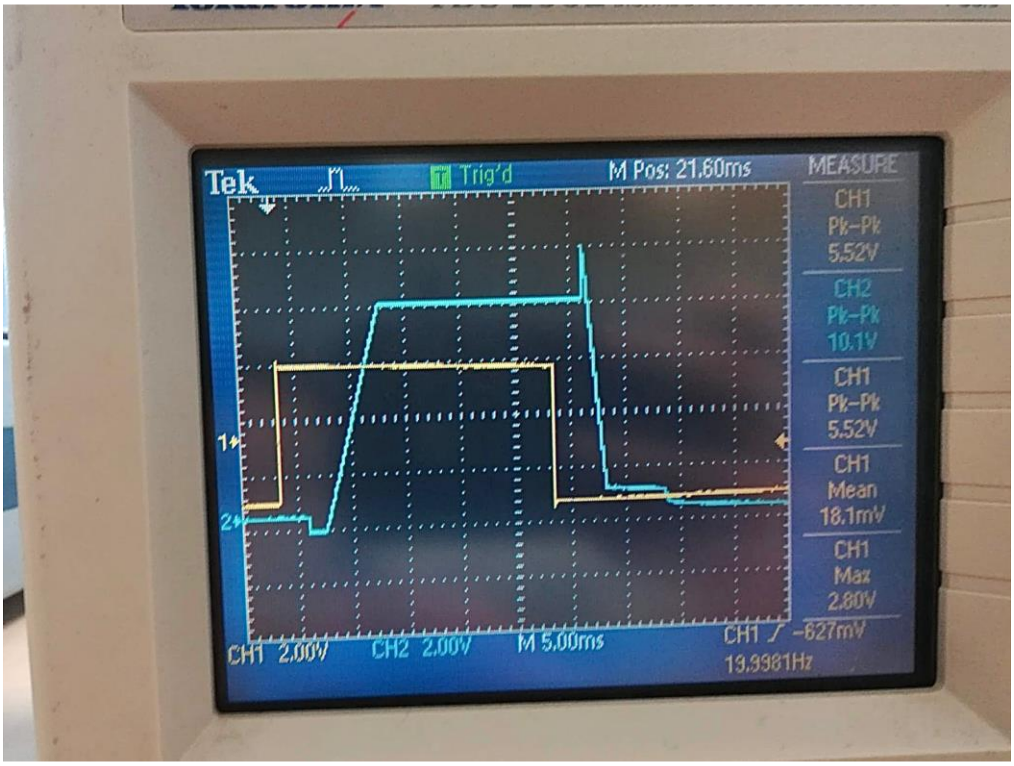

Figure 22: Second integrator circuit's output

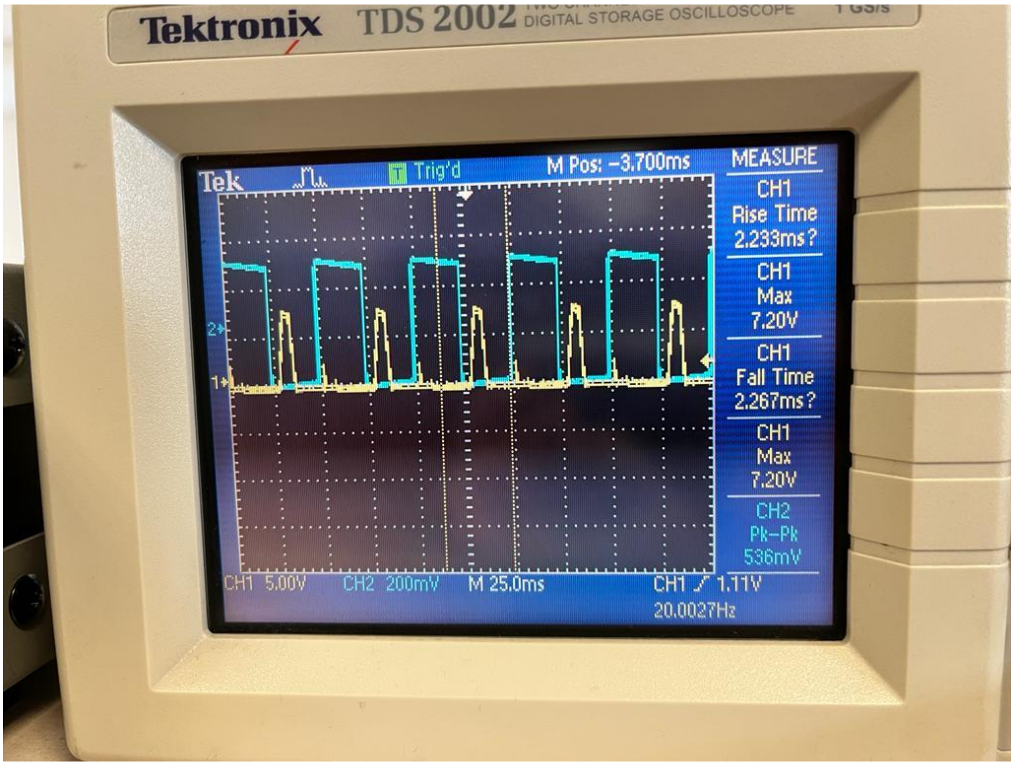

Figure 23: Input (shown in blue) and output voltages (shown in yellow), Vmax=7.2V

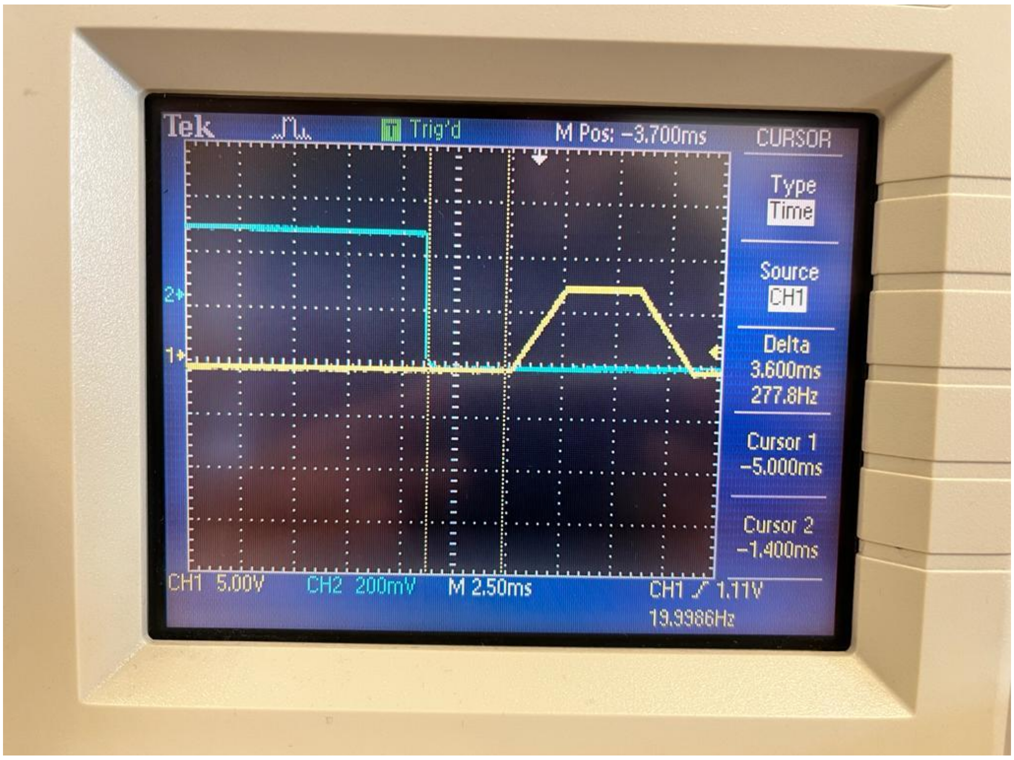

Figure 24: Δt_0=3.6ms

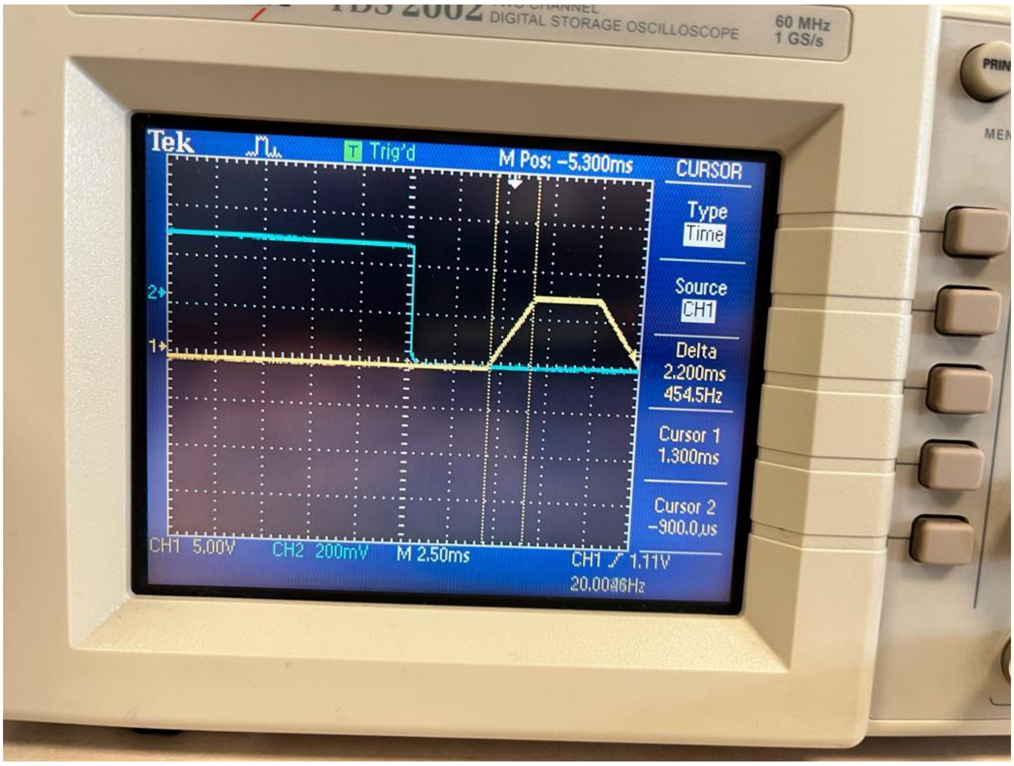

Figure 25: Δt_1=2.2ms

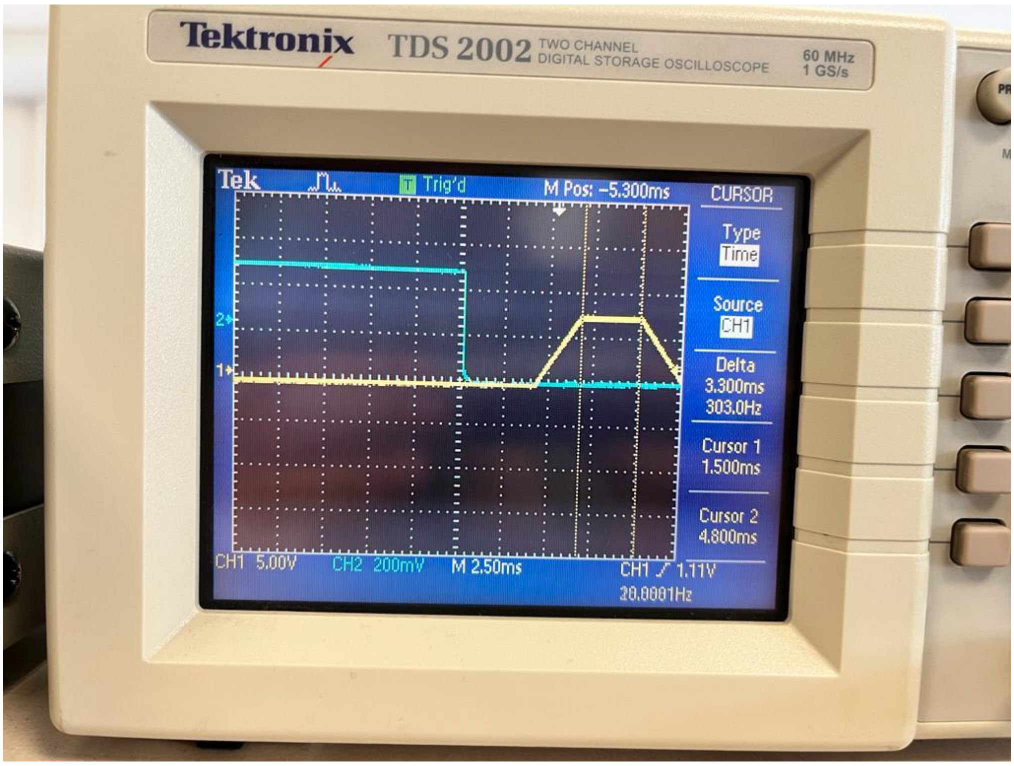

Figure 26: Δt_2=3.3ms

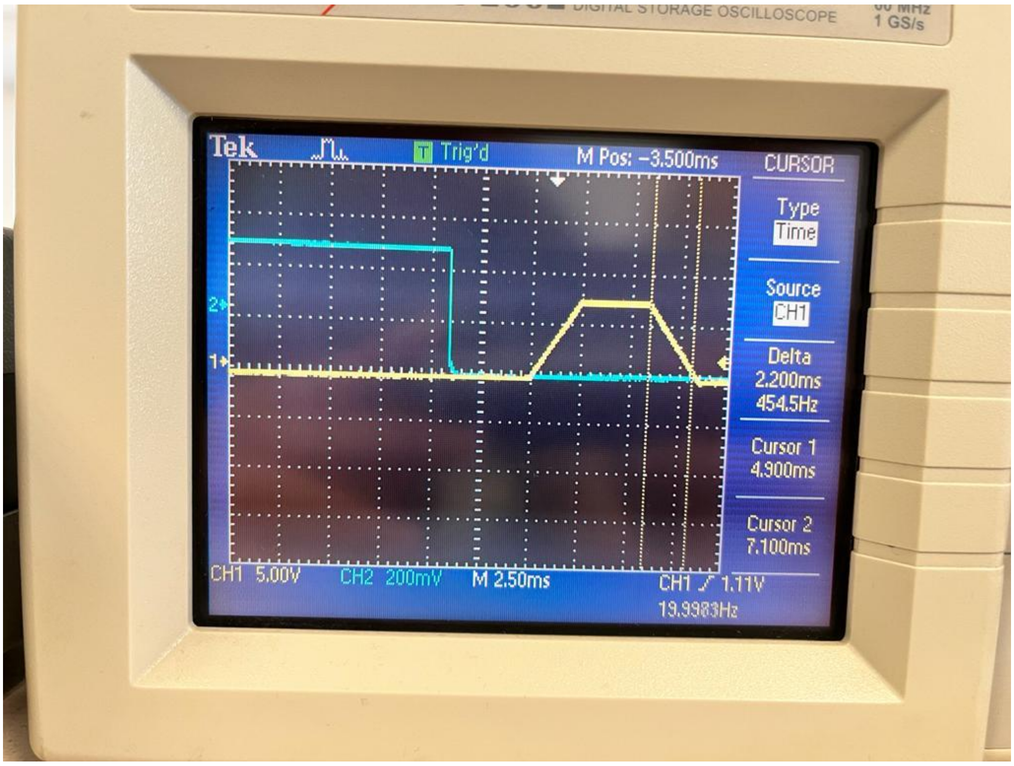

Figure 27: Δt_3=2.2ms

	Δt_0	Δt_1	Δt_2	Δt_3	V_{max}
Expected value	3 ms	2 ms	3 ms	2 ms	7.5V
Measured value	3.6 ms	2.2 ms	3.3 ms	2.2 ms	7.2V
Error	20%	10%	10%	10%	4%

Table 2: Hardware results

As seen in Table 2, all the errors are within the ±20% bound as required.

Conclusion

In the software part, the results for Δt_0, Δt_1, Δt_2, Δt_3 and Vmax matched with 5%, 2.5%, 0.33%, 5% and 0.53% respectively. The errors might have occurred due to the fact that for the resistors and capacitors, standard values were chosen. The values, although chosen closest to the ones that are applicable, don't exactly satisfy the derived equations. However, the differences are very small so that the errors are in the ±10% bound as required.

In the hardware lab however, the errors were high, with 20%, 10%, 10%, 10% and 4% respectively. This might have occurred due to the inner resistances of wires or the 10% tolerances of resistors and capacitors. The LM324 IC has also inner resistances which lead to imperfections. The resistor tolerances also affect the circuits, for example the 90 kΩ resistors used in the subtractor circuit may not have exactly the same values. This changes the circuit's output completely since it was assumed that all resistors in the subtractor circuit were identical.

Overall, this lab demonstrated how to manipulate a given waveform into a wanted shape using OPAMPs and RC circuits. It gave insight to deriving OPAMP input/output equations and creating delays using them. It revealed that by using these equations, OPAMP circuits can be used as operators (e.g., integrator, subtractor, …) and the required waveform can therefore be generated.