Bilkent University
EE-202 Circuit Theory
Lab 5
Band-Pass Filter

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Section 02

Introduction

This lab aims to design a band-pass filter for 50Ω load resistance with given specifications shown in Figure 1.

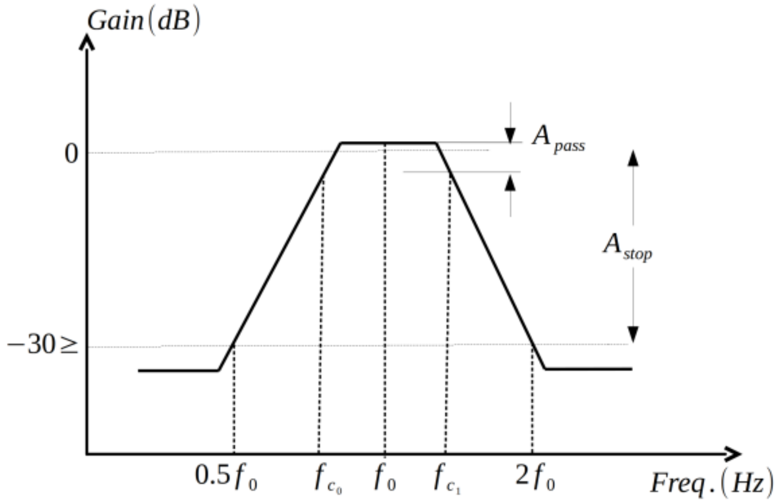

Figure 1: Frequency response of the filter

Central frequency: $3Mhz \leq f_0 \leq 6Mhz$
Passband width: $f_{c1} - f_{co} = 0.05 f_0$
Gain variation in the passband: $A_{pass} \leq 3dB$
Stopband attenuation: $A_{stop} \geq 30dB$

Figure 1: Lab task

The central frequency f_0 is chosen as 3MHz for this case. Therefore the bandwidth is $0.05f_0 =$ 150 kHz. The input voltage is chosen to have 2V peak value.

Analysis

To achieve the given specifications, a second-order Butterworth filter can be designed as a band-pass filter. Second order is chosen since it will be easier to implement on hardware. The overall design of a second-order Butterworth filter can be seen in Figure 2. For this case, R_1 (source resistance) and R_2 (load resistance) are both 50Ω, the inductor and capacitor values are to be determined.

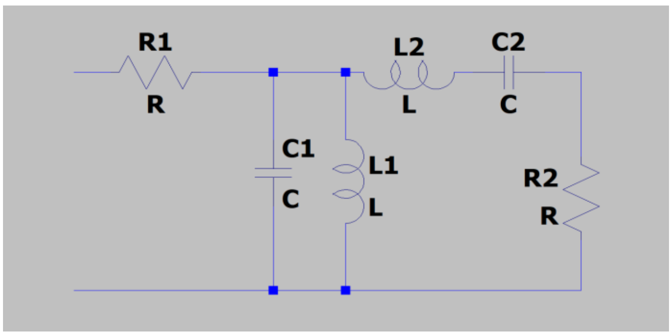

Figure 2: Second-order Butterworth filter

A band-pass filter is designed in two steps:

1. Design a second-order Butterworth low-pass filter with its cut-off (-3dB) frequency equal to the BPF's bandwidth (150 kHz).
2. Tuning the inductor with a series capacitor, and the capacitor with a parallel inductor such that the resonance occurs at f_0=3MHz.

A generic Butterworld low-pass filter can be seen in Figure 3:

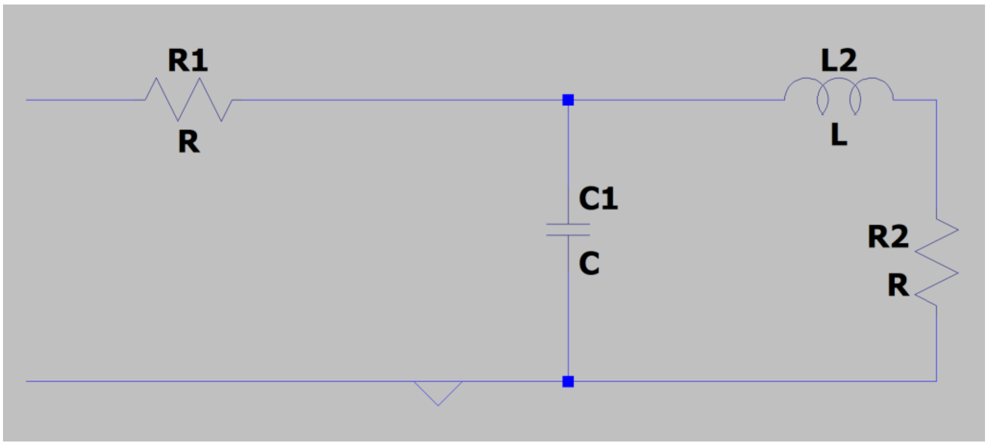

Figure 3: Butterworth low-pass filter

To determine the values of C1 and L2, the Butterworth coefficients will be used from the table shown in Figure 4. The values for the second order circuits will be used.

n	b_1	b_2	b_3	b_4	b_5	b_6	b_7	b_8
1	2.000							
2	1.4142	1.4142						
3	1.0000	2.0000	1.0000					
4	0.7654	1.8478	1.8478	0.7654				
5	0.6180	1.6180	2.0000	1.6180	0. 6180			
6	0.5176	1.4142	1.9319	1.9319	1.4142	0.5176		
7	0.4450	1.2470	1.8019	2.0000	1.8019	1.2470	0.4450	
8	0.3902	1.1111	1.6629	1.9616	1.9616	1.6629	1.1111	0.3902

Figure 4: Butterworth filter coefficients

For the second order circuits, the values are:

$$C_1 = b_1 = 1.4142$$

$$L_2 = b_2 = 1.4142$$

Then, to have the cut-off frequency at 150 kHz, the values are divided by the angular frequency (2πf):

$$C_1 = \frac{1.4142}{2\pi * 150\ kHz}, L_2 = \frac{1.4142}{2\pi * 150\ kHz}$$

Since the load resistance is $R_L=50\Omega$, the inductance is multiplied by 50, and the capacitance is divided by 50:

$$C_1 = \frac{1.4142}{2\pi * 150\, kHz * 50}\,, L_2 = \frac{1.4142 * 50}{2\pi * 150\, kHz}$$

Therefore, the values are found as:

$$C_1 = 30pF\,, L_2 = 75\mu H$$

The Butterworth LPF is implemented with the calculated values:

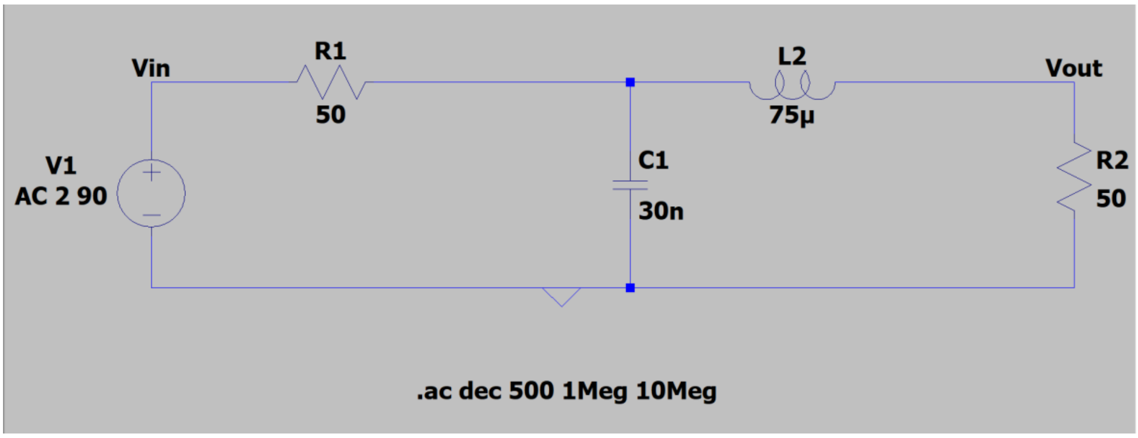

Figure 5: Butterworth low-pass filter

The second step is to tune in the inductor and capacitor to have resonance at the center frequency 3 MHz. This will be achieved by connecting a series capacitor C2 near the inductor L2, and connecting a parallel inductor L1 near the capacitor C1. To calculate these values:

$$L_1 = \frac{1}{\omega^2 C_1}\,, C_2 = \frac{1}{\omega^2 L_2}\; where\; \omega = 2\pi * 3MHz$$

$$L_1 = \frac{1}{(2\pi * 3\, MHz)^2 * 30 * 10^{-9}}\,, C_2 = \frac{1}{(2\pi * 3\, MHz)^2 * 75 * 10^{-6}}$$

Finally, the results are obtained as:

$$L_1 = 94nH\,, C_2 = 37.7pF$$

Using the calculated values, the band-pass filter will be implemented both on LTSpice and hardware. LTSpice can measure the gain at the output directly. In the hardware lab, however, the gain will be calculated with the formula:

$$A = 20\log(\frac{V_{out}}{V_{in}}) \qquad (1)$$

where the peak-to-peak values for V_{out} and V_{in} will be considered.

Simulations

Before implementing the BPF, first the LPF is tested, shown in Figure 6:

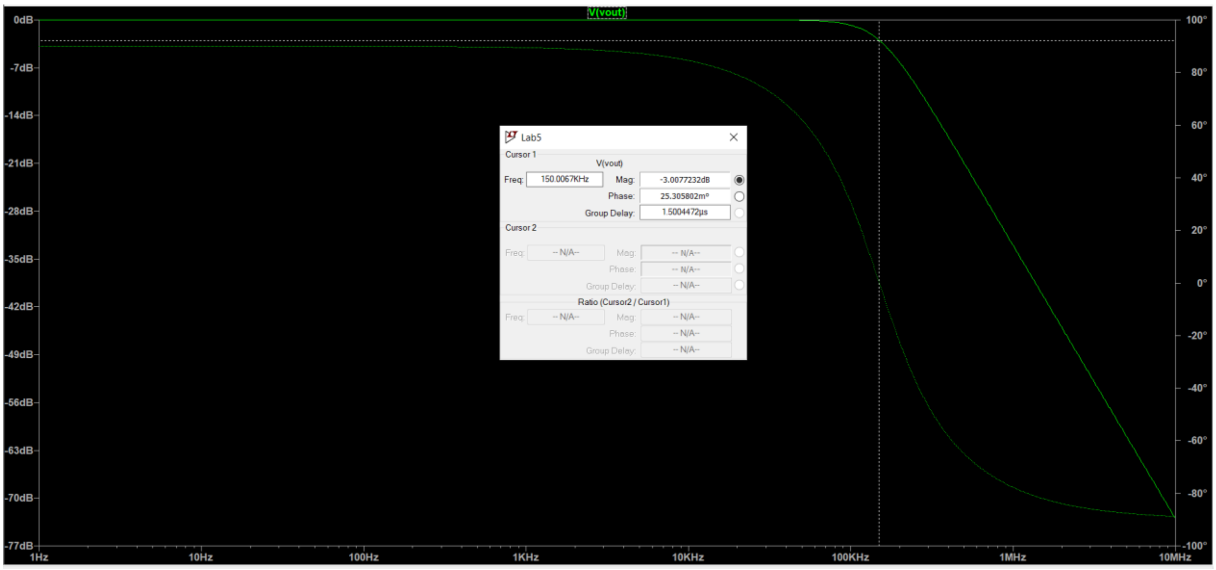

Figure 6: Low-pass filter gain

As expected, the -3dB cut-off frequency is 150 kHz, the bandwidth of the BPF. After that, the circuit is implemented on LTSpice with the calculated values as shown in Figure 7.

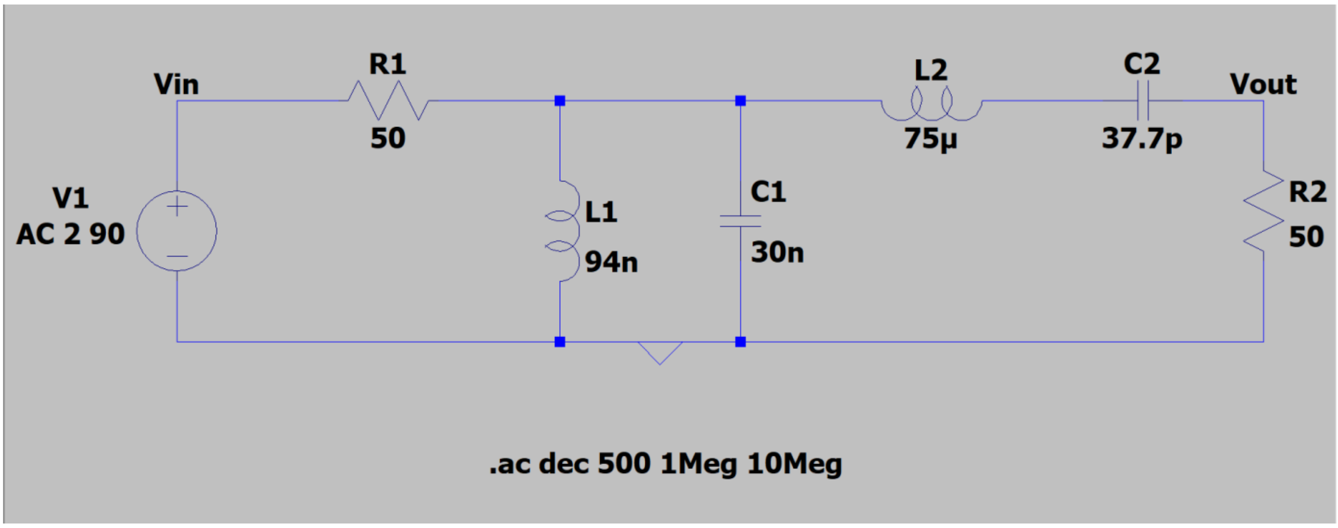

Figure 7: Band-pass filter circuit

Then using the AC analysis on LTSpice, the gain at the center frequency, along with the -3dB cut-off frequencies, $0.5f_0$ (1.5MHz) and $2f_0$ (6MHz) points are measured. Figures 8-11 show the measurements, and the results are presented in Table 1. The bandwidth is measured as the difference between the two -3dB frequencies, as indicated in the lab task.

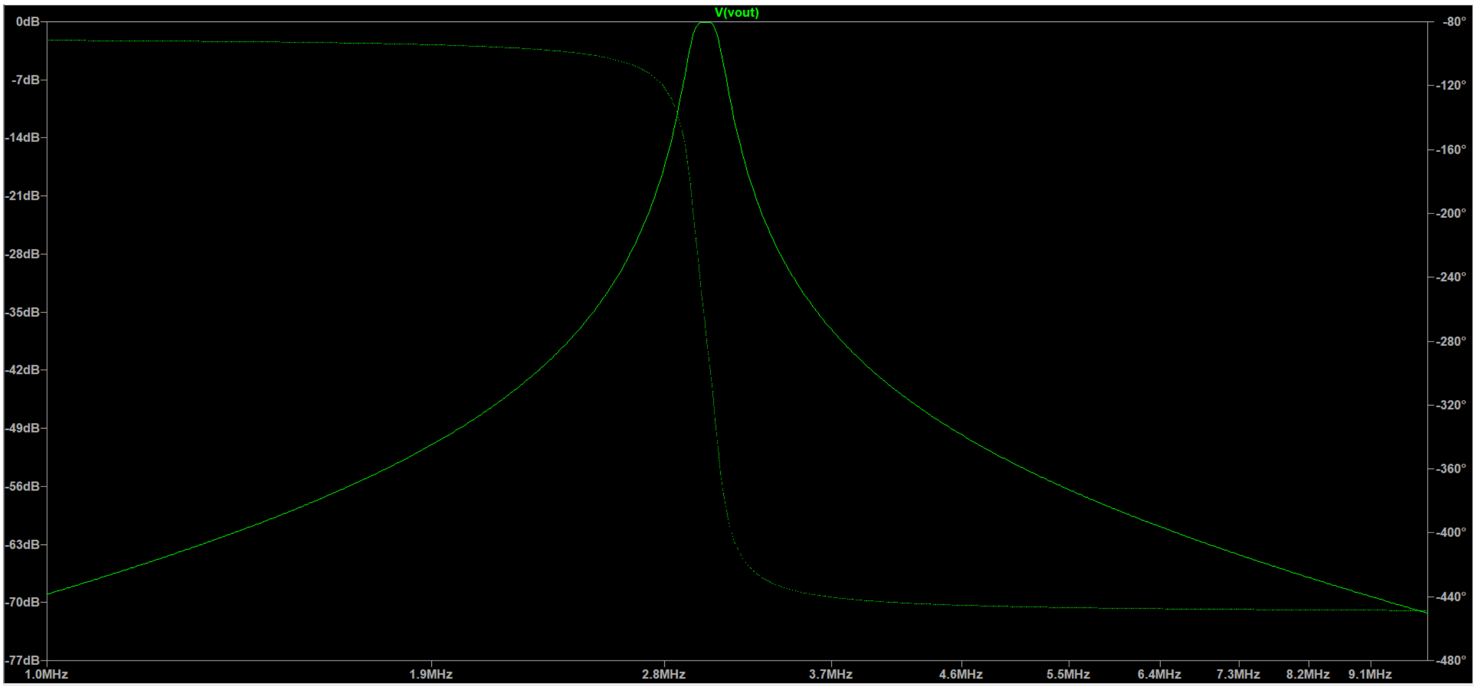

Figure 8: Output gain plot

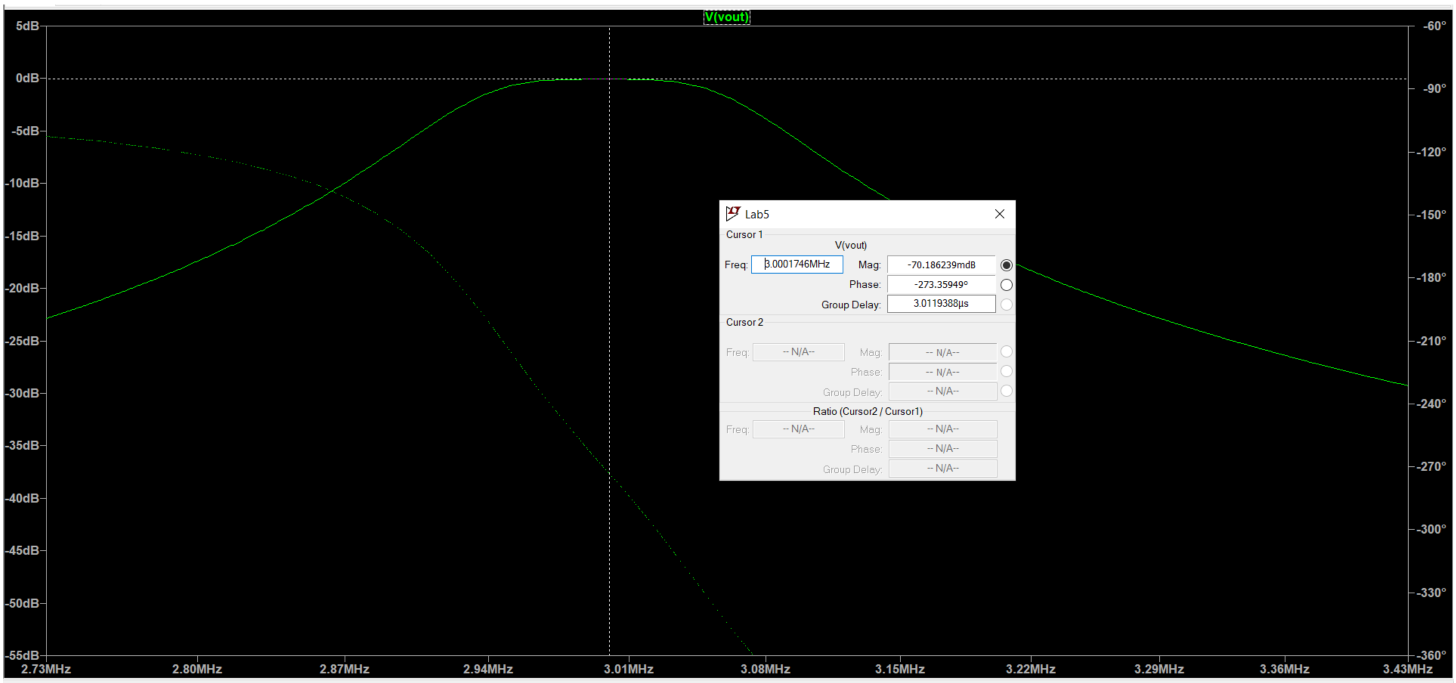

Figure 9: Gain is -70.2 mdB at the center frequency 3MHz

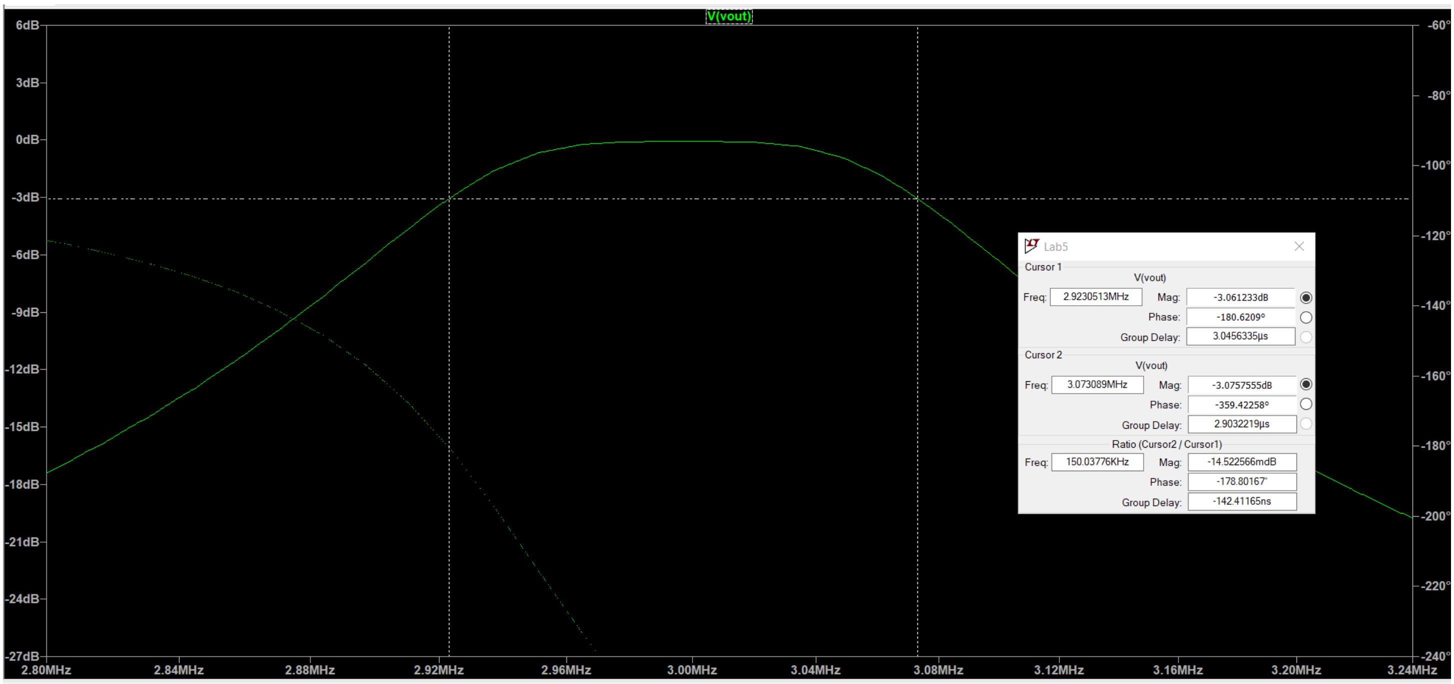

Figure 10: The -3dB cut-off frequencies f_{c1} and f_{c0} are 2.92MHz and 3.07MHz, bandwidth is 150.04 kHz

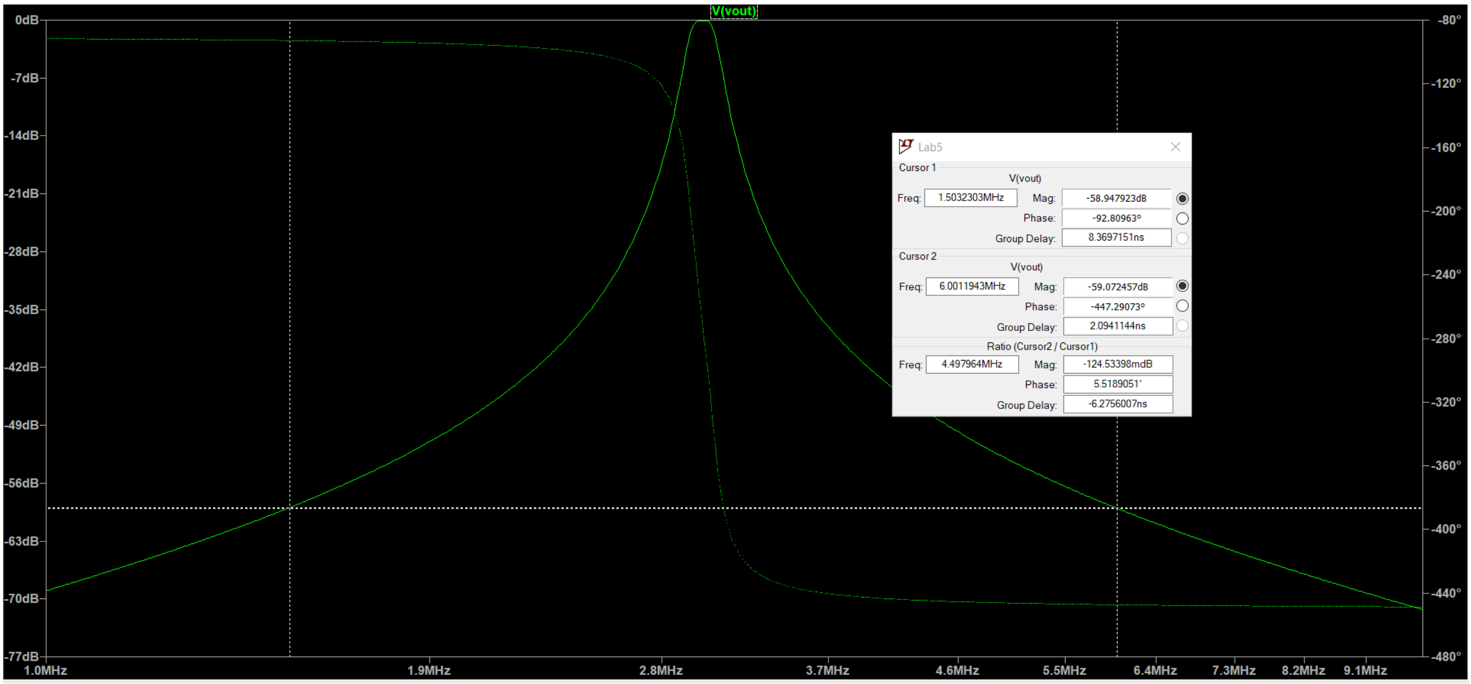

Figure 11: Gain is -58.95dB and -59.07dB at 1.5MHz ($0.5f_0$) and 6MHz ($2f_0$)

	Expected value	Measured value	Comparison
Gain at f_0	_	-0.072dB	_
Bandwidth (f_{c1}-f_{c0})	150kHz	150.04kHz	0.027% error
Gain at $0.5f_0$	≤-30dB	-58.95dB	Satisfied
Gain at $2f_0$	≤-30dB	-59.07dB	Satisfied
Gain variation in the passband	≤3dB	$\lvert -3.06 + 0.072 \rvert$=2.99dB	Satisfied

Table 1: Software results

As seen in Table 1, the errors are within the 10% bound, therefore all conditions for the lab are satisfied.

Hardware Implementation

In the hardware part, the inductor and capacitor values were obtained by soldering the available values in series or parallel combinations. Since the source has 50Ω inner resistance inside, only the load resistor was connected. The hardware circuit can be seen in Figure 12.

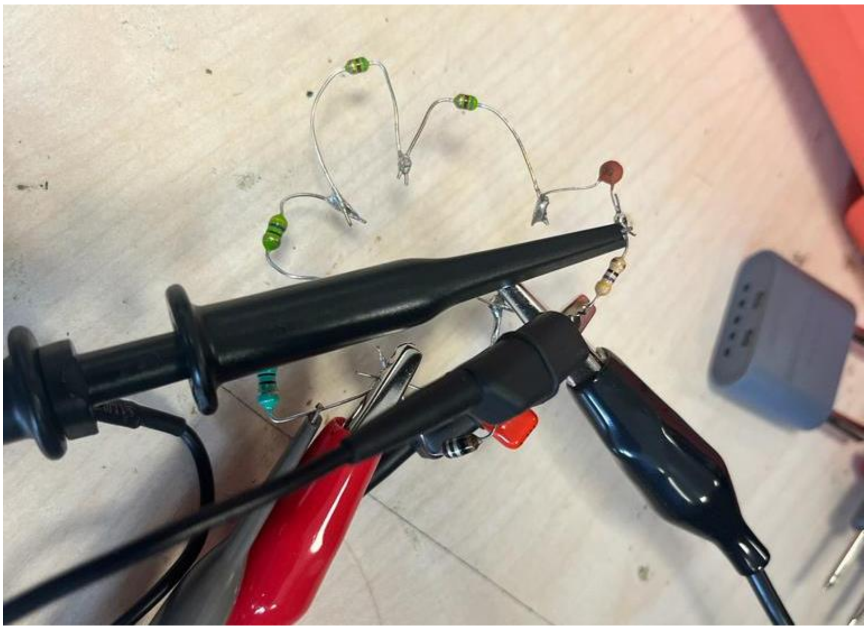

Figure 12: Hardware circuit

After that, the input and output peak-to-peak voltages are measured, first five measurements are in the passband range, and the other five is outside the passband range. Figures 13-22 show the measurements at different frequencies.

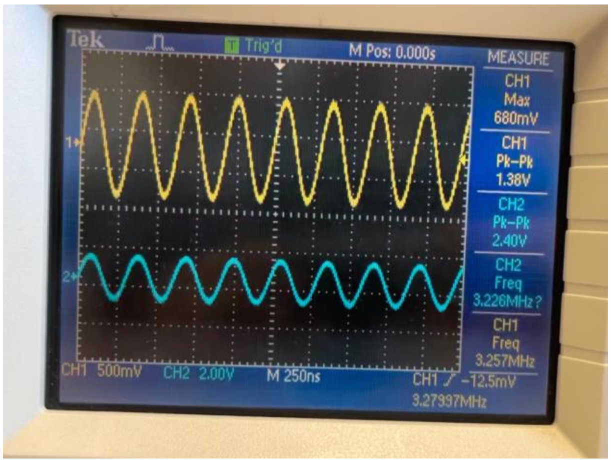

Figure 12: The center frequency f_0 is found as 3.28MHz, Vin=2.4V, Vout=1.38V

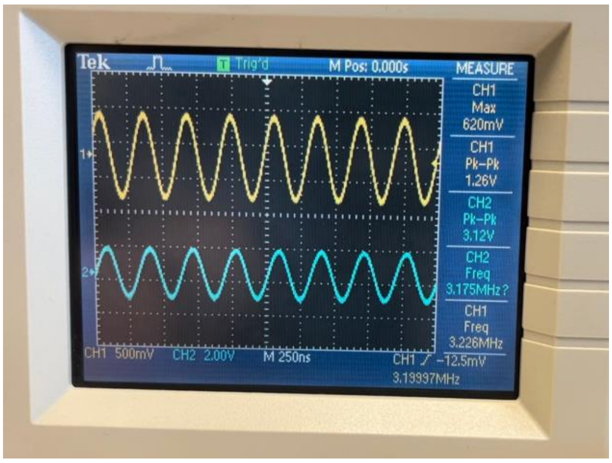

Figure 13: The first center frequency f_{c0} is found as 3.2MHz, Vin=3.12V, Vout=1.26V

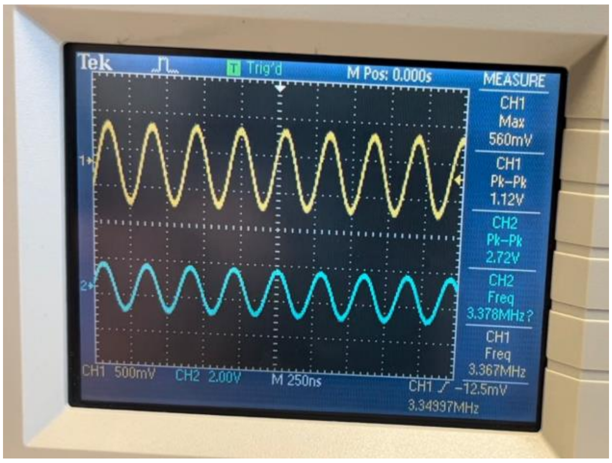

Figure 14: The second center frequency f_{c1} is found as 3.35MHz, Vin=2.72V, Vout=1.12V

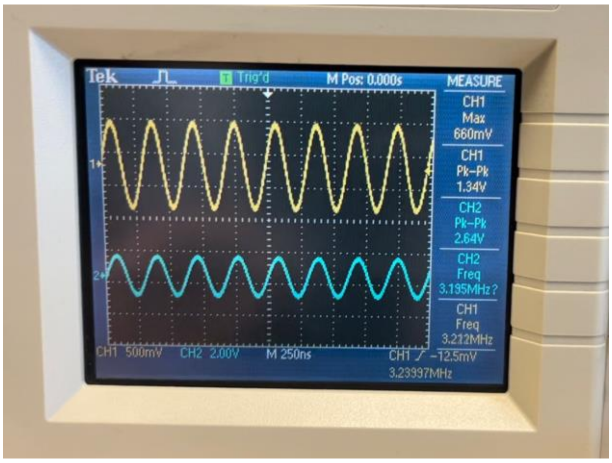

Figure 15: At f=3.24 MHz, Vin=2.64V, Vout=1.34V

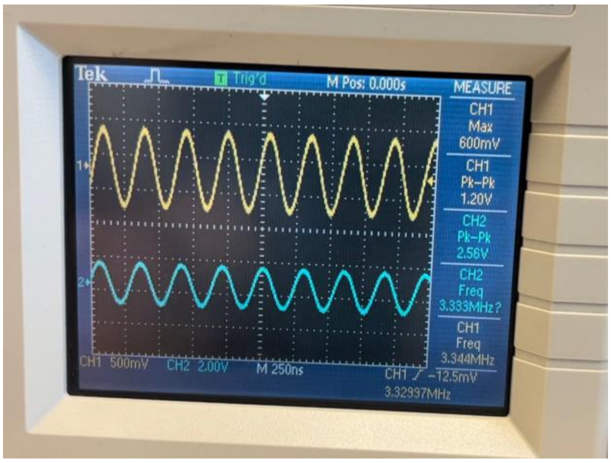

Figure 16: At f=3.33 MHz, Vin=2.56V, Vout=1.2V

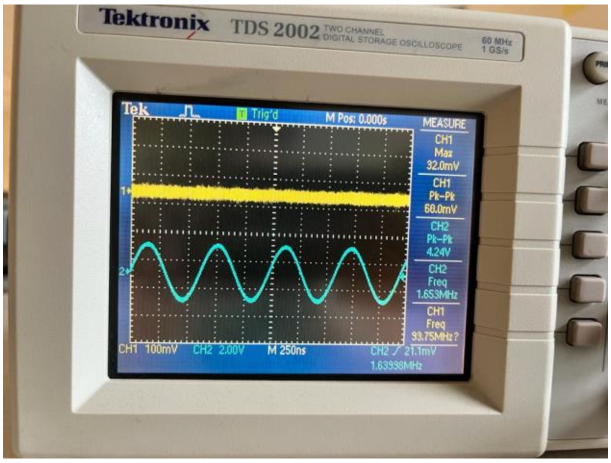

Figure 17: At 0.5f_0=1.64 MHz, Vin=4.24V, Vout=60mV

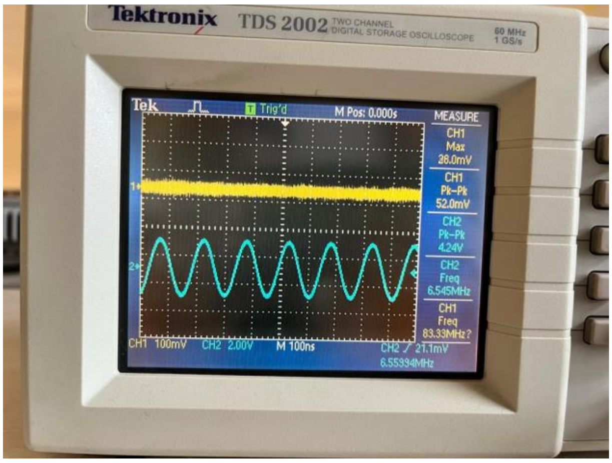

Figure 18: At 2f_0=6.56 MHz, Vin=4.24V, Vout=52mV

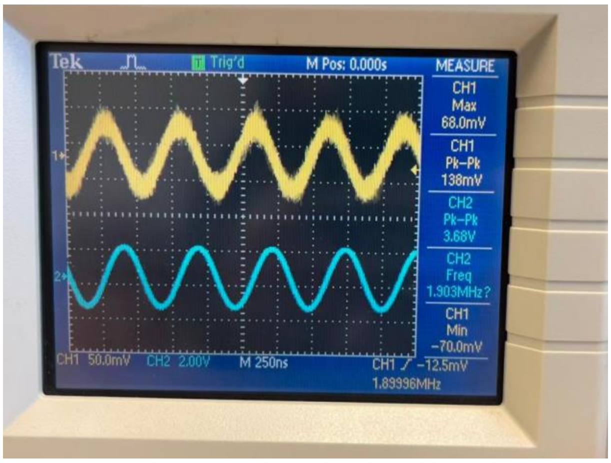

Figure 19: At f=1.9 MHz, Vin=3.68V, Vout=138mV

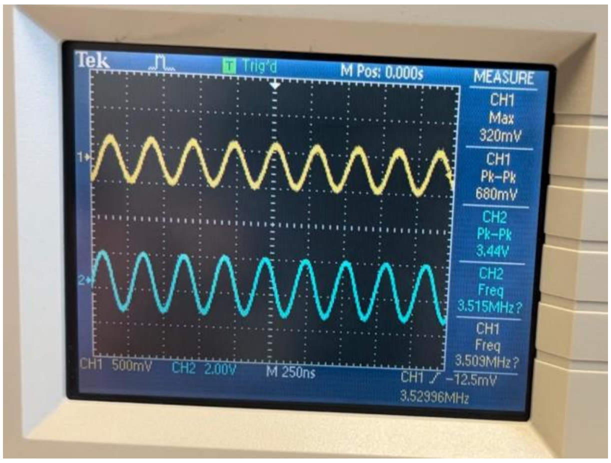

Figure 20: At f=3.53 MHz, Vin=3.44V, Vout=680mV

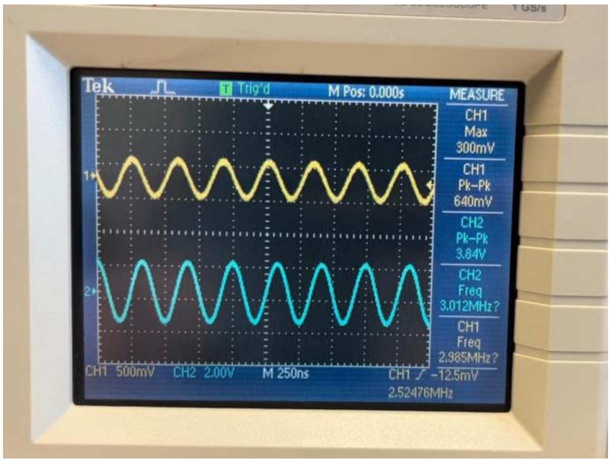

Figure 21: At f=2.52 MHz, Vin=3.84V, Vout=640mV

Then using equation (1) in the analysis section, the dB gains are calculated for every frequency. The results are presented in Tables 2-4.

Frequency	**V_{in}(p-p)**	**V_{out}(p-p)**	**Gain**
3.2MHz (f_{c0})	3.12V	1.26V	-7.8dB
3.24MHz	2.64V	1.34V	-5.9dB
3.28MHz (f_0)	2.4V	1.38V	-4.81dB
3.33MHz	2.56V	1.2V	-6.58dB
3.35MHz (f_{c1})	2.72V	1.12V	-7.7dB

Table 2: Gains in the passband region

Frequency	**V_{in}(p-p)**	**V_{out}(p-p)**	**Gain**
1.64MHz (0.5f_0)	4.24V	60mV	-36.98dB
1.9MHz	3.68V	138mV	-28.52dB
2.52MHz	3.84V	640mV	-15.56dB
3.53MHz	3.44V	680mV	-14.08dB
6.56MHz (2f_0)	4.24V	52mV	-38.23dB

Table 3: Gains outside the passband region

	Expected value	**Measured value**	**Comparison**
Center frequency (f_0)	3MHz	3.28MHz	9.3% error
Gain at f_0	_	-4.81dB	_
Bandwidth (f_{c1}-f_{c0})	150kHz	150kHz	0% error
Gain at $0.5f_0$	≤-30dB	-36.98dB	Satisfied
Gain at $2f_0$	≤-30dB	-38.23dB	Satisfied
Gain variation in the passband	≤3dB	$\|-7.8+4.81\|$=2.99dB	Satisfied

Table 4: Hardware results

As seen from the results, the errors are within the 10% bound, therefore all conditions for the lab are satisfied. Lastly, using the data in Tables 2 and 3, the frequency response plot of the output gain is generated using MATLAB. It is shown in Figure 22.

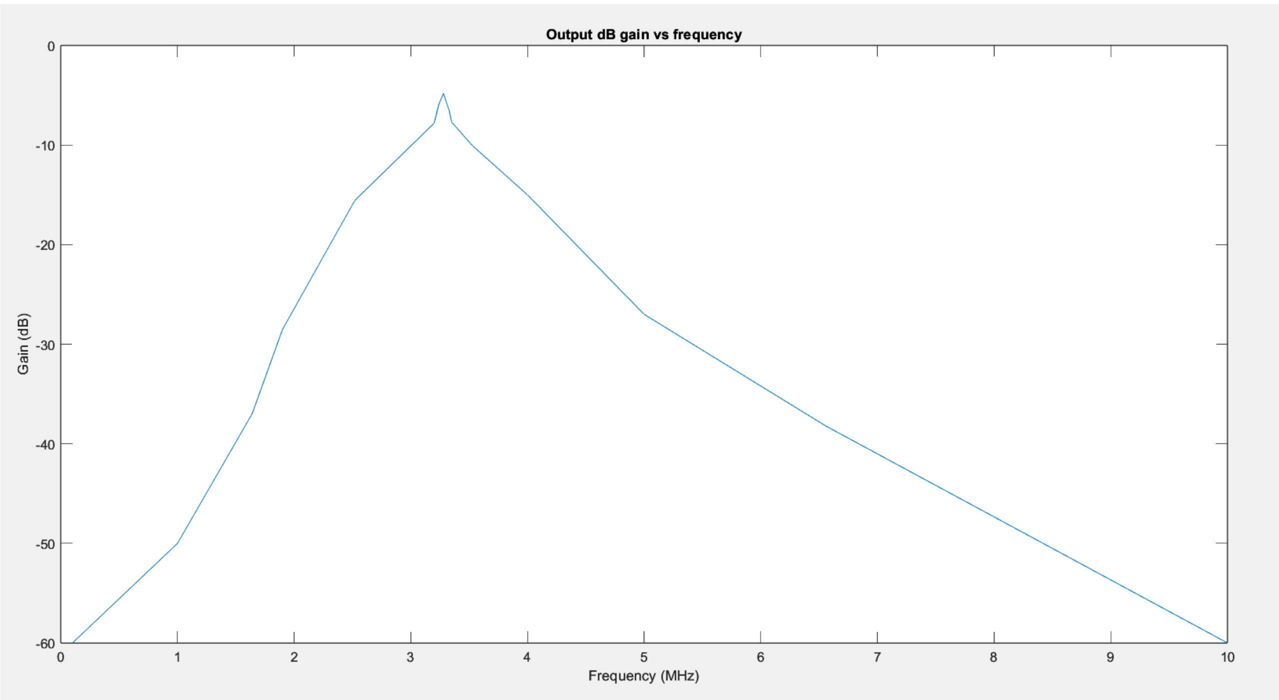

Figure 22: Frequency response plot

Conclusion

The software results for the band-pass filter were promising since all conditions were satisfied. The center frequency was 3MHz as expected, and the bandwidth was obtained with a very small error of 0.027%. In the hardware lab, however, the center frequency in which the maximum gain was obtained was 3.28MHz. The 9.3% error in the center frequency might have occurred since the inductances and capacitances were acquired with series and parallel combinations of components, and their exact value may not have been obtained. Moreover, the components in the lab have tolerance values and inner resistances.

In the hardware lab, the gain at center frequency was -4.81dB, whereas in the software lab it was -70.2mdB. To find the cut-off frequencies, instead of looking for the -3dB value, this time the -7.81dB value (3dB less than the maximum gain) was searched by varying the frequency. They were found as 3.2MHz and 3.35MHz. So, despite the error in the center frequency, the bandwidth was obtained with 0% error. The other conditions were also satisfied in the hardware.

Overall, when the data was plotted, the result was a distorted graph which partly resembles the plot in the software part. To improve this, and also to minimize the errors, higher order Butterfield filters can be designed, in other words, more components can be used. As the order increases, the accuracy also increases. In conclusion, this lab demonstrated how to create a band-pass filter in both software and hardware. Band-pass filters are crucial circuits in electrical engineering; hence this lab was helpful to grasp the concept overall.