Bilkent University

EE-202 Circuit Theory

Lab 1

Time-Domain and Frequency-Domain Analyses in LTSpice

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Section 02

Introduction

This lab aims to perform time-domain and frequency-domain analyses, along with OPAMP circuit analysis using LTSpice for software, and to construct and analyze the circuits with hardware components. The task includes 3 parts, which will be implemented separately.

Analysis

To find the 3-dB cut-off frequency of the RL circuit in parts 1 and 2, the following formula is used:

$$f_c = \frac{R}{2\pi L}$$

where f_c is the cut-off frequency (Hz), R is the resistance (Ohm) and L is the inductance (Henry) in the circuit. For the first RL circuit, the values are chosen as R=20 Ω and L= 100 µH. The cut-off frequency of the first circuit f_{c1} is:

$$f_{c1} = \frac{20}{2\pi \times 100 \times 10^{-6}} = 31.83\ kHz$$

For the second circuit with the realistic voltage source model, the 50 Ω series resistance of the source is also considered. So, this time the value of R is 50 Ω + 20 Ω= 70 Ω. The cut-off frequency of the second circuit f_{c2} is:

$$f_{c2} = \frac{70}{2\pi \times 100 \times 10^{-6}} = 111.41\ kHz$$

Simulations

Part 1: Transient (time-domain) Analysis

For part 1, firstly a simple voltage divider circuit is implemented. The values are chosen as R1=4 Ω, R2= 16 Ω, and the voltage source is a sinusoidal wave with an amplitude of 8V and frequency of 5 kHz. The circuit and the plot of input and output voltages are shown in Figure 1.

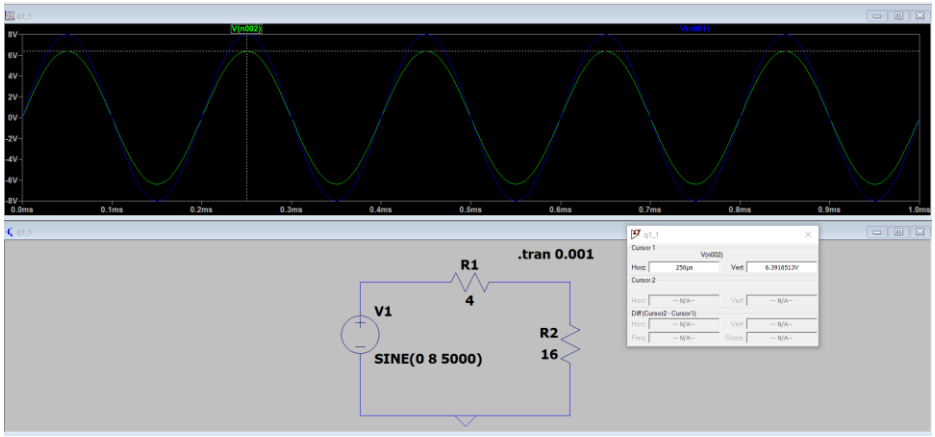

Figure 1: Voltage divider circuit and output plot

In the second step, the value of R1 is changed to 20 Ω and R2 is replaced with an inductor with a value of 100 µH. The voltage source is a sinusoidal wave with an amplitude of 5V, and a frequency of 100 kHz. The modified circuit is shown in Figure 2.

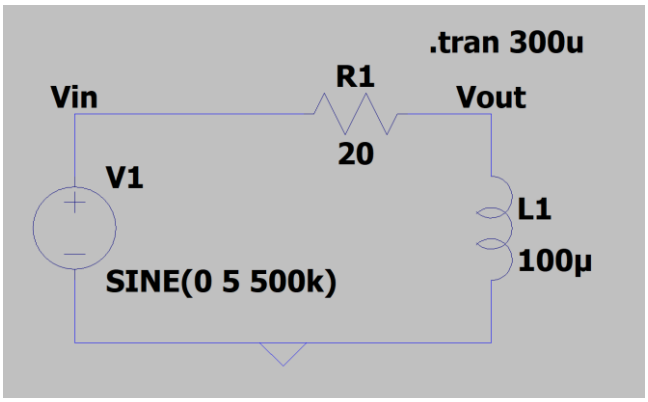

Figure 2: RL circuit

The circuit is then simulated. The plot for 100 kHz frequency is shown in Figure 3. After that, the frequency is changed to 10 kHz, 500 kHz and lastly to the circuit's cut-off frequency 31.8 kHz, and the circuit is simulated again. The results are shown in Figures 4-6. The output voltage amplitudes are presented in Table 1.

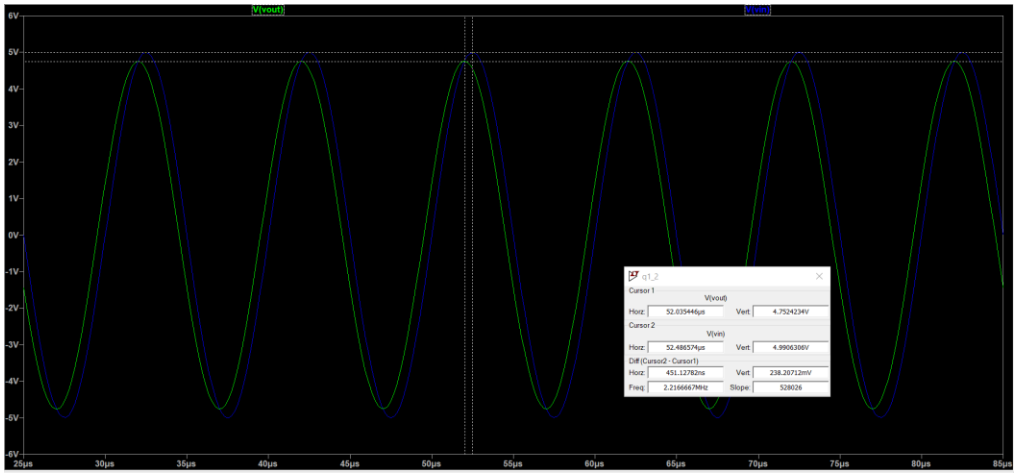

Figure 3: Input and output voltages at 100 kHz frequency

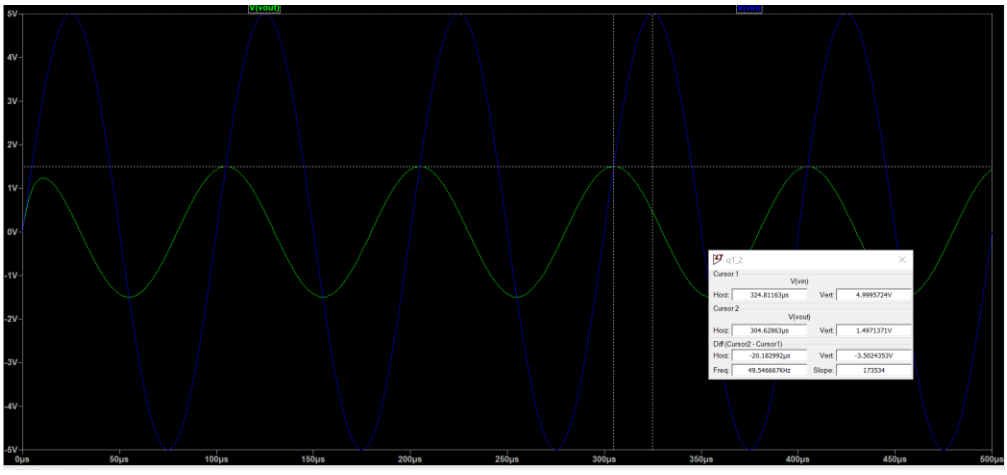

Figure 4: Input and output voltages at 10 kHz frequency

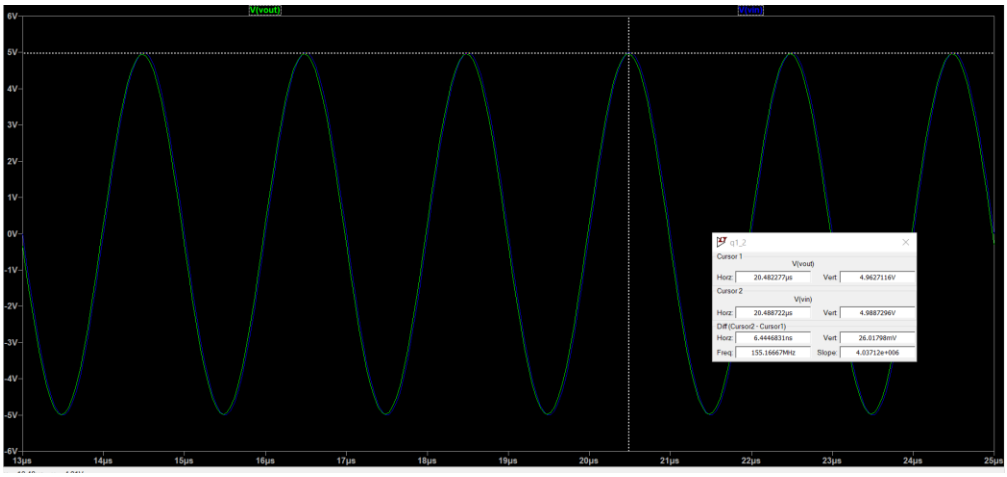

Figure 5: Input and output voltages at 500 kHz frequency

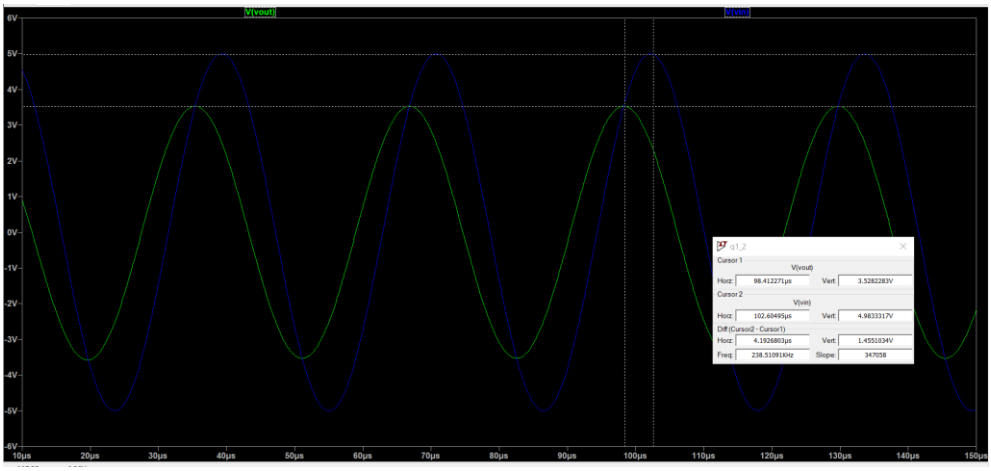

Figure 6: Input and output voltages at 31.8 kHz frequency, the cut-off frequency of the circuit

Frequency (kHz)	Output Voltage Amplitude (Volts)
10	1.5
31.8	3.53
100	4.75
500	4.96

Table 1: Output voltage amplitudes.

As the frequency is increased, the amplitude of the output signal is getting larger and the phase is decreasing. It shows that this circuit is a high-pass filter.

Part 2: AC (frequency-domain) Analysis

After the simulation parameters are modified for AC analysis, the same circuit is simulated. The voltage source has an AC amplitude of 1 for small signal AC analysis. The output plot is

a logarithmic plot from 100 Hz to 10 MHz and it shows the magnitude and phase of the output with respect to frequency. Figure 7 shows the output voltage plot. For this RL circuit, the 3-dB cut-off frequency is around 32 kHz.

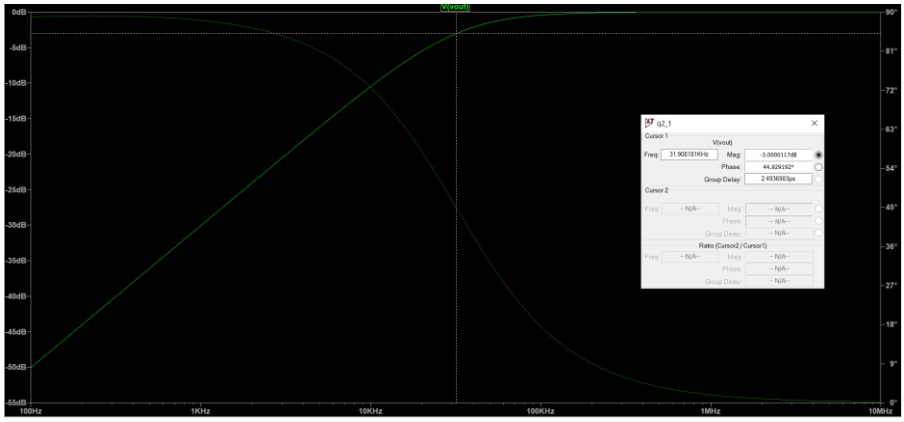

Figure 7: Output voltage plot on logarithmic axis, the -3 dB frequency is shown

The voltage source in the circuit is then modified to have a 50 Ω series resistance to match the voltage source in the hardware labs. The modified circuit is shown in Figure 8. After the circuit is simulated, a new logarithmic plot is obtained, shown in Figure 9. The magnitude of the output voltage decreased compared to the previous circuit. Also, the 3-dB cut-off frequency is around 112 kHz this time.

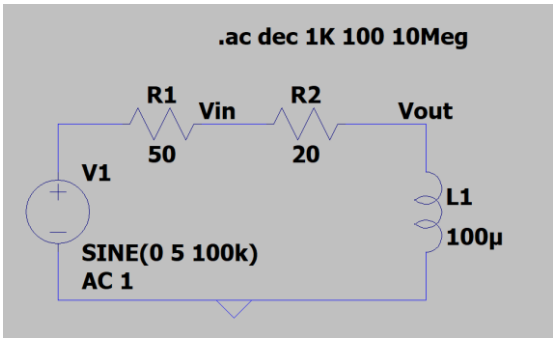

Figure 8: Modified RL circuit

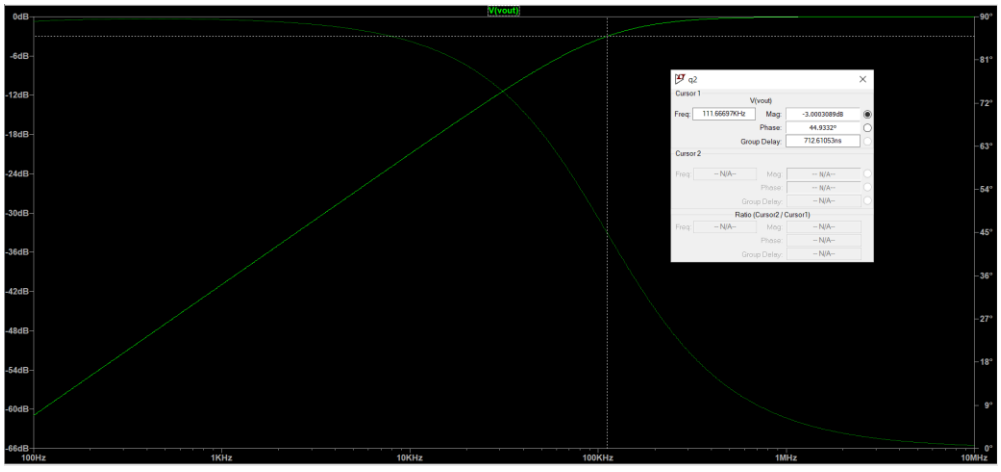

Figure 9: Logarithmic plot of the second circuit's output, the -3 dB frequency is shown

When the ratio of output voltage and the voltage at the output of the realistic signal generator is plotted, shown in Figure 10, the cut-off frequency again turned out as approximately 32 kHz, and the same plot in Figure 7 is obtained. It is because the plotted voltage source consists of the 50 Ω resistance inside, the same RL circuit from the first step is implemented with the same values.

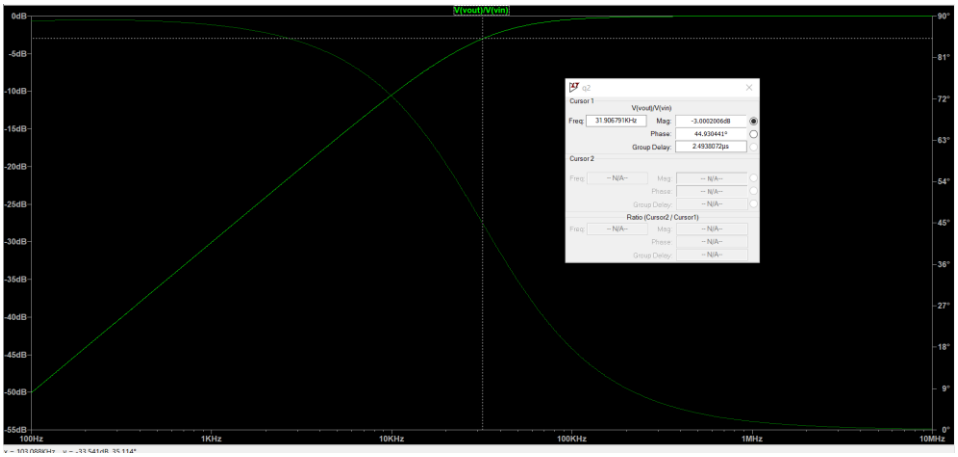

Figure 10: Output voltage versus input voltage of the realistic source model, plotted on logarithmic scale

Part 3: OPAMP Circuits

For the first step, LM324 OPAMP model is used in the circuit. 8 V DC voltages are connected to the DC supplies of the OPAMP. The input voltage to a sinusoidal wave with an amplitude of 1V, and frequency of 1 kHz. The value of R3 is 1 kΩ, and R1 and R2 are chosen as 170 Ω and 680 Ω respectively, with R2/R1 = 4. The OPAMP circuit can be seen in Figure 11.

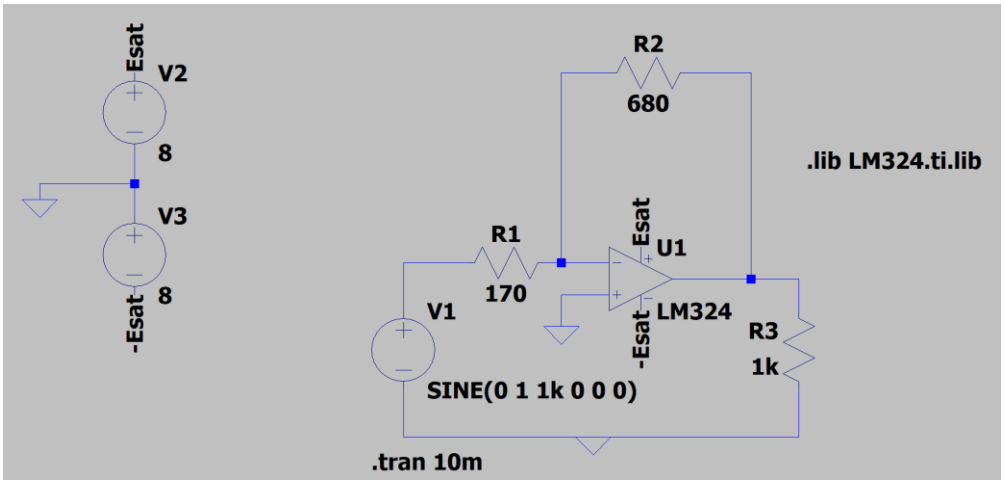

Figure 11: First OPAMP circuit

The output and input signal plot is shown in Figure 12. The signal is amplified from 1V to 4V, and by node analysis, the ratio of the output voltage magnitude to that of the input is equal to the ratio R2/R1, which is also 4. The signal is also inverted with respect to the input; hence this circuit is an inverting amplifier.

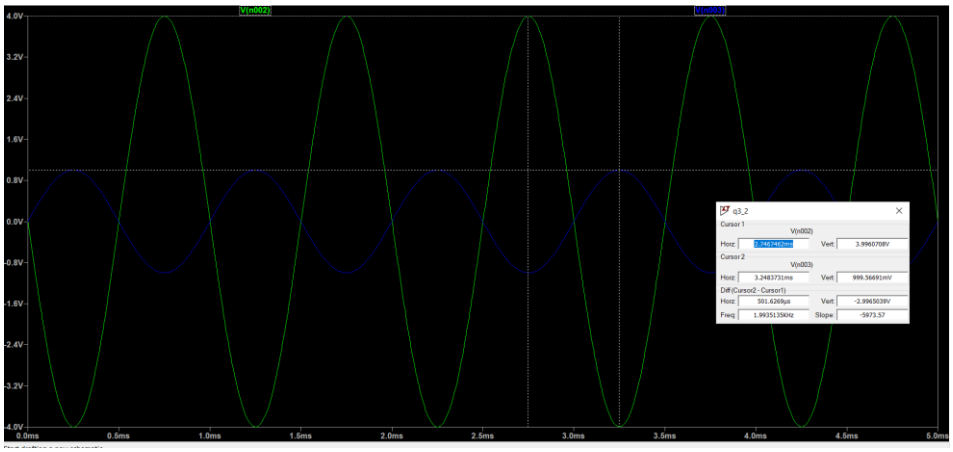

Figure 12: The input and amplified output waveforms

When the input is changed to a square wave (pulse) with 1V amplitude with 1ms period and % 50 duty cycle, and with the rise and fall times of 10ns, the circuit is simulated again. The output plot is shown in Figure 13.

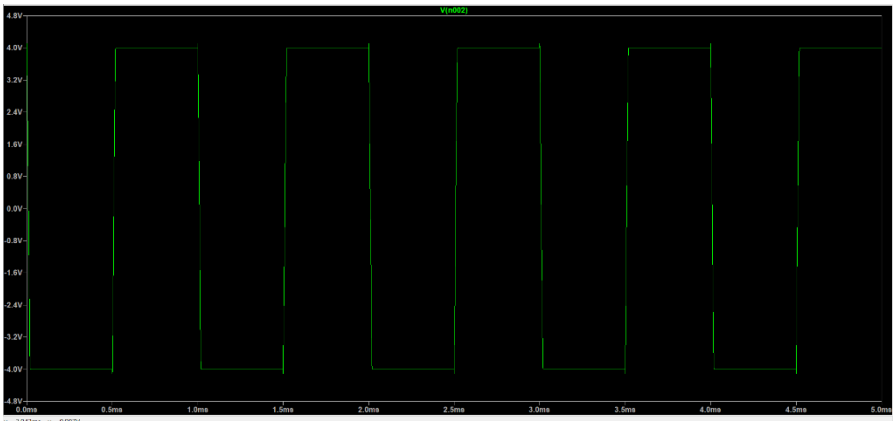

Figure 13: The output waveform for square wave input

To observe the saturation, the value of R2 is then increased to 5 kΩ. The saturated output is shown in Figure 14.

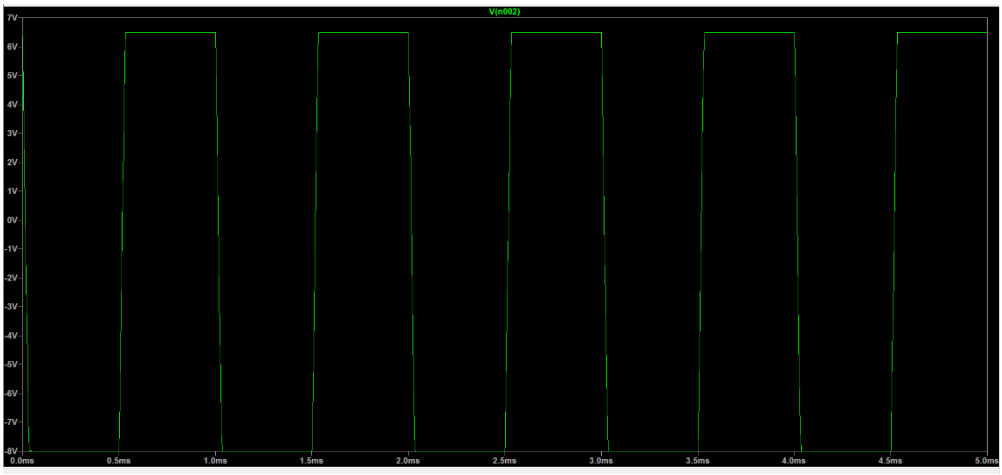

Figure 14: The saturated output waveform for square wave input

Lastly, the value of R1 is changed to 8 kΩ and R2 is replaced with a 3 nF capacitor. The new circuit is shown in Figure 15.

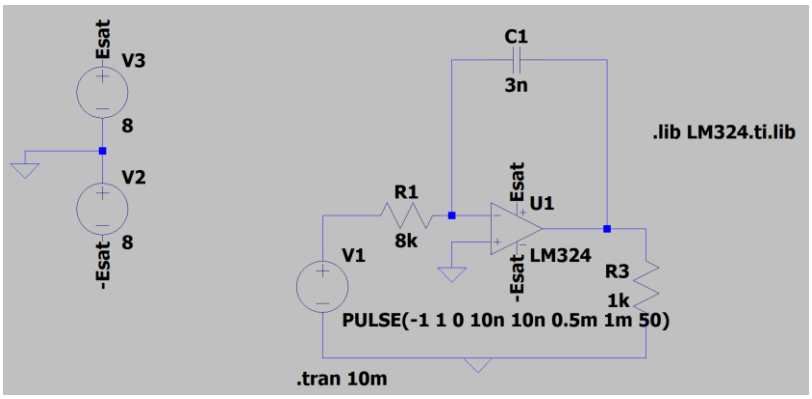

Figure 15: The second OPAMP circuit with the capacitor

After the circuit is simulated with the same square wave input, the output plot is shown in Figure 16. The output signal is a saturated trapezoid wave, and it is actually the integrated form of the input signal. Hence this is an integrator circuit.

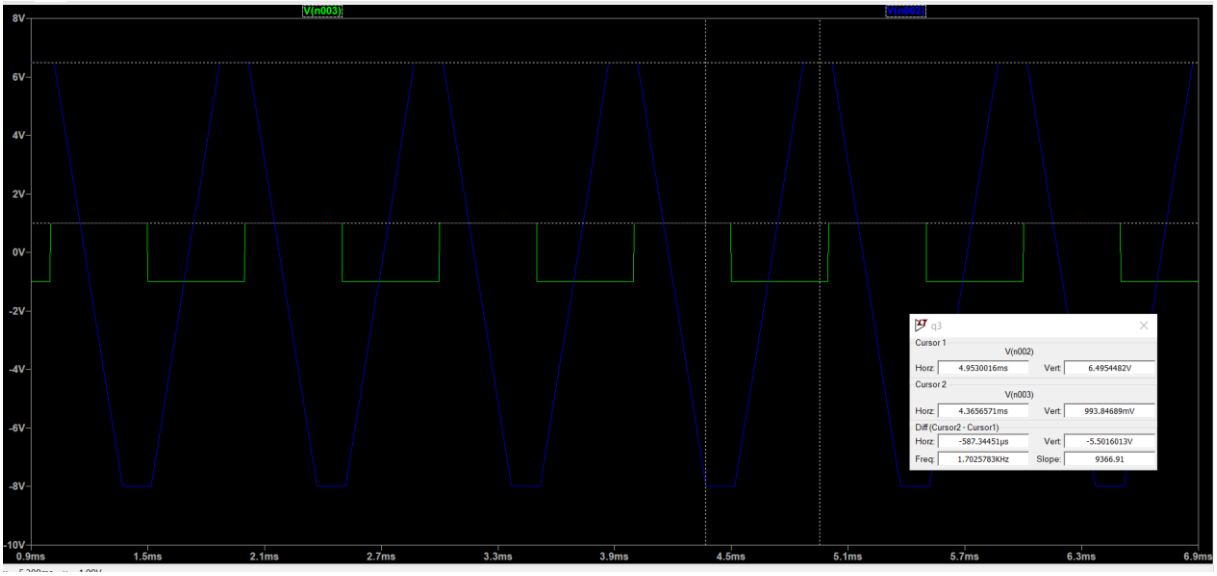

Figure 16: The input and output waveform, output is a trapezoid wave

Hardware Implementation

Part 1: RL circuit

Before implementing the RL circuit in Part 1, the circuit in the software part is modified so that the voltage source's series resistance of 50 Ω is also considered, just like in part 2 of the software lab. The hardware results will be compared to see whether they match the results in the software part. Figures 17-21 show the new circuit and the results corresponding to 10 kHz, 100 kHz, and 500 kHz frequencies along with the cut-off frequency 111.4 kHz. The output voltage amplitudes are presented in Table 2.

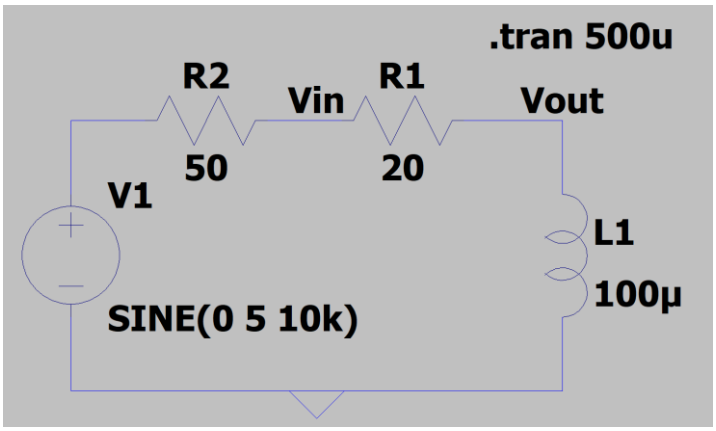

Figure 17: RL circuit modified for the hardware implementation

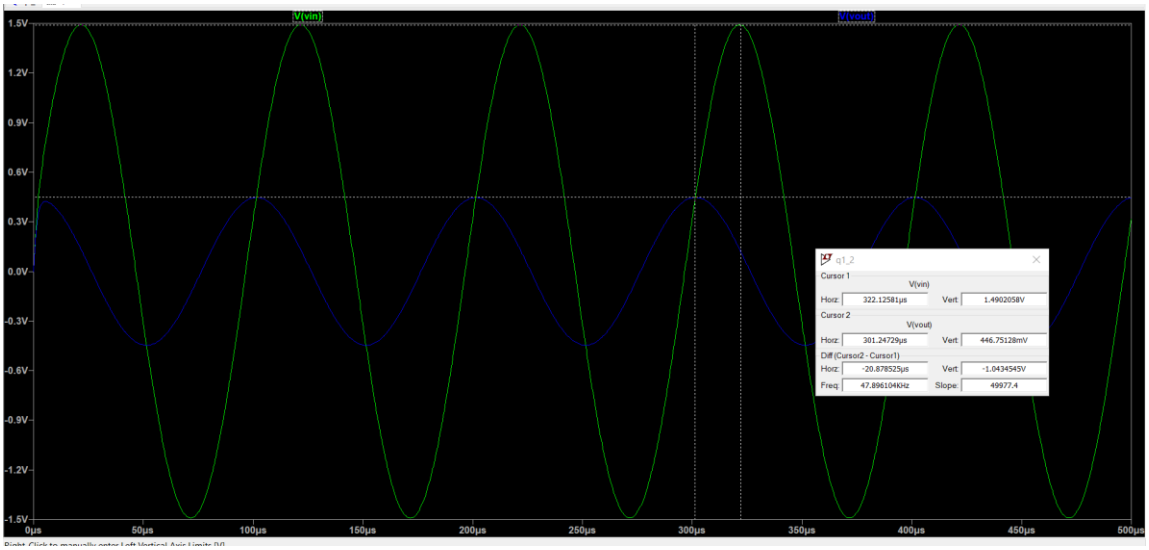

Figure 18: Output voltage for 10 kHz frequency

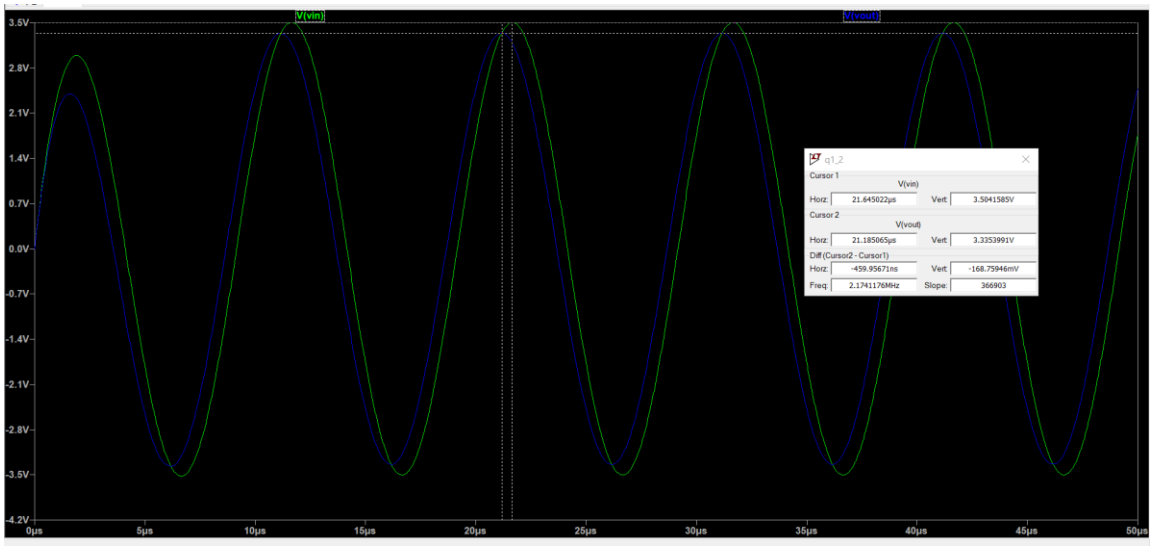

Figure 19: Output voltage for 100 kHz frequency

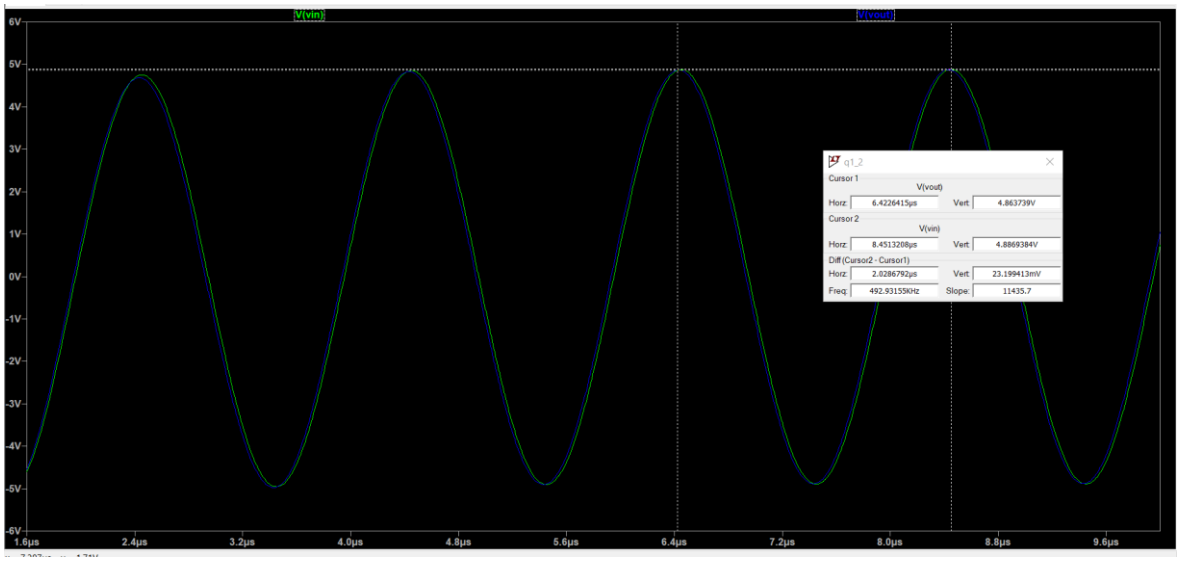

Figure 20: Output voltage for 500 kHz frequency

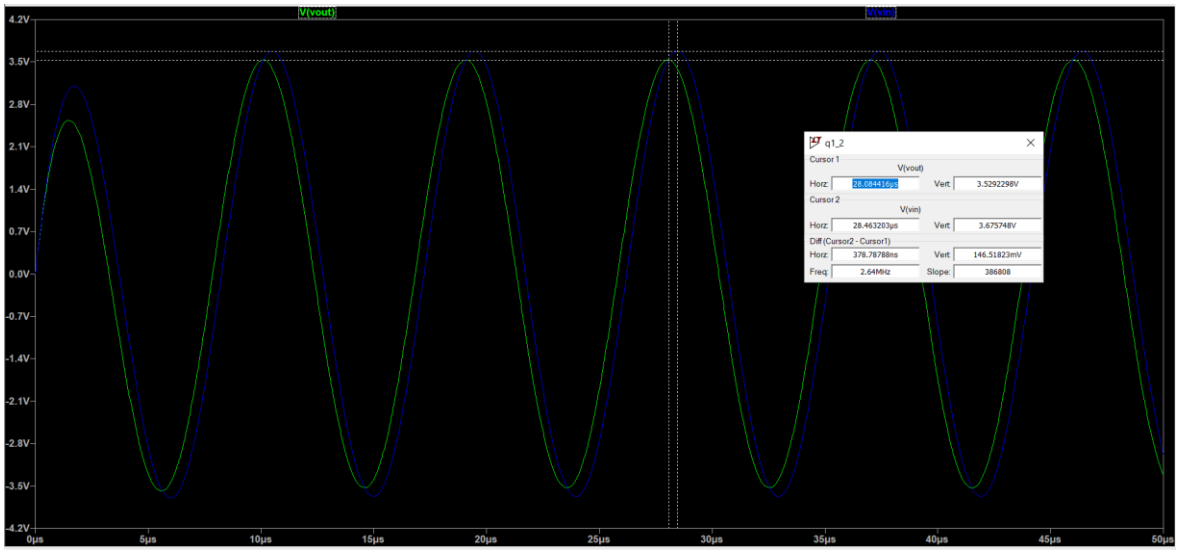

Figure 21: Output voltage for 111.5 kHz frequency, the second circuit's cut-off frequency

Frequency (kHz)	Output Voltage Amplitude (Volts)
10	0.44
100	3.34
111.5	3.53
500	4.86

Table 2: Output voltage amplitudes.

To construct the RL circuit, a 22 Ω resistance and an axial inductor of 100 μH are used on a breadboard. The hardware circuit can be seen in Figure 22.

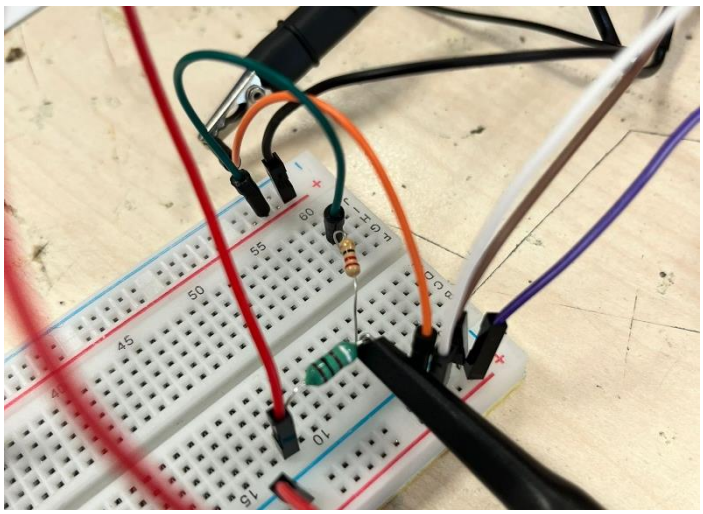

Figure 22: Hardware RL circuit

After the implementation, the sinusoidal input voltage and the output voltage on the inductor are measured with an oscilloscope for 10 kHz, 100 kHz, and 500 kHz frequencies. Also, to find the cut-off frequency of the circuit, the frequency where the output voltage amplitude was around 3.53 V was measured since the ratio of the output voltage to the input is $1/\sqrt{2}$ at that frequency and the input has 5 V amplitude. The cut-off frequency turned out as approximately 111.5 kHz. The results are shown in Figures 23-26 and in Table 3, where also error percentages were calculated with respect to the data in Table 2.

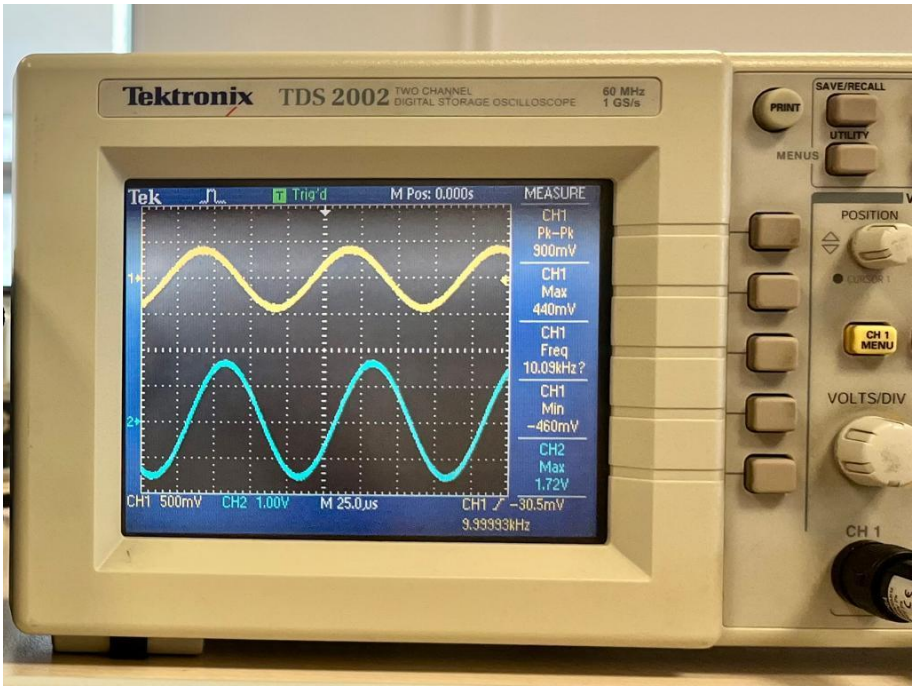

Figure 23: Input and output voltage for 10 kHz frequency (output waveform is shown in yellow, input is blue)

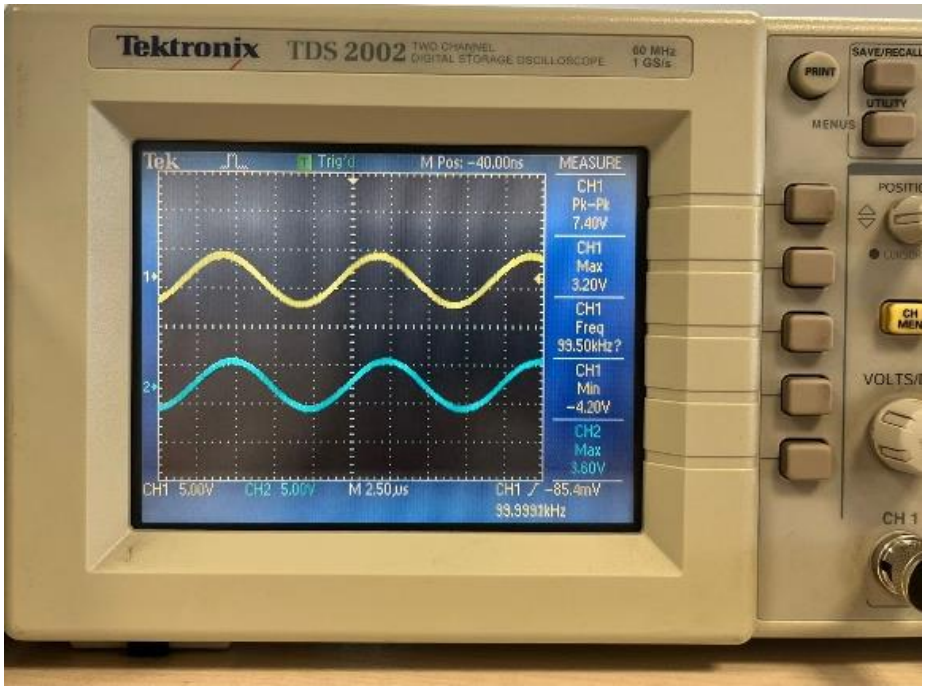

Figure 24: Input and output voltage for 100 kHz frequency

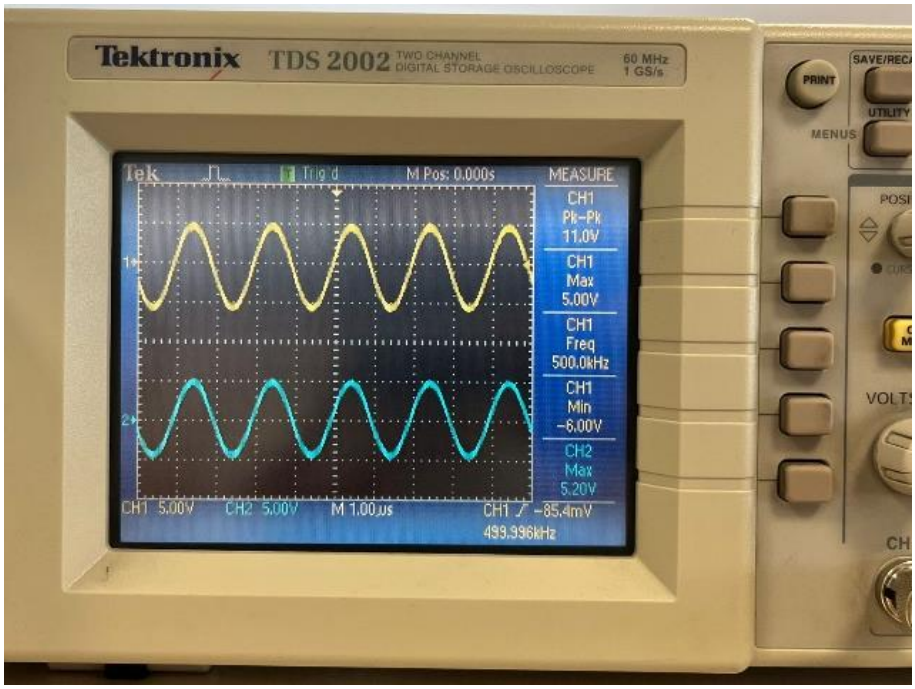

Figure 25: Input and output voltage for 500 kHz frequency

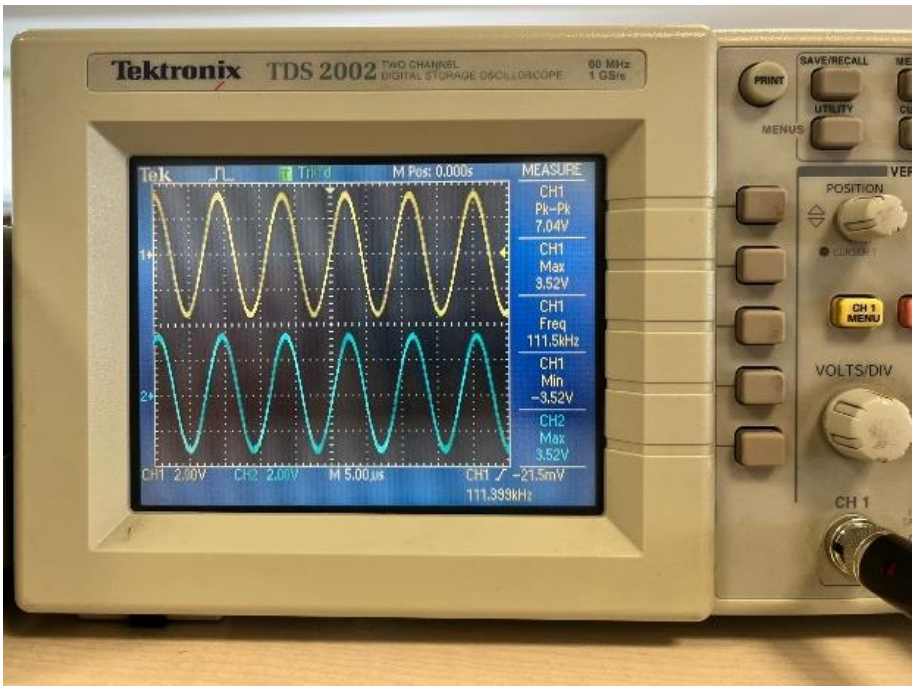

Figure 26: Voltages for 111.5 kHz frequency, the circuit's cut-off frequency

Frequency (kHz)	Output Voltage Amplitude (Volts)	Error percentage
10	0.44	0%
100	3.2	4.2%
111.5	3.52	0.28%
500	5	2.8%

Table 3: Results of voltage measurements.

The dB magnitude is then calculated using the formula:

$$A = 20 \log_{10} \frac{V_{out}}{V_{in}}$$

where V_{in}= 5 V, then a rough frequency response plot is drawn for the measured frequencies in Figure 27. The drawn plot is similar to the logarithmic plot in Figure 9, where the circuit was modified to consider the series resistance of the voltage source. Likewise, as the frequency increases, the gain approaches to unity. The cut-off frequency where the gain is -3 dB also match, which was 111.6 kHz in the logarithmic plot.

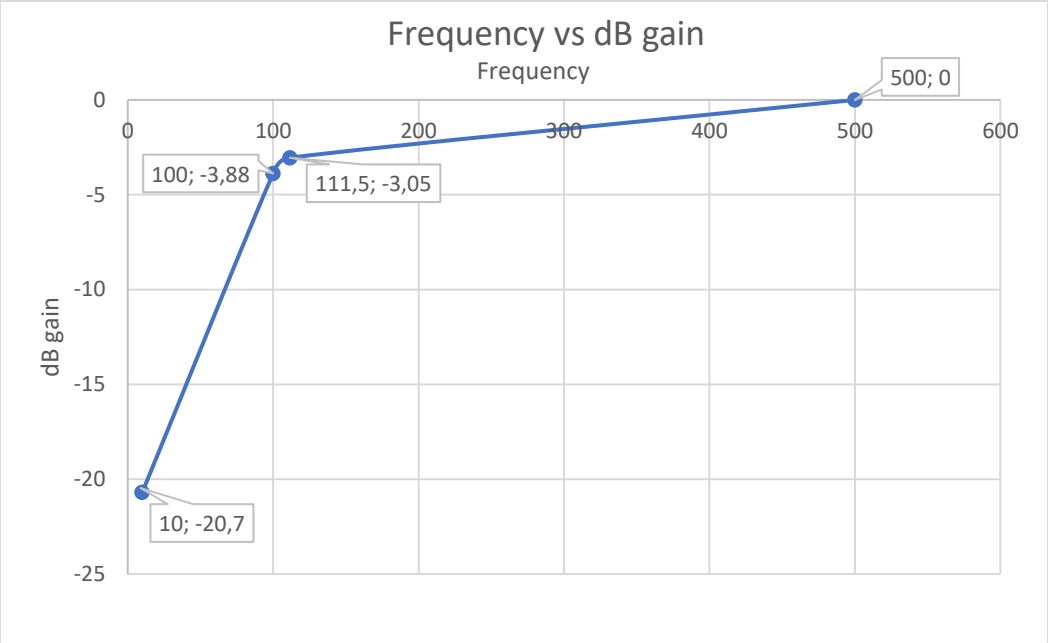

Figure 27: Plot of frequency versus dB gain

Part 2: OPAMP circuit

The first OPAMP circuit is implemented using the LM324 OPAMP available in the lab, along with 120 Ω, 680 Ω, and 1 kΩ resistors. The reason why R1 is chosen as 120 Ω is that the remaining 50 Ω of the original 170 Ω value comes from the series resistance of the voltage source. The hardware circuit and the output and input voltage measurement on the oscilloscope can be seen in Figures 28-29. Then the output amplitudes are noted for several different input amplitudes in Table 4.

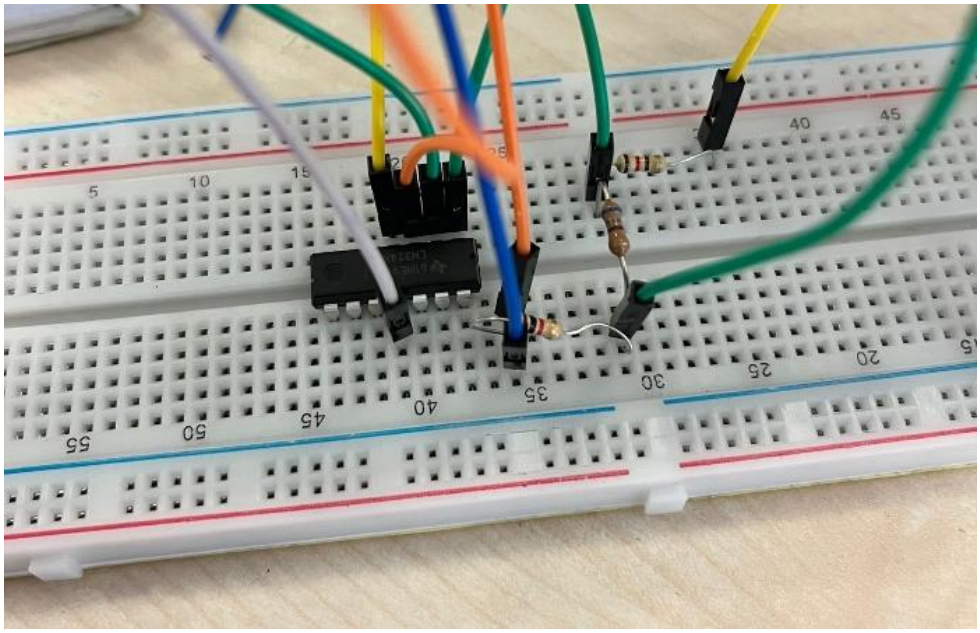

Figure 28: First OPAMP circuit on hardware

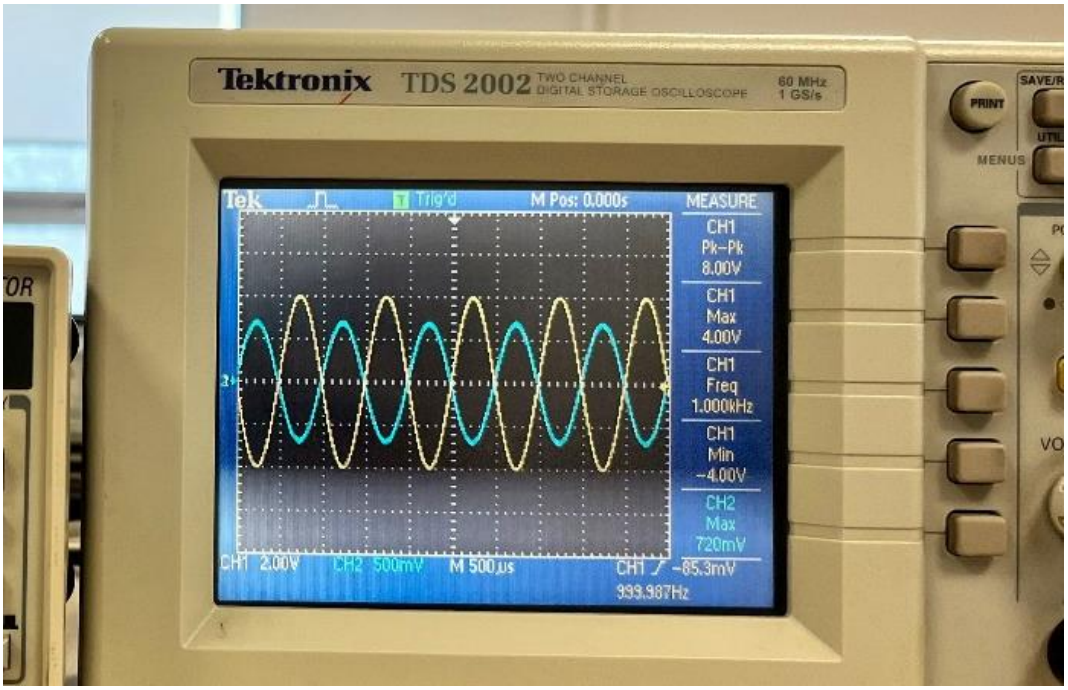

Figure 29: Output (shown in yellow) and input (shown in blue) waveform

Input Voltage Amplitude (Volts)	Output Voltage Amplitude (Volts)
1	4
2	8.2
5	21.2
10	39.7

Table 4: Results of voltage measurements.

The second OPAMP circuit is also implemented by changing R2 to 8.2 kΩ, and connecting 2 nF and 1 nF capacitors in parallel. The input voltage is changed to a square wave with 1 V amplitude and 1 Hz frequency, then the output is measured. The hardware circuit, along with the output and input voltage measurement on the oscilloscope can be seen in Figures 30-31.

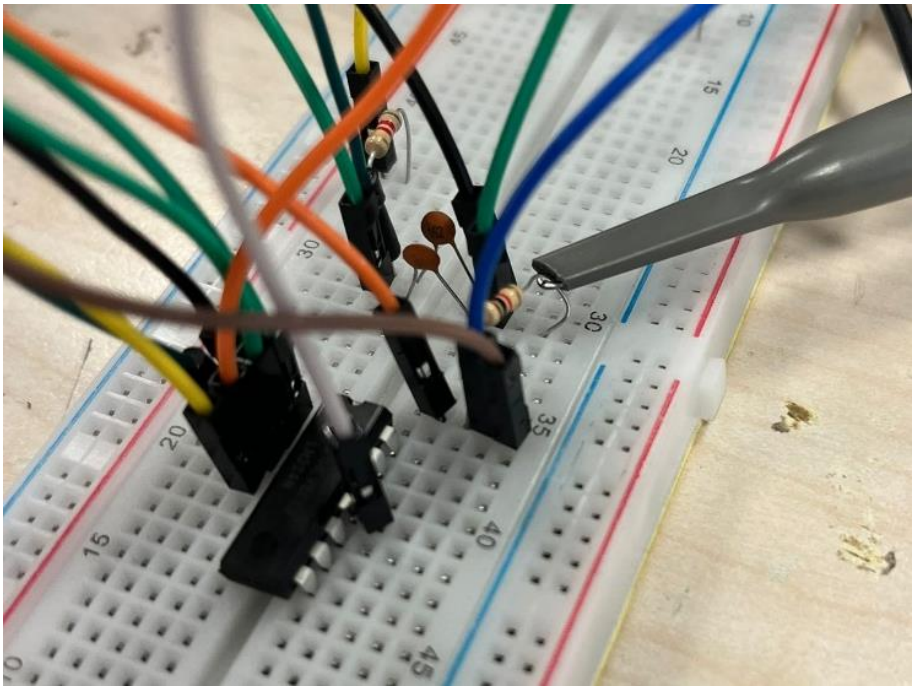

Figure 30: Second OPAMP circuit on hardware

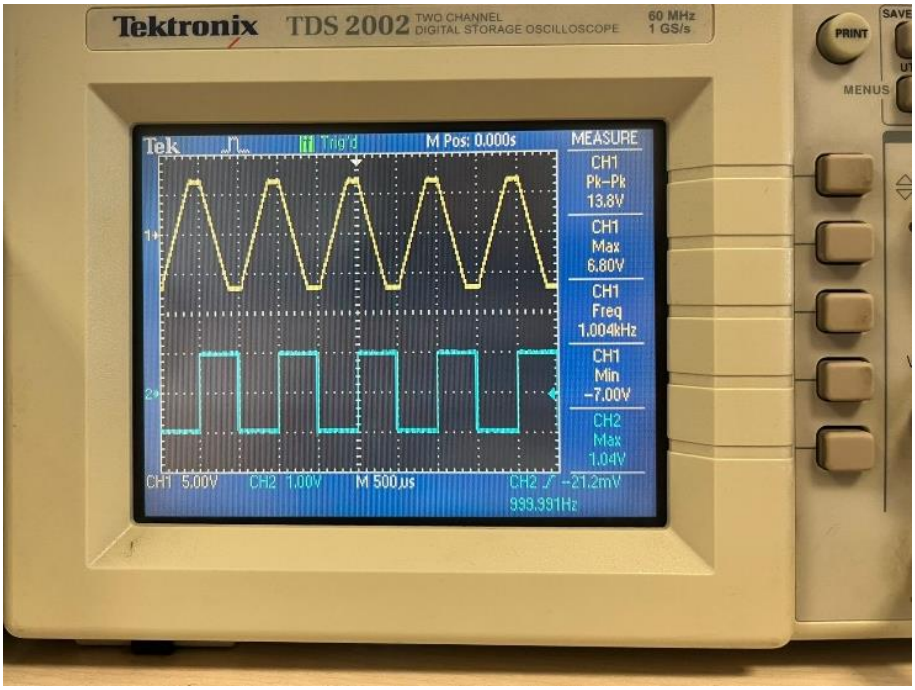

Figure 31: Output (shown in yellow) and input (shown in blue) waveforms

Conclusion

For the RL circuit, the results of the software and hardware implementations matched with slight numerical errors. Comparing the data from Tables 1 and 2, the errors were very small, with 0%, 4.2%, 0.28% and 2.8% for 10, 100, 111.5 and 500 kHz frequencies. However, comparing the data to that of Table 1, the results don't match. The reason is that the series resistance of the voltage is ignored for the first RL circuit, however, it is implemented in the second.

The cut-off frequency of the hardware RL circuit turned out approximately 111.5 kHz, and it was calculated previously as 111.41 kHz for the second RL circuit. For the first RL circuit without the series resistance, the frequency was 31.8 kHz, which was the case when the ratio of output voltage and the voltage at the output of the realistic signal generator was plotted in Figure 10. It is because the plotted voltage source consists of the 50 Ω resistance inside, the same RL circuit from the second step of software lab is implemented with the same values. As the output voltage magnitude approached to unity as the frequency increased, this RL circuit is a high pass filter.

For the first OPAMP circuit, both the simulated and the hardware measurement of the output voltage amplitude was 4 V. The reason why the results exactly matched was because the series resistance of the voltage source was taken into consideration and the resistors were chosen accordingly. As seen from the input and output waveforms, the circuit is an inverting amplifier with the equation:

$$V_{out} = -\frac{R_2}{R_1} V_{in}$$

For this case R2/R1 was chosen as 4, so the resulting waveform was amplified with a factor of 4 and was inverted with respect to the time axis.

The second OPAMP circuit's software and hardware results also matched with very small differences, with an error of 5.4% with respect to the peak-to-peak voltages. In both software and hardware, the output was a trapezoid wave. This circuit is an integrator circuit, the triangular waveform is actually the integrated form of the square waveform input. It is then saturated from the top and bottom parts, giving it the trapezoid shape. The output voltage of the circuit has an equation as:

$$V_{out} = -\frac{1}{R_1 C} \int_0^t V_{in} dt$$

where in this case R1 = 8 kΩ, C = 3 nF and V_{in} is a square wave input voltage. Overall, this lab demonstrated how to make analyses using LTSpice and implementing the circuits using hardware components.