Bilkent University

EEE-313

Lab 3

nMOS Common Source Amplifier

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Section 01

I. Introduction

This experiment aims to characterize a 2N7000 nMOS transistor and design an nMOS common source voltage amplifier using the obtained results. The conditions are shown in Figure 1.

$R_{in} > 30k\Omega$
$R_{out} < 2k\Omega$
$10mA < I_D < 15mA$
$|A_V| = |v_{out} / v_{in}| > 9$ when v_{in}=100mV$_{pp}$ sine wave @ 10kHz

Figure 1: Conditions for the amplifier

The lab consists of 4 parts. In the first part, the threshold voltage (V_{TH}) of the nMOS will be found and the drain current (I_{DS}) versus the drain-source voltage (V_{DS}) will be plotted, given a test circuit. In the second part, for different gate voltages, again I_{DS} vs. V_{DS} will be plotted, then the parameters K_N and λ will be determined, given another test circuit.

Using these values in part 3, the amplifier will be constructed, by first calculating the g_m and r_o (small signal parameters) and performing analysis on the small signal model of the circuit. For the gain, the intervals given in Figure 1 should be considered. After the circuit is constructed, the gain will be measured by giving 100 mV sine wave as an input. Then, the input voltage will be increased to the point where the output voltage is distorted. Lastly, in part 4, a capacitor will be placed parallel to the source resistance R_E and the result will be investigated.

In the circuit, resistors and capacitors are present. The resistors bias the transistor so that it operates in the SAT region, while the coupling capacitors help isolate the DC and AC voltages. The resistor and capacitor values in the amplifier should be determined considering the gain and the limits for R_{in} and R_{out} (AC input/output resistances). The 2N7000 transistors are present in the lab, and the current must not exceed 50 mA during testing.

II. Hardware Implementation and Analysis

- **Part 1 - Finding the threshold voltage V_{DS}**

The test circuit schematic is given in Figure 2. In the circuit, it can be seen that the gate and drain are connected together. This transistor is therefore “diode-connected”, enabling it to operate always in SAT mode whenever it is ON (since V_{DS}=V_{GS}, the saturation condition V_{DS}>V_{GS}-V_{TH} is always satisfied if it is on and if its threshold voltage is bigger than 0, which is true for our case). By applying KVL, the relation of I_{DS} and V_{DS} can be explained as:

$$V_{DS} = V_{GS} = V_{DD} - I_{DS}(100\Omega) \quad (1)$$

given that R=100Ω, which is added for safety purposes and should not be skipped.

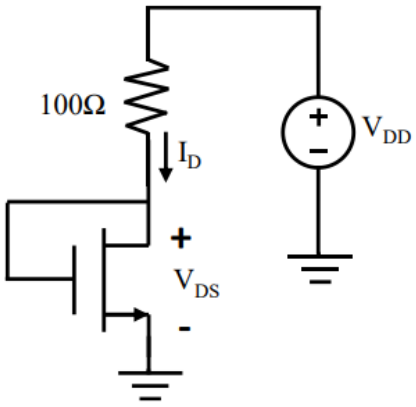

Figure 2: Test circuit for part 1

After the circuit is set on hardware, the supply voltage V_{DD} will be increased continuously and the current will be measured by a multimeter and be noted. The multimeter must be connected in series with the resistor and transistor. Then, given the relation in equation 1, the corresponding V_{DS} will be calculated. With the collected data, the I-V curve will be generated.

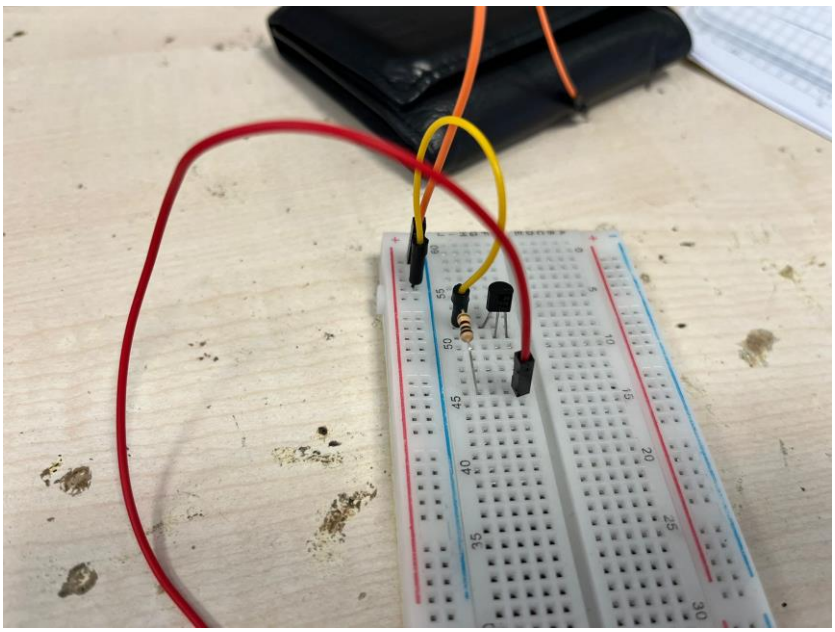

Figure 3: Circuit set up

First, to find V_{TH}, we may assume that the transistor is on when I_{DS}=1 mA, as given in the manual. Noting that V_{GS}=V_{DS}, the V_{DS} value found for this case will be the threshold voltage. When the input is increased slowly, the 1 mA current is first observed for V_{DD}=1.65 V. Using equation 1, and substituting I_{DS}=1mA, V_{DD}=1.65 V, the threshold voltage is found as:

$$V_{TH} = 1.65 - 1mA * 100\Omega = 1.55\,V$$

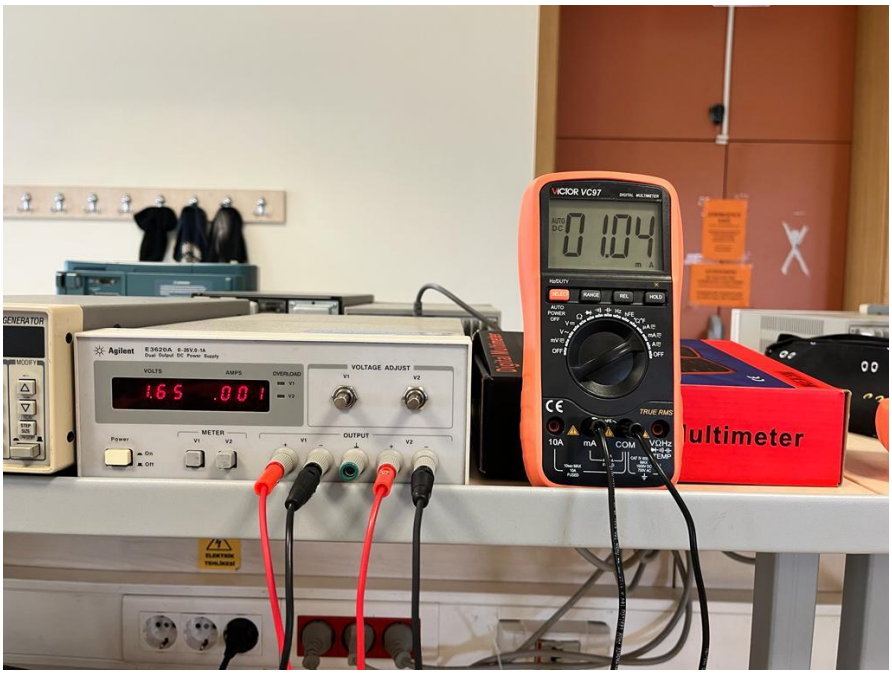

Figure 4: Transistor is on for V_{DD}=1.65V

After that, the given V_{DD} and measured I_{DS} values are recorded until 30 mA. Using the relation in equation 1, I_{DS} vs V_{DS} is plotted using MATLAB. The measurements are presented in Table 1.

V_{DD} (V)	I_{DS} (mA)	V_{DD} (V)	I_{DS} (mA)	V_{DD} (V)	I_{DS} (mA)	V_{DD} (V)	I_{DS} (mA)
0	0	2.05	4	3.24	14	4.38	24
0.5	0	2.24	5	3.41	15	4.47	25
1	0	2.35	6	3.47	16	4.59	26
1.2	0	2.46	7	3.59	17	4.71	27
1.3	0	2.57	8	3.68	18	4.88	28
1.4	0	2.62	9	3.88	19	4.92	29
1.5	0	2.82	10	3.98	20	5	30
1.65	1	2.9	11	4.09	21		
1.83	2	3.09	12	4.15	22		
1.94	3	3.17	13	4.3	23		

Table 1: Measurements of V_{DD} and I_{DS}

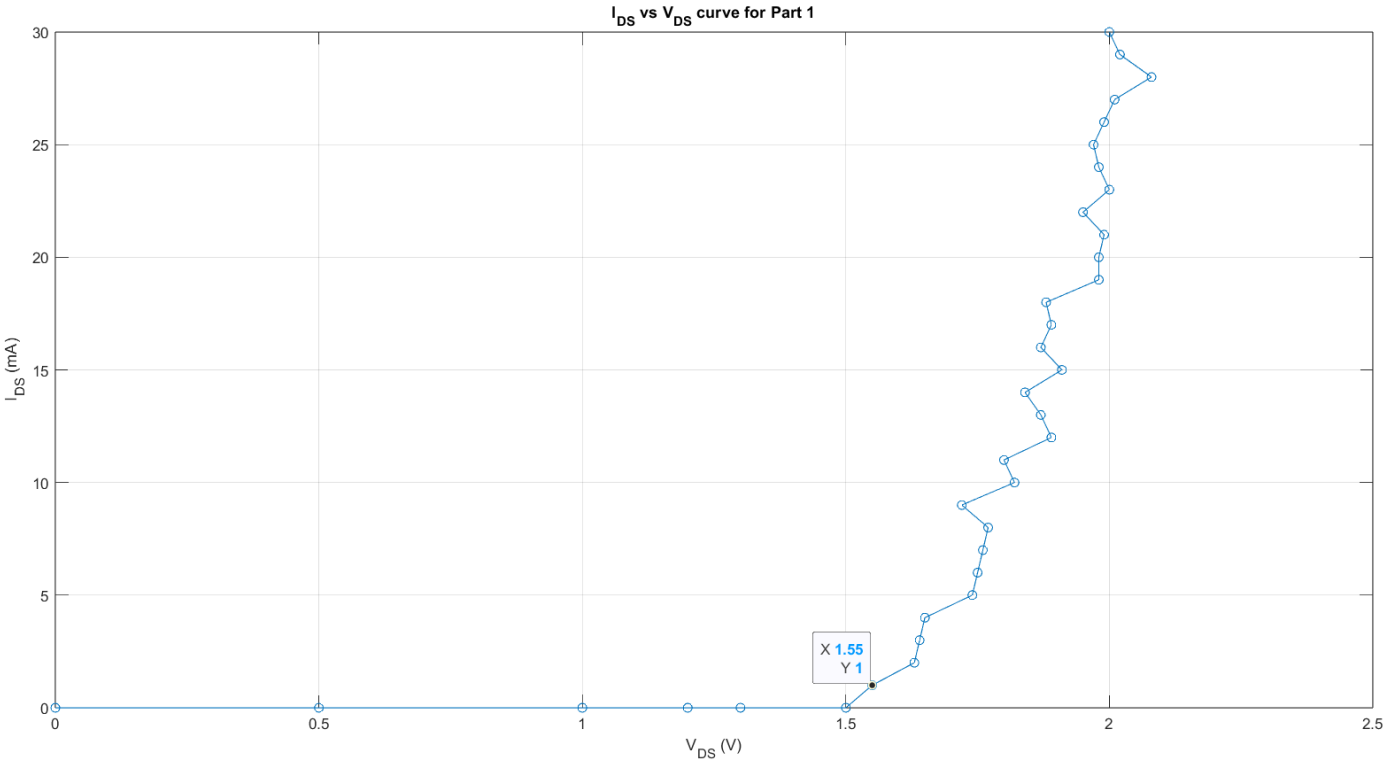

Figure 5: I-V plot of test circuit, the turn-on point is marked.

Later, using the curve fitter tool in MATLAB, this is fitted to an exponential curve, shown in Figure 6.

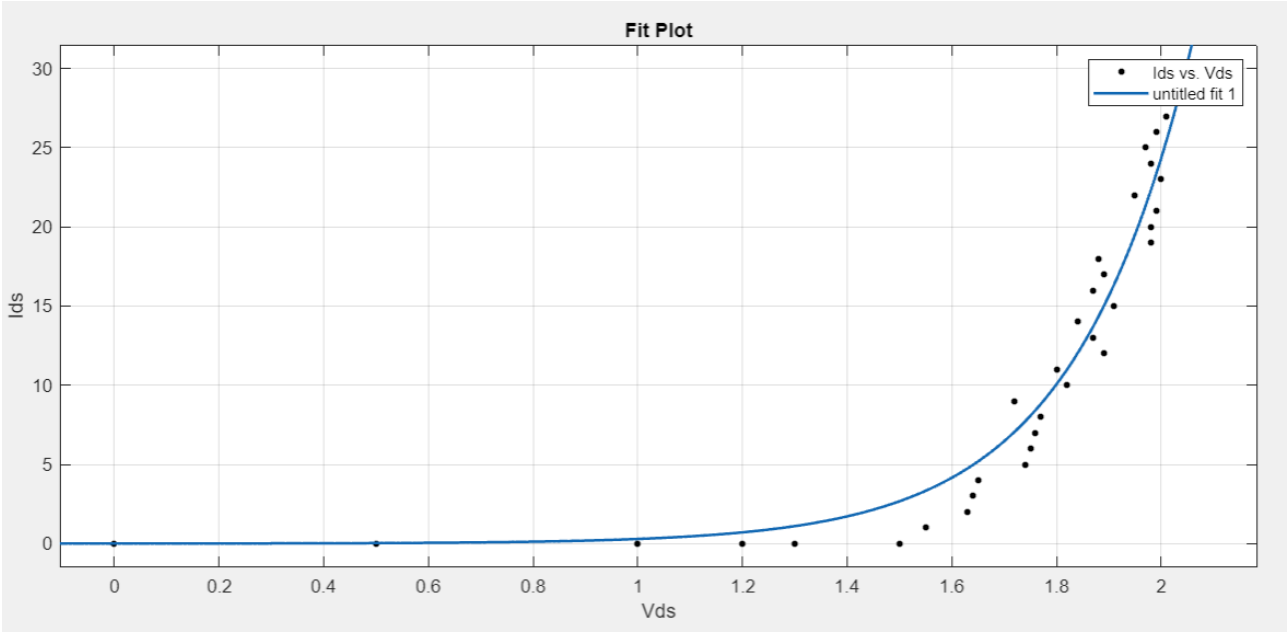

Figure 6: The plot fitted to an exponential curve.

As expected, the I-V curve is exponential and is fitted to an exponential curve with very small error (with R-square: 0.9354). This is because the gate and voltage is connected together, and the current in saturation mode is given as:

$$I_{DS} = K_N(V_{GS} - V_{TH})^2 = K_N(V_{DS} - V_{TH})^2 \quad (2)$$

giving a quadratic relation between V_{DS} and I_{DS}. Since the plot resembles an exponential I-V curve of a diode, this is called a "diode-connected" transistor.

- **Part 2 - Generating I-V curves to calculate K_N and λ**

The circuit schematic for this part is given in Figure 7.

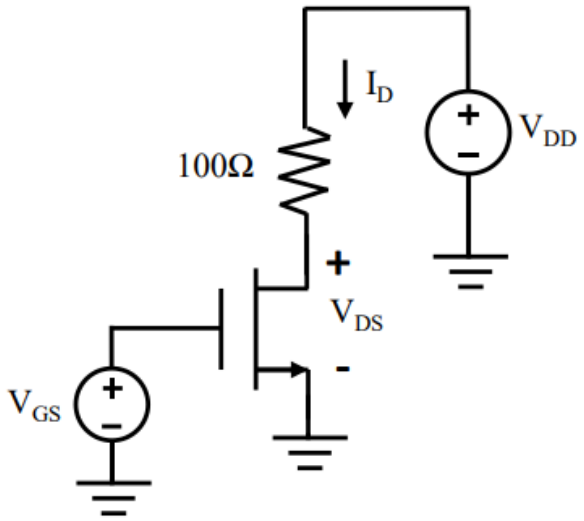

Figure 7: Test circuit for part 2

This time, V_{GS} is also given from the power supply. Three different values of V_{GS} will be given to obtain 3 different I-V curves: V_{TH}+0.3 V, V_{TH}+0.4 V, and V_{TH}+0.5 V, corresponding to 1.85 V, 1.95 V, 2.05 V respectively. Then, like in the previous part, V_{DD} will be increased and I_{DS} will be measured and recorded. By applying KVL, it can be seen that equation 1 still holds:

$$V_{DS} = V_{DD} - I_{DS}(100\Omega) \quad (3)$$

but this time V_{GS} is fixed. As V_{DD} is increased, the transistor is expected to move out of TRIODE mode to SAT. This will occur when:

$$V_{DS} > V_{GS} - V_{TH} \quad (4)$$

and the difference between V_{GS} and V_{TH} are given as 0.3, 0.4, 0.5 V respectively. In SAT mode, the current is given as:

$$I_{DS} = K_N(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \quad (5)$$

For the three curves, therefore;

$$I_{DS,1} = K_N(0.3)^2(1 + \lambda V_{DS,1}) \quad (6)$$

$$I_{DS,2} = K_N(0.4)^2(1 + \lambda V_{DS,2}) \quad (7)$$

$$I_{DS,3} = K_N(0.5)^2(1 + \lambda V_{DS,3}) \quad (8)$$

when in the SAT region. The coefficients K_N and λ are to be determined using these equations. K_N is a transconductance parameter determined by the mobility of electrons, oxide capacitance per unit area, also the width/length ratio (design parameters) of the transistor. It has units mA/V^2. λ is the channel length modulation parameter, which increases I_{DS} with increasing V_{DS} in SAT mode. Ideally, it is taken as zero, but the real value is needed to determine the finite output resistance in part 3. It has units of V^{-1}. Both values can vary within the MOSFET transistors.

The circuit for part 2 is set up as shown in Figure 8.

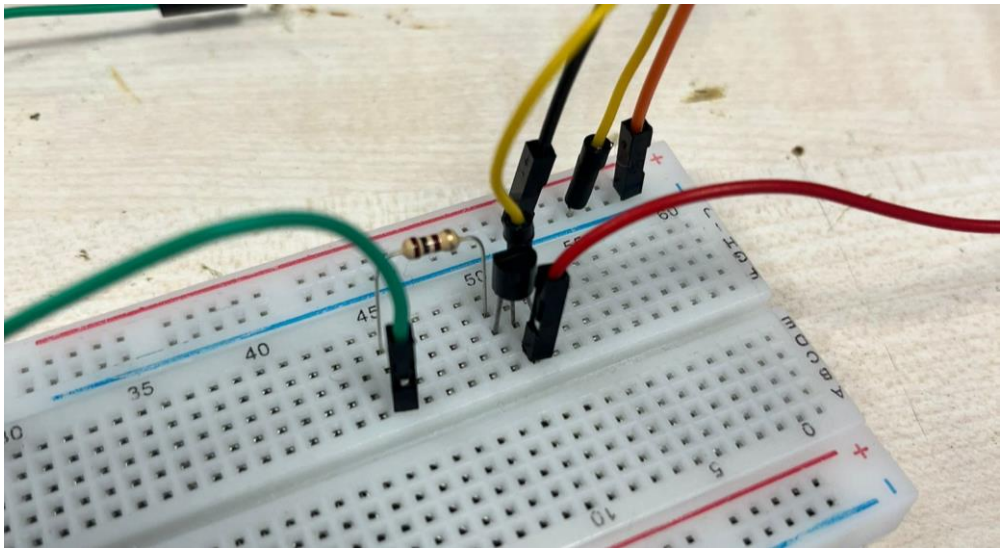

Figure 8: Circuit set up

Now, V_{DD} and I_{DS} values will be recorded for V_{GS}=1.85 V, 1.95 V and 2.05 V. The results are presented in Tables 2-4.

V_{DD} (V)	I_{DS} (mA)	V_{DD} (V)	I_{DS} (mA)	V_{DD} (V)	I_{DS} (mA)
0.1	1.02	1.2	9.15	3.2	10.82
0.15	1.36	1.3	9.61	3.5	10.9
0.2	1.68	1.5	10.23	3.71	10.94
0.35	3.04	1.7	10.45	4	11.01
0.5	4.08	2	10.58	4.2	11.6
0.7	5.79	2.2	10.62	4.5	11.72
0.8	6.66	2.3	10.66	4.7	11.8
0.9	7.43	2.5	10.72	5	12.03
1	7.98	2.7	10.76		
1.1	8.74	3	10.8		

Table 2: Measurements of V_{DD} and I_{DS} for V_{GS}=1.85 V

V_{DD} (V)	I_{DS} (mA)	V_{DD} (V)	I_{DS} (mA)	V_{DD} (V)	I_{DS} (mA)	V_{DD} (V)	I_{DS} (mA)
0.12	1.16	1	9.13	2.7	21.46	5.2	25.6
0.15	1.4	1.1	9.43	3	22.94	5.5	26.52
0.22	1.96	1.2	10	3.2	24.10	5.7	26.7
0.3	2.67	1.3	10.96	3.5	24.57	6	26.73
0.4	3.42	1.5	11.69	3.7	24.89		
0.5	4	1.7	13.4	4	25.03		
0.6	4.8	2	15	4.2	25.1		
0.7	5.39	2.2	17.67	4.5	25.2		
0.8	6.38	2.3	19.43	4.7	25.25		
0.9	7.45	2.5	20.08	5	25.35		

Table 3: Measurements of V_{DD} and I_{DS} for V_{GS}=1.95 V

V_{DD} (V)	I_{DS} (mA)	V_{DD} (V)	I_{DS} (mA)	V_{DD} (V)	I_{DS} (mA)	V_{DD} (V)	I_{DS} (mA)
0.12	1.21	1	10.35	2.7	28.96	5.2	38.02
0.15	2.06	1.1	12.1	3	31.41	5.5	38.24
0.22	2.71	1.2	13.98	3.2	32.8	5.7	38.6
0.3	3.61	1.3	15.86	3.5	35.12	6	38.63
0.4	4.83	1.5	18.48	3.7	35.9		
0.5	5.45	1.7	20.36	4	36.8		
0.6	6.57	2	21.28	4.2	37.25		
0.7	7.58	2.2	23.02	4.5	37.62		
0.8	8.57	2.3	24.54	4.7	37.84		
0.9	9.46	2.5	27.11	5	37.9		

Table 4: Measurements of V_{DD} and I_{DS} for V_{GS}=2.05 V

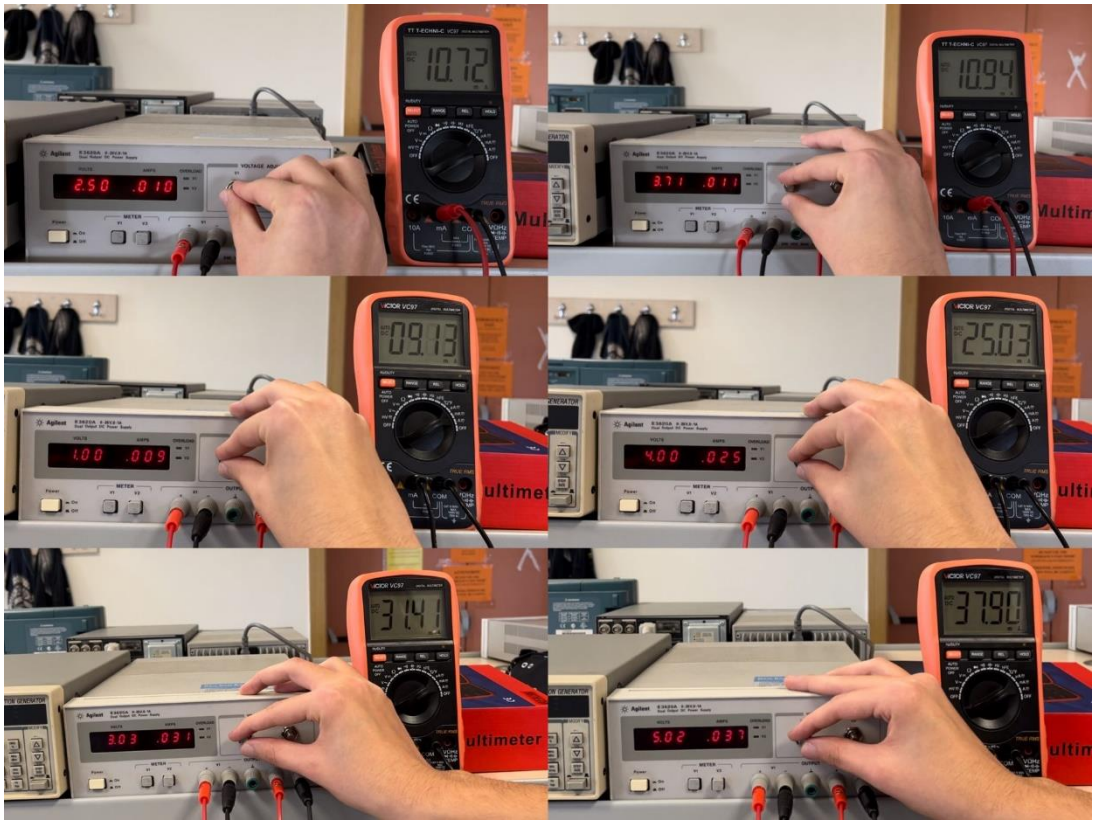

Figure 9: Some measurement records, first row is for V_{GS}=1.85 V, second row is for V_{GS}=1.95 V, third row is for V_{GS}=2.05 V

Noting the relation between V_{DD} and V_{DS} as shown in equation 3, three I-V curves are generated using MATLAB.

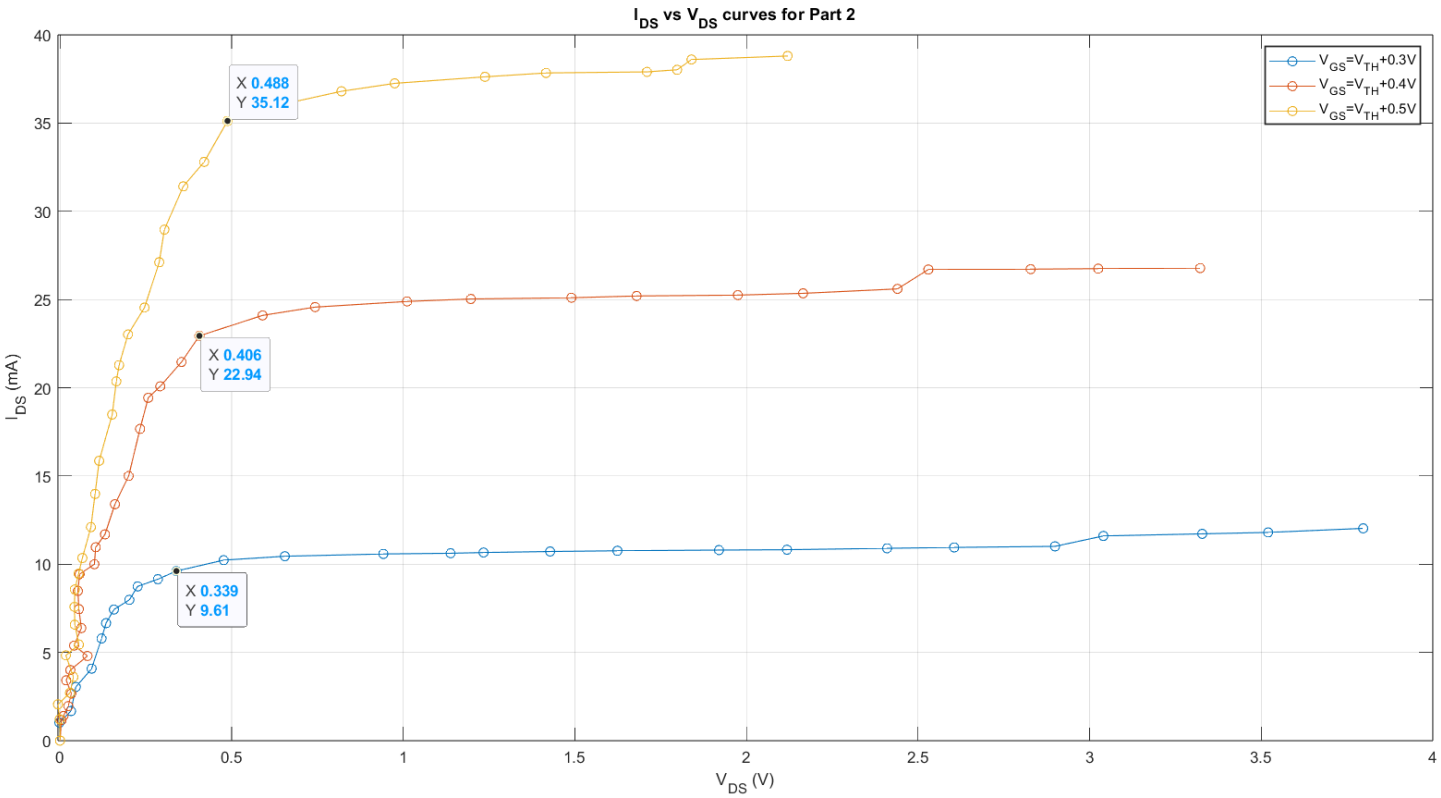

Figure 10: Three I-V curves are generated, approximated saturation points are marked

After that, to determine K_N and λ, I used the curve fitter tool again. Writing a custom equation as $y=K*(0.3)^2*(1+L.x)$, where y is the I_{DS} data vector and x is the V_{DS} data vector, MATLAB fits the data into the given equation and determines the best fitting value for K and L (K_N and λ). Note that the data after saturation is taken, since the equation holds for only that part. Repeating it for 0.4 V and 0.5 V (V_{GS}-V_{TH}) cases also, I took the best fitting data (highest R-square), which is for 0.4 V. The fitted curve for the saturated part and the estimation is given Figures 10-11.

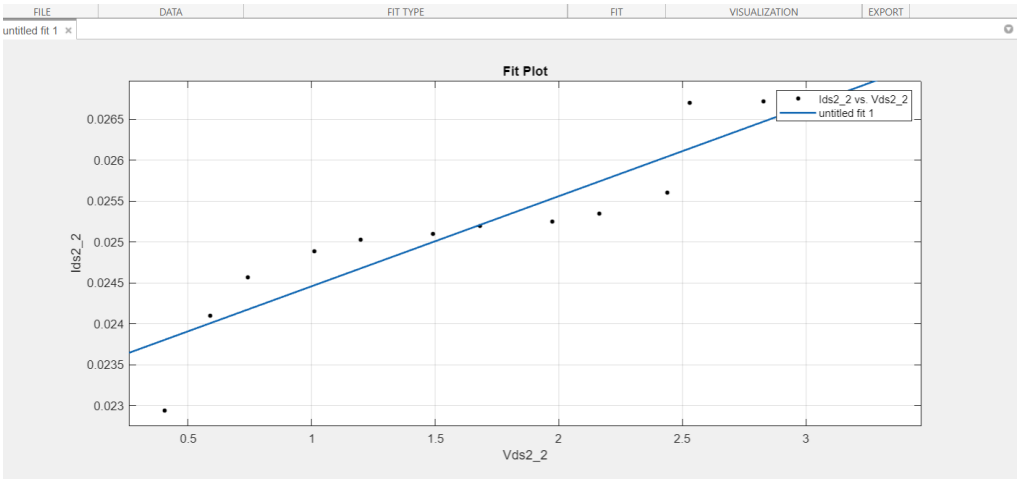

Figure 11: Fit plot for the saturation part

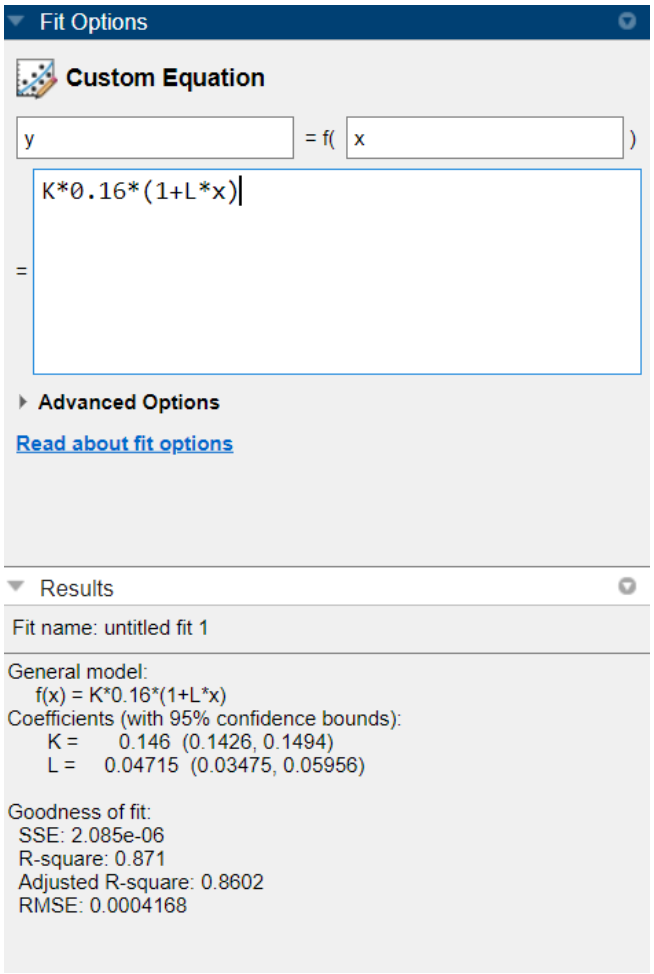

Figure 12: K is estimated as 0.146 (A/V^2) and L is 0.047 (V^{-1})

Converting to appropriate units, we have:

$$K_N = 146\, mA/V^2, \lambda = 0.047\, V^{-1}$$

The values are within the expected range of K_N and λ [2]. Considering the three I-V curves, they also conform to the expected I-V curve of an nMOS transistor. After the V_{DS} reaches approximately 0.3, 0.4 and 0.5 V (at V_{DS}=0.339, 0.406, 0.488 respectively), the current's increase nearly stops, indicating SAT region. This is consistent with the fact that SAT mode is reached when V_{DS} exceeds V_{GS}-V_{TH}. Still, there is still a minor increase in current in SAT mode, due to the channel length modulation effect, indicating the presence of λ.

- **Part 3 - Common source amplifier design**

The schematic for the amplifier is given in Figure 13. The resistance and capacitor values are to be determined, considering the required gain and intervals for R_{in}, R_{out}.

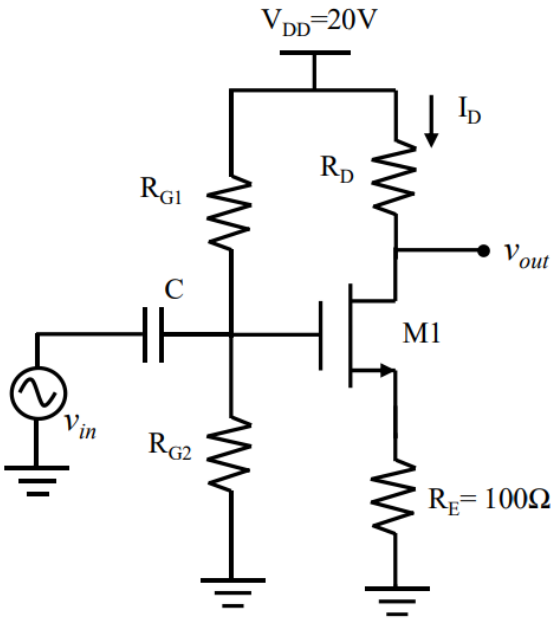

Figure 13: Common source amplifier schematic

First, we are given that the current at the DC operating point I_D should be between 10 mA and 15 mA. I chose I_D as 12.5 mA. Now, for the analysis of the circuit so that we can design it, a DC analysis is needed in the first place [2]. Knowing the current, first the V_{GS} of the transistor can be calculated. Assuming SAT and using equation 5 (and ignoring λ for the DC analysis part), we need:

$$I_{DS} = K_N(V_{GS} - V_{TH})^2 \Rightarrow 12.5\,mA = 146 * (V_{GS} - 1.55)^2$$

using the previously found results. Solving the equations, we have V_{GS}=1.25 V or V_{GS}=1.84 V. Since we need $V_{GS}>V_{TH}$ for the transistor to be ON, the needed V_{GS} is therefore:

$$V_{GS} = 1.84\,V$$

To have this value for the V_{GS}, it can be seen that at the gate of the transistor there is a voltage divider, since the capacitor is open-circuited in the DC analysis, and the gate current for a MOSFET is zero (the gate is isolated with an oxide). The source voltage can also be calculated, since the current and the resistance value at the source is given. To find R_{G1} and R_{G2}, therefore, the following procedure can be conducted:

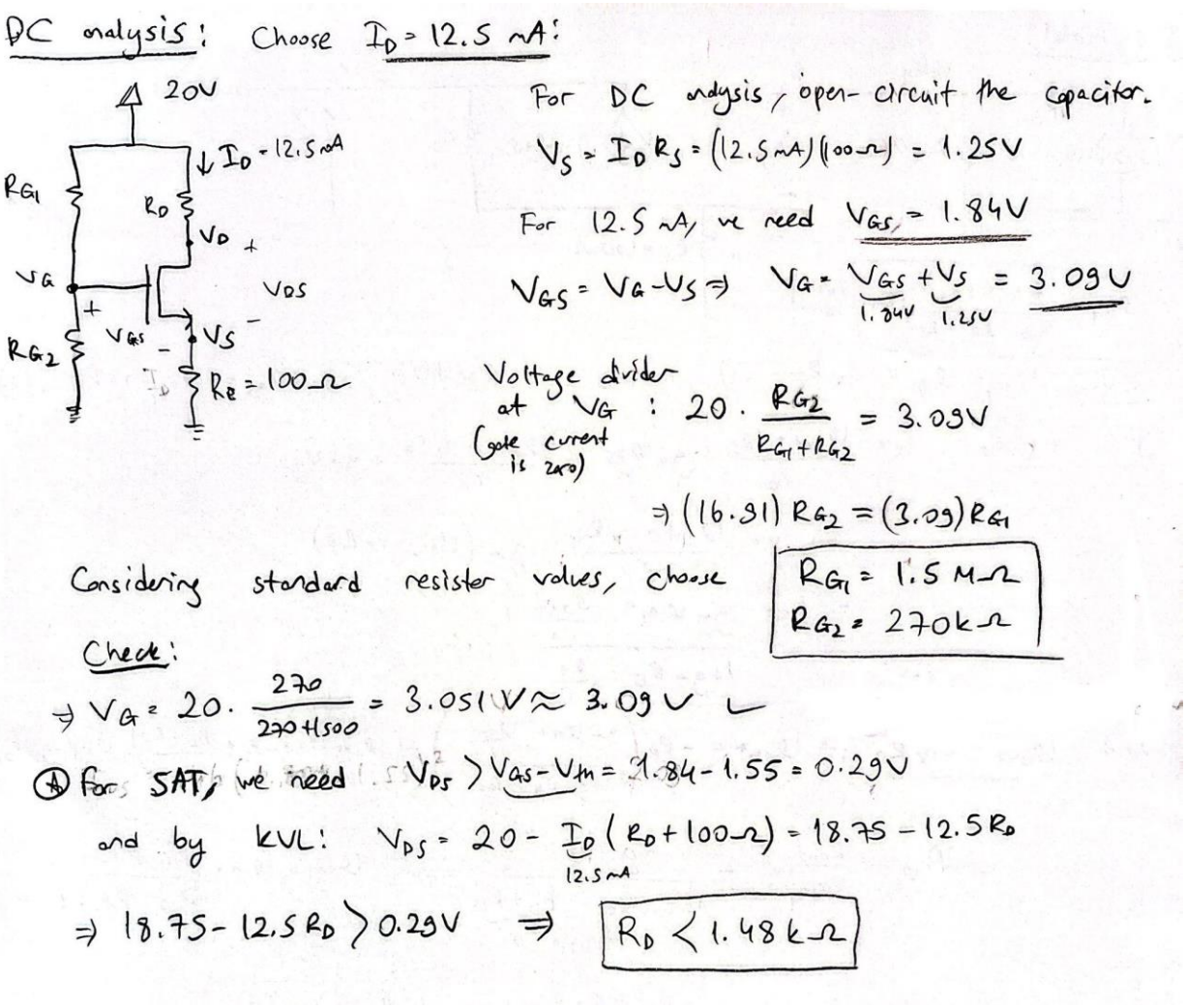

Figure 14: DC analysis for the amplifier

For R_{G1} and R_{G2}, considerably large standard resistance values (available in the lab) were chosen, to satisfy R_{in}>30 kΩ. This will be checked later. Also, for the transistor to operate in SAT region, we need R_D<1.48 kΩ. I chose R_D as 1.2kΩ, which will be explained later.

Now, the small signal model can be drawn. Before that, the small signal parameters g_m and r_O should be calculated using the results of previous parts:

$$g_m = 2\sqrt{K_N * I_D} = 2\sqrt{146 * 12.5} = 85.44\ mA/V$$

$$r_O = \frac{1}{\lambda I_D} = \frac{1}{0.047 * 12.5} = 1.7k\Omega$$

g_m is the transconductance parameter for the small signal gain, and r_O is the finite output resistance, caused by the channel modulation parameter λ. If λ is taken as 0, r_O will be infinite. Also, before the small signal model, the capacitance value can be determined. The capacitors in the circuit are called coupling capacitors. They are placed in the circuit to isolate DC and AC signals (so that small signal analysis can be performed), also to prevent the DC current coming from V_{DD} to flow towards the AC signal source. It enables DC biasing of the transistor and application of AC input to the gate of the transistor. They are open-circuited at DC, and they need to have very low impedance at AC, acting like a short circuit. To determine the capacitance value, we need $\frac{1}{j\omega C}$ to be small, where ω is the operating frequency (2π*10kHz). Hence, we need a very large capacitance value. Choosing C as 680nF, the impedances of the capacitors are calculated as approximately 23.4Ω (in terms of magnitude only), which is smaller than all the resistors in the circuit.

Drawing the small signal model and calculating the gain [2]:

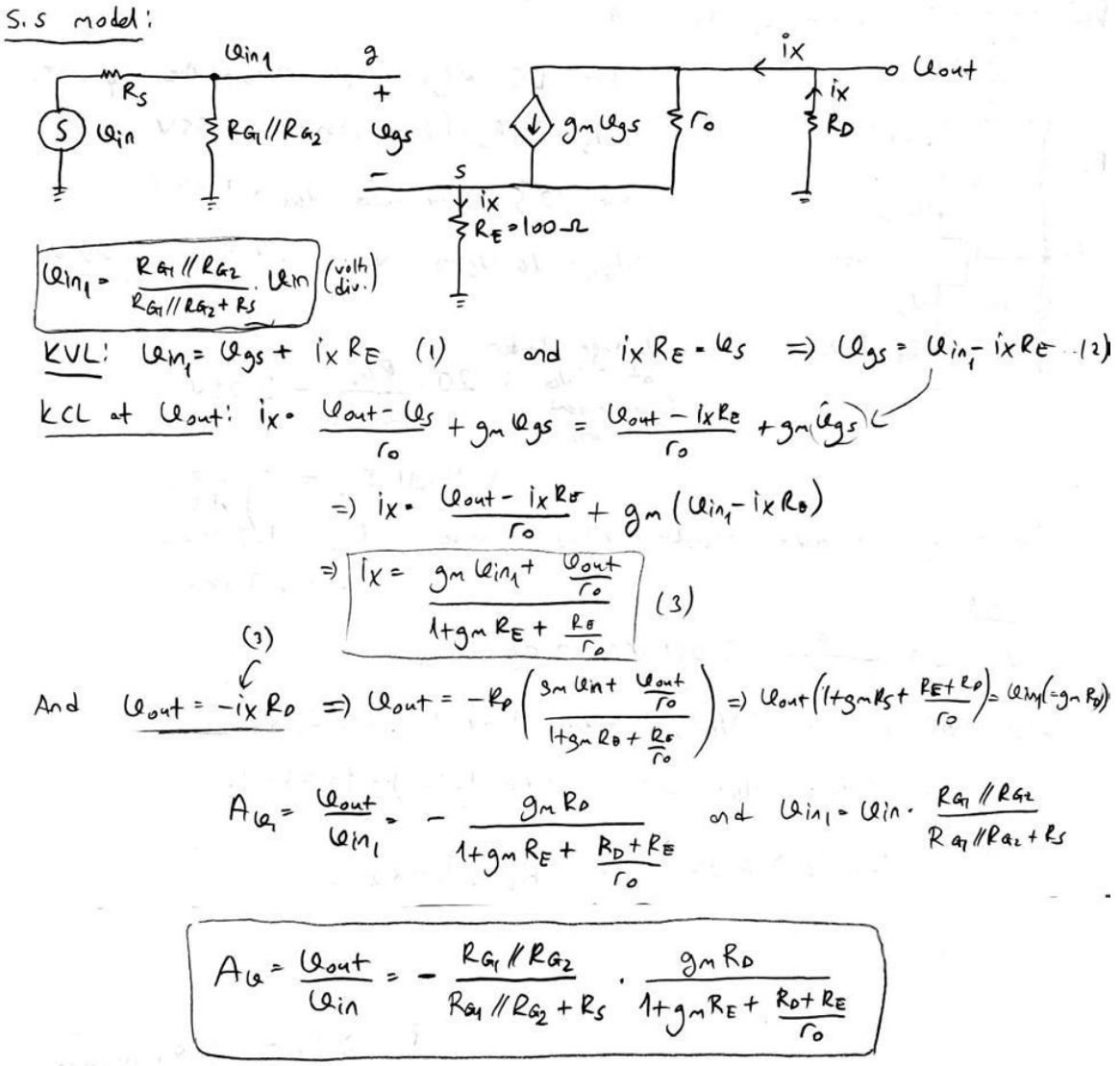

Figure 15: Small signal model and gain calculation

In small signal analysis, the DC sources are killed and the coupling capacitors are assumed short circuit. The internal 50Ω resistance of the signal generator is added as R_S into the model. Now, to find R_{in} and R_{out}:

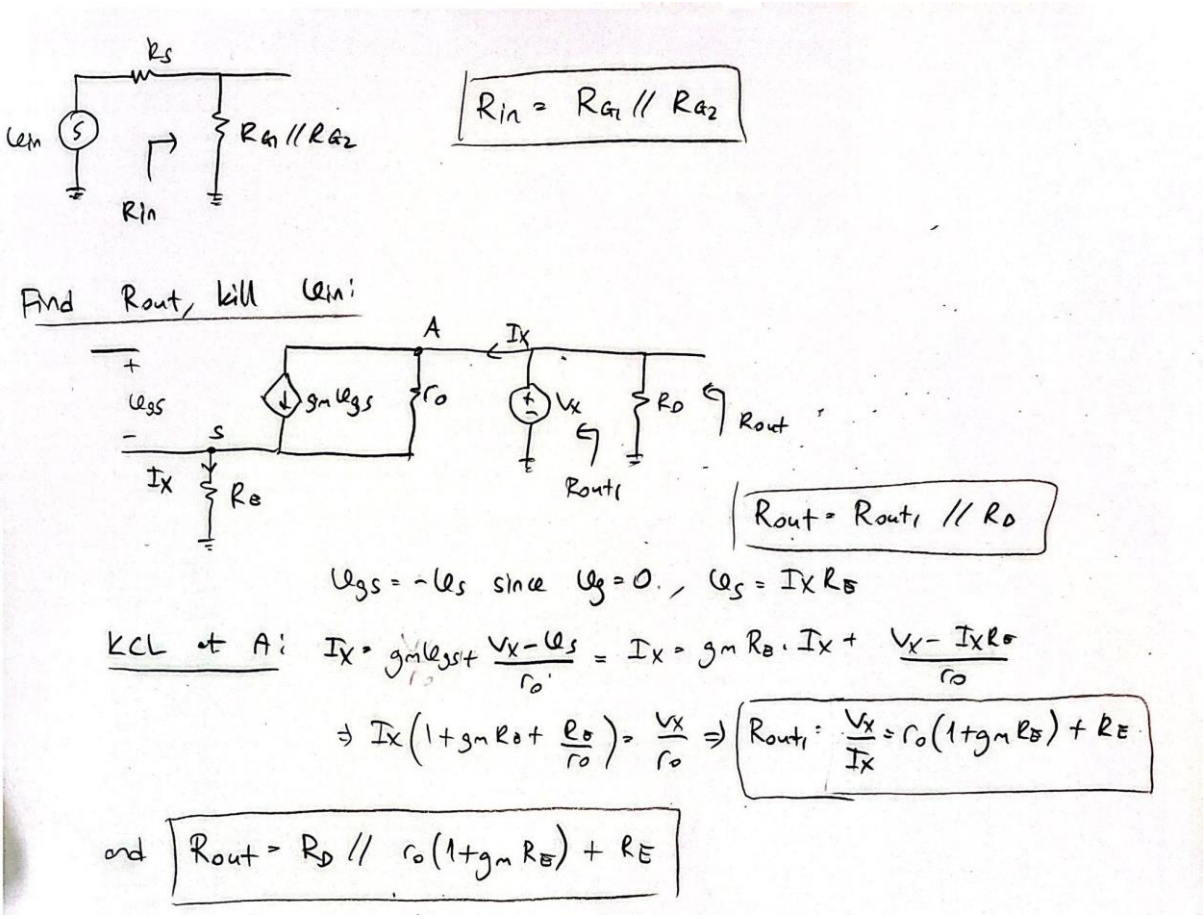

Figure 16: Calculations for R_{in} and R_{out}

To find R_{out}, the voltage source v_{in} is killed. Now, the chosen values for the components, along with the parameters for the transistor can be summarized as:

Component	**Chosen Value**	**Parameter**	**Value**
R_D	1.2 kΩ	g_m	85.44 mA/V
R_{G1}	1.5 MΩ	r_O	1.7 kΩ
R_{G2}	270 kΩ	K_N	146 mA/V^2
R_E	100 Ω	λ	0.047 V^{-1}
C	680 nF	V_{TH}	1.55 V

Table 5: Chosen values and parameters for the amplifier

When all of the values are inserted to the above calculated equation, the following results are obtained:

Parameter	**Value**
I_{DQ}	12.5 mA
$\lvert A_v \rvert = \lvert v_{out} / v_{in} \rvert$	9.944 V/V
R_{in}	228.81 kΩ
R_{out}	1.20 kΩ

Table 6: Resulting values for the amplifier

As seen from Table 6, all the conditions given in Figure 1 are satisfied. Also, the DC operation current I_D is in the desired range. One change I made was to choose R_D as 1.2 kΩ. Normally, to not exceed the saturation limit I was going to choose a smaller value. However, to increase the gain and also to satisfy R_D<1.48 kΩ (found in DC analysis, to keep the transistor in SAT), my final choice was 1.2 kΩ.

After the values are chosen, the circuit is implemented on hardware, as shown in Figure 17. The input voltage is a 100mVpp sine wave with 10kHz frequency, and the V_{DD} is given as 20 V. To obtain 100mV peak-to-peak voltage, I gave 50 mV from the signal generator, due to its working principles. The measurements are given in Figures 18-19.

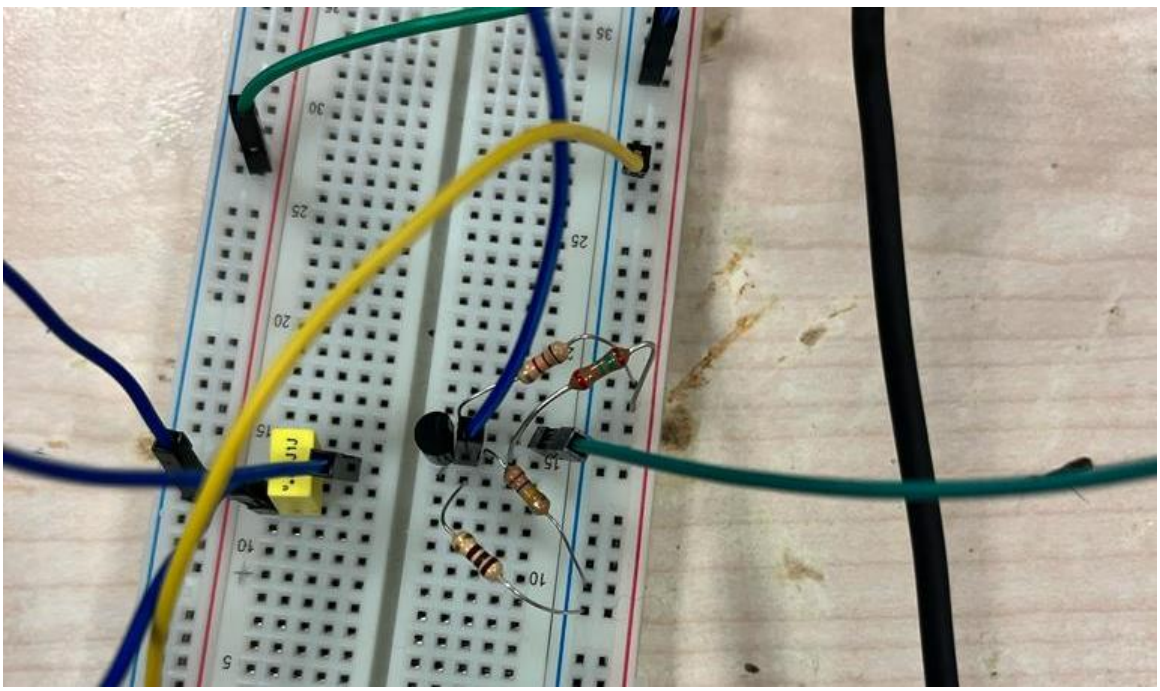

Figure 17: The circuit is implemented with chosen values

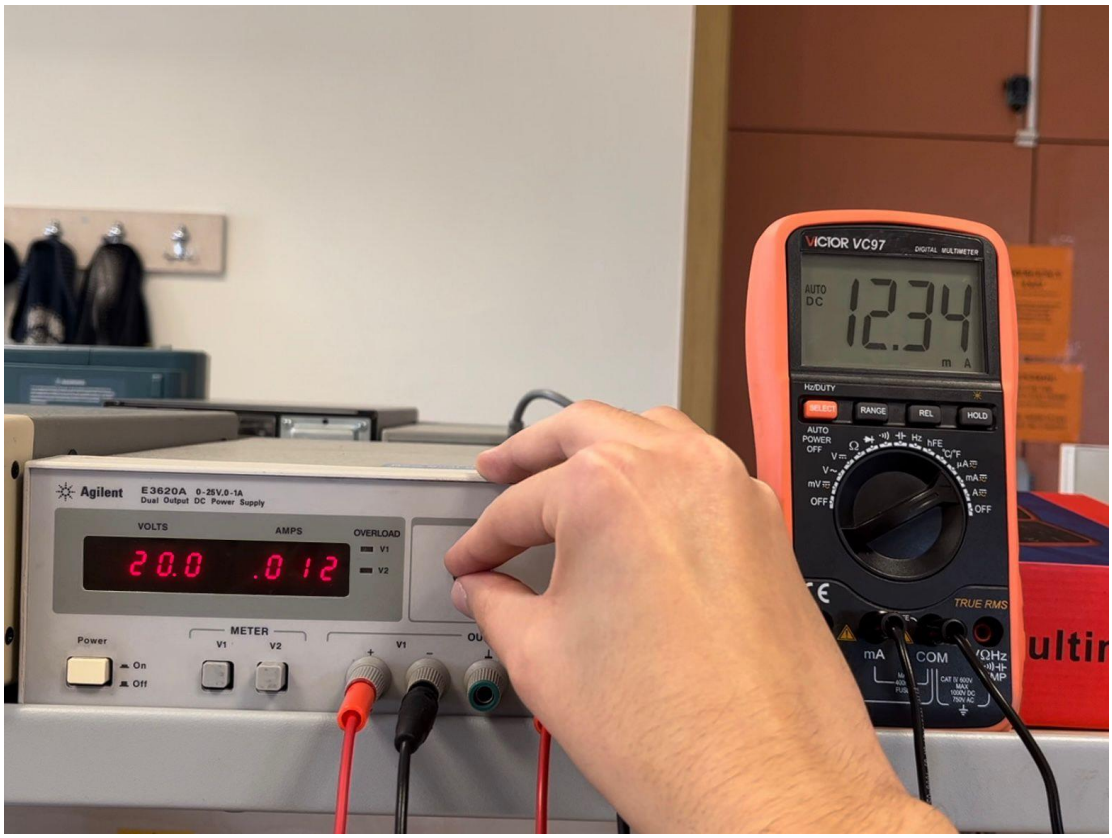

Figure 18: The drain current is 12.34 mA, corresponding to I_D

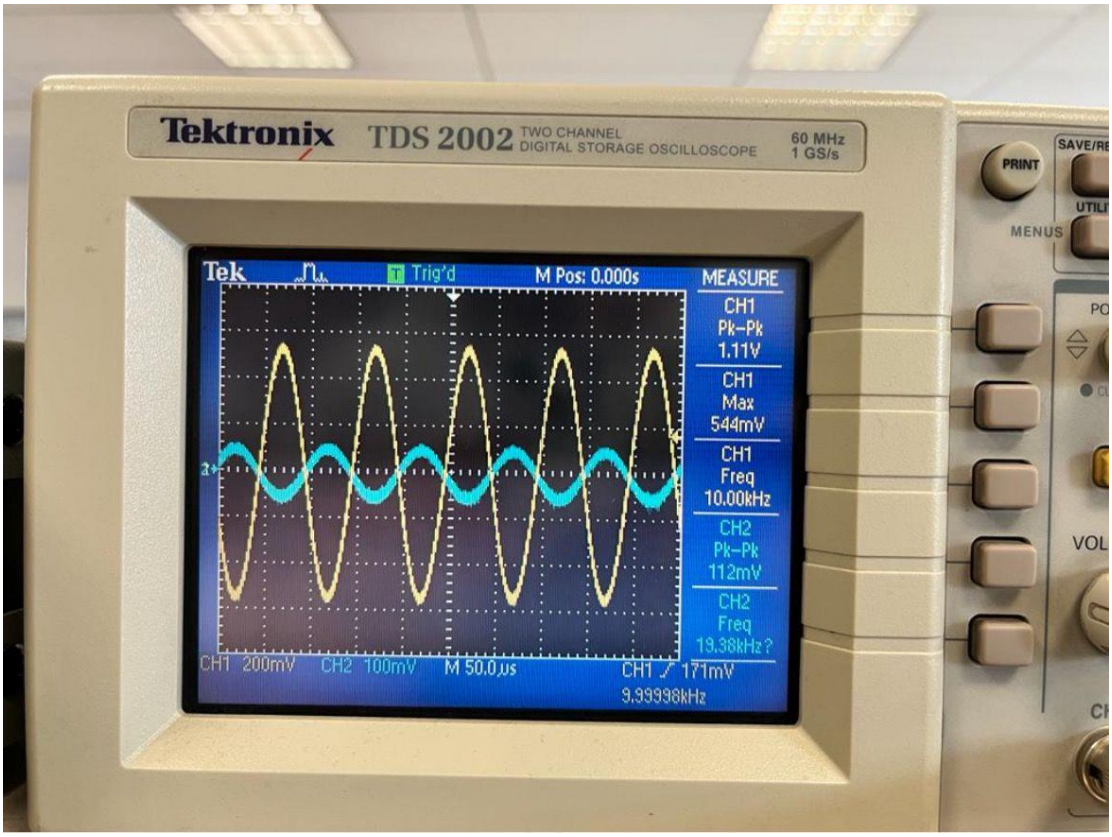

Figure 19: The input/output measurement, input is shown in blue, output is shown in yellow

Considering the peak-to-peak voltages of the input and output, the experimental gain is calculated as:

$$|A_{v,experimental}| = \frac{1.11\,V}{112\,mV} = 9.911\,V/V$$

Hence, the error between the calculated gain and the experimental gain is:

$$Error = \frac{||A_{v,theoretical}| - |A_{v,experimental}||}{|A_{v,theoretical}|} \times 100\% = \frac{9.944 - 9.911}{9.944} \times 100\% = 0.33\%$$

As expected, both the theoretical and the measured gain is bigger than 9, and the error between them is 0.33%, indicating a very small error. The drain current I_D was measured as 12.34 mA, and it is in the desired interval as well (10 mA-15 mA). The reason for the minimal difference between the chosen current (12.5 mA) and the measured current can be the external resistances caused by the wires or measurement devices, or the resistors not corresponding to their specific value. Also, the DC gate voltage does not correspond exactly to the desired value (since standard resistor values were chosen), as shown in Figure 14.

After the gain calculation, the input peak-to-peak voltage is slowly increased. It can be observed that at V_{pp} = 390 mV, the distortion occurs.

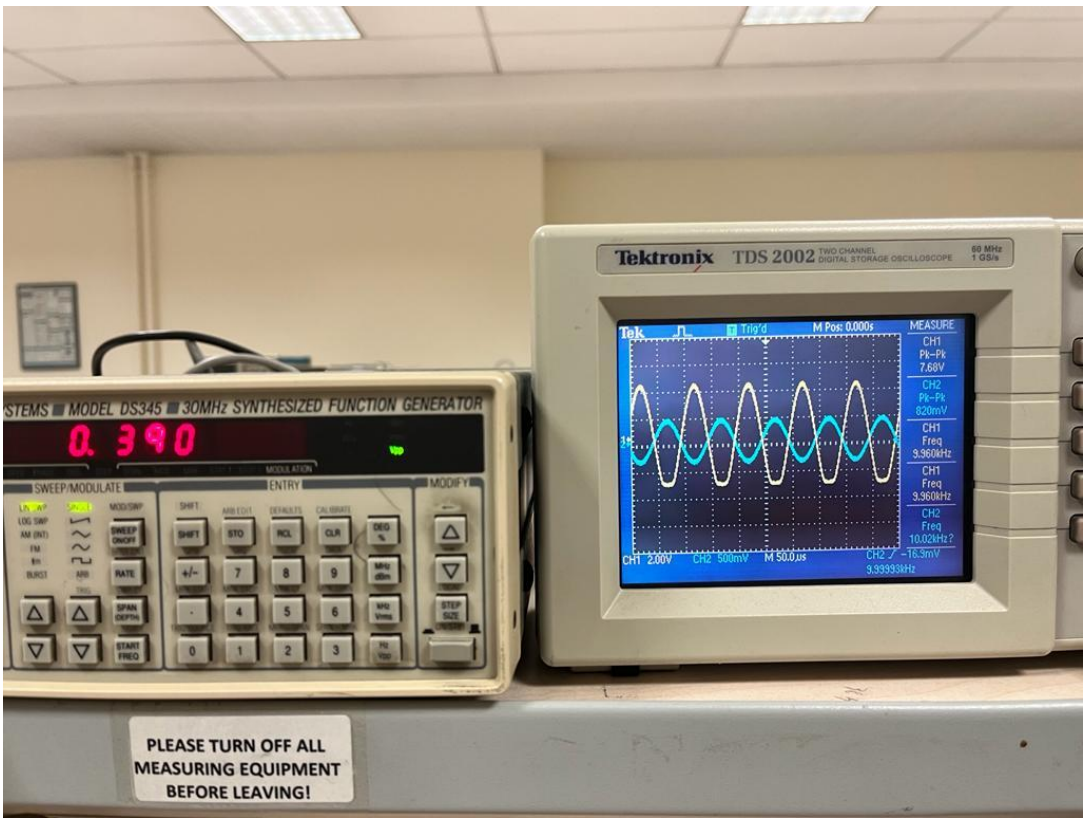

Figure 20: Distortion first occurs at 390 mV peak-to-peak input

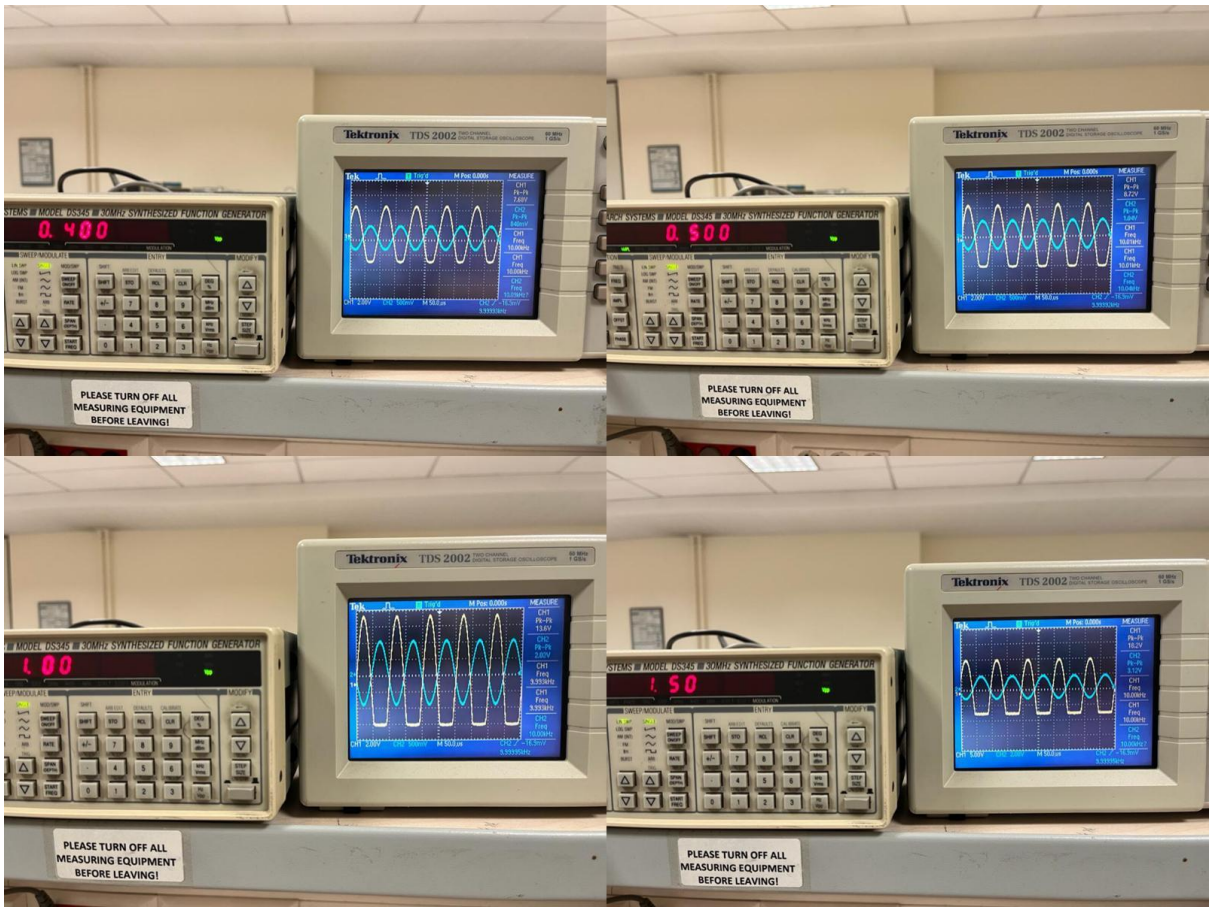

Figure 21: Output voltages for V_{in}=0.4V, 0.5V, 1V and 1.5V peak-to-peak

After 390mV peak-to-peak, for every input, distortion was observed. The reason why distortion occurs as the input AC voltage is increased is because at the gate of the transistor, there is both a DC and an AC voltage. The DC voltage is used to bias the transistor, and is supplied by the power supply (the 20V input for V_{DD}). V_{DD} biases the transistor with the gate resistors R_{G1}, R_{G2} with a voltage divider. However, along the constant DC voltage, there is also a sinusoidal AC signal present at the gate. As the sinusoidal signal increases, the gate voltage also increases. Normally, since this voltage is small (hence the name small signal), this doesn't affect the transistor. However, after a certain amplitude which is comparable with the DC voltage, the voltage at the gate becomes bigger and eventually bigger than the drain voltage, when the input sinusoidal voltage is at the positive cycle. Since the output is inverted with respect to the input, distortion is observed at the negative cycle of the output, but corresponding to the positive cycle of the input.

With drain voltage getting smaller than the gate voltage, eventually V_{DS} becomes less than V_{GS}-V_{TH}, which causes the transistor to move into the NON-SAT (triode) region, since V_{DS}>V_{GS}-V_{TH} is needed for the operation of the transistor. In the triode region, the current changes with changing V_{DS}, causing a distorted output. Therefore, the distortion voltage is determined by the DC gate and drain voltages V_G and V_D and the threshold voltage V_{TH}. In this case, the distortion voltage (voltage where the distortion begins) was found as 390 mV or 0.39 V peak-to-peak.

- **Part 4 - Adding a parallel capacitor**

When a parallel capacitor is added parallel to R_E with the same value as the previous part, it can be observed that in the small signal model R_E becomes shorted, since the capacitor is shorted in the small signal analysis. Therefore, the small signal model and the gain can be modified as:

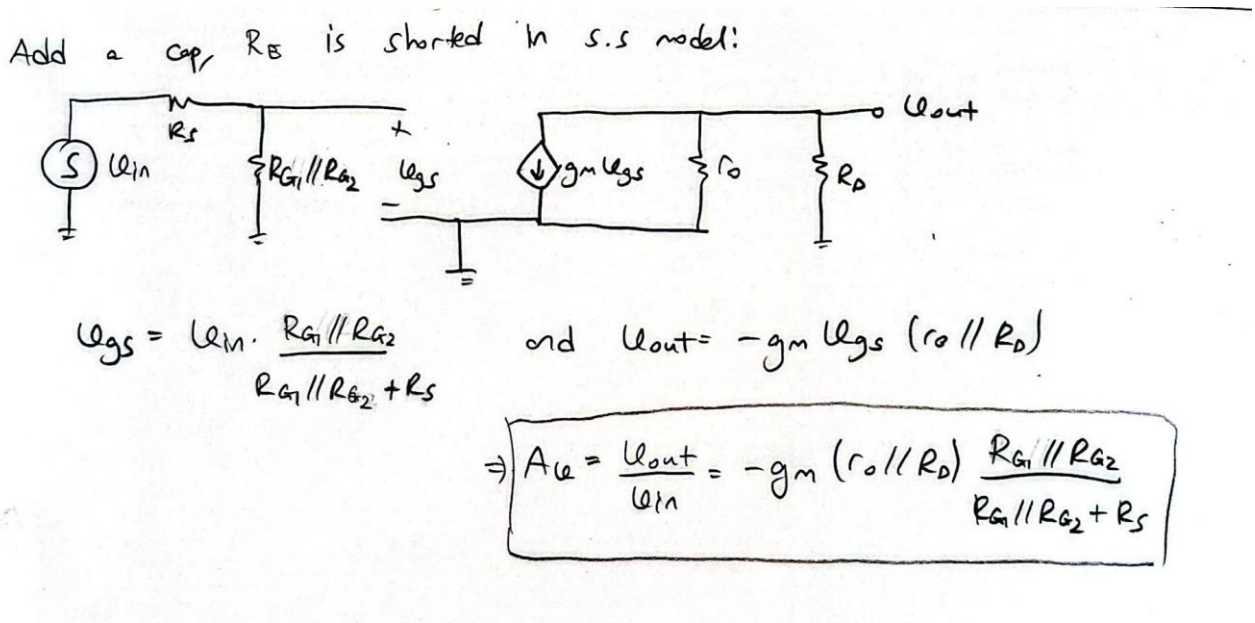

Figure 22: Small signal model and the gain for the capacitor added circuit

The gain has increased since the terms involving R_E at the denominator of the previous gain have vanished. Inserting the values chosen previously, the new gain is found as:

$$|A_{v,cap}| = 52.29\ V/V$$

which is very large compared to the calculated gain in the previous part (9.944 V/V). When the capacitor is added to the hardware circuit, the output is measured again. Figures 23-24 show the circuit and the input/output measurements.

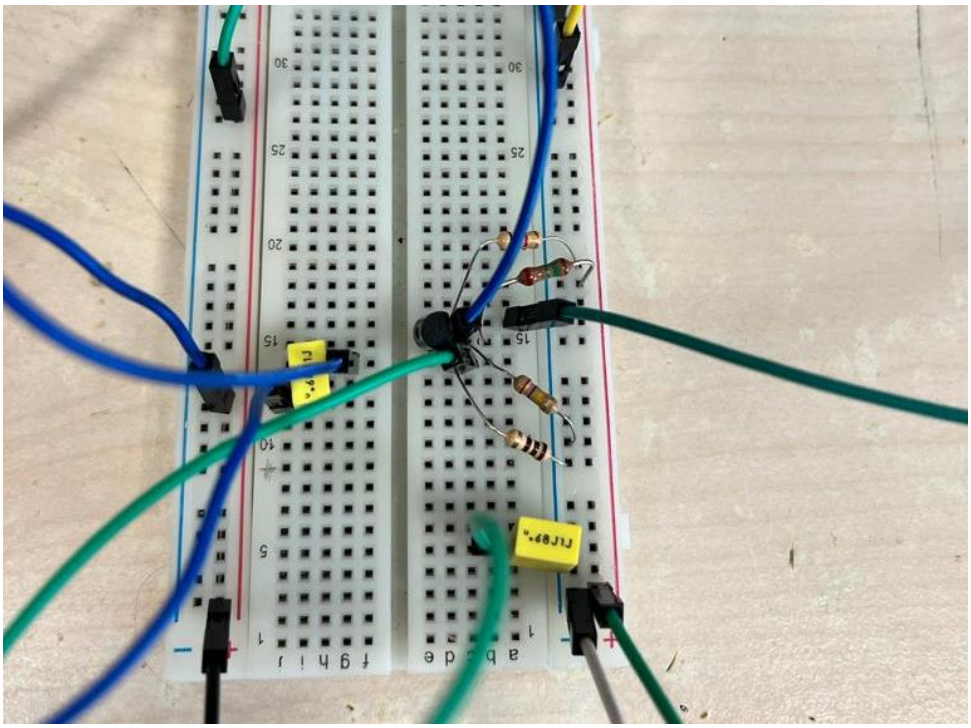

Figure 23: A capacitor is added to the circuit

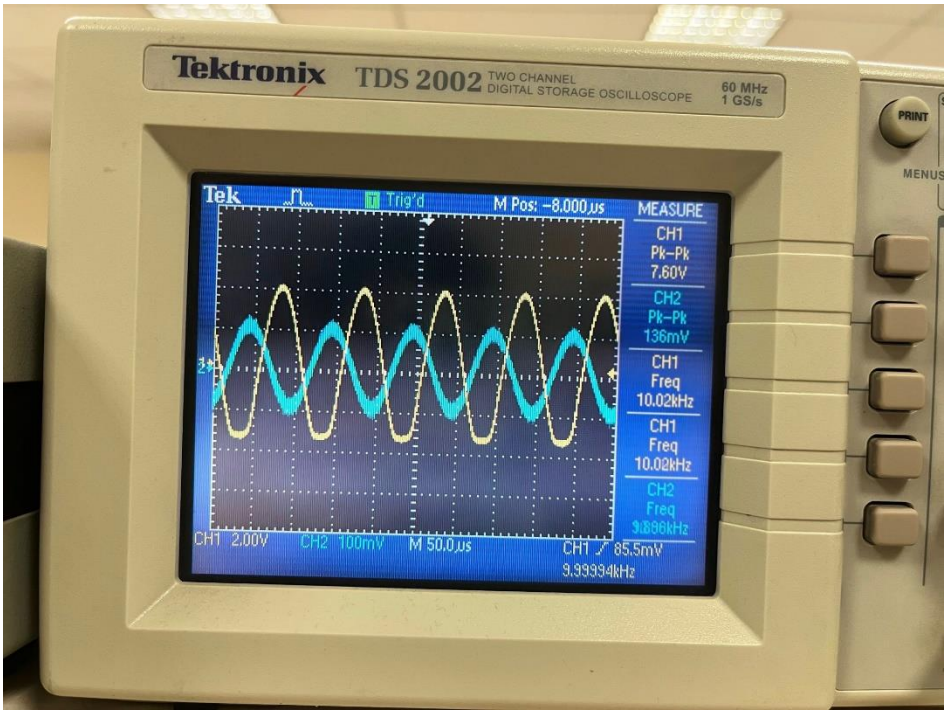

Figure 24: The input/output measurement, input is shown in blue, output is shown in yellow

The experimental gain is calculated, using again the peak-to-peak voltages of input and output:

$$|A_{cap,experimental}| = \frac{7.6\,V}{136\,mV} = 55.88\,V/V$$

Hence, the error between the calculated gain and the experimental gain is:

$$Error = \frac{||A_{v,theoretical}| - |A_{v,experimental}||}{|A_{v,theoretical}|} \times 100\% = \frac{55.88 - 52.29}{52.29} \times 100\% = 6.87\%$$

As expected, both the theoretical and experimental value of the gain increased when the capacitor was added. This is because with the AC signal, the low-impedance capacitor acts like a short circuit, therefore shorting R_E and increasing the gain. The error between the theoretical and experimental gain was 6.87%, which is again a small error but is more compared to that of the previous part. The reason for the errors may be the measurement errors, as well as the resistor/capacitor values not matching their exact supposed value.

III. Conclusion

In this lab experiment, I implemented a common source amplifier with specifications given in the lab manual. The implementation was successful, where the gain was obtained as 9.944 V/V in theory, while in the experiment it was measured and calculated as 9.911 V/V. The drain current was measured as 12.34 mA. The output impedance was found as 1.20 kΩ, and the input impedance was 228.81 kΩ. Hence, all the specifications were satisfied.

In the first part, the threshold voltage of the transistor was determined as 1.55 V. This conforms to the specified interval of the threshold voltage as specified in the 0.8V - 3V range [1]. Since the nMOS was diode-connected in this part, meaning that its drain and gate were connected together, the current-voltage relationship was expected to turn out as exponential. As expected, the I-V curve generated with the data was also exponential, hence the results were successful.

In the second part, with three different V_{GS} values, I generated three I_{DS}-V_{DS} curves. As V_{GS} was increased, the saturation voltage and the saturation current also increased. Using the data obtained and by using a curve fitting method, I also calculated the K_N and λ parameters as 146 mA/V^2 and 0.047 V^{-1} respectively, which are again in the expected intervals [2]. Using these parameters, the amplifier was ready to be designed.

After a detailed DC and AC analysis, the resistor values were chosen and the amplifier was implemented. All the conditions in the lab manual were satisfied, and the error for the gain was found as 0.33%, regarding the theoretically found gain and the experimental gain. The error can be reduced further if bigger capacitance values are chosen, since the impedance will decrease even more. Still, for both in theory and in experiment, the gain was bigger than 9 and all conditions were satisfied. The distortion voltage, where the transistor moves from SAT to

NON-SAT region, was also found as 0.39V peak-to-peak for the input. In the last part, where the capacitor was added, the gain increased up to 52.29 V/V in theory and 55.88 V/V in experiment, with 6.87% error. This was as expected since R_E was shorted by the capacitor, the gain should increase. The errors' causes may include measurement errors, internal resistances of wires/devices and the resistor/capacitor tolerances. Also, with bigger capacitance values, the errors may decrease since it corresponds to even smaller impedances, approaching more to becoming short-circuit.

In conclusion, an nMOS common source amplifier was implemented successfully with the input amplified nearly 10 times. To construct it, I used all the knowledge I achieved in the course regarding the transistor operations, including the small signal and DC analyses. Overall, the experiment was successful with all the conditions satisfied. The experiment was also beneficial for me since I was able to implement the knowledge I learned. Starting with this experiment, my knowledge can be used to implement other real-life applications involving amplifiers and MOSFETs.

References

[1] “2N7000 datasheet,” ALLDATASHEET, https://pdf1.alldatasheet.com/datasheet-pdf/view/1115779/SECELECTRONICS/2N7000.html. (accessed Nov. 11, 2023).

[2] D. Neaman, in *Microelectronics Circuit Analysis and Design*, McGraw-Hill Science Engineering, 2007, pp. 222–226