ECD- HW 1

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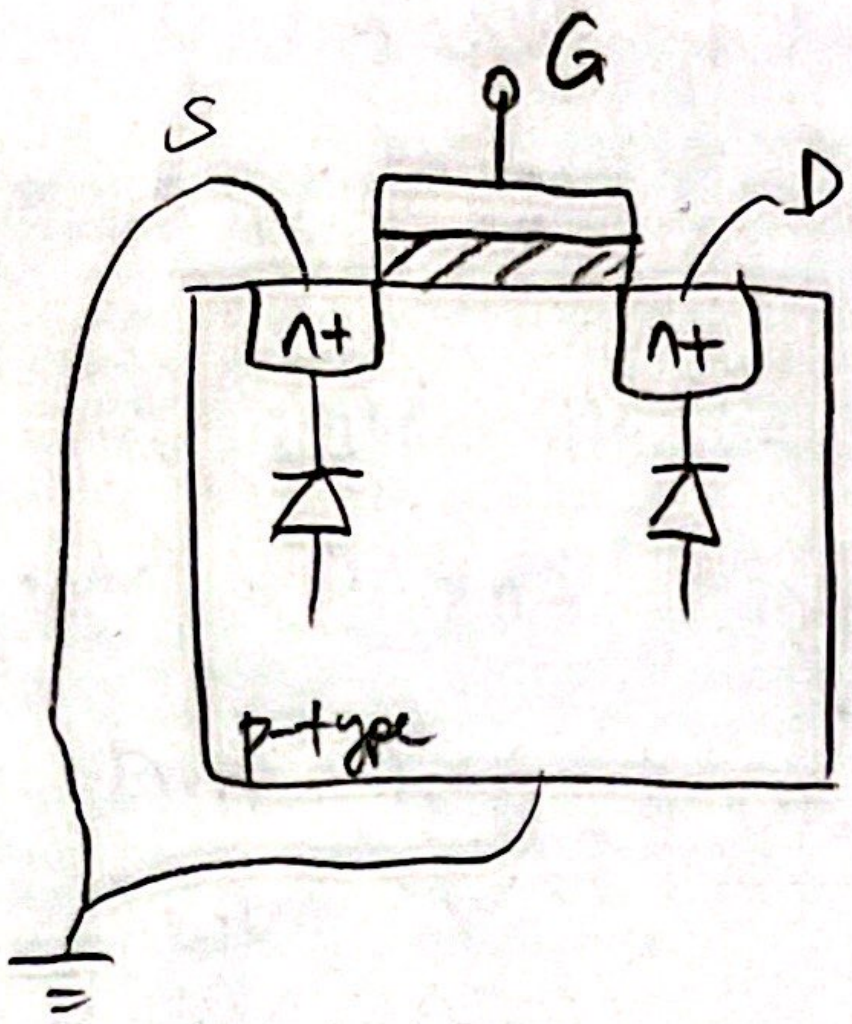
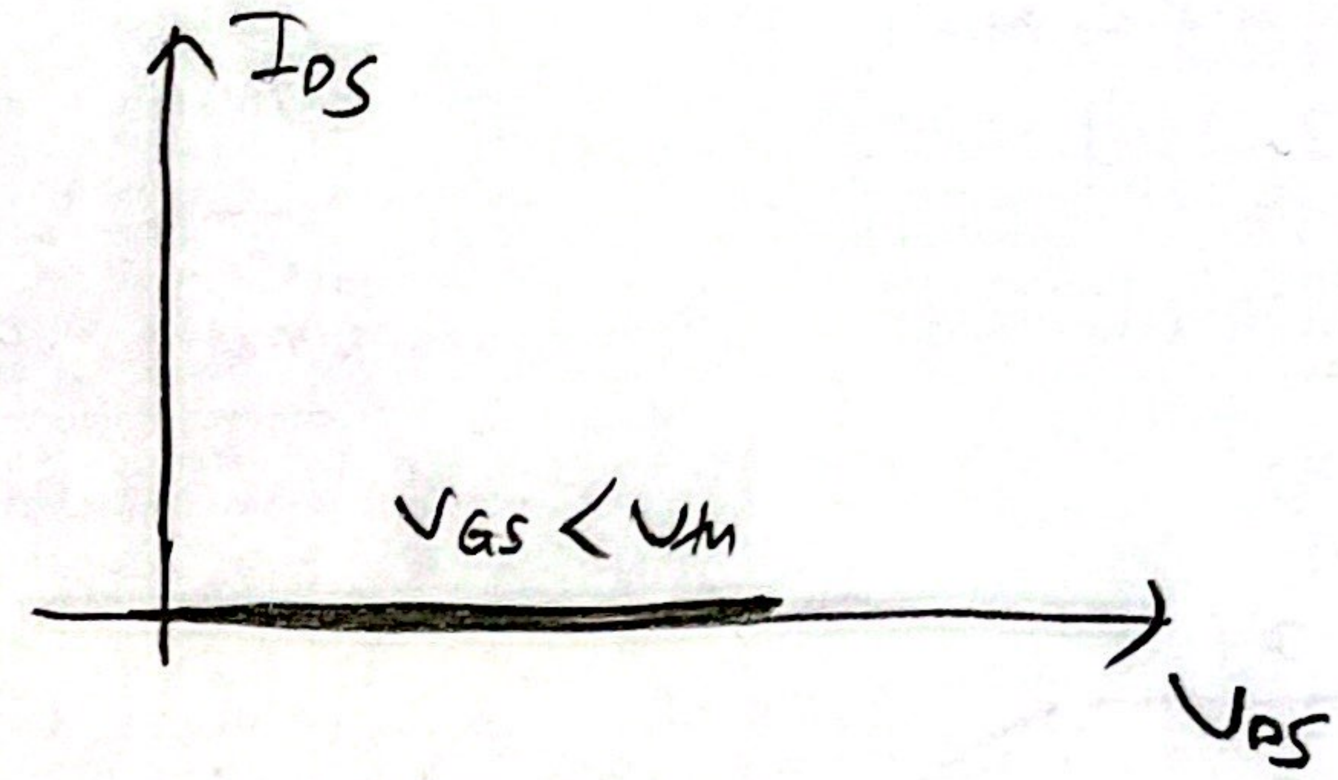
1) a) $V_{GS} < V_{th}$ →



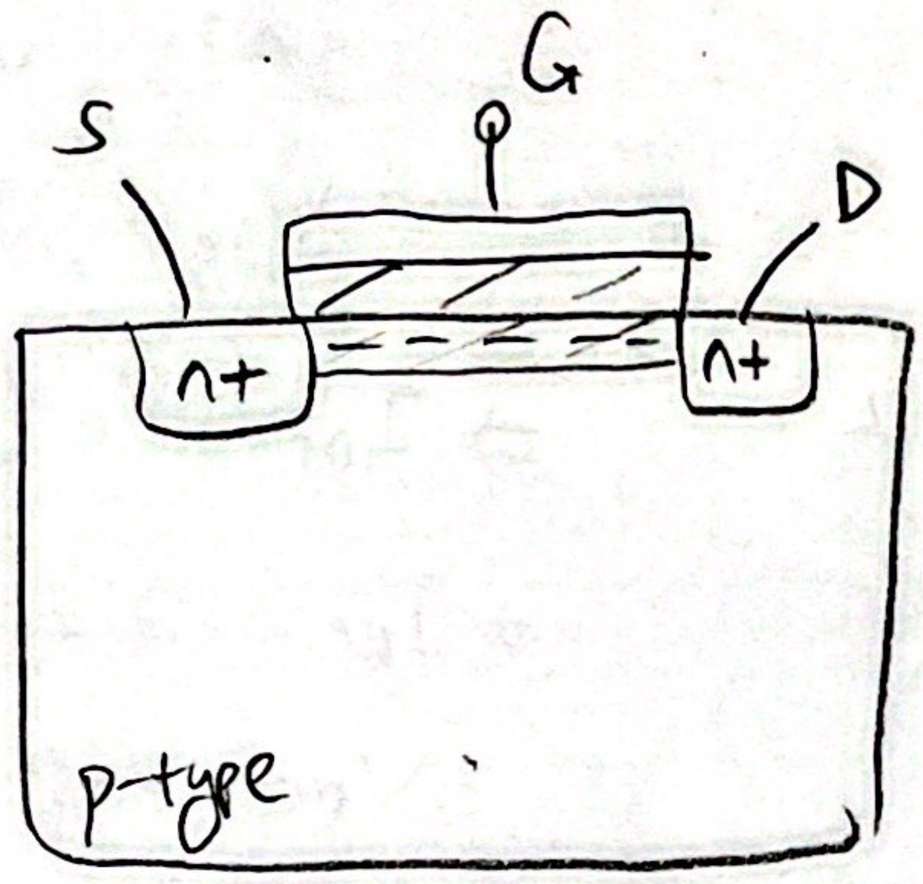
⇒ no e^- inversion layer
⇒ drain current is zero, since no inversion layer.

$I_{DS} = 0$ ⇒ OFF mode



b) $V_{GS} > V_{th}$
small V_{DS}

⇒ e^- inversion layer is created.



$$I_{DS} = K_n\left(2(V_{GS}-V_{th})V_{DS} - V_{DS}^2\right)$$

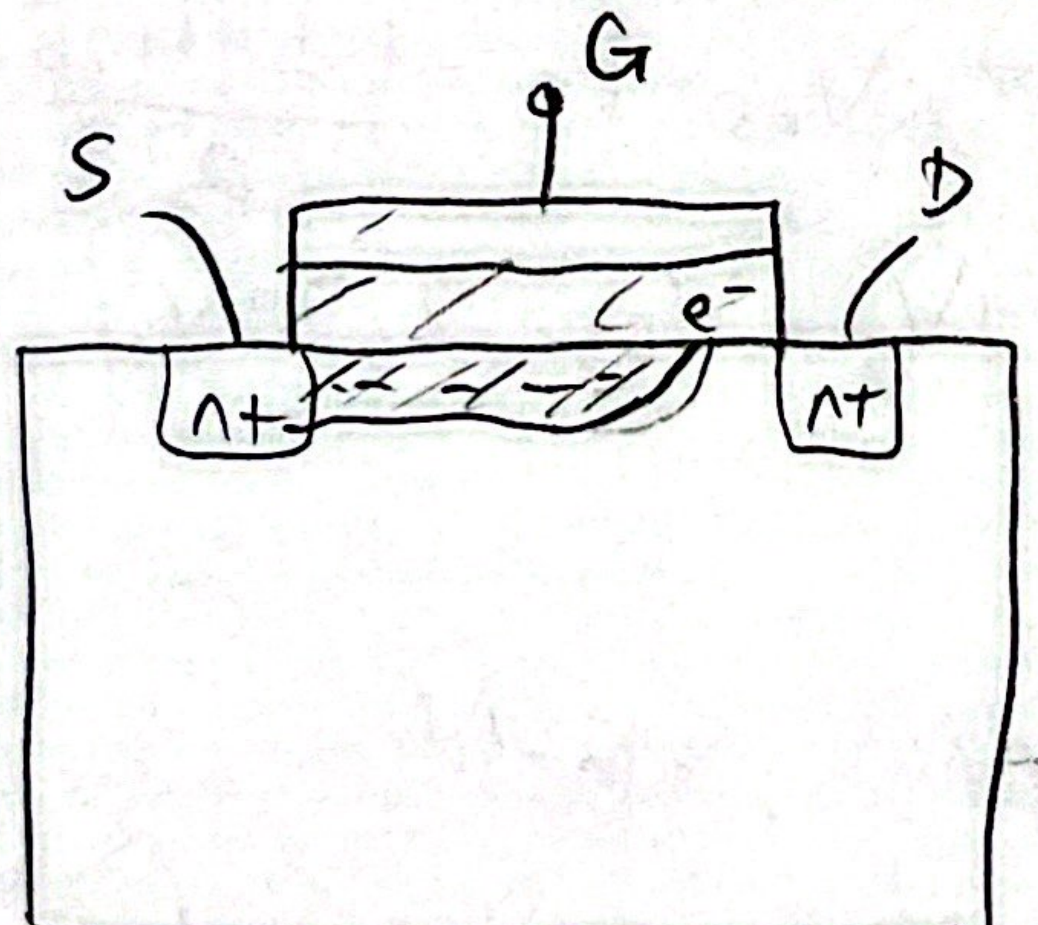
for $V_{DS} < V_{GS}-V_{th}$

⇒ TRIODE mode

c) $V_{GS} > V_{th}$
large V_{DS}

⇒ when $V_{DS} > V_{DSAT} = V_{GS}-V_{th}$

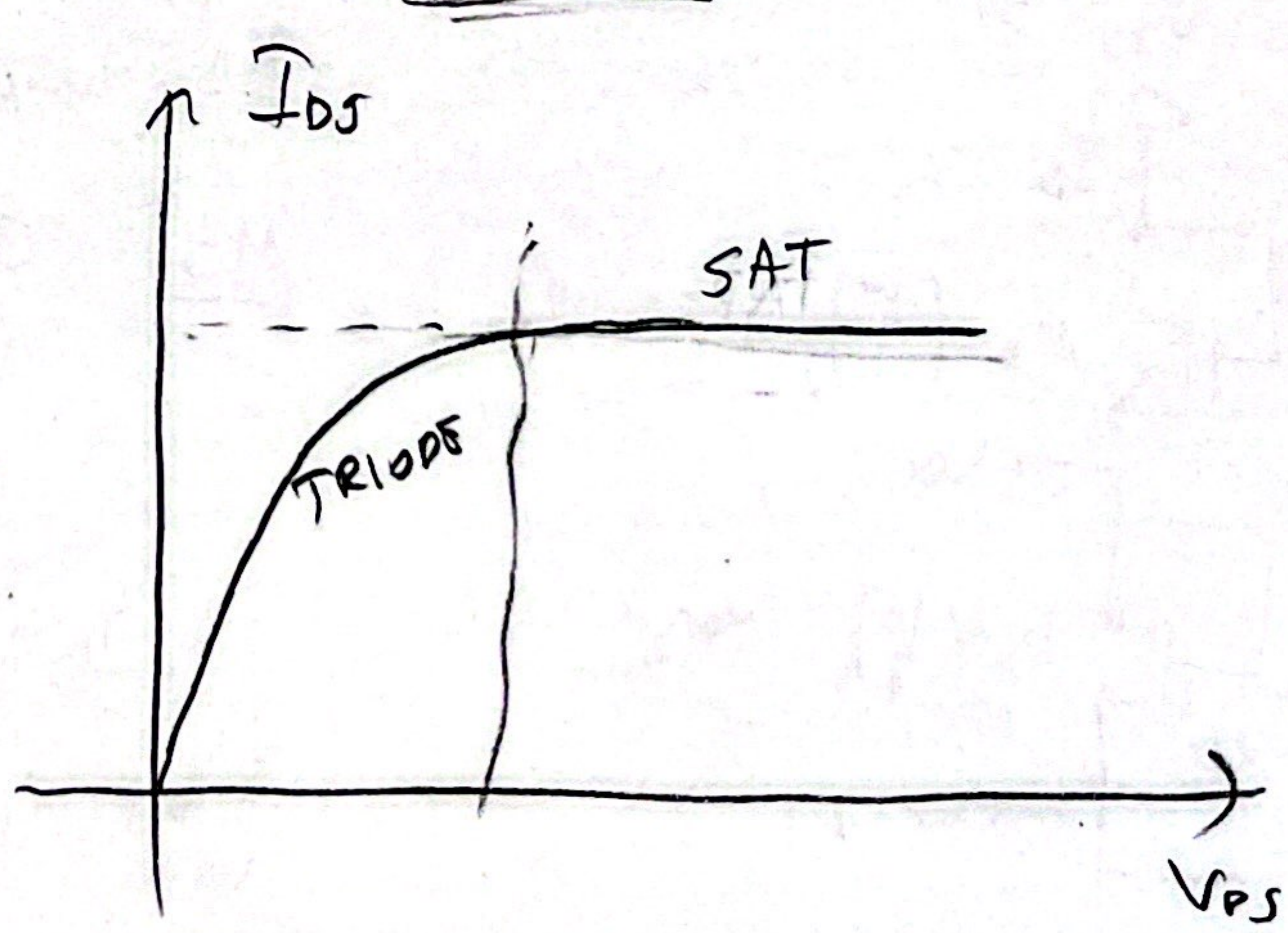
the e^- inversion layer moves to the source terminal, e^-'s are swept by $\vec{E}$ field.



$$I_{DS} = K_n\left(V_{GS}-V_{th}\right)^2$$

for $V_{DS} > V_{GS}-V_{th}$

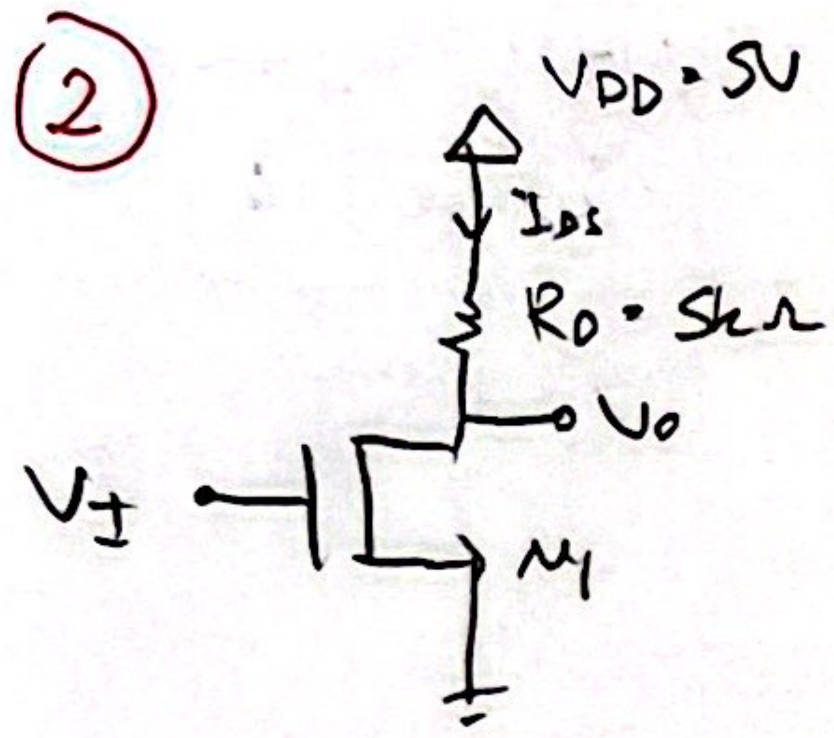
⇒ SAT mode



⇒ The gate is isolated with an oxide so there is no DC gate current.

⇒ No source-substrate or drain-substrate currents since those p-n junctions (diodes) are OFF.

(2)



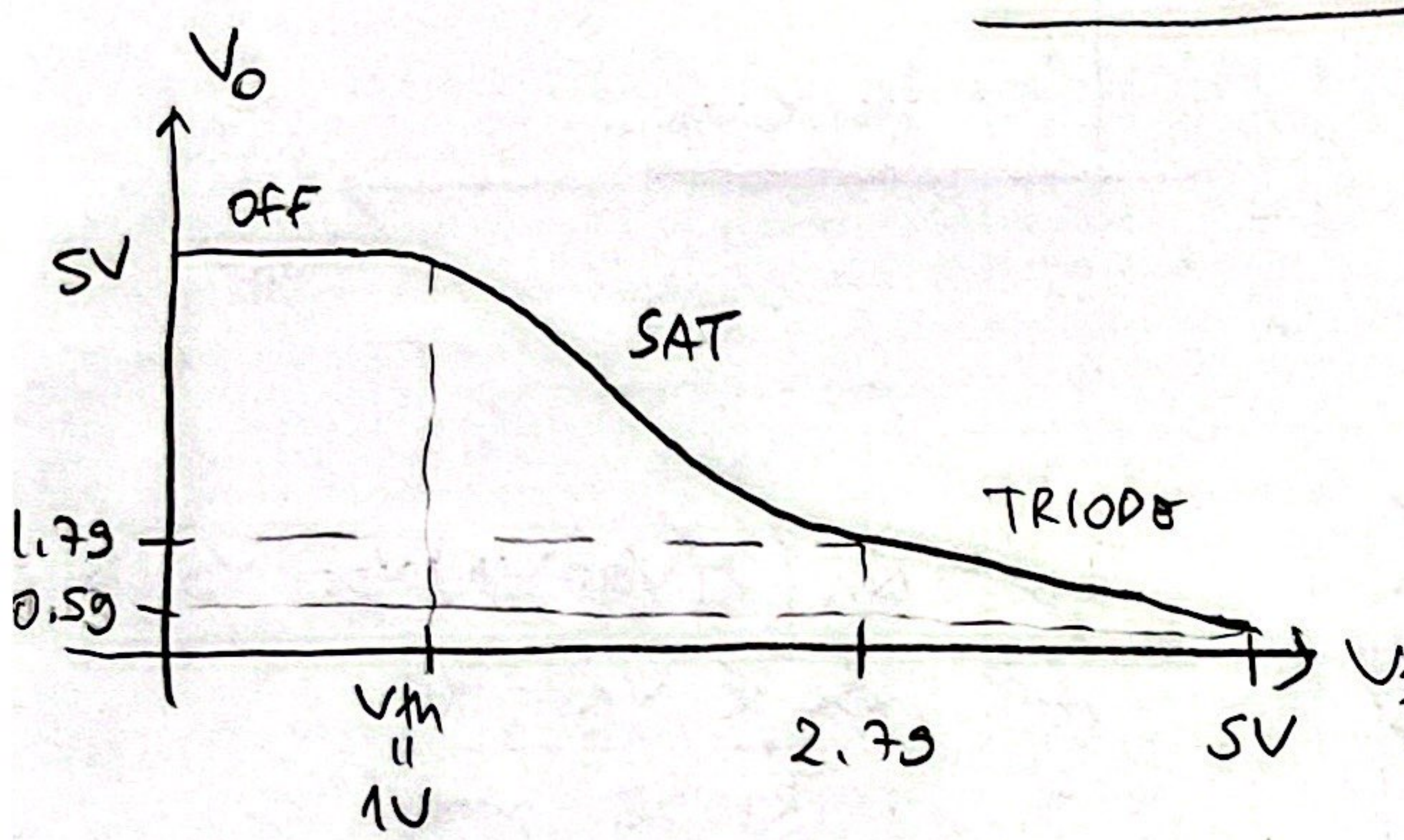
$V_{th} = 1V$, $K_n = 0.2\ mA/V^2$

From KVL: $V_{DD} = I_D R_D + V_o$

$$\Rightarrow \boxed{V_o = V_{DS} = 5 - 5 I_{DS}} \quad \ldots (1)$$

when $V_I < \underbrace{V_{th}}_{1V} \Rightarrow I_{DS} = 0$, $V_{DS} = 5V \rightarrow$ nMOS is OFF

when $V_I > V_{th} = 1V \rightarrow$ first start from SAT since the V_{DS} is large (close to 5V) and V_I is close to V_{th} ($V_I - V_{th}$ is small)



When changing from TRIODE to SAT, we need:

$$V_{DS} = V_{GS} - V_{th} = V_{GS} - 1$$

$$\Rightarrow I_{DS} = K_n\left(2(V_{GS} - V_{th})V_{DS} - V_{DS}^2\right)$$

$$\Rightarrow I_{DS} = 0.2(V_{GS} - 1)^2 \text{ and}$$

$V_{DS} = V_{GS} - 1$, insert into (1):

$$V_{GS} - 1 = 5 - 5 \cdot 0.2(V_{GS} - 1)^2$$

$$\Rightarrow \boxed{(V_{GS} - 1)^2 + (V_{GS} - 1) - 5 = 0}$$

$$\Rightarrow V_{GS} - 1 = \frac{-1 \pm \sqrt{1+20}}{2} \cong 1.79 \quad \left(\begin{array}{c}\text{take positive} \\ \text{since } V_{GS} - 1 > 0 \\ \text{for ON}\end{array}\right)$$

$$\Rightarrow \boxed{V_I = V_{GS} = 2.79V}, \quad \boxed{V_{DS} = 1.79V} = V_o$$

$$\boxed{I_{DS} = 0.64\ mA}$$

when $V_I = 5V$: In triode.

$$I_D = K_n\left(2(V_{GS} - V_{th})V_{DS} - V_{DS}^2\right)$$

$$\Rightarrow I_D = 0.2\left[2(5-1)V_o - V_o^2\right)$$

and $V_o = 5 - 5I_D$

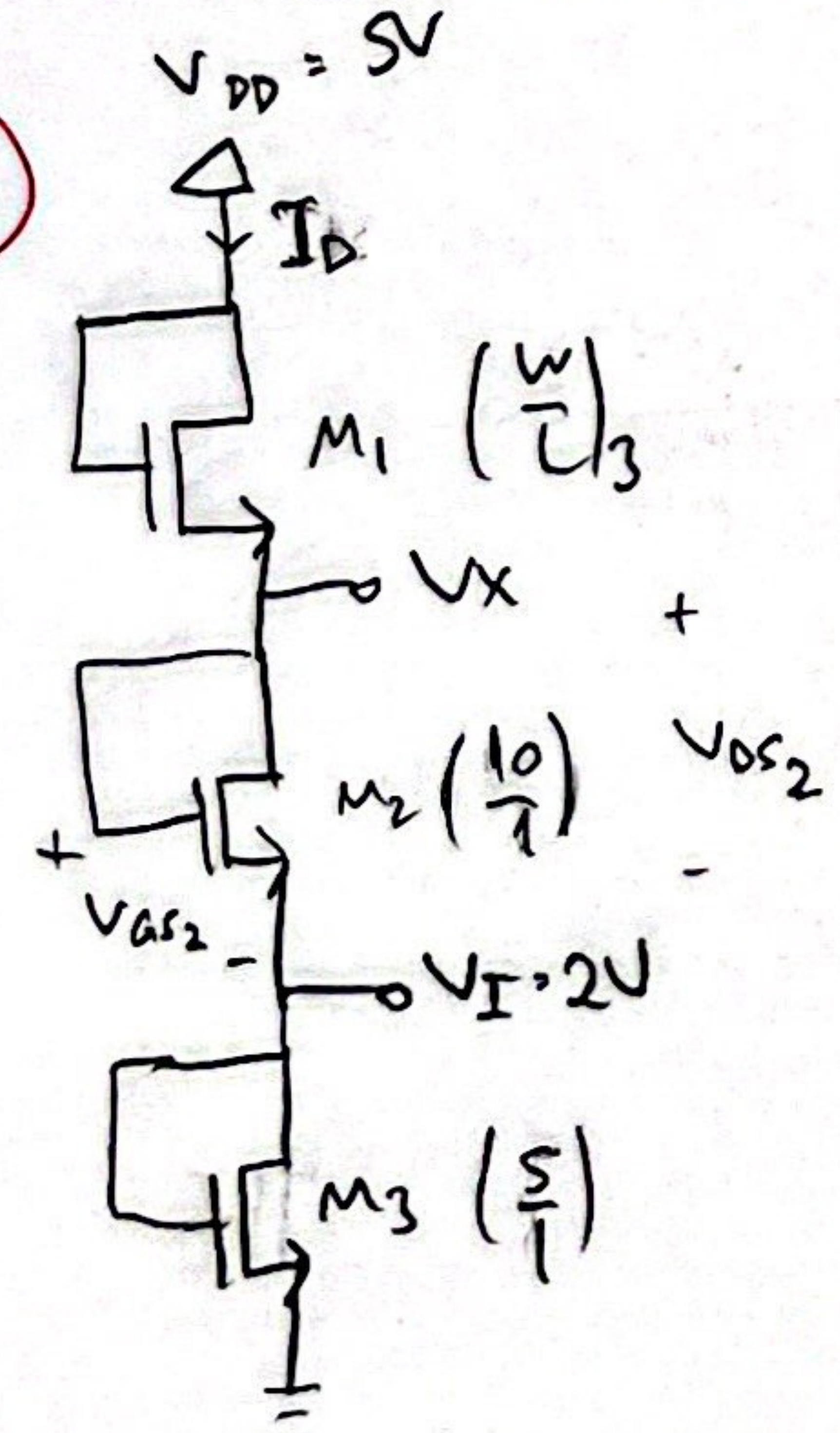
$$\Rightarrow 5 - V_o = 1(8V_o - V_o^2)$$

$$\Rightarrow V_o^2 - 9V_o + 5 = 0$$

$V_o = 8.4V$ or $\boxed{V_o = 0.59V}$

since in triode $V_{DS} < V_{GS} - V_{th}$

(3)



$\frac{K_n'}{2} = 100\mu A/V^2$, $V_{th} = 1V$

M3: ON since $V_{GS_3} = 2V > V_{th} = 1V$

in SAT since $V_{DS_3} = V_{GS_3} = 2V$ (diode connected)

and $\underbrace{V_{DS_3}}_{2V} > \underbrace{V_{GS_3} - V_{th}}_{1V}$ ✓

$$\boxed{\begin{aligned} \Rightarrow I_D &= \frac{K_n'}{2}\left(\frac{W}{L}\right) \cdot (V_{GS} - V_{th})^2 \\ &= 100 \cdot 5(2-1)^2 = 500\ \mu A \end{aligned}}$$

M2: Assume SAT:

$$I_{DS_2} = I_D = \underbrace{\frac{K_n'}{2}}_{100}\underbrace{\left(\frac{W}{L}\right)_2}_{10} (V_{GS_2} - V_{th})^2 = 500\mu A$$

$$\Rightarrow (V_{GS_2} - 1)^2 = 0.5$$

$$\Rightarrow V_{GS_2} = 1.71V$$

and $V_X = V_{GS_2} + 2V = \underline{\underline{3.71V}}$ (from KVL)

$V_{DS_2} = \underbrace{V_X}_{3.71V} - \underbrace{V_I}_{2V} = \underline{\underline{1.71V = V_{GS_2}}}$ Check: $\overbrace{V_{DS_2}}^{1.71V} > \overbrace{\underbrace{V_{GS_2}}_{1.71} - \underbrace{V_{tn}}_{1}}^{0.71V}$ ✓ in SAT mode.

and $\underbrace{V_{GS2}}_{1.71V} > \underbrace{V_{tn}}_{1V}$ ✓ (diode connected)

M1: Assume SAT:

$I_{DS_1} = I_D = \frac{k_n'}{2}\left(\frac{W}{L}\right)_3 (V_{GS_1} - V_{tn})^2 = 500\mu A$ and $V_{GS_1} = V_{DD} - V_X$
$= \underline{1.29V}$ (from KVL)

$= 100\left(\frac{W}{L}\right)_3 (1.29-1)^2 = 500\mu A \Rightarrow \boxed{\left(\frac{W}{L}\right)_3 = 59.45}$

Check: $V_{DS_1} = V_{DD} - V_X = 1.29V = V_{GS_1}$ $\underbrace{V_{GS_1}}_{1.29V} > \underbrace{V_{tn}}_{1V} \Rightarrow$ ON

$\underbrace{V_{GS_1}}_{1.29V} > \underbrace{V_{DS_1}}_{1.29V} - \underbrace{V_{tn}}_{1V}$ ✓ in SAT mode

$\Rightarrow \boxed{V_X = 3.71V}$, $\boxed{I_D = 500\mu A}$, $\boxed{\left(\frac{W}{L}\right)_3 = 59.45}$

All transistors are in SAT mode (diode connected)

(4) $K_p = 0.25\ mA/V^2$, $V_{tp} = -1V \Rightarrow |V_{tp}| = 1V$

$V_G = 10 \cdot \frac{30k}{30k + 70k} = \underline{\underline{3V}}$ (by voltage div. and $I_G = 0$)

By KVL: $10 = I_D(R_S + R_D) + V_{SD} = I_D(R_S + 3) + V_{SD} \Rightarrow V_{SD} = 10 - I_D(R_S + 3)$

$V_S = 10 - I_D R_S$, $V_D = 3 I_D$, $V_{SG} = 7 - I_D R_S$

a) $R_S = 5k\Omega$, $V_S = 10 - 5 I_D$

Assume SAT: $I_D = 0.25(V_{SG} - |V_{tp}|)^2 = 0.25(6 - 5I_D)^2$

$\Rightarrow -6.25 I_D^2 + 16 I_D - 9 = 0$

$\Rightarrow \boxed{I_D = 0.83\,mA}$ or $I_D = 1.73\ mA$

since we need

$V_{SG} = 7 - I_D \cdot 5 > 1$

Check: $V_{SD} \overset{?}{>} V_{SG} - |V_{tp}| \Rightarrow V_{SD} = 10 - (0.83) \cdot 8 = 3.36V$
$V_{SG} = 7 - (0.83) \cdot 5 = 2.85V$

$\Rightarrow \underbrace{V_{SD}}_{3.36V} > \underbrace{V_{SG} - |V_{tp}|}_{1.85V} \Rightarrow$ in SAT mode ✓

$\Rightarrow \boxed{(V_{SD}, I_D) = (3.36V, 0.83mA)}$

b) $R_S = 1k\Omega$, $V_{SD} = 10 - 4I_D$
$V_{SG} = 7 - I_D$

Assume SAT:
$I_D = 0.25(7 - I_D - 1)^2 = 0.25(6 - I_D)^2$
$\boxed{I_D = 2.71\ mA}$ or $I_D = 13.3\ mA$
since $V_{SG} > |V_{tp}|$

Check: $\cancel{V_{SD} = -0.84V}$
$\cancel{V_{SG} = 4.29\ V}$ $\Rightarrow$ in TRIODE mode.

Triode $\Rightarrow$ $I_D = 0.25\left(2(V_{SG} - |V_{tp}|)V_{SD} - V_{SD}^2\right)$
$I_D = 0.25\left(2(6 - I_D)(10 - 4I_D) - (10 - 4I_D)^2\right)$
$\Rightarrow 2I_D^2 - 2I_D - 5 = 0 \Rightarrow \cancel{I_D = -1.15\ mA}$ or $\boxed{I_D = 2.16\ mA}$

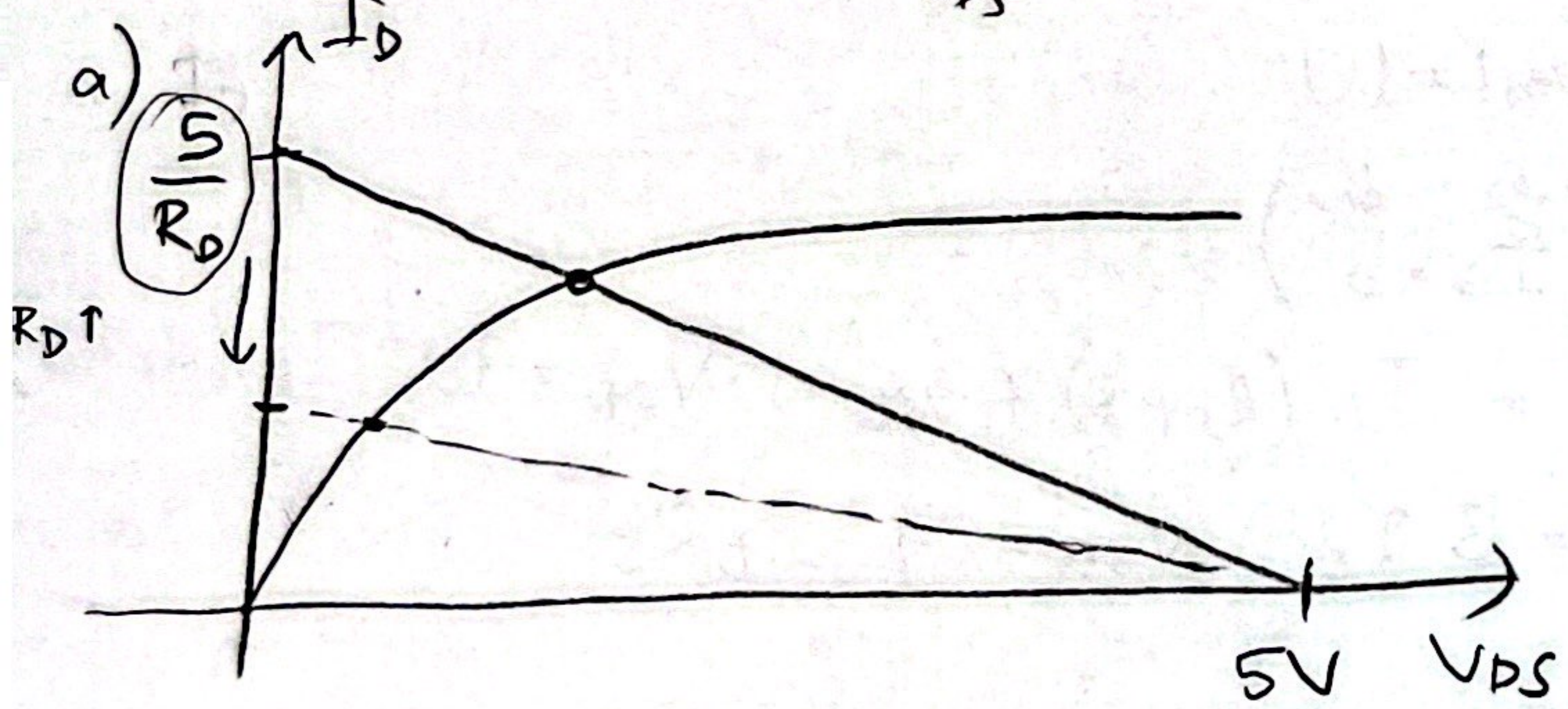
and $V_{SD} = 10 - 4I_D = 1.36\ V$

Check: $\underbrace{V_{SD}}_{1.36} < \underbrace{V_{SG} - 1}_{3.84}$ ✓ $\Rightarrow$ in TRIODE

$\Rightarrow \boxed{(V_{SD}, I_D) = (1.36\ V, 2.16\ mA)}$

5 KVL: $5 = I_D R_D + \underbrace{V_o}_{V_{DS}} \Rightarrow V_{DS} = 5 - I_D R_D$

a)



Use load line approach:
For SAT, we need
$\underbrace{V_{DS}}_{5 - I_D R_D} > \underbrace{V_{GS}}_{5V} - \underbrace{V_{th}}_{1.5V}$
$\Rightarrow 5 - I_D R_D > 3.5$
$\Rightarrow \boxed{R_D I_D < 1.5}$

As the value of R_D is increased the state of M1 is approaching NON-SAT (TRIODE). It can be seen from the plot ($\frac{5}{R_D}$ decreases and the line intersects in the NON-SAT mode).

b) Just when $\boxed{V_{DS} < V_{GS} - V_{th}}$, M1 will go to NON-SAT mode $\Rightarrow$ $V_{DS} = 5 - I_D R_D$ and $I_D = 0.2(5 - 1.5)^2 = 2.45\ mA$ (in SAT)

hence we need:
$V_{DS} > V_{GS} - V_{th} \Rightarrow 5 - 2.45R_D > 3.5$
$2.45 R_D < 1.5$

$\boxed{R_D < 0.612\ k\Omega = 612\ \Omega}$

(6) KVL: $V_{SD_2} + V_{DS_1} = 5V$, $V_{SG_2} = 5 - V_b$,

To have M2 in TRIODE: $V_{SD_2} < \underbrace{V_{SG_2}}_{5-V_b} - \overbrace{|V_{tp}|}^{1V} = 4 - V_b$ (1)

a) $V_I = 2V$, to have M2 in TRIODE: $\boxed{V_{SD_2} < 4 - V_b}$ and to have ON: $V_{SG} > |V_{tp}|$, $5 - V_b > 1$ $\Rightarrow \boxed{V_b < 4V}$ (*)

and $I_D = K_p\left(2 \cdot V_{SD_2}(4 - V_b) - V_{SD_2}^2\right)$ (+)

to have M1 in SAT: $\underbrace{V_{DS_1}}_{5-V_{SD_2}} > \underbrace{V_{GS_1}}_{V_I=2V} - \underbrace{V_{tn}}_{1V} \Rightarrow 5 - V_{SD_2} > 1$ $\boxed{V_{SD_2} < 4V}$ (2)

and $I_D = K_n(\underbrace{V_{GS_2}}_{2V} - \underbrace{V_{tn}}_{1V})^2 = \cancel{K_n} = \cancel{K_p}\left(2V_{SD_2}(4 - V_b) - V_{SD_2}^2\right)$ (+)

$\Rightarrow V_{SD_2}^2 - (8 - 2V_b)V_{SD_2} + 1 = 0$

To have real solutions: $(8 - 2V_b)^2 - 4 \geq 0 \Rightarrow (4 - V_b)^2 - 1 \geq 0$

$4 - V_b \geq 1$ or $4 - V_b \leq -1$

$\boxed{V_b \leq 3}$ $V_b \geq 5$

by (+), but check

$V_{SD_2} = \dfrac{8 - 2V_b \pm \sqrt{4(4-V_b)^2 - 4}}{2} = 4 - V_b \pm \sqrt{(4-V_b)^2 - 1} = 4 - V_b - \sqrt{(4-V_b)^2 - 1}$ to satisfy (1)

$\Rightarrow$ Insert into 2: $\cancel{4} - V_b - \sqrt{(4-V_b)^2 - 1} < \cancel{4} \Rightarrow \underbrace{V_b - \sqrt{(4-V_b)^2 - 1} > 0}_{\text{holds true for all } V_b \leq 3}$

$\boxed{0 < V_b < 3V}$ $\Longleftarrow$

(+) Check limit:

At $V_b = 3V$:

$\Rightarrow V_{SD}^2 - 2V_{SD} + 1 = 0 \Rightarrow V_{SD} = 1V$

Ineq. (1) isn't satisfied! : $\underbrace{V_{SD_2}}_{1V} \not< \underbrace{4 - V_b}_{1V}$

b) $V_I = 3\,V$, to have M2 in TRIODE: $\boxed{V_{SD_2} < 4 - V_b}$ ①

and $I_D = K_p\left(2V_{SD_2}(4-V_b) - V_{SD}^2\right)$

to have M1 in SAT: $V_{DS_2} > \underbrace{V_{GS_2}}_{3V} - 1 \Rightarrow 5 - V_{SD_2} > 2$

$\Rightarrow \boxed{V_{SD_2} < 3\,V}$ ②

to have the pMOS ON: $V_{SG} > |V_{tp}| \Rightarrow 5 - V_b > 1$

$\boxed{V_b < 4V}$ ⊕

and $I_D = K_n(\underbrace{V_{GS_2}}_{3} - \underbrace{V_{tn}}_{1})^2 \Rightarrow 4\cancel{K_n} = \cancel{K_p}\left(2V_{SD_2}(4-V_b) - V_{SD_2}^2\right)$

$\Rightarrow V_{SD_2}^2 - (8 - 2V_b)V_{SD_2} + 4 = 0$

To have real solutions: $(8 - 2V_b)^2 - 16 \geq 0 \Rightarrow (4 - V_b)^2 - 4 \geq 0$

$4 - V_b \geq 2$ or $4 - V_b \leq -2$

$\boxed{V_b \leq 2}$ or $V_b \geq 6$

by ⊕, but check

$V_{SD_2} = \dfrac{8 - 2V_b \pm \sqrt{4(4-V_b)^2 - 16}}{2} = 4 - V_b - \sqrt{(4-V_b)^2 - 4}$ to satisfy ①

$\Rightarrow$ Insert into 2: $\cancel{4} - V_b - \sqrt{(4-V_b)^2 - 4} < \cancel{4} \Rightarrow \underbrace{V_b - \sqrt{(4-V_b)^2 - 4} > 0}_{\text{holds for all } V_b \leq 2}$

$\boxed{0 < V_b < 2V}$

Check limits:

(*) At $V_b = 2$:

$\Leftarrow$ $V_b = 2 \Rightarrow V_{SD}^2 - 4V_{SD} + 4 = 0$

$V_{SD} = 2V$

$\Rightarrow \underbrace{V_{SD}}_{2V} \not< \underbrace{4 - V_b}_{2V}$

Ineq. ① isn't satisfied!