Bilkent University

EEE-313

Lab 4

Common Emitter Stage Cascaded with Push-Pull Voltage Buffer

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Section 01

I. Introduction

In this lab, the circuit shown in Figure 1 is going to be implemented. The circuit is essentially an amplifier with two stages.

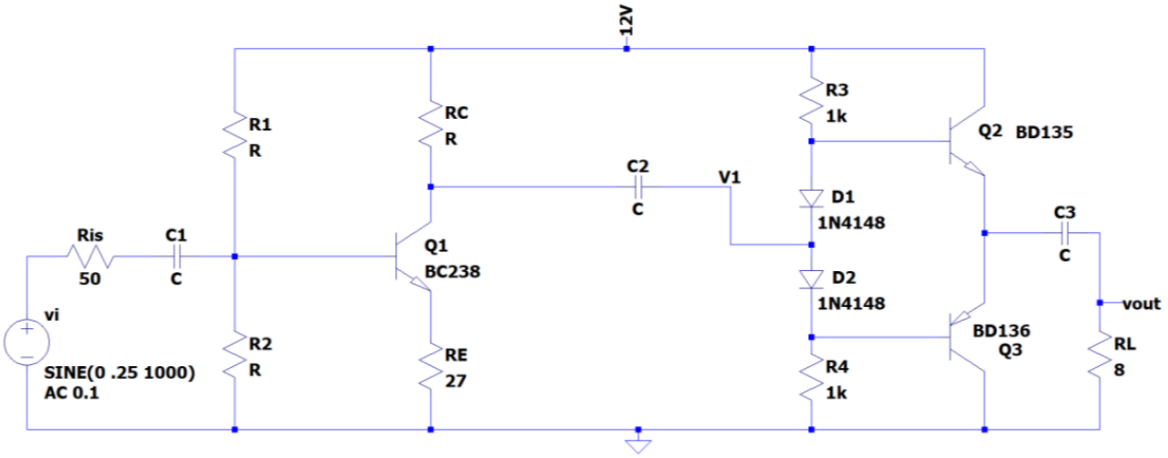

Figure 1: Circuit to be used in the lab

The lab consists of two parts: software and hardware analysis. In the software part, the circuit will be implemented and analyzed by LTSpice. In the hardware part, the circuit is going to be implemented on a breadboard. In the manual, it is stated that the first stage of the amplifier should have a gain of about -10 without the second stage connected (i.e., when C_2 is removed). The overall gain should be around -5. The output should not get clipped up to an ac input of 0.5V peak.

Based on these specifications, the values of R_1, R_2 and R_C are to be determined. Some components' values, such as R_{is}, R_E, R_3, R_4 and R_L, are given. The input and output resistances, also the resistance seen from V_1 to the right, are going to be measured. Later, by changing the capacitors to the specified values, the low and high cut-off frequencies are going to be measured. Lastly, the purpose of the diodes is going to be investigated by observing the output without their presence.

In the hardware part, first, the Q-point values I_C and V_{CE} are going to be measured, and they will be adjusted to the desired values. Then by applying an input as Asin(wt), for different amplitudes and frequency 1kHz, the gain will be investigated. The harmonics of the signal are also to be observed. Later, the input voltage where the distortion begins will be determined, also the low and high cut-off frequencies will be found by measuring the output again.

The models of the transistors are BC238, BD135, and BD136, whose datasheets and their SPICE models are available [1], [2], [3]. The diode model 1N4148 is already available in LTSpice. The models are also found in the lab.

II. Hardware Implementation and Analysis

Before implementing the circuit, the purposes of the first stage and the output stage should be explained. The first stage is essentially a common emitter amplifier, and it is specified that it should have a gain around -10 by itself. The output stage consists of a pnp and an npn BJT, and it is used as a voltage buffer. The reason is that if the load R_L is connected directly to the first stage, the gain will drop significantly due to the fact that R_L is very small (8Ω). But unlike the first stage, whose output resistance is larger causing the gain to drop with small load, the output stage has low output resistance, providing a gain around -5.

To determine R_C, R_1 and R_2, first they should be chosen such that the transistor Q1 is in forward active region, since transistors can amplify signals in forward active but not in SAT mode. This requires a DC analysis for the first stage. Later, to check if the gain is -10 for the first stage, the first stage's AC analysis should be performed also. The analyses are provided below.

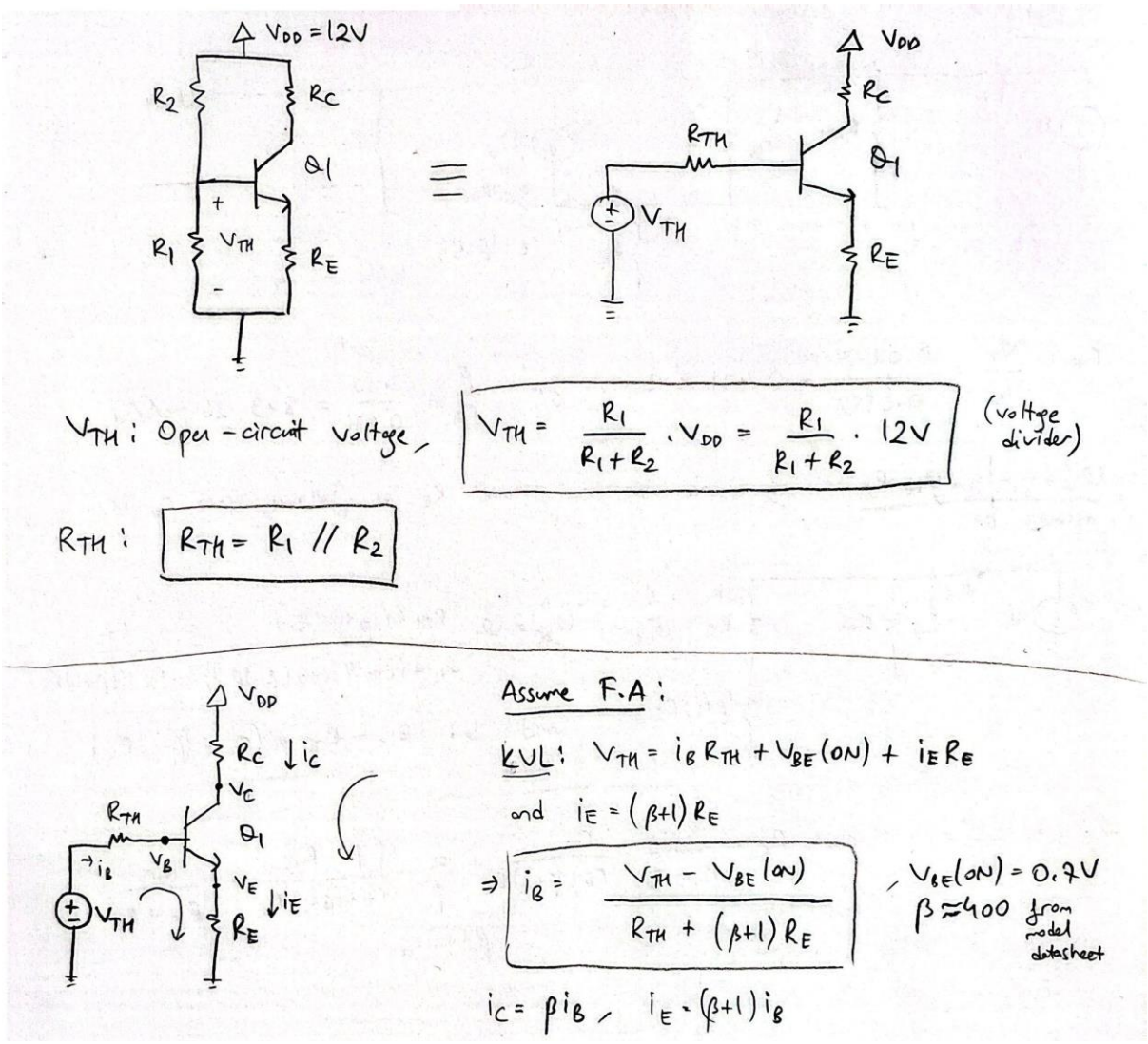

Figure 2: DC analysis and Thévenin conversion for the first stage

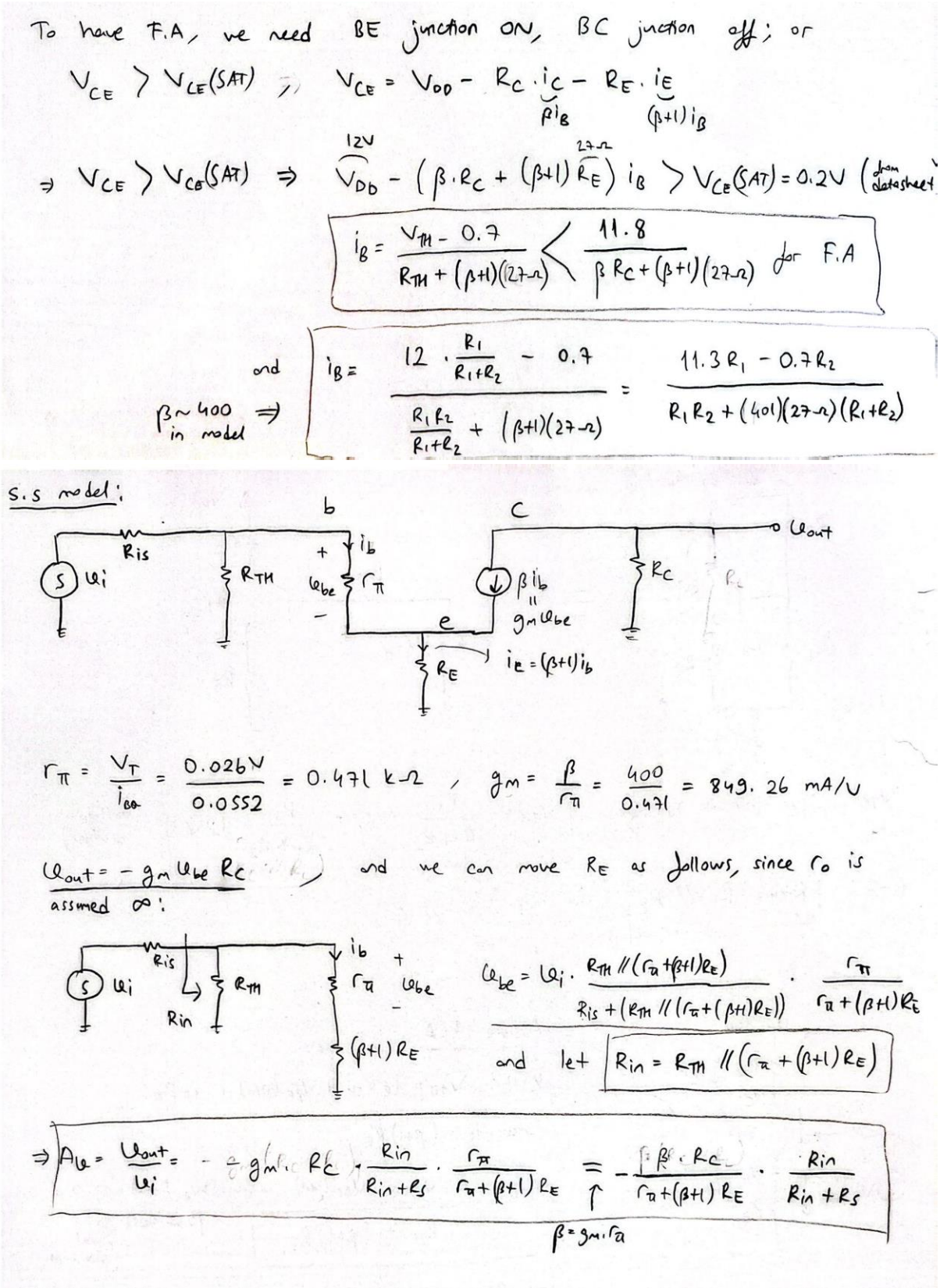

Figure 3: DC and AC anaylsis for the first stage

When the following standard values for the resistors are chosen and are inserted into the equations, it is seen that the F.A. condition is satisfied and the gain is approximately -10.

Component	**Value**
R_1	2.2 kΩ
R_2	270 Ω
R_C	400 Ω

Table 1: Chosen component values.

With the chosen values, the circuit is implemented on LTSpice.

- **Part A - Software Analysis**

A1. The implemented circuit is shown in Figure 4. At this stage the capacitors are set to very high values so that they may be considered as short at 1KHz. I chose 1000μF for all of them.

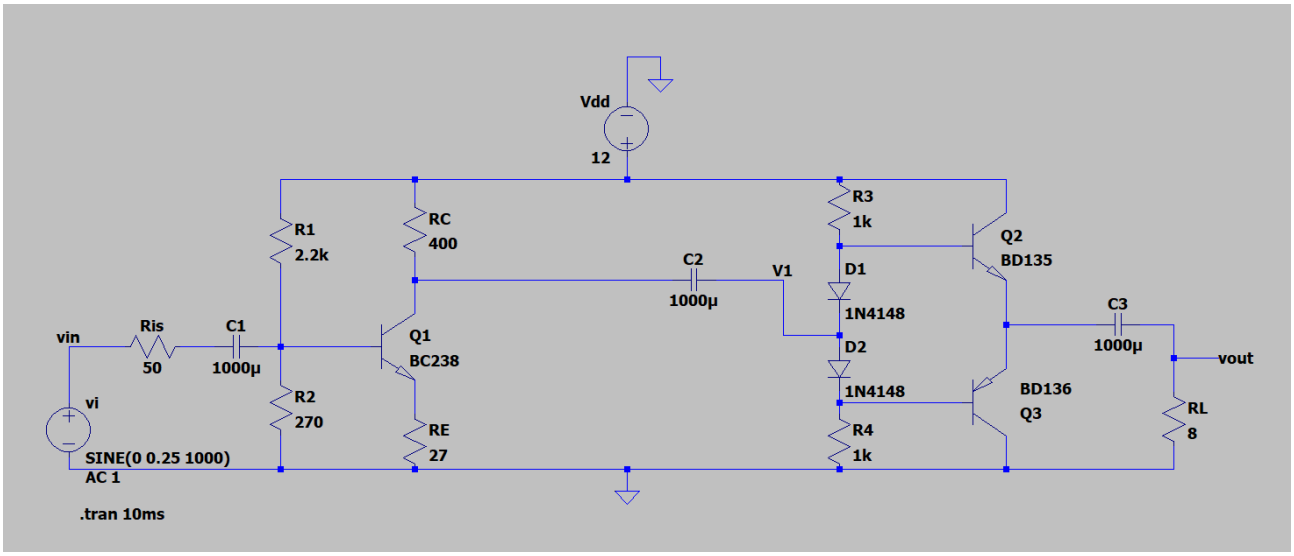

Figure 4: Circuit implemented on LTSpice

Before connecting the AC source and the output stage, first the DC operating points of Q1, in other words the collector current I_C and collector-to-emitter voltage V_{CE} should be measured, since these will determine the values of g_m and r_π present in the small signal model.

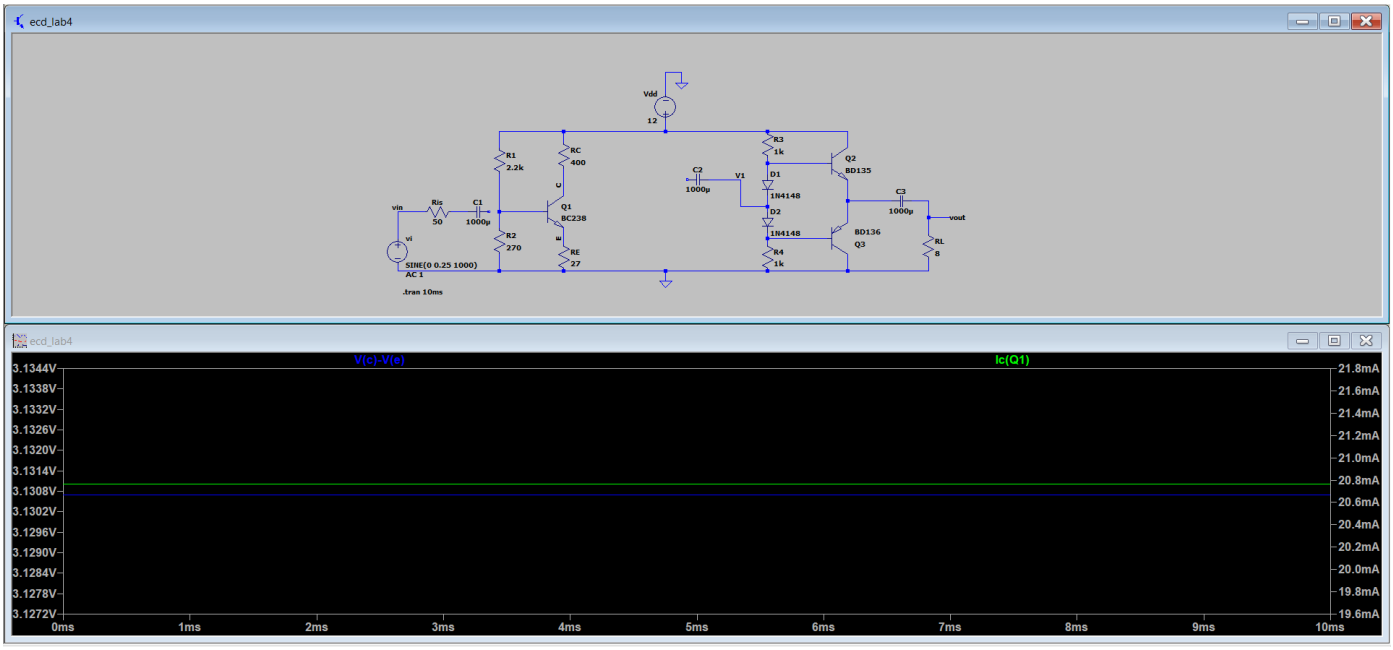

Figure 5: Measuring the DC operating points of Q1

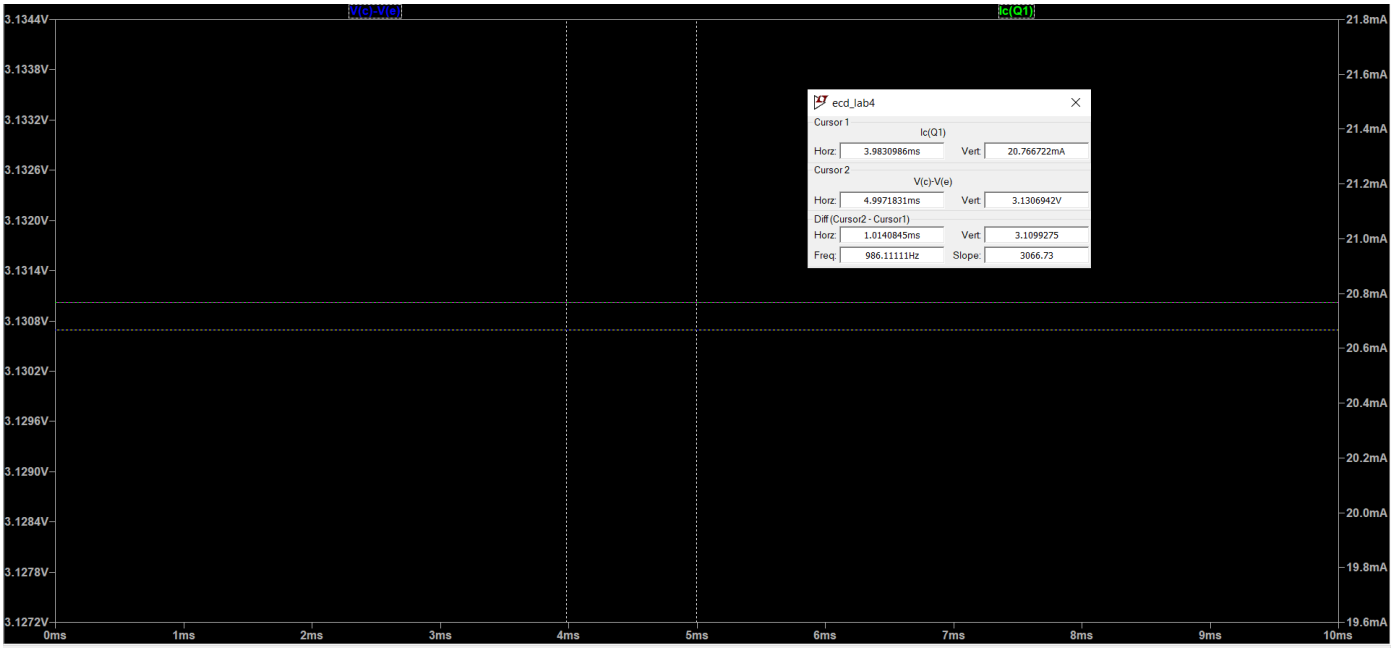

Figure 6: I_C = 20.77 mA and V_{CE} = 3.13 V

First, to make sure that the first stage works properly, C_2 is taken out and the first stage's output is measured. The measurement is shown in Figure 8. It should be noted that since there is not a DC block (coupling) capacitor at the first stage's output without C_2 connection, there is also a DC component present. To find the gain, the peak-to-peak value of the output (i.e variation) should be considered and be divided to the input peak-to-peak, which is 0.5V since input has amplitude 0.25V.

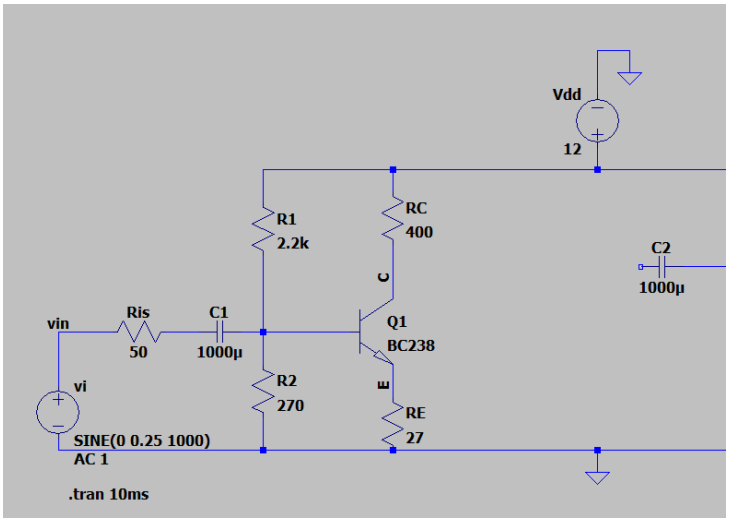

Figure 7: C_2 is disconnected

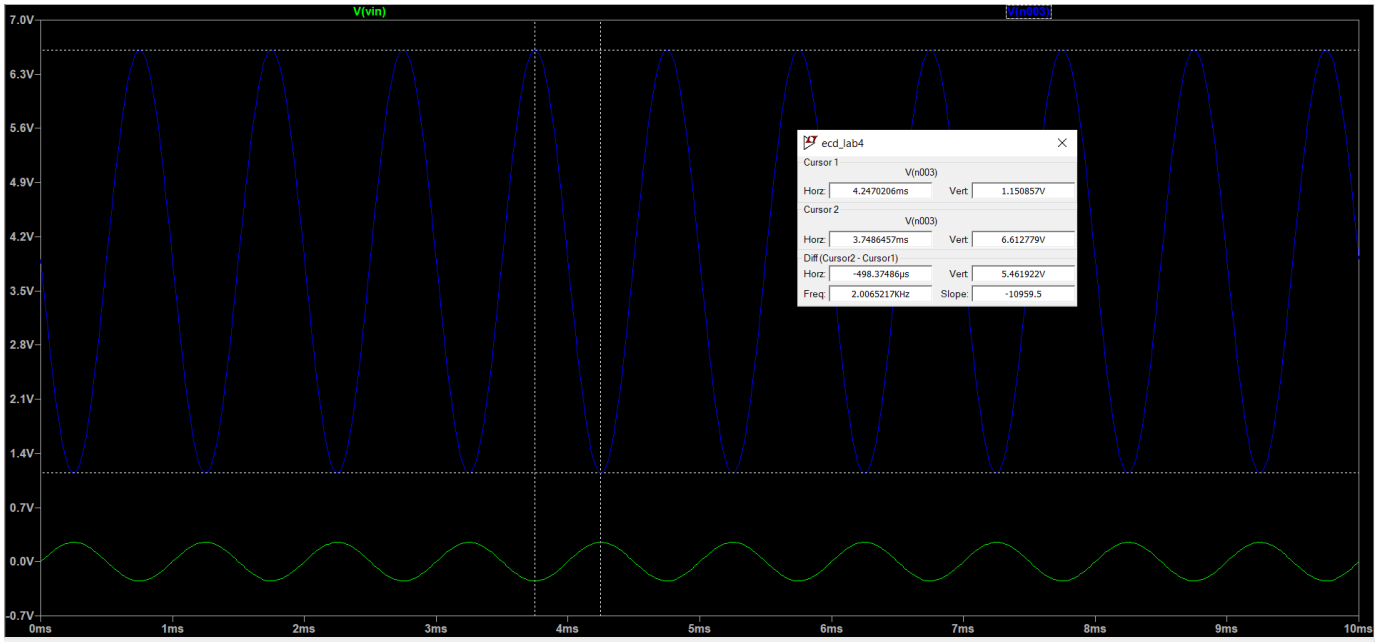

Figure 8: Input/output of first stage, output is shown in blue

Since the output has 5.462 V peak-to-peak value without considering the DC offset, the gain is found as -5.462 V/ 0.5 V = -10.92 V/V. The (-) is due to the fact that output is inverted with respect to the input. As expected, the gain is very close to -10. Now, with the second stage connected, the overall gain can be measured.

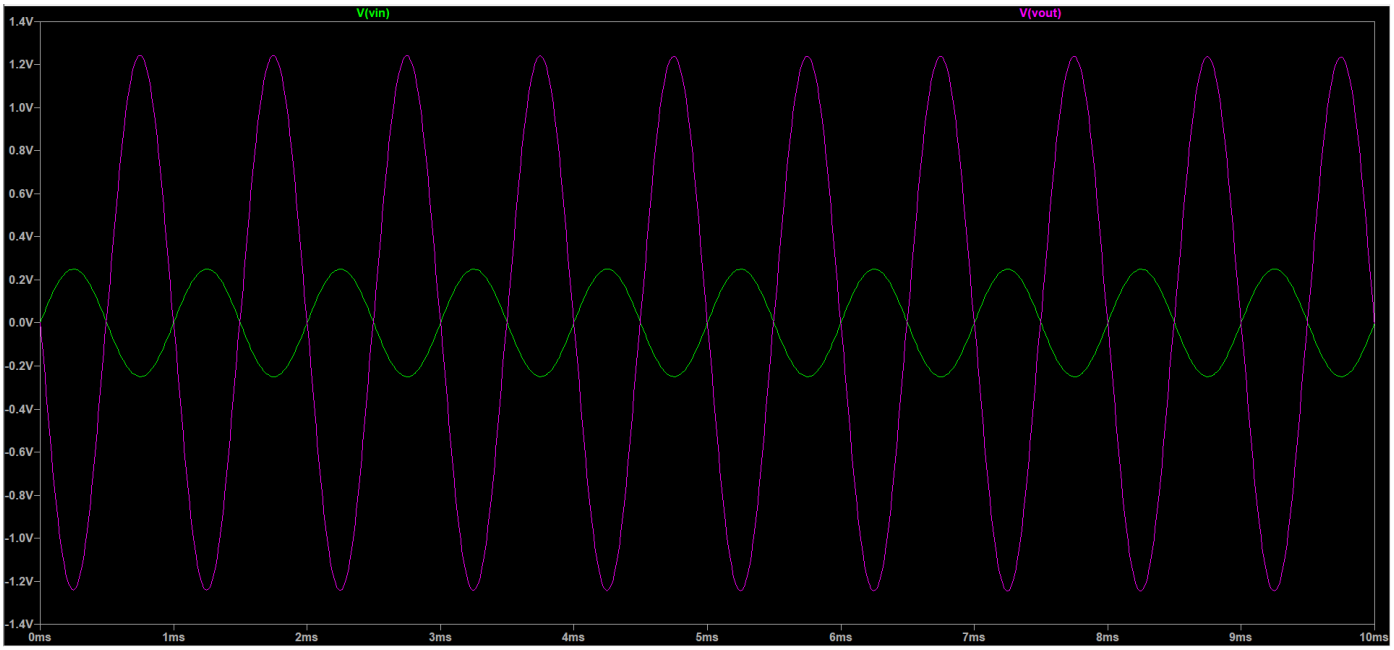

Figure 9: Input is shown in green, output is shown in pink

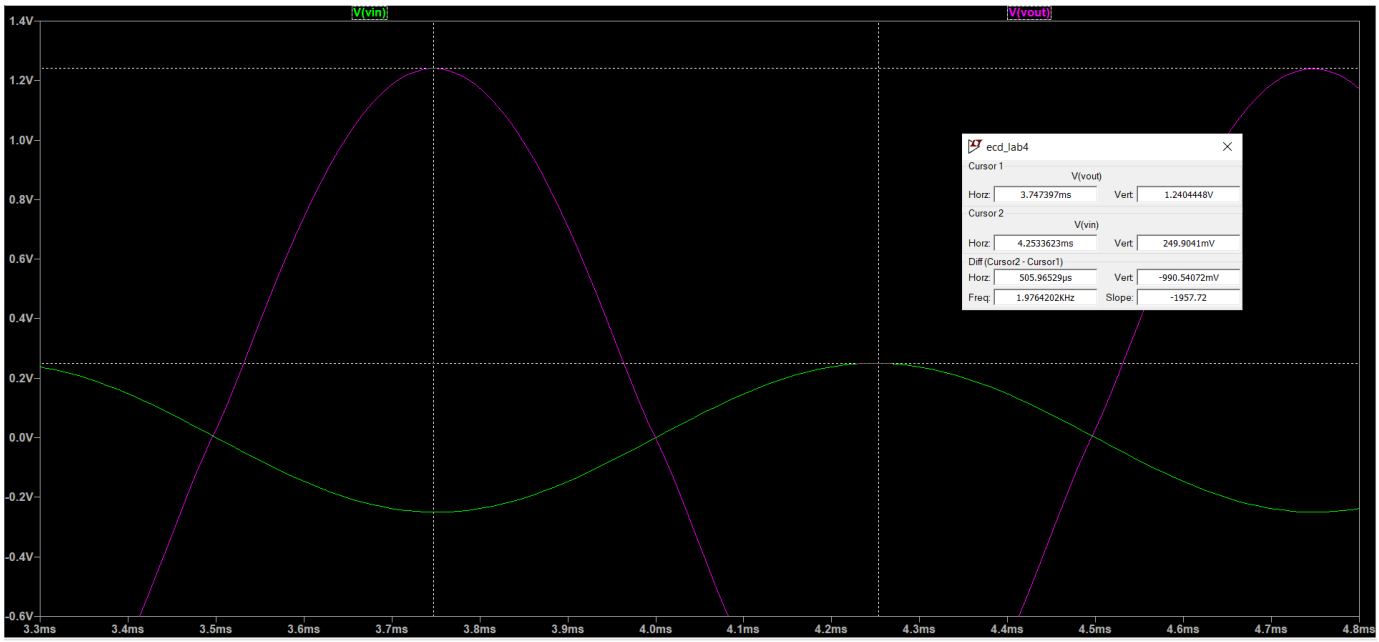

Figure 10: Input/output peak voltage measurement.

Therefore, the overall gain is:

$$A_v = \frac{v_{out}}{v_{in}} = \frac{-1.24\ V}{0.25\ V} = -4.96\ V/V \tag{1}$$

which is very close to -5 as desired.

To measure R_{in} seen from point V_1 to the right, also the input and output impedance of the amplifier, the voltage variation at these points can be divided to the current variation. This is similar to connecting a test source to these points. First, for R_{in} seen from V_1:

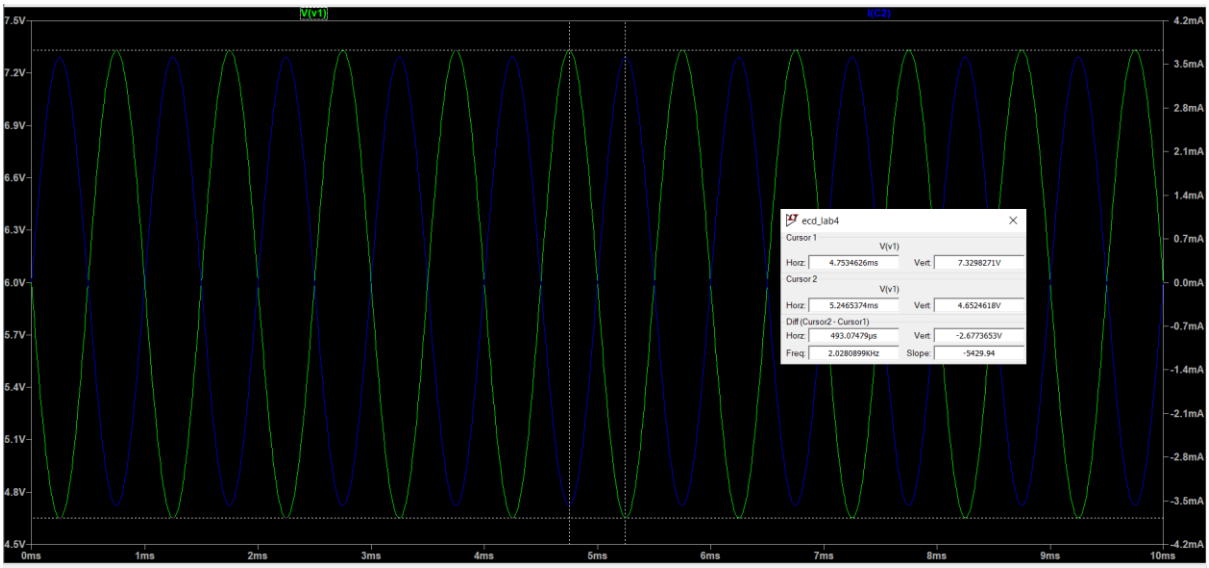

Figure 11: Voltage variation is 2.67 V

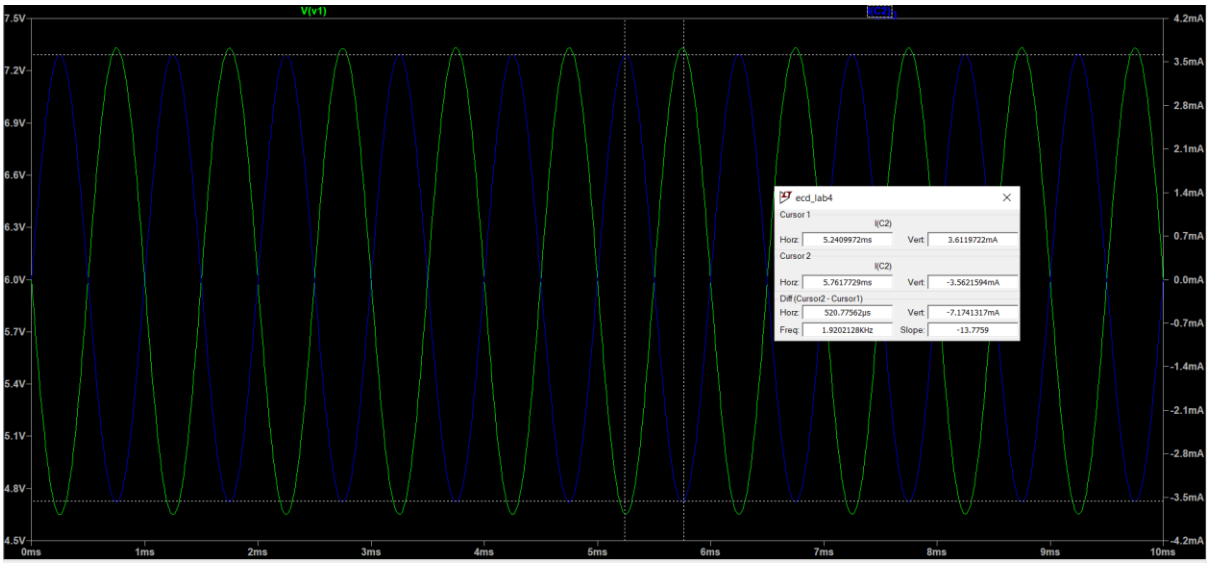

Figure 12: Current variation is 7.17 mA

Therefore:

$$R_{in,1} = \frac{2.67\ V}{7.17\ mA} = 372.38\ \Omega \tag{2}$$

which is close to 400Ω as specified.

To find R_{in} and R_{out}, since the voltages and currents don't have any offsets, we can directly divide the peak voltage by the peak current as they both correspond to half of the variation.

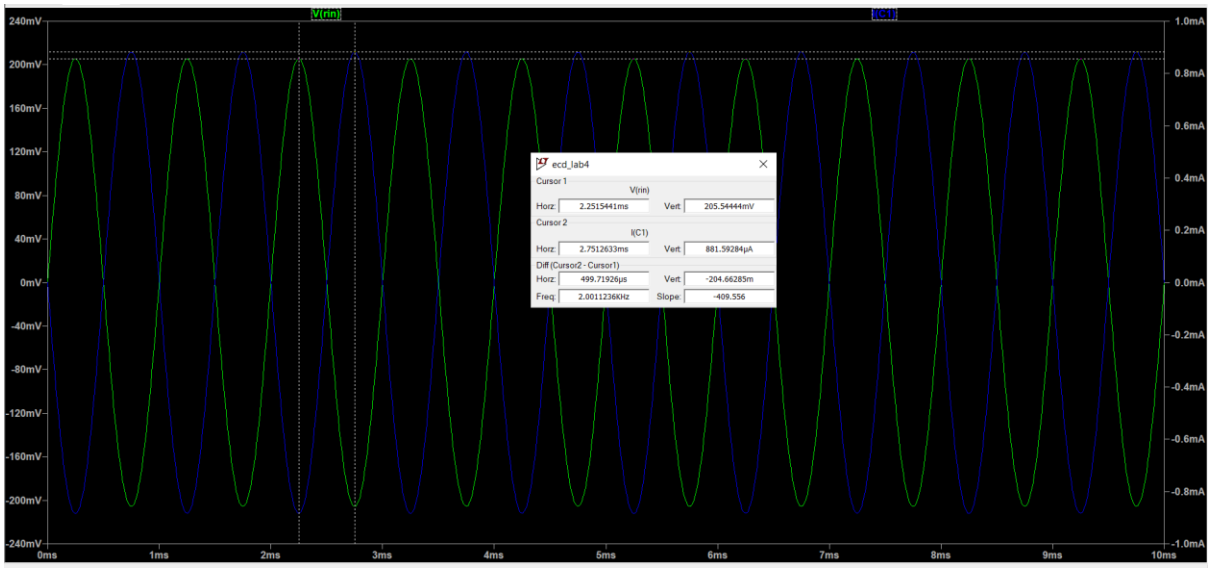

Figure 13: For R_{in}, the peak voltage is 205.54 mV, the peak current is 881.59 µA.

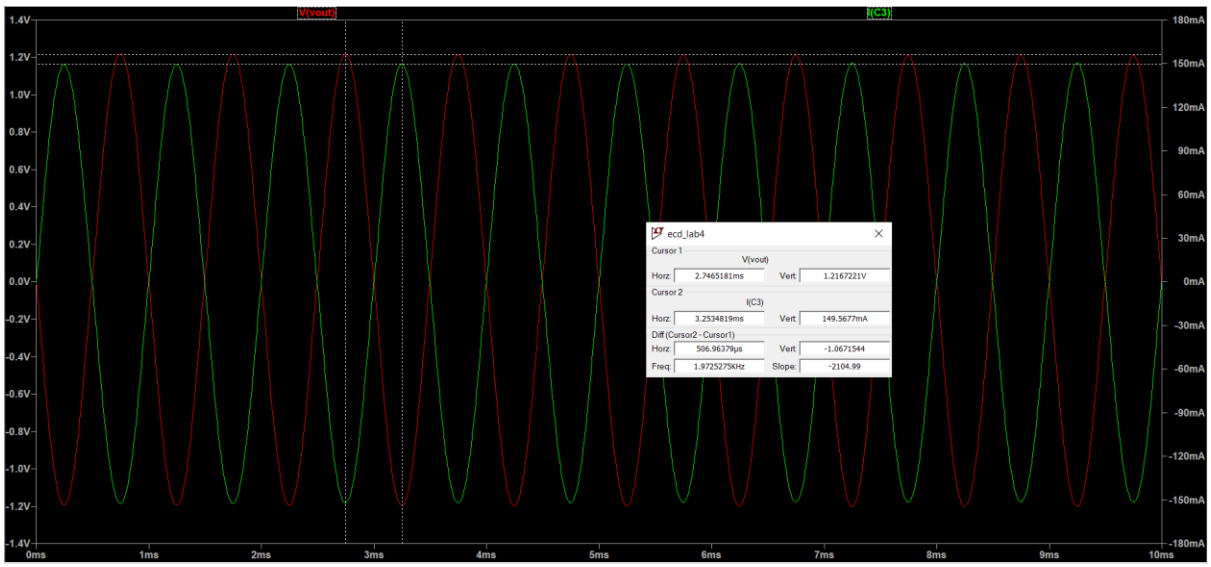

Figure 14: For R_{out}, the peak voltage is 1.22 V, the peak current is 149.56 mA.

Therefore;

$$R_{in} = \frac{205.54\ mV}{881.59\ \mu A} = 232\ \Omega,\ \ R_{out} = \frac{1.22\ V}{149.56\ mA} = 8.157\ \Omega \tag{3}$$

As expected, the output voltage is very small, and very close to 8Ω, since the output stage is essentially a voltage buffer, which should have small output resistance. The input resistance is also small due to the very small emitter resistance R_E (27Ω) and small chosen R_2 = 270 Ω.

Lastly, to check whether the output is distorted up to an AC input of 0.5V peak:

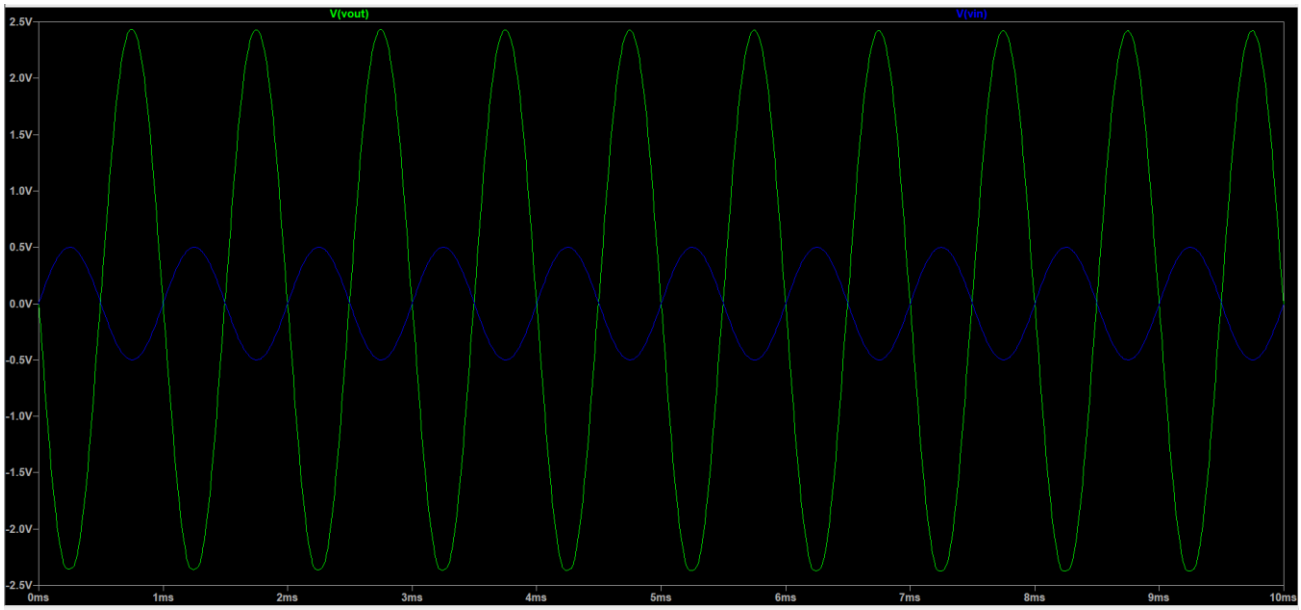

Figure 15: Input/output when V_{in} has 0.5V amplitude

As seen from Figure 15, the output is not distorted for 0.5V, hence the specifications are satisfied.

A2. The -3dB low cut-off frequency f_L of the amplifier is determined by the external capacitors and high cut-off frequency f_H is set by the internal device capacitances. For f_L it can be thought that the external capacitors see an equivalent resistor and the RC circuit acts like a low-pass filter. First, the circuit is modified such that C_1=10µF, C_2=100µF, and C_3=1000µF.

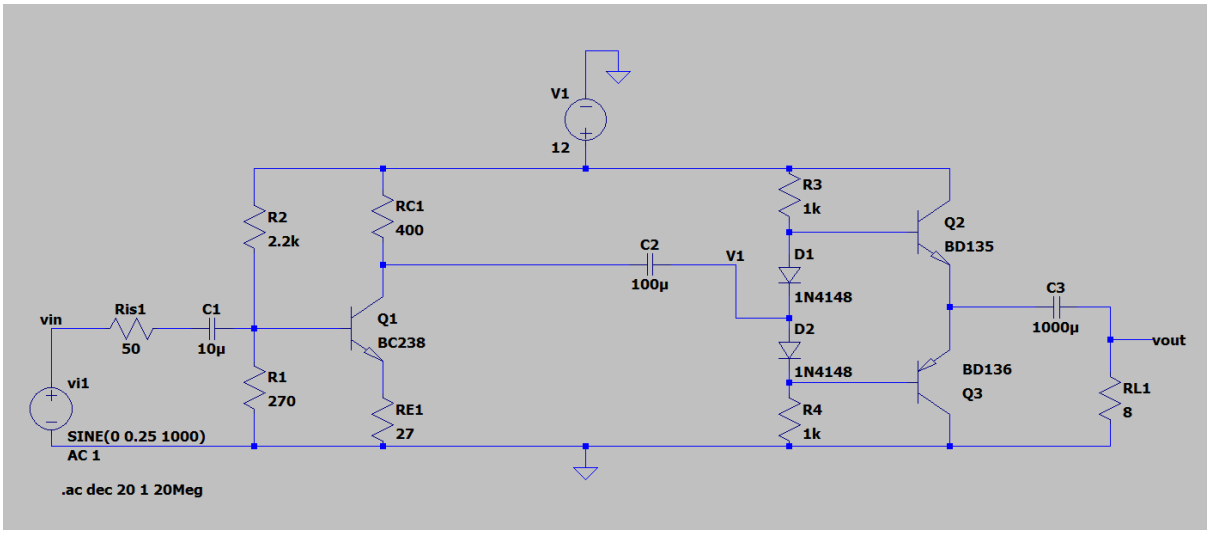

Figure 16: Modified circuit

Since the capacitor C_1 and the resistance seen from that point, which are R_{in} and R_{is} in series, act like an RC circuit, the low cut-off frequency is expected to be around:

$$f_L \approx \frac{1}{2\pi(R_{in}+R_{is})C_1} = \frac{1}{2\pi(232\Omega + 50\Omega)(10\mu F)} = 56.48\,Hz \quad (4)$$

The Bode plots are presented in Figures 17-18.

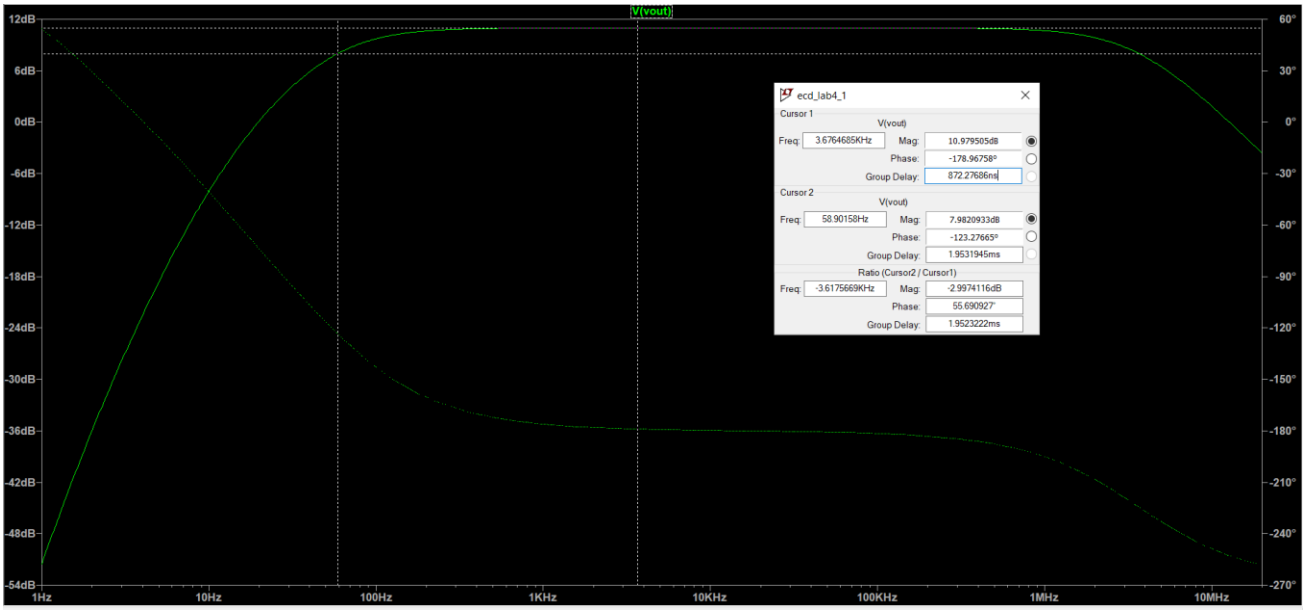

Figure 17: f_L is 58.9 Hz

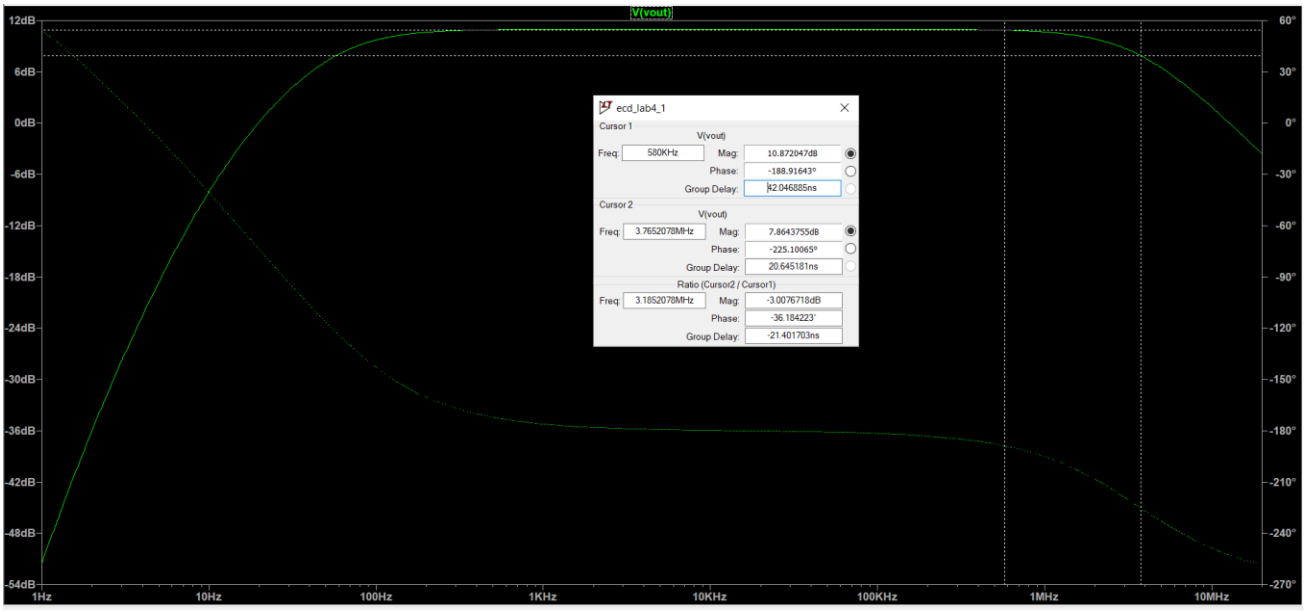

Figure 18: f_H is 3.765 MHz

As expected f_L is very close to the calculated value of 56.48 Hz, with 4.28% error. f_H is set by the internal capacitors present in the transistors.

A3. The diodes form a push-pull voltage buffer (giving the name to the amplifier) so that the output is not distorted. The voltage at the point V_1 is purely sinusoidal, since C_2 blocks the DC voltage coming from the first stage.

When this sinusoidal voltage is at the positive cycle, the diode D2 is on and D1 is off. Hence when the diode is on, it is essentially a 0.7V (V_{on} of the diode) voltage source, and therefore the pnp transistor Q3 is on (since there is a biasing voltage coming from the diode's forward voltage at the base) while the npn transistor Q2 is off (the diode D1 is open circuit, i.e off).

In the negative cycle, as the voltage decreases, now D1 is on and D2 is off, meaning Q2 is on and Q3 is off. This way, only one of the transistors are off and they cannot be on at the same time. Since they contribute to the output voltage separately, the output is also a pure sinusoidal wave, where the positive cycle comes from one transistor and the negative cycle comes from another.

When the diodes are shorted:

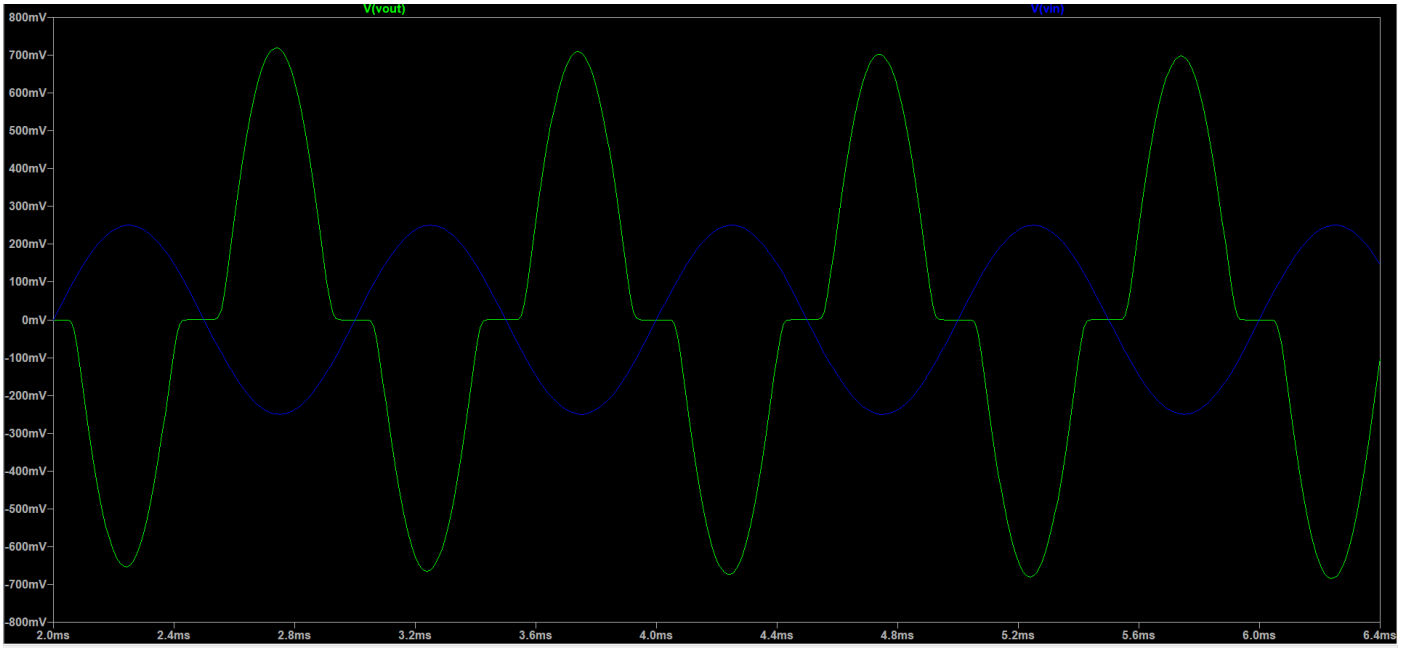

Figure 19: Output when the diodes are shorted

As expected, the output is distorted, which proves that the diodes function for an undistorted output.

Overall, the values obtained at the simulations can be summarized as:

	Value		**Value**
R_C	400 Ω	f_L	58.9 Hz
R_1	2.2 kΩ	f_H	3.765 MHz
R_2	270 Ω	R_{in} (from V_1)	372.38 Ω
I_C	20.77 mA	R_{in}	232 Ω
V_{CE}	3.13 V	R_{out}	8.157 Ω
A_v of first stage	-10.92 V/V	A_v (V_{out}/V_{in})	-4.96 V/V

Table 2: Overall results of the simulations

- **Part B - Hardware Analysis**

The circuit is set up with the chosen values as shown Figure 20:

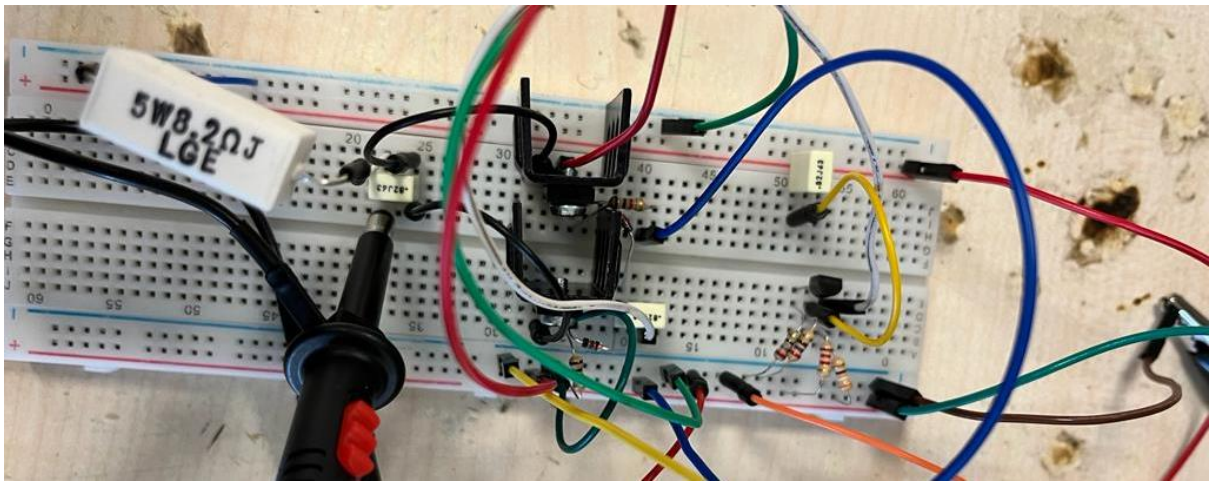

Figure 20: Circuit set up on hardware

To prevent the BJTs from burning since high currents may pass over them, some additional parts are present. This keeps the currents from increasing too much, otherwise, the currents on the BJTs keep on increasing up to the point where they might be damaged. For the same reason, the 8Ω load resistor is also a stone resistor. Since they take less space, I used 820 nF capacitors as DC block capacitors, which can still be considered as short circuit in 1 kHz.

B1. The DC operating points of the transistor Q1, which are the collector current I_C and collector-emitter voltage V_{CE}, are measured with a multimeter, before the second stage is implemented and the AC source is connected:

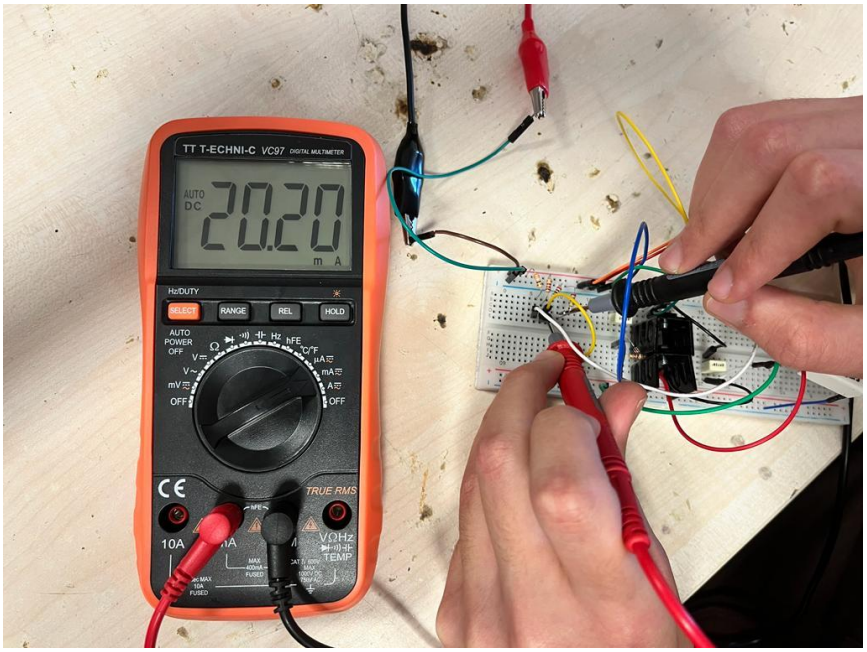

Figure 21: I_C is measured as 20.20 mA

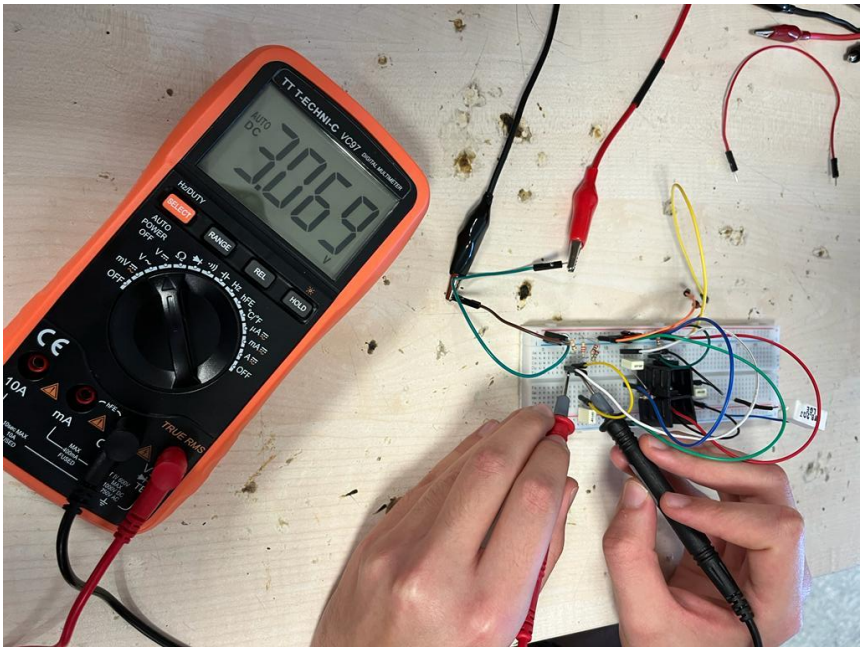

Figure 22: V_{CE} is measured as 3.069 V

Compared to the simulation results, which are 20.77 mA and 3.13 V respectively, the error percentages are 2.74% for I_C and 1.92% for V_{CE}, meaning that the desired Q-point is achieved with minimal error.

B2. In this part, the input is a sinusoidal signal with 0.1 V amplitude and 1 kHz frequency. The output is shown in Figure 23.

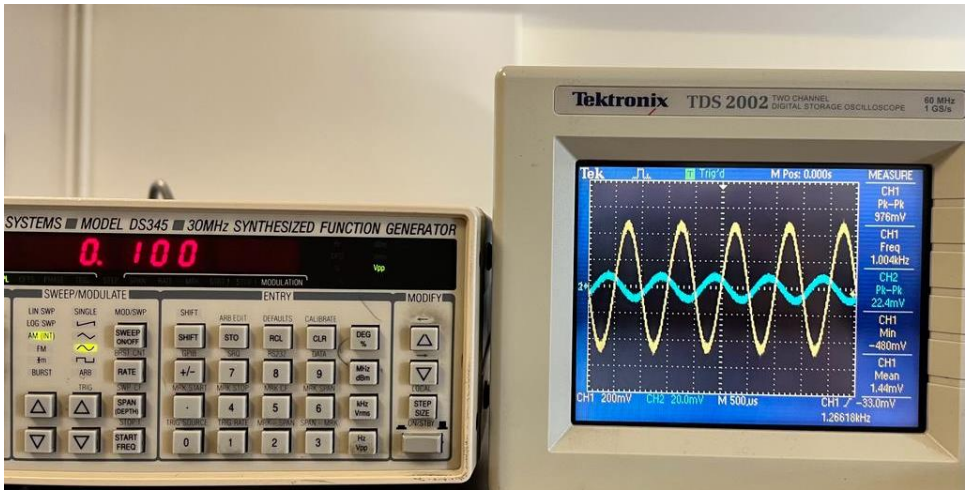

Figure 23: Input/output measurement for V_{in} = 0.1sinwt, input voltage (in blue) is incorrect due to a problem in the oscilloscope probe

Considering the peak-to-peak values for the output (976 mV) and the input (200 mV), the gain is:

$$A_v = -\frac{976\ mV}{200\ mV} = -4.88\ V/V \tag{5}$$

which is close to -5 as desired.

B3. Now, the measurements are repeated for V_{in} = 0.2sinwt, 0.3sinwt, 0.4sinwt, and 0.5sinwt, where the frequency is still 1 kHz.

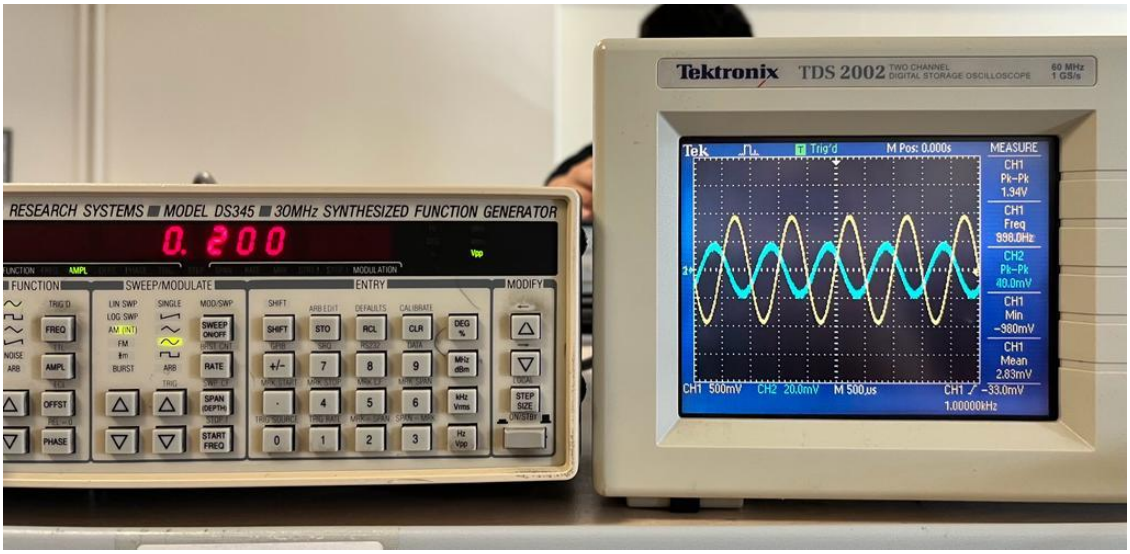

Figure 24: V_{in} = 0.2sinwt, $V_{out,p\text{-}p}$=1.94 V

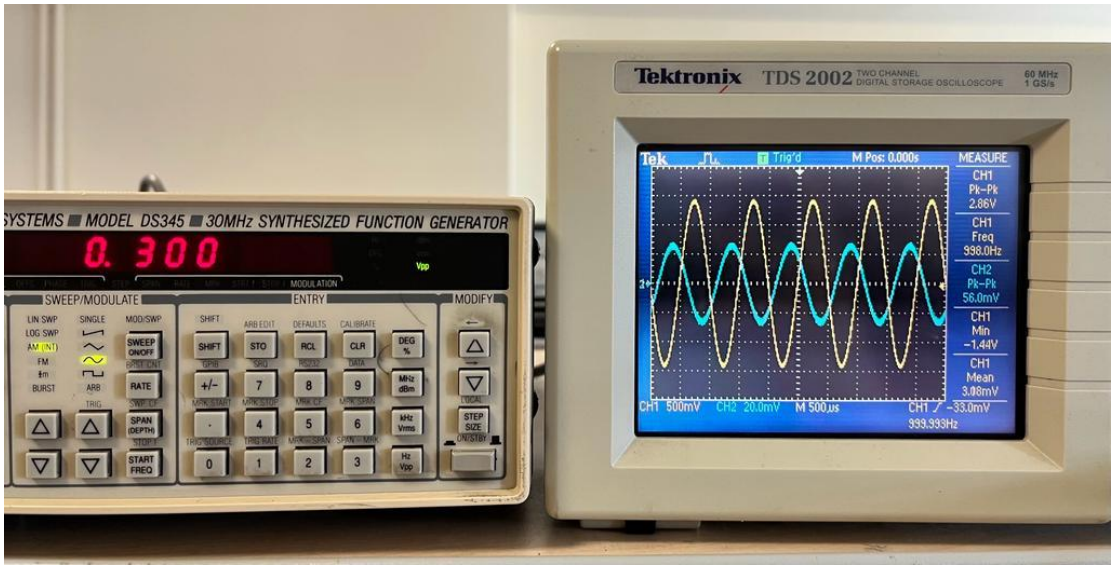

Figure 25: V_{in} = 0.3sinwt, $V_{out,\ p\text{-}p}$=2.86 V

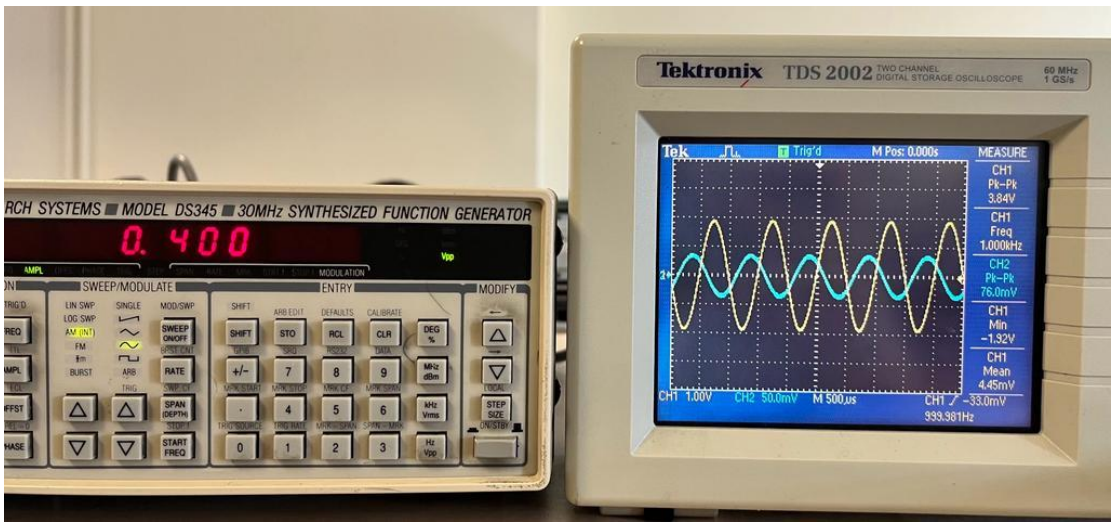

Figure 26: V_{in} = 0.4sinwt, $V_{out,\ p\text{-}p}$=3.84 V

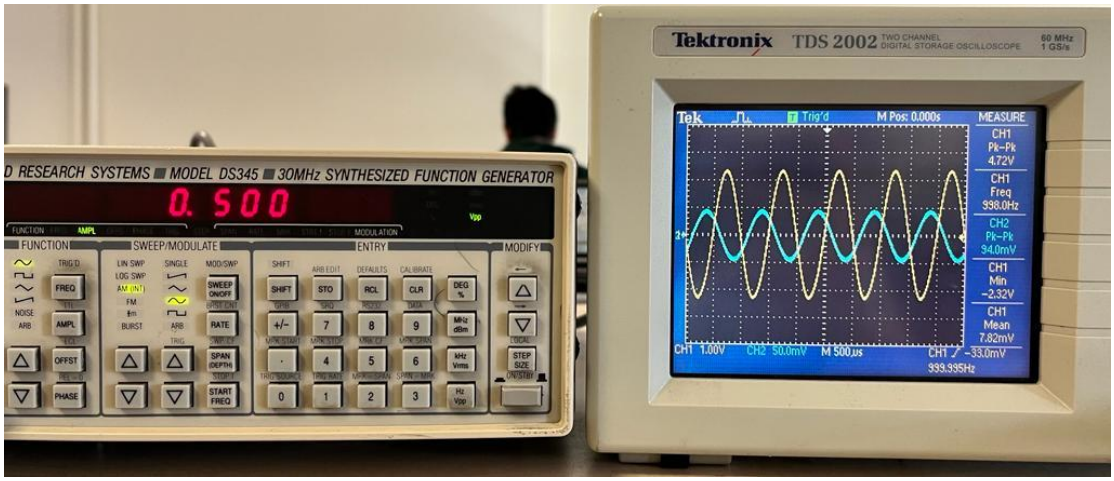

Figure 27: V_{in} = 0.5sinwt, $V_{out,\ p\text{-}p}$=4.72 V

Then, using the following formula:

$$A_{dB} = 20log_{10}\left|\frac{V_{out}}{V_{in}}\right| \quad (6)$$

where A_{dB} is the gain in dB, the gain for each voltage is shown in Table 3. Note that the gain is calculated again considering the input/output peak-to-peak voltages. Also, the gains are negative since the output is inverted with respect to the input.

Input voltage amplitude (V)	**Input peak-to-peak voltage (V)**	**Output peak-to-peak voltage (V)**	**$A_v = V_{out}/V_{in}$ (V/V)**	**Deviation from desired gain (-5 V/V)**	**A_{dB} (dB)**
0.1	0.2	0.976	-4.88	2.4%	13.77
0.2	0.4	1.94	-4.85	3%	13.71
0.3	0.6	2.86	-4.77	4.6%	13.57
0.4	0.8	3.84	-4.8	4%	13.62
0.5	1	4.72	-4.72	5.6%	13.48

Table 3: Gains for different input voltages

Even though the gain decreases with increasing input amplitude, still they are close to -5 with indicated errors. It should be noted that when V_{in} = 0.5sinwt, the output is not distorted, therefore conforms to the specification.

After that, the frequency content of the output is observed using the FFT operation of the oscilloscope. This is called the "harmonic content" of the signal, and by taking the Fourier transform of the signal, it shows which frequency content is present is the cosine basis representation. Since up to 0.5V input, the output is an undistorted sinusoid with frequency 1 kHz, the only harmonic content present is 1 kHz, which represents the signal in the frequency domain. Figure 28 shows the harmonic content of the output for V_{in}=0.2V amplitude. For the other input voltages, again the harmonic content only contains 1 kHz, since the output is not distorted and can be represented by only 1 kHz in the frequency domain.

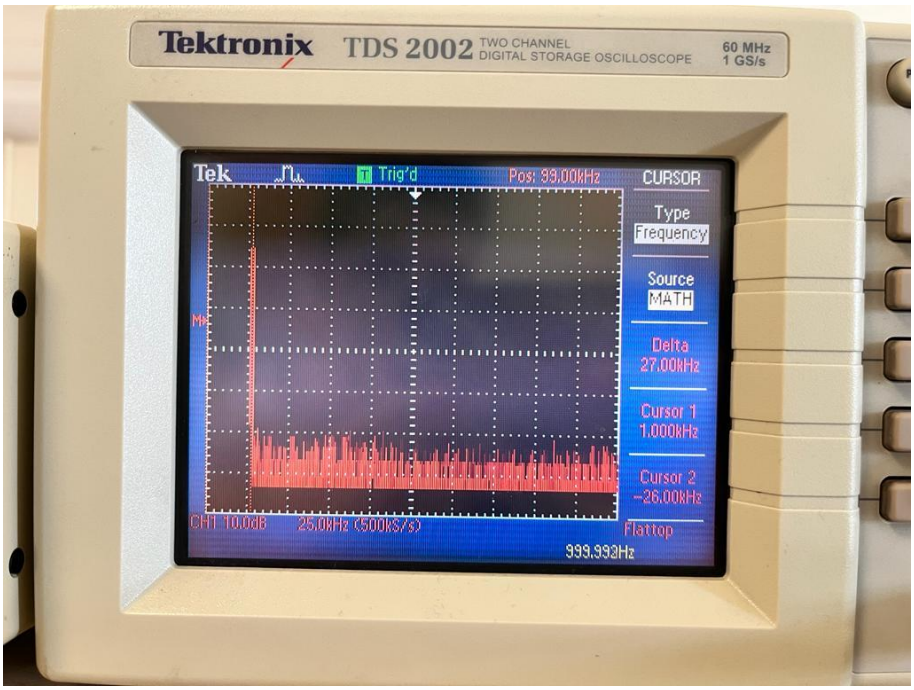

Figure 28: Harmonic content of the output for V_{in}=0.2sinwt

B4. To find the input voltage where the distortion begins, the input is increased slowly, as shown in Figures 29-30.

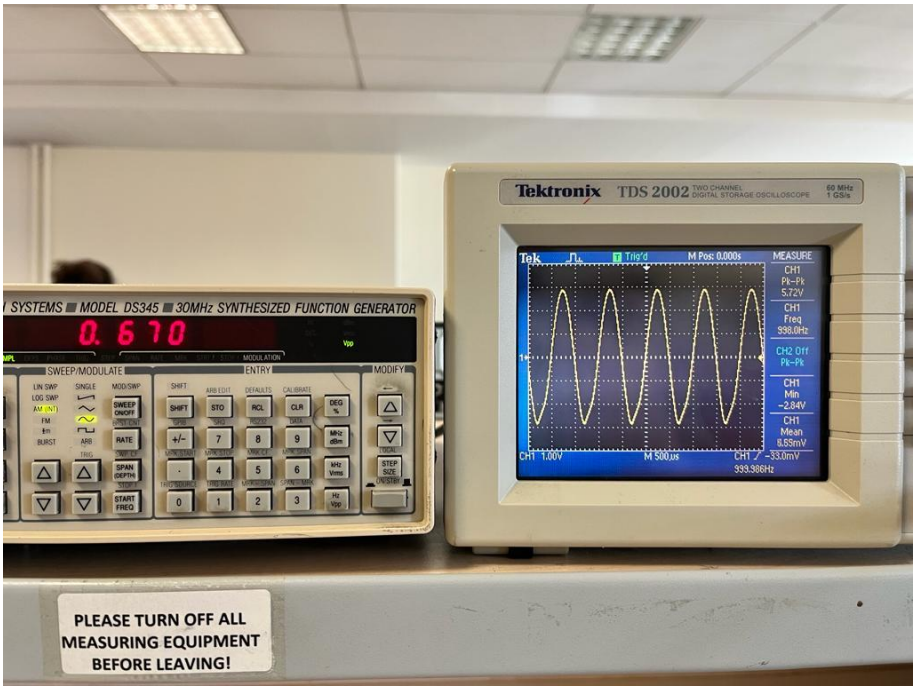

Figure 29: Distortion at the bottom is observed at V_{in}=0.67 V amplitude

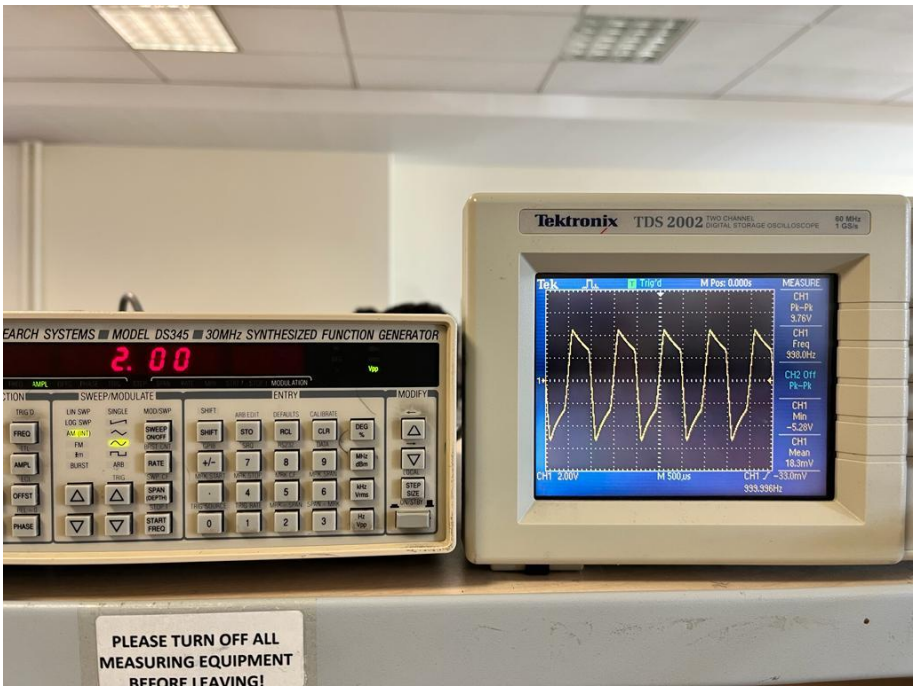

Figure 30: Distortion at the top is observed at V_{in}=2V amplitude

The reason why distortion occurs at the bottom can be explained as follows: The negative cycle of the output corresponds to the input voltage's positive cycle since the output is inverted with respect to the input. Since the AC input is connected to transistor Q1's base, the voltage increase at its base affects the transistor after a certain voltage. Normally, in "small signal" analysis, since the input is small, this effect is not considered. But after 0.67V amplitude, the base voltage goes up such that the B-C junction of Q1 is turned on, due to the fact that V_B-V_C difference exceeds V_{BC}(ON). This causes Q1 to go into the SAT region, where the transistor cannot amplify a signal since the current amplification is not possible in SAT mode.

The distortion at the bottom, similarly, corresponds to the input voltage's negative cycle. This time, after a point at the negative cycle, the base voltage goes down such that the B-E junction turns off, since the V_B-V_E difference becomes less than V_{BE}(ON). This causes the transistor to turn OFF, therefore causing a distortion at the top, for V_{in}=2V amplitude (a signal comparable with the bias voltage at the base).

Also, for the distorted output at V_{in}=2sinwt, the harmonic content is measured again. This time, since the output is distorted, it is represented not only by 1 kHz, but also its "harmonics" at (1+2k) kHz at the frequency domain, where k is an integer. On the oscilloscope therefore, the peaks occur at 1kHz, 3kHz, 5kHz, ... as shown in Figures 31-33.

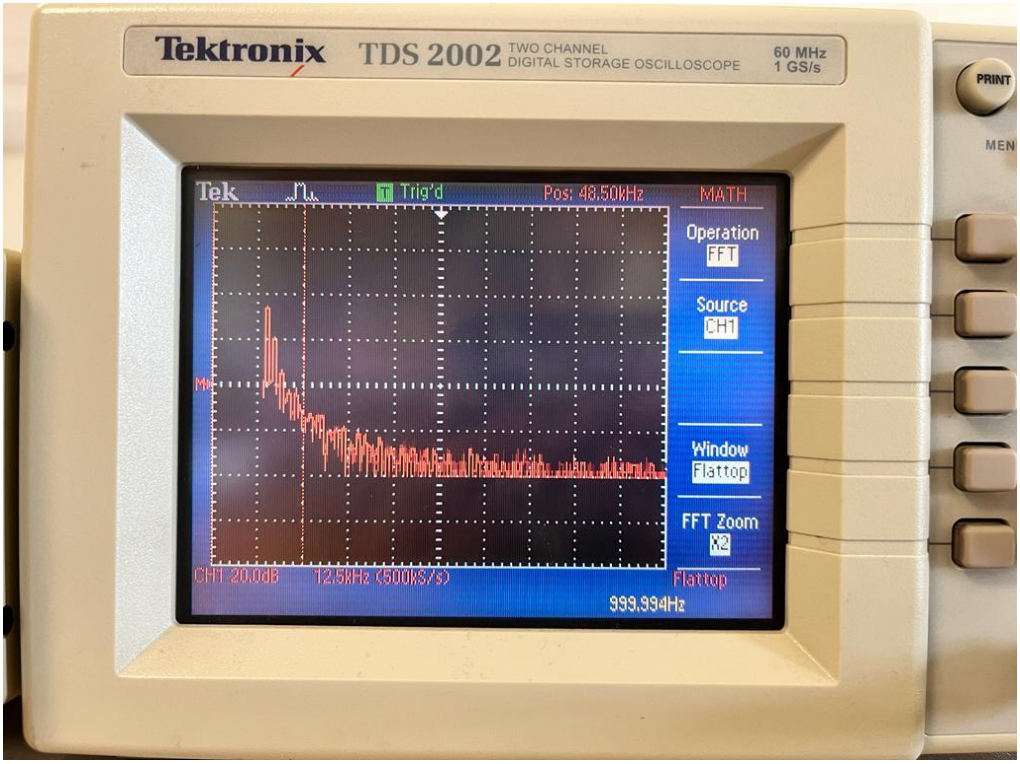

Figure 31: Harmonic content of the distorted signal

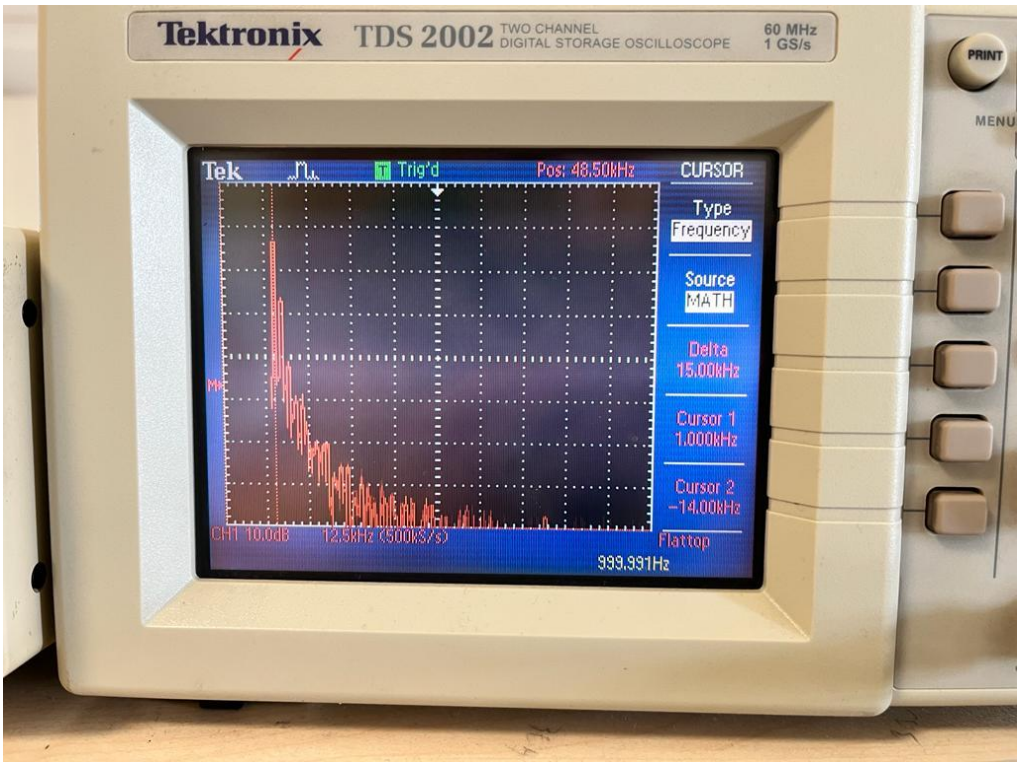

Figure 32: Highest peak occurs at 1 kHz frequency

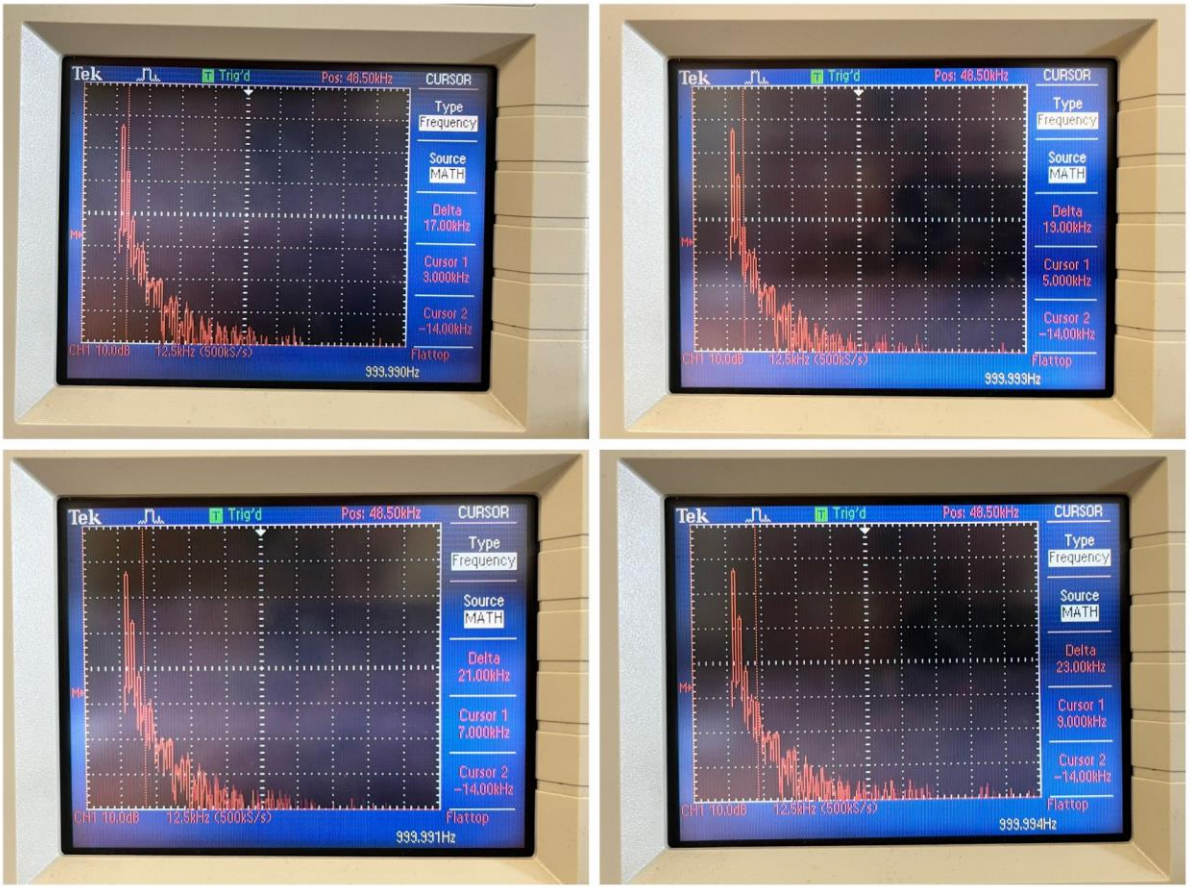

Figure 33: Other peaks occur at f= 3 kHz, 5 kHz, 7 kHz, 9 kHz

B5. To find the cut-off frequencies, the capacitors are replaced with C_1=10μF, C_2=100μF, and C_3=1000μF.

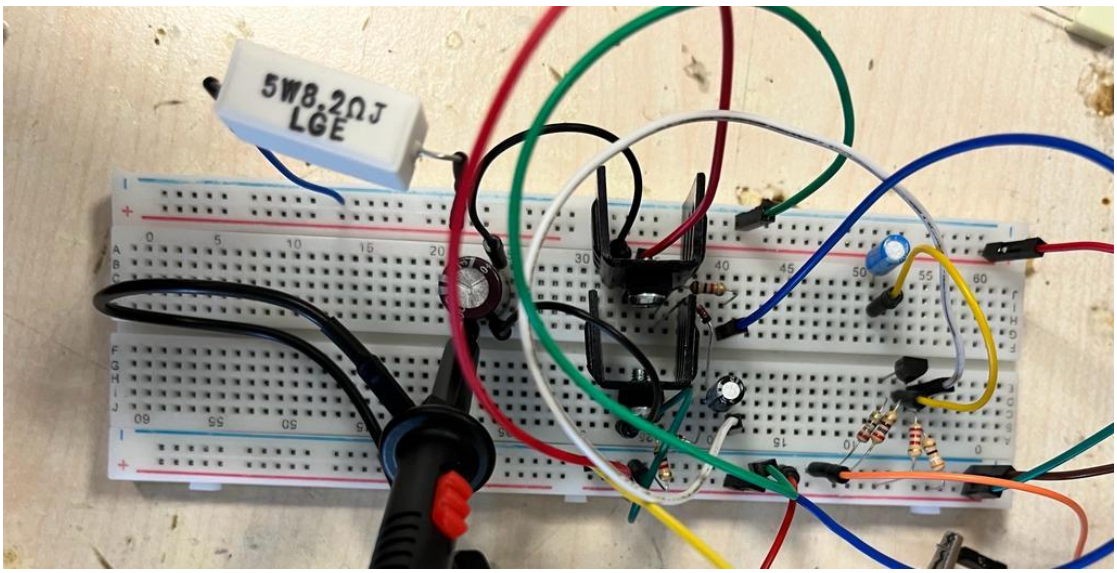

Figure 34: Capacitors are replaced

Then, by keeping the input amplitude at 0.2 V and by the fact that the gain is 13.71 dB at 0.2 V amplitude (0.4 V peak-to-peak), at the -3 dB frequencies the gain should approximately be 13.71-3 = 10.71 dB. Therefore, using equation 6, the frequencies where the output has the peak-to-peak voltage of:

$$V_{out,peak-to-peak} = 0.4 \times 10^{\frac{10.71}{20}} \approx 1.4\,V \tag{7}$$

are to be determined. The frequencies are determined as seen in Figures 35-36:

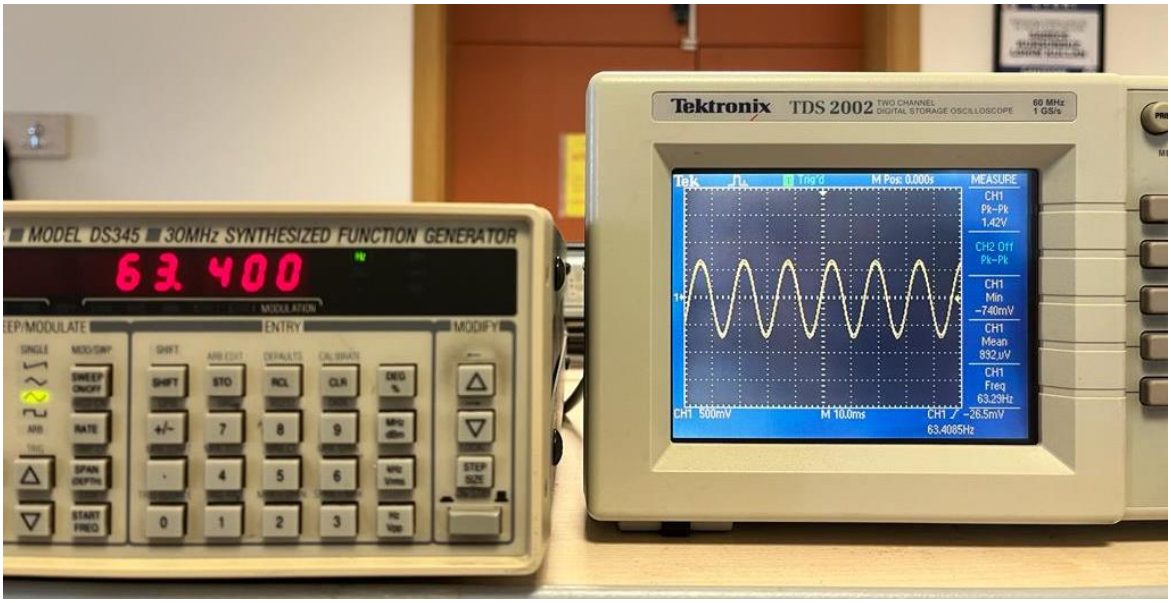

Figure 35: Lower cut-off frequency f_L is approximately 63.4 Hz

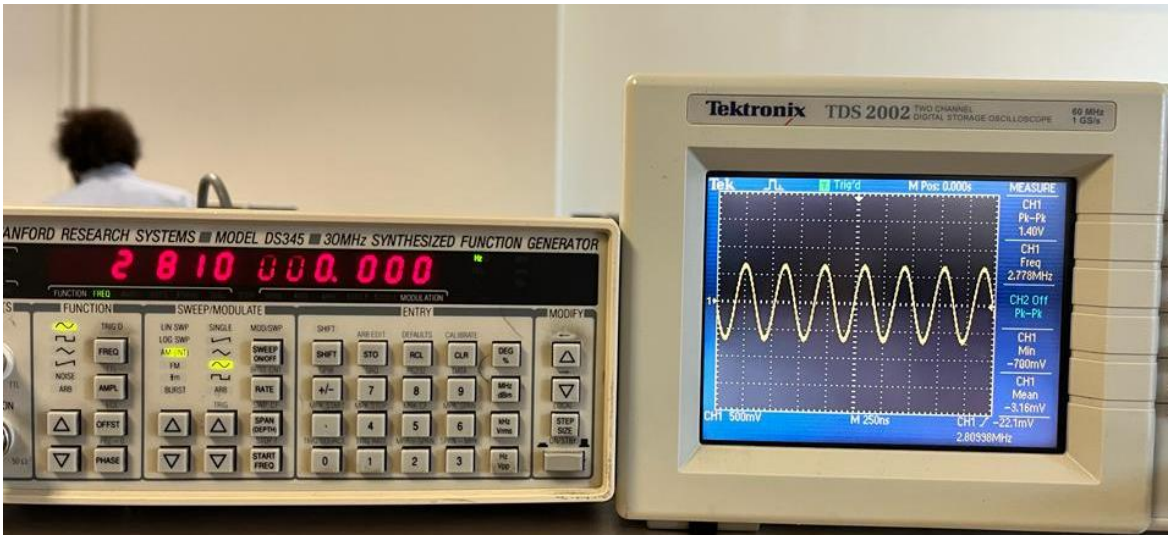

Figure 36: Higher cut-off frequency f_H is approximately 2.81 MHz

Even though the frequencies are very close to those found in the simulations, there is still an error. This difference may have occurred due to the fact that the internal capacitances of the transistors used in hardware is different from the ones in the LTSpice simulation. Also, the internal capacitances and resistances of other components in the circuit (jumpers, resistors, wires, ...) were neglected in the simulations. This especially affects the higher cut-off frequency which is determined by the transistors' internal capacitors, which may be different in the LTSpice model and the real-life model.

Lastly, the gain at a frequency lower than f_L and higher than f_H should be measured. I chose 30 Hz and 4 MHz for these purposes.

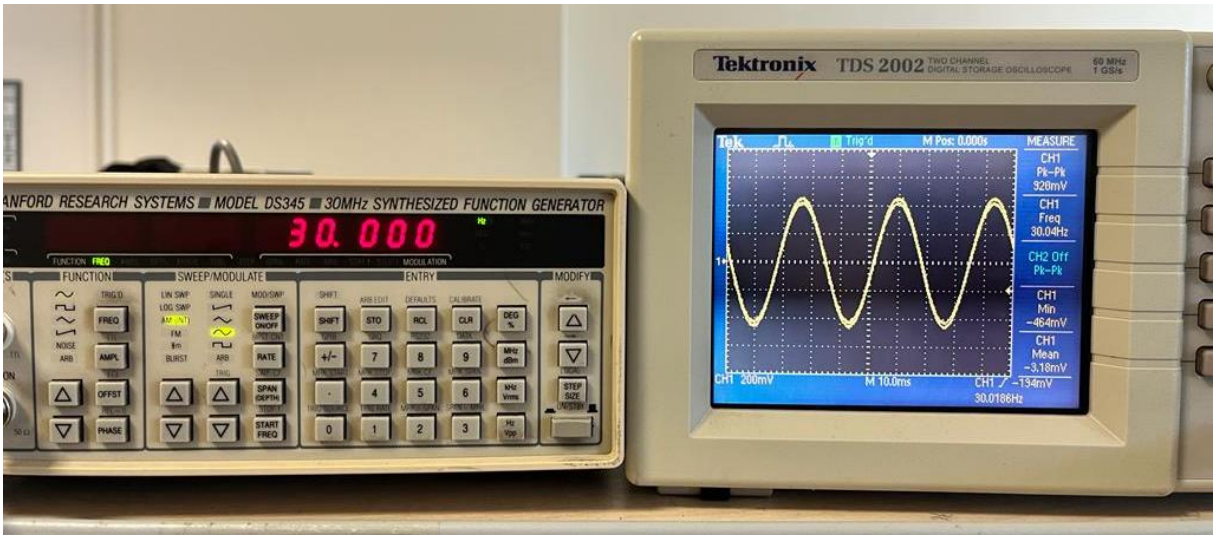

Figure 37: At f=30 Hz, $V_{out,peak\text{-}to\text{-}peak}$=920 mV

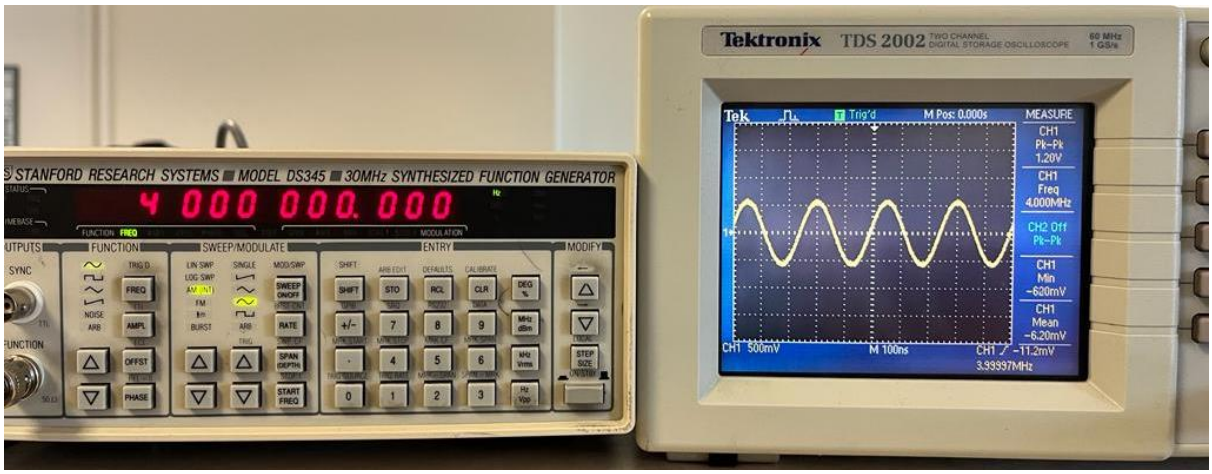

Figure 38: At f=4 MHz, $V_{out,peak\text{-}to\text{-}peak}$=1.2 V

Lastly, the gains for the frequencies (using equation 6) at this part can be tabulated as:

Frequency	**Input peak-to-peak voltage (V)**	**Output peak-to-peak voltage (V)**	**Voltage gain A_v (V/V)**	**dB gain (dB)**
1 kHz	0.4	1.94	-4.85	13.71
f_L = 63.4 Hz	0.4	1.40	-3.5	10.71
f_H = 2.81 MHz	0.4	1.40	-3.5	10.71
30 Hz	0.4	0.92	-2.3	7.23
4 MHz	0.4	1.2	-3	9.54

Table 4: Gains at different frequencies

III. Conclusion

In this lab experiment, a common emitter stage cascaded with a push-pull voltage buffer was implemented, first on software then on hardware. The results were successful for both cases, where the gain was around -5 (with 0.8% error for software, and errors in 2.4%-5.6% range for hardware). The reason for bigger errors on hardware was because of the imperfections in the real-life components, like the internal resistances of jumpers or the variation in resistance/capacitance values. There was no distortion up to a 0.5V AC input, and DC values I_C and V_{CE} were as desired in the hardware part. The distortion voltage was determined as 0.67V for the bottom, and 2V for the top part.

One problem was that as the input increased, the gain changed. This is because, as mentioned before, the hardware components' internal resistances, and also the internal capacitors and inductors create variation in gain for different inputs. For the same reason, the low and high cut-off frequencies, which were 58.9 Hz and 3.765 MHz respectively in software, deviated in hardware implementation. Even though the low cut-off frequency on hardware (63.4 Hz) is close to the software value, the high frequency (2.81 MHz) has varied with respect to the value measured on LTSpice. This has happened due to the different internal capacitors from the LTSpice model, which essentially determines the high cut-off frequency.

Overall, the experiment taught me to implement a cascaded BJT amplifier and also a voltage buffer which are used in applications like loudspeakers. I implemented two different stages and observed their effects, and therefore I was able to implement my theoretical knowledge in this lab.

References

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