

Bilkent University

EEE-313

Project Report

Analog Multiplier



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Section 03 - Section 01

I. Introduction

We chose the analog multiplier as our project. The project aims to design a multiplier that can multiply two sine waves. For this purpose, the Gilbert cell is going to be implemented, which is the most commonly used analog multiplier. A common design for a Gilbert cell is shown in Figure 1.

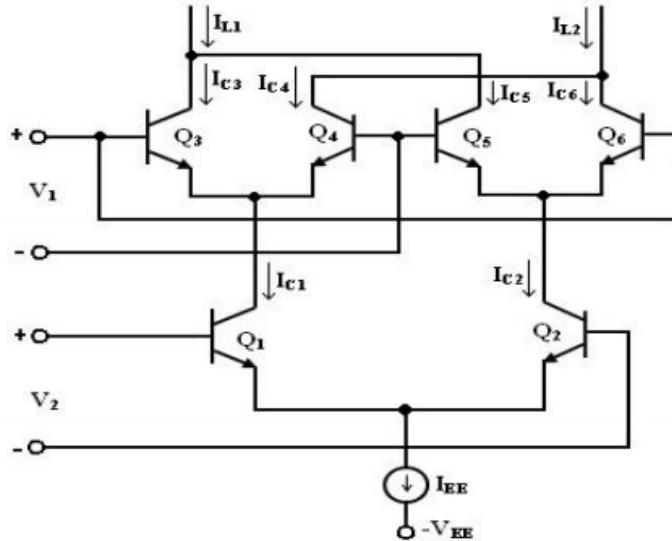


Figure 1: Gilbert cell [1]

The circuit consists of three differential amplifiers. For an analog multiplier implemented with a Gilbert cell, the sine wave (essentially the wave that will be multiplied) is added to the base of the bias generator of the differential amplifier. With the sinusoidal wave, the quiescent current of the input transistors, along with the gain and transconductance g_m of the amplifier, then changes sinusoidally [1]. With the varying current, which is determined by the second sine wave, the output is the multiplication of these sine waves, which is an AM modulated signal [2].

The fundamental specifications for the project are:

- Dual power supplies ($+/- V_{DD}$) no more than $+/-10V$.
- Power consumption should be less than $200mW$, i.e., $<10mA$ total current per supply.
- Resistors are allowed.
- The circuit should generate its own biasing, if you need different voltages you should generate them from the supplies.
- A double balanced mixing cell is required.

Given 1kHz and 20kHz sine waves, the resulting output of the circuit should be the multiplication of these two signals, i.e an AM modulated signal. To bias the transistors so that they all operate in forward active region, a voltage divider network from the power supply is going to be designed with resistors. DC block (coupling) capacitors will be another fundamental addition to the circuit, to stop the DC current going into the AC signal generator,

also to separate the DC bias voltage and the AC voltages. The capacitors should be chosen such that they can be considered short circuit at both 1 kHz and 20 kHz frequencies (frequencies of the multiplied waves).

There will be a single power supply in the circuit that is going to provide 12 V voltage, instead of using a dual power supply. Since it does not exceed the 20V difference as required, it can be used alone. Then the voltage will bias the circuit using a voltage divider network implemented with resistors. To not exceed the 200 mW power consumption limit, the current on the 12V supply must not exceed $200/12 = 16.67$ mA.

An analysis of the differential amplifier, also of the Gilbert cell is provided in the next section, along with the software and hardware implementation of the circuit and the results.

II. Hardware Implementation and Analysis

a. Theoretical Analysis

The project consists of three differential amplifiers and 6 BJT npn transistors in total. Therefore, it is first essential to understand the DC transfer characteristics and also the operation in differential mode. Below, the analysis of a simple BJT differential amplifier is provided [2].

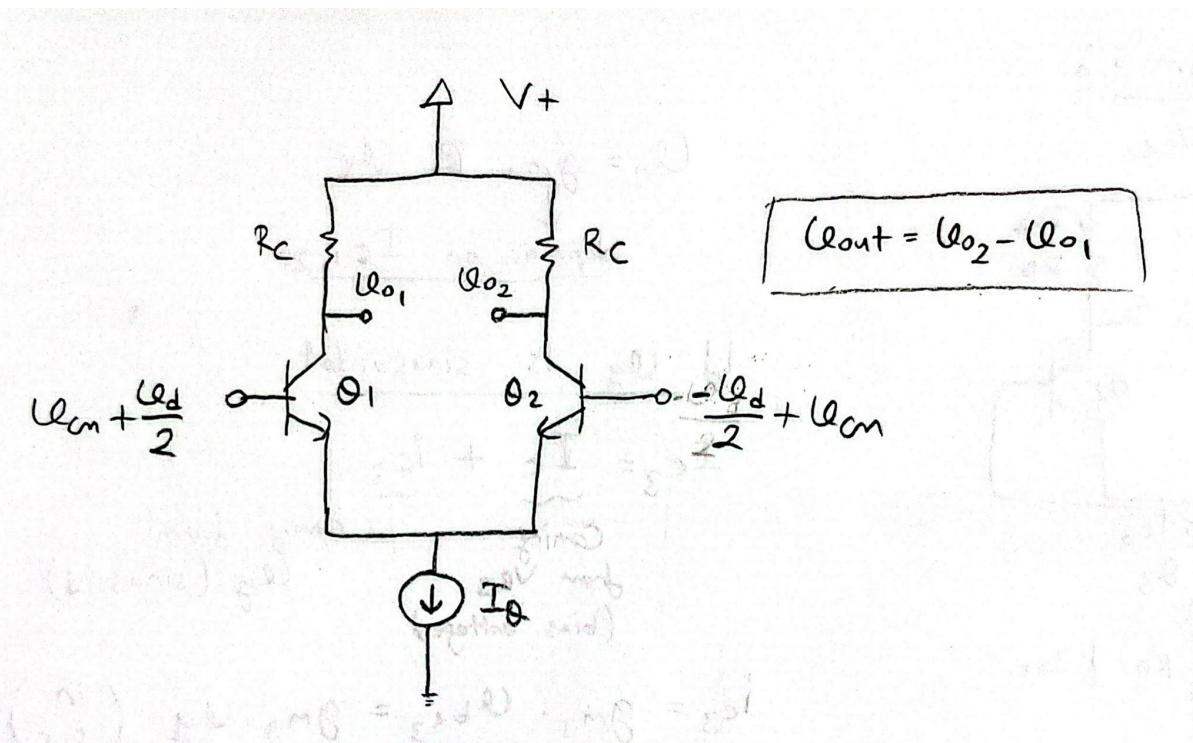


Figure 2: A simple BJT differential amplifier

DC transfer characteristics:

$$i_{C_1} = I_o e^{\frac{V_{BB1}}{VT}}, \quad i_{C_2} = I_o e^{\frac{V_{BB2}}{VT}} \Rightarrow I_o \approx i_{C_1} + i_{C_2} = I_o \left(e^{\frac{V_{BB1}}{VT}} + e^{\frac{V_{BB2}}{VT}} \right)$$

↓
large β

and we have $V_{BB1} - V_{BB2} = U_d$ in differential mode.

$$\Rightarrow \frac{i_{C_1}}{I_o} = \frac{I_o e^{\frac{V_{BB1}}{VT}}}{I_o (e^{\frac{V_{BB1}}{VT}} + e^{\frac{V_{BB2}}{VT}})} = \frac{1}{1 + e^{\frac{U_d}{VT}}} \Rightarrow \boxed{i_{C_1} = \frac{I_o}{1 + e^{-\frac{U_d}{VT}}}}$$

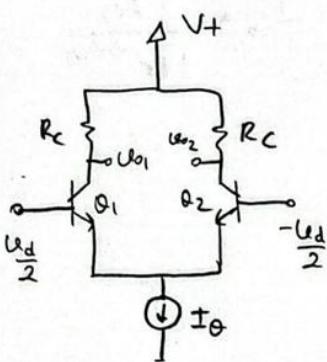
$$\boxed{i_{C_2} = \frac{I_o}{1 + e^{\frac{U_d}{VT}}}}$$

Linearize i_C 's:

$$i_C = i_C \Big|_{U_d=0} + \frac{\partial i_C}{\partial U_d} \Big|_{U_d=0} \cdot U_d$$

$$= \frac{I_o}{2} + \left(I_o \cdot \frac{1}{(1+e^{-\frac{U_d}{VT}})^2} \cdot \frac{-1}{VT} e^{-\frac{U_d}{VT}} \Big|_{U_d=0} \right) \cdot U_d = \boxed{\frac{I_o}{2} + \underbrace{\frac{I_o}{4VT} \cdot U_d}_{\text{small signal}}}$$

$$I_{C_{1,2}} \approx g_m \cdot U_d \Rightarrow g_m = \frac{I_o}{2VT}$$



in small signal:

$$\text{In DC} \Rightarrow I_{C_1} = I_{C_2} = \frac{I_o}{2}, \text{ due to symmetry}$$

$$g_{m1} = g_{m2} = \frac{I_{C_{1,2}}}{VT} = \frac{I_o}{2VT}$$

↳ A fraction of I_o

$$U_{o2} = g_m \frac{U_d}{2} R_C, \quad U_{o1} = -g_m \frac{U_d}{2} R_C \rightarrow \text{Common emitter amp gain}$$

$$A_{dm} = \frac{U_{o2} - U_{o1}}{U_d} = g_m R_C$$

$$(U_{o2} - U_{o1}) = g_m U_d R_C = \frac{I_o}{2VT} U_d R_C \rightarrow \text{The diff. output is a function of } I_o.$$

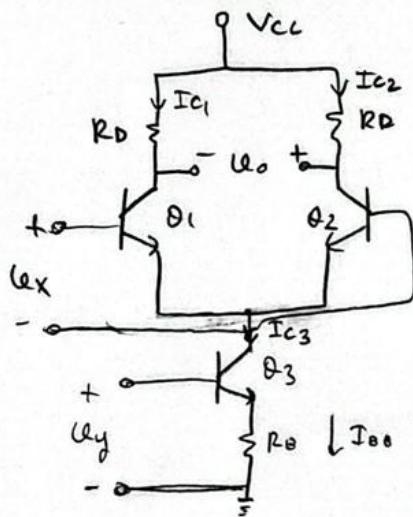
If I_o varies,
 g_m changes \Rightarrow U_o changes
main idea of Gilbert cell.

Figure 3: DC characteristics and small signal differential gain in differential mode

The main idea of the analog multiplier relies on the fact that the transconductance parameters of the BJTs (g_m) is a function of I_Q , in other words, the tail current in the emitter nodes of the BJTs. This results in the output voltage v_o is also a function of I_Q . It should be noted that the two BJTs should be symmetrical (their current gain β and their base-to-emitter turn on voltages $V_{BE(ON)}$ should be the same) so that their collector currents can be the same.

Using this fact, the next step is to variate g_m , which will be achieved by variating I_Q with another BJT connected to the circuit. This implementation is known as a **single balanced cell**:

Variation of g_m 's :



$$u_o = g_m \cdot R_L u_x$$

depends on $I_{C1,2}$

If u_y is sinusoidal:

$$I_{C3} = \underbrace{I_C}_{\substack{\text{Coming} \\ \text{from} \\ V_{B3} \\ (\text{bias voltage})}} + \underbrace{i_{C3}}_{\substack{\text{Coming from} \\ u_y (\text{sinusoid})}}$$

$$i_{C3} = g_{m3} \cdot \underbrace{u_{be3}}_{\substack{\text{from model} \\ \text{s.s}}} = g_{m3} \cdot u_y \quad (\text{s.s})$$

$$\Rightarrow I_{C3} = I_C + g_{m3} u_y$$

$$\text{and } I_{C1} = I_{C2} \approx \frac{I_{C3}}{2} = \underbrace{\frac{I_C}{2}}_{\substack{\text{Coming} \\ \text{from a D.C. source}}} + \frac{g_{m3} u_y}{2}$$

large β ,
due to
symmetry

$$\Rightarrow g_{m1} = g_{m2} = \frac{I_{C1,2}}{V_T} = \frac{I_C}{2V_T} + \frac{g_{m3}}{2V_T} u_y$$

$$\Rightarrow u_o = g_m R_L \cdot u_x = \underbrace{\frac{I_C}{2V_T} R_L u_x}_{\substack{\text{Need to} \\ \text{eliminate}}} + \left(\frac{g_{m3} \cdot R_L}{2V_T} \right) u_x \cdot u_y$$

multiplication

Figure 4: Variation of g_m and the output with single balanced cell

It can be seen that a varying current can be achieved by a source variation at the base of Q_3 (denoted by V_y). In the small signal analysis of Q_3 , the collector current of Q_3 becomes dependent on V_y with the transconductance parameter of Q_3 (g_m). This results in a variation of $Q_{1,2}$'s collector currents, and hence the g_m 's and the output voltage v_o , which is now a product of V_x and V_y , along with a term that only depends on V_x . To obtain an AM modulated signal, the only term present should be a product of the two voltages.

The problem is that there exists a term that depends only on V_x . This is the result of implementing a single balanced cell. To eliminate this term which is not the desired multiplication, another differential couple can be added as cross-coupled to the first pair. The collectors of the transistors from different pairs will be connected, along with the bases. Also, to variate the tail currents of these pairs, another differential pair can be added that will variate the g_m 's and with applying a sinusoid to this pair, the output will be a product of the two voltages applied. Figure 5 illustrates this connection.

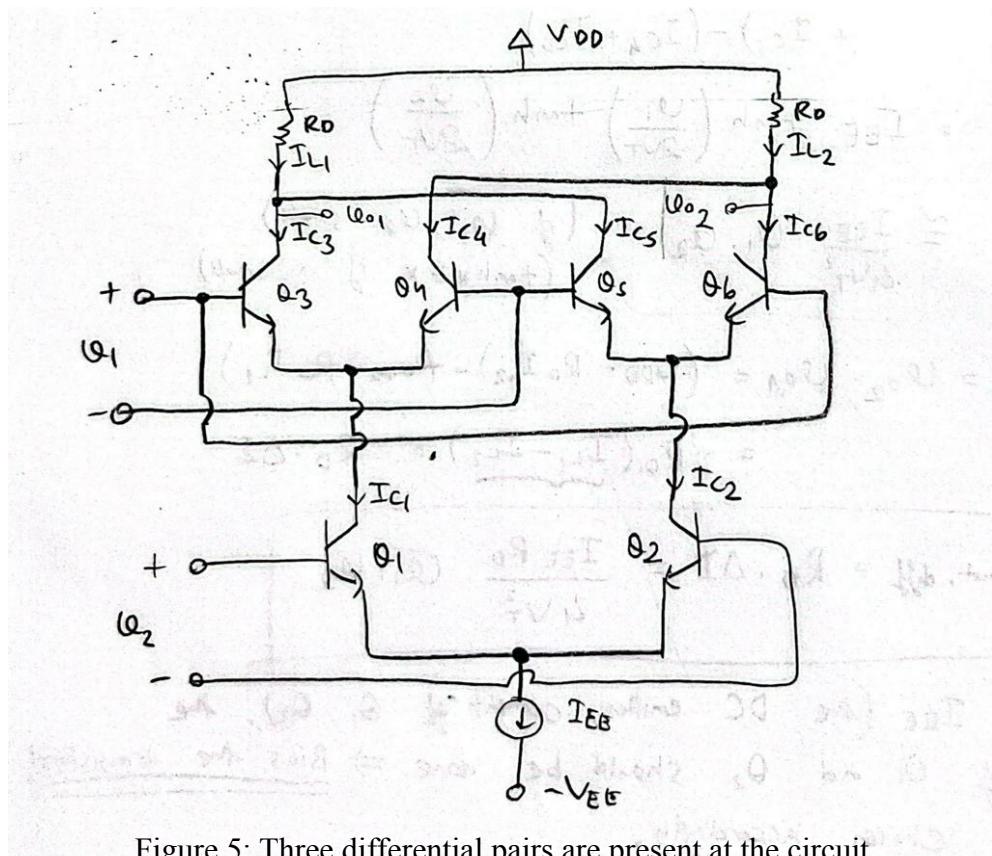


Figure 5: Three differential pairs are present at the circuit

Therefore, the circuit will result in two cross-coupled emitter-coupled pairs in series connection with an emitter coupled pair. Since both inputs are applied to two differential circuits -such that the terms that depend solely on one of the inputs are eliminated and only the product of these two appears at the output- this circuit is now called a **double balanced mixing cell** [3], whose output is also a difference of two nodes. This circuit is actually the fundamental Gilbert cell, which is used as a four quadrant analog multiplier, also as a variable gain amplifier, balanced modulator, frequency mixer and phase detector.

Without drawing the small signal model, the overall output can be found by determining the differential current [4], hence the DC transfer characteristics will be used again:

$$I_{C_3} = \frac{I_{C_1}}{1 + e^{-v_1/V_T}}, \quad I_{C_4} = \frac{I_{C_1}}{1 + e^{v_1/V_T}}, \quad I_{C_5} = \frac{I_{C_2}}{1 + e^{-v_2/V_T}}, \quad I_{C_6} = \frac{I_{C_2}}{1 + e^{v_2/V_T}}$$

$$\text{and } I_{C_1} = \frac{I_{EE}}{1 + e^{-v_1/V_T}}, \quad I_{C_2} = \frac{I_{EE}}{1 + e^{-v_2/V_T}}$$

Combining we have;

$$I_{C_3} = \frac{I_{EE}}{(1 + e^{-v_2/V_T})(1 + e^{-v_1/V_T})}, \quad I_{C_4} = \frac{I_{EE}}{(1 + e^{-v_2/V_T})(1 + e^{v_1/V_T})}$$

$$I_{C_5} = \frac{I_{EE}}{(1 + e^{v_2/V_T})(1 + e^{v_1/V_T})}, \quad I_{C_6} = \frac{I_{EE}}{(1 + e^{v_2/V_T})(1 + e^{-v_1/V_T})}$$

The differential current:

$$\begin{aligned} \Delta I &= I_{L_1} - I_{L_2} = (I_{C_3} + I_{C_5}) - (I_{C_4} + I_{C_6}) \\ &= I_{EE} \tanh\left(\frac{v_1}{2V_T}\right) \tanh\left(\frac{v_2}{2V_T}\right) \end{aligned}$$

$$\approx \boxed{\frac{I_{EE}}{4V_T^2} v_1 v_2} \quad (\text{if } v_1, v_2 \text{ small})$$

(tanh x ≈ x if x small)

$$\begin{aligned} \text{and } U_{\text{out, diff}} &= U_{O_2} - U_{O_1} = (V_{DD} - R_D I_{L_2}) - (V_{DD} - R_D I_{L_1}) \\ &= R_D (\underbrace{I_{L_1} - I_{L_2}}_{= -R_D \cdot \Delta I}) = -R_D \cdot \Delta I \end{aligned}$$

$$\Rightarrow \boxed{U_{\text{out, diff}} = R_D \cdot \Delta I = \frac{I_{EE} R_D}{4V_T^2} (v_1 v_2)}$$

- To obtain I_{EE} , (the DC emitter current of O_1, O_2), the DC biasing of O_1 and O_2 should be done. \Rightarrow Bias the transistors!
- R_D will be chosen accordingly.
- v_1, v_2 should not have too big amplitudes so that $\tanh x \approx x$.

Figure 6: Determining the differential output using the differential circuit

Without going into small signal analysis, only the fact that v_1, v_2 are small AC voltages are used while approximating $\tanh(x) \approx x$. Hence the amplitudes should not be too big (should not be comparable to the large DC signals present in the circuit). The same result can be obtained by drawing the small signal model, where the exponential terms would be linearized (as shown in Fig. 3, but with more terms present).

I_{EE} , which directly determines the gain and therefore the overall output, is essential since it will make the differential pairs operate. The term I_{EE} is essentially the sum of DC emitter currents of Q_1 and Q_2 . Due to the lack of current source in the lab, one can bias these transistors with DC voltages so that they generate DC emitter currents, and their sum will be the I_{EE} that determines the overall gain. Also, R_D can be picked so that the gain is as desired, also to observe the output easily on hardware (a very small output would be hard to observe).

As a last step, therefore, all the six transistors must be biased to ensure they are operating in forward active region. Since only one positive power supply is allowed in the project, the transistors should be connected to a single V_{DD} with a resistive network, which will essentially function as a voltage divider [5]. The network should provide voltage from one voltage source to all six BJTs, which will make the circuit considerably more complex, and will require a large number of biasing resistors.

The biasing resistors should not be chosen too small so that the BJTs don't move into SAT region, also the total current drawn from the power supply does not exceed the limit (200mW power consumption). Hence they are chosen in the 2.2 - 4.7 k Ω range. Capacitors are added to various locations, primarily to separate the DC bias voltage and the AC voltages, to eliminate DC components at the output and also to stop the DC current going into the AC signal generator. They are chosen as a considerably large value (0.1 μ F) so that they can be considered short circuit in AC. With the resistor and capacitor values chosen and added, the overall circuit is shown in Figure 7.

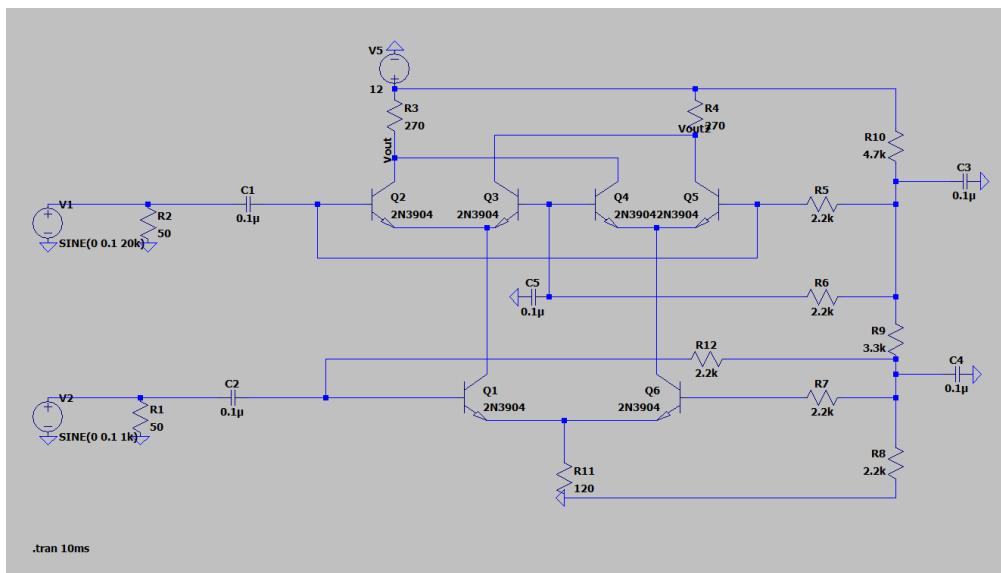


Figure 7: The overall circuit design

At the differential output ($V_{out2} - V_{out1}$), the multiplied signal should be AM modulated [6], which is shown in Figure 8.

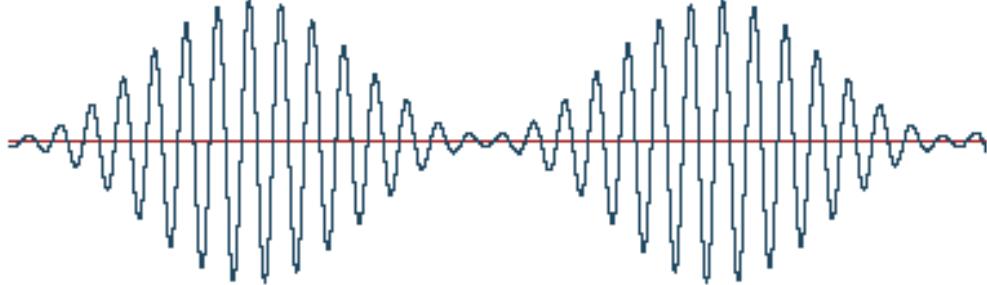


Figure 8: Example of an AM modulated signal [6]

This curve is the multiplication of two sine/cosine functions. Since the resulting signal will be a multiplication of two sinusoidal signals, for example with amplitudes A_1 , A_2 and frequencies f_1 , f_2 , using the cosine multiplication formula [7]:

$$\cos(a)\cos(b) = \frac{1}{2} (\cos(a + b) + \cos(a - b))$$

the output can be expressed as:

$$v_{out} = K \times v_1 \times v_2 = K \times A_1 A_2 \cos(2\pi f_1 t) \cos(2\pi f_2 t)$$

$$v_{out} = \frac{K \times A_1 A_2}{2} (\cos(2\pi(f_1 + f_2)t) + \cos(2\pi(f_1 - f_2)t))$$

where K is the overall gain of the circuit found previously. In other words, the frequency content (spectrum) of the output will include the sum and the difference of the multiplied signals' frequencies. When the Fourier transform (FFT) of the output is taken with the oscilloscope's MATH menu, the sum and difference of the frequencies should be observed as a harmonic in the frequency domain.

Overall, with the circuit implemented and when two sinusoidal signals with 1 kHz and 20 kHz frequencies are applied, the output should be AM modulated, and the harmonics (frequency content) should be observed at 19 kHz (difference of the frequencies) and 21 kHz (sum of the frequencies). The frequency spectrum will indicate whether the modulation is successful or not.

b. Implementation and Results

i. Software Implementation

The digital representation of our analog multiplier involves modeling the behavior of the Gilbert cell, differential amplifiers, and transistors within the LTspice. The software implementation stage involves verifying the viability of biasing strategies, examining the impact of resistor and capacitor values, and ensuring that the circuit operates within the specifications. The implemented circuit with the final chosen values is shown in Figure 9.

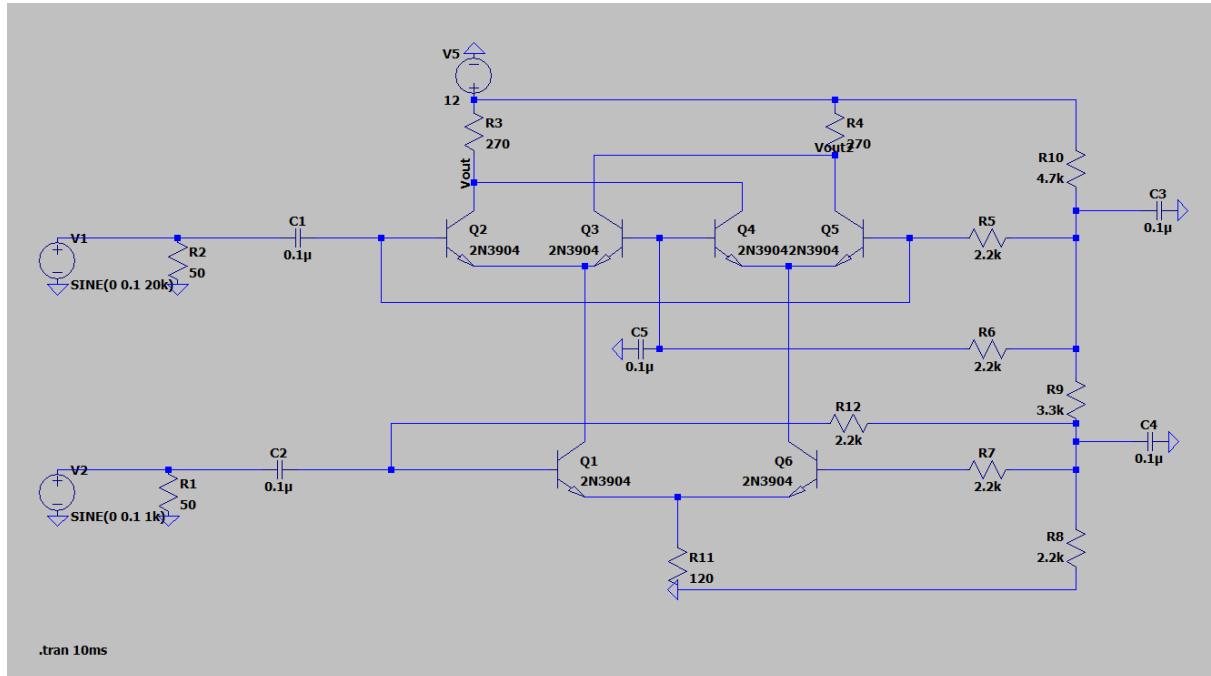


Figure 9: Analog Multiplier Circuit Software Implementation

We used 0.1 Vpp sine wave for each input 1kHz and 20 kHz for V_2 and V_1 respectively and 12 V DC for biasing. Two sided output model is used hence we simulated them separately and found their difference.

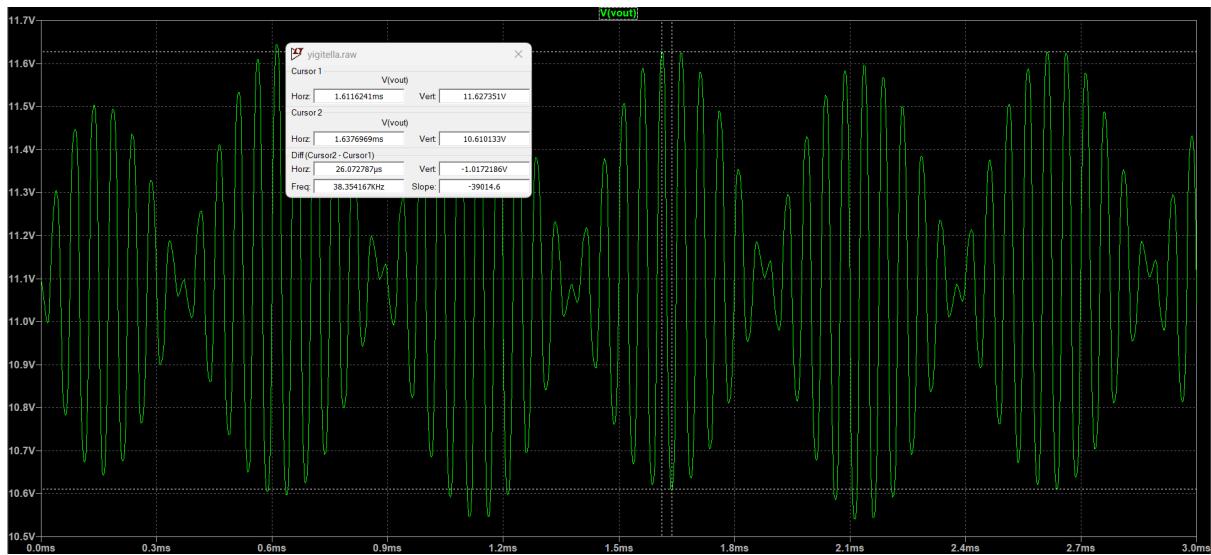


Figure 10: Output 1 of Analog Multiplier

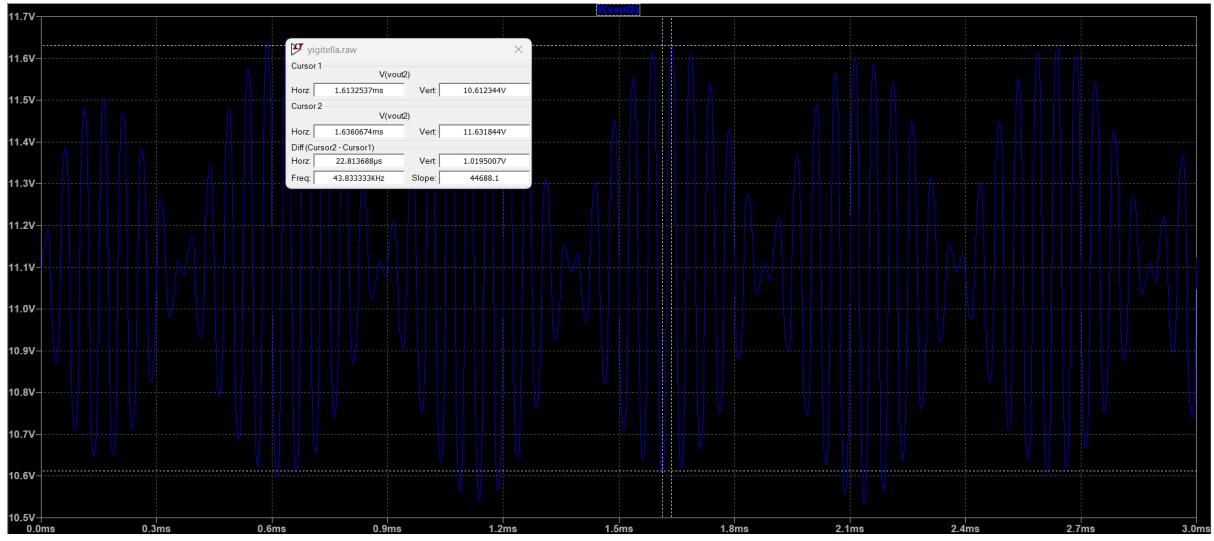


Figure 11: Output 2 of Analog Multiplier

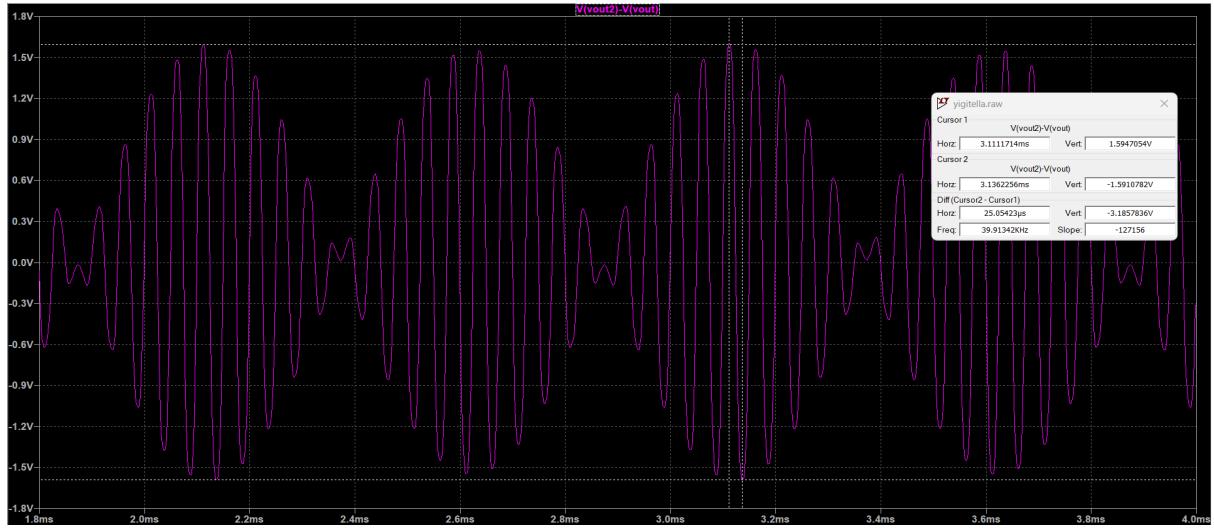


Figure 12: Difference of Output 2 and Output 1 of Analog Multiplier

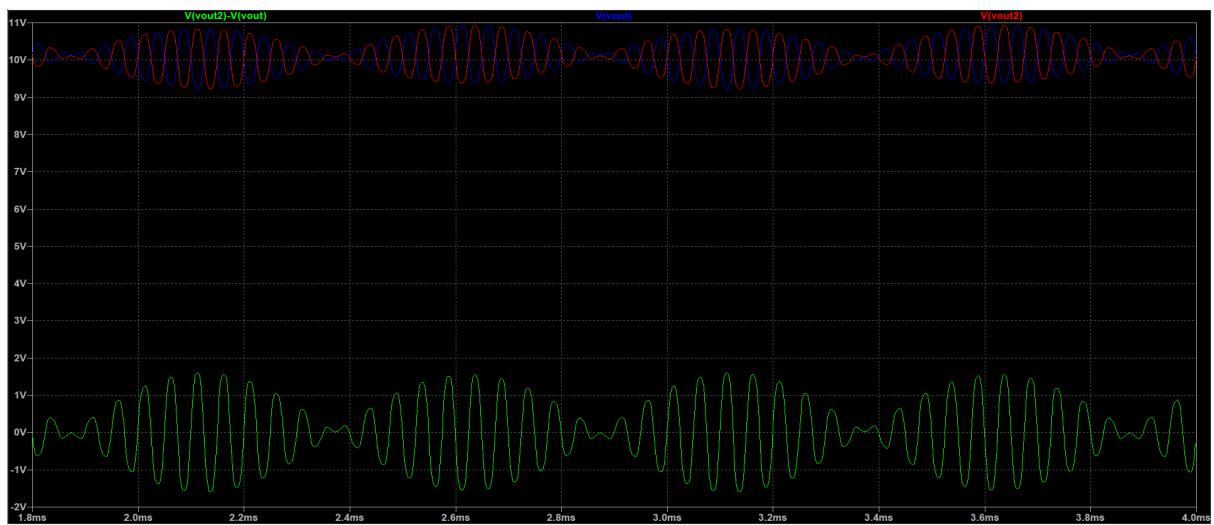


Figure 13: All Outputs Together

As it can be seen from Figures 10 to 13 our LTspice model outputs an AM modulated signal.

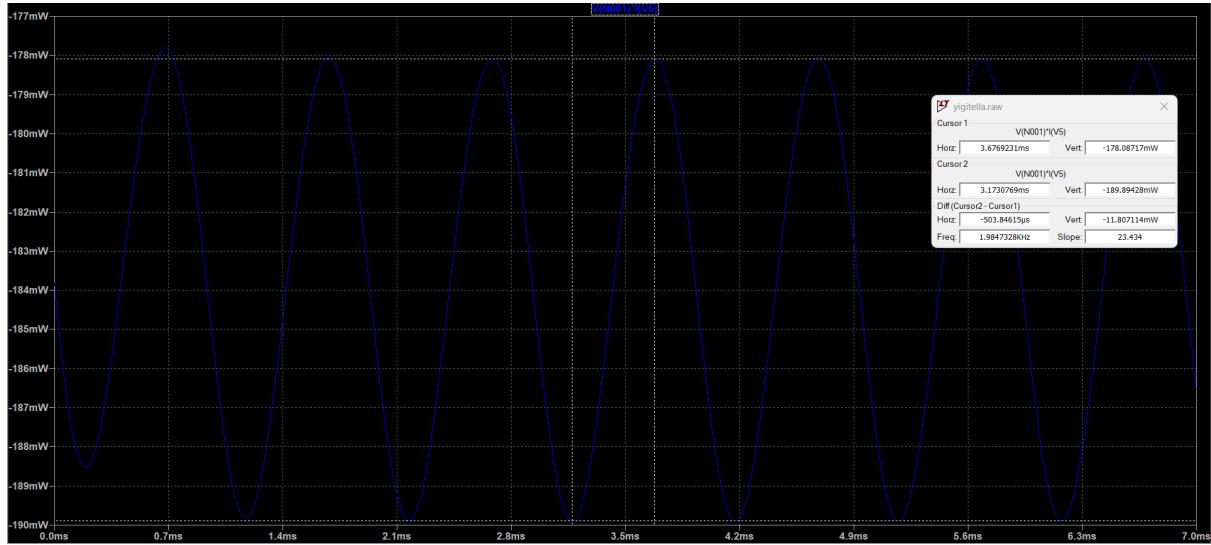


Figure 14: Power Consumption of the Circuit

As it can be seen from Figure 14 our LTspice model has power consumption around 180 mW which is lower than 200 mW as specified.

To check if our simulation is working we have calculated the K values of the formula down below:

$$v_{out} = K \times v_1 \times v_2$$

where $v_{1,2,out}$ are the amplitudes of the input and output voltages. If the simulation is working K values should be constant for different input voltages.

$v_1(mV)$	$v_2 (mV)$	K
10	10	296.2
20	10	296.6
20	20	294.5
30	20	290.7
30	30	285.4
50	50	277.9
60	60	270.4
80	80	262.9
100	100	252.3
200	100	241.6
200	200	226.9
300	200	210.4
300	300	187.5

Table 1: K values according to simulation

There is no such one single K value because for higher input voltages more loss is introduced by the circuit so that gain decreases more. As evident from the table, the rate of change in the values of K experiences a notable shift, particularly noticeable in the transition from 200-100 to 200-200, where we see the start of distortion at the top and bottom. This is caused by the fact that as the input voltage gets too big, it can make the transistors move into the SAT region due to the variation at the base that is not negligible.

ii. Hardware Implementation

The physical setup involves constructing the analog multiplier circuit on a breadboard, arranging components, and establishing connections based on the circuit diagram developed during the software analysis. The implemented circuit is shown in Figure 15.

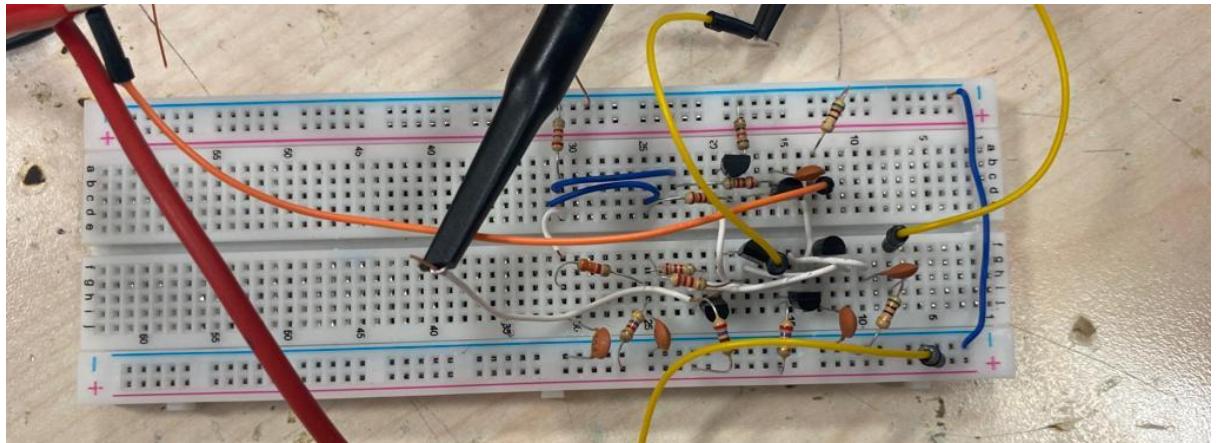


Figure 15: Hardware Implementation of the Analog Multiplier

We used 0.1 Vpp sine wave for each input 1kHz and 20 kHz for V_2 and V_1 respectively and 12 V DC for biasing as in the software part (see Figure 16 and Figure 17).



Figure 16: Input Voltage Values



Figure 17: 1kHz for V_2 and 20 kHz for V_1

As seen from the DC voltage supply, the circuit draws 15 mA current, which meets the specification of “Power consumption should be less than 200 mW.” $0.015 \times 12 = 180$ mW. The current is not smaller than 10 mA, but it is reasonable since we used 12 V for biasing, which is greater than 10 V.

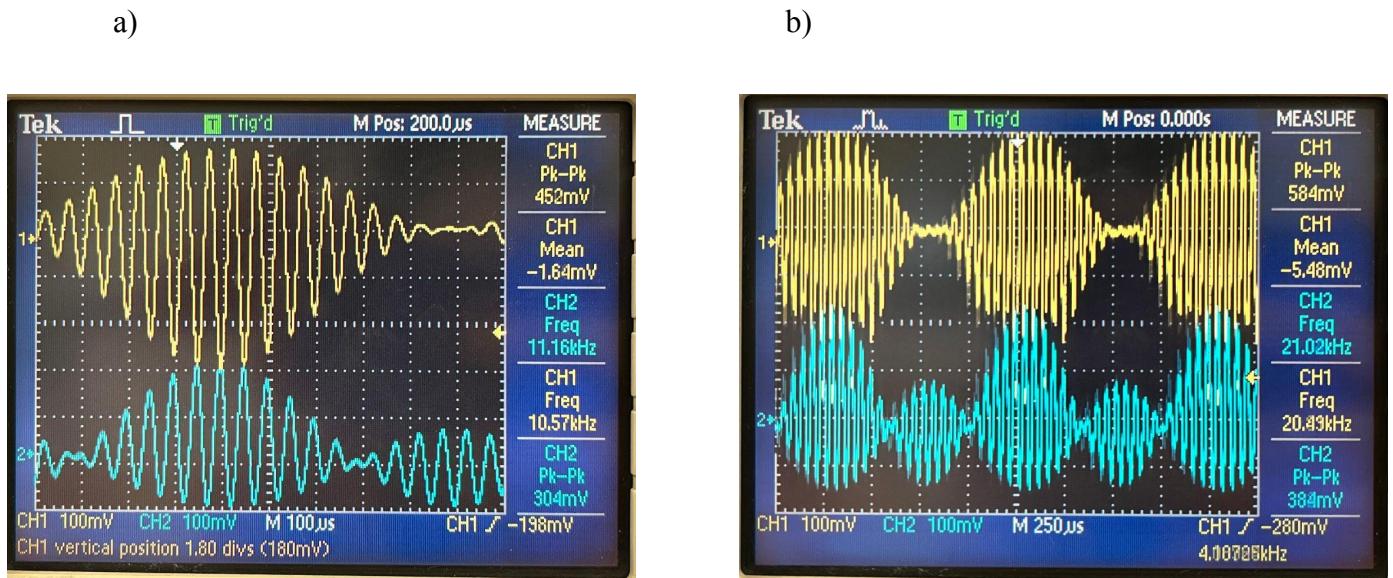


Figure 18: $V_{out,1}$ in yellow, $V_{out,2}$ in blue a) 100 μ s b) 250 μ s

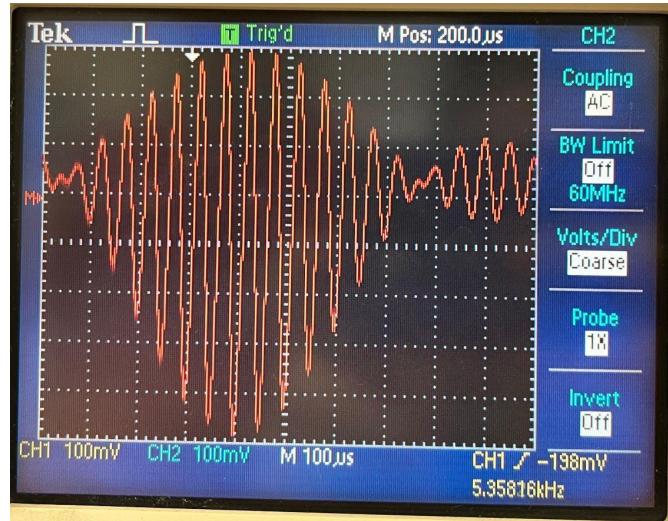


Figure 19: V_{out} of Analog Multiplier

$v_{in1}(mV)$	$v_{in2}(mV)$	$v_{1pp}(V)$ Simulation	$v_{2pp}(V)$ Simulation	$v_{1pp}(mV)$ Hardware	$v_{2pp}(mV)$ Hardware
100	100	1.02	1.02	584	384

Table 2: Comparison of Amplitudes

The observed decrease compared to the software arises from the internal resistances of the hardware cables, variations in the beta values of the BJTs, and non-ideal circuit components. Also the large number of BJTs used in the circuit increases the risk of mismatching, whereas for a differential amplifier BJTs should be matched for an equal current distribution, so that we can proceed with the calculations in the theoretical analysis part.

Looking at Figure 19 we see an AM-modulated signal. Its shape is distorted, i.e one cycle has lower amplitude compared to the other's, from what we simulated in Figure 12. This can be caused by:

- Variations in the characteristics of individual transistors, even if they are the same type, can lead to mismatches. This affects the symmetry of the circuit, which distorts the output.
 - Distortion of symmetry can introduce harmonics and unwanted signal components, leading to signal distortion.
 - Distortion in symmetry introduces nonlinearity, which impacts the linearity of the multiplier's response to input signals. For the previous calculations, we made approximations assuming symmetry (in g_m 's for example), if symmetry is not achieved the approximations and linearizations don't hold.
 - Mismatch also causes the tail current not being equally distributed to the BJTs, causing difference in their g_m 's, and it leads to a gain difference between two different cycles.
- The resistors used in the circuit have values that deviate significantly from their specified values, which affects the biasing.
- Fluctuations or noise in the power supply impact the stability of the circuit.
- If the biasing of the transistors is affected by variations in operating conditions, it leads to asymmetric amplification.

Lastly, we have checked the FFT of the resulting signal to check if the circuit does the multiplication. Hence we expect spikes at 20-1 kHz and 20+1 kHz.

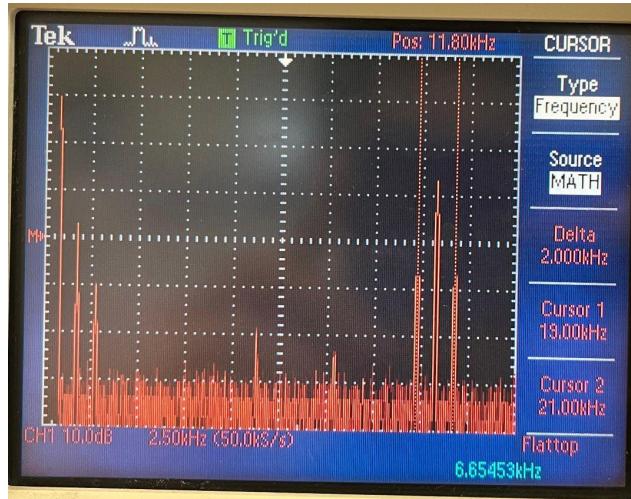


Figure 20: FFT Response of the Circuit

As it can be seen from Figure 20 we see spikes at expected frequencies hence we can conclude the circuit works as desired.

III. Conclusion

The aim of the project was to implement an analog multiplier, whose output should be an AM modulated signal, i.e the multiplication of two sine waves. The power consumption should be under 200 mW. Using the concepts we learned in the course like the differential amplifier, we were able to implement a circuit with npn BJT transistors which achieves this. The circuit is essentially a Gilbert cell, the most commonly used multiplier involving a double-balanced mixing cell as required in the conditions. A voltage divider network is also added to ensure the transistors' operation.

We first implemented the circuit on software. The results were successful, in terms of observing an AM modulated output and not exceeding the power consumption limit. The hardware implementation was more challenging, since the number of BJTs made it hard to implement. The number of BJTs and their variations also caused a slight distortion in the output, even though the output is still an AM modulated signal. Despite encountering waveform distortion in the hardware output, due to device mismatch, resistor tolerances, and stability concerns; our FFT analysis demonstrated successful multiplication with expected spikes at specified sum and difference of the frequencies (19 kHz and 21 kHz). Power consumption remained within specified limits, affirming the circuit's efficiency. Different peak-to-peak voltage amplitude values in hardware and simulation parts can be caused by power loss due to cables or error percentages of components.

Overall, the project was successful both on software and hardware, in which we were able to achieve an AM modulated signal while satisfying the conditions. It was certainly a beneficial and motivating experience for us since we were able to analyze and implement a very common circuit used frequently in today's technology (for example in mixers and phase detectors), by using our knowledge from this course.

References

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