HACETTEPE UNIVERSITY

Department of Electrical and Electronics

ELE313 ELECTRONICS II LABORATORY DESIGN PROJECT

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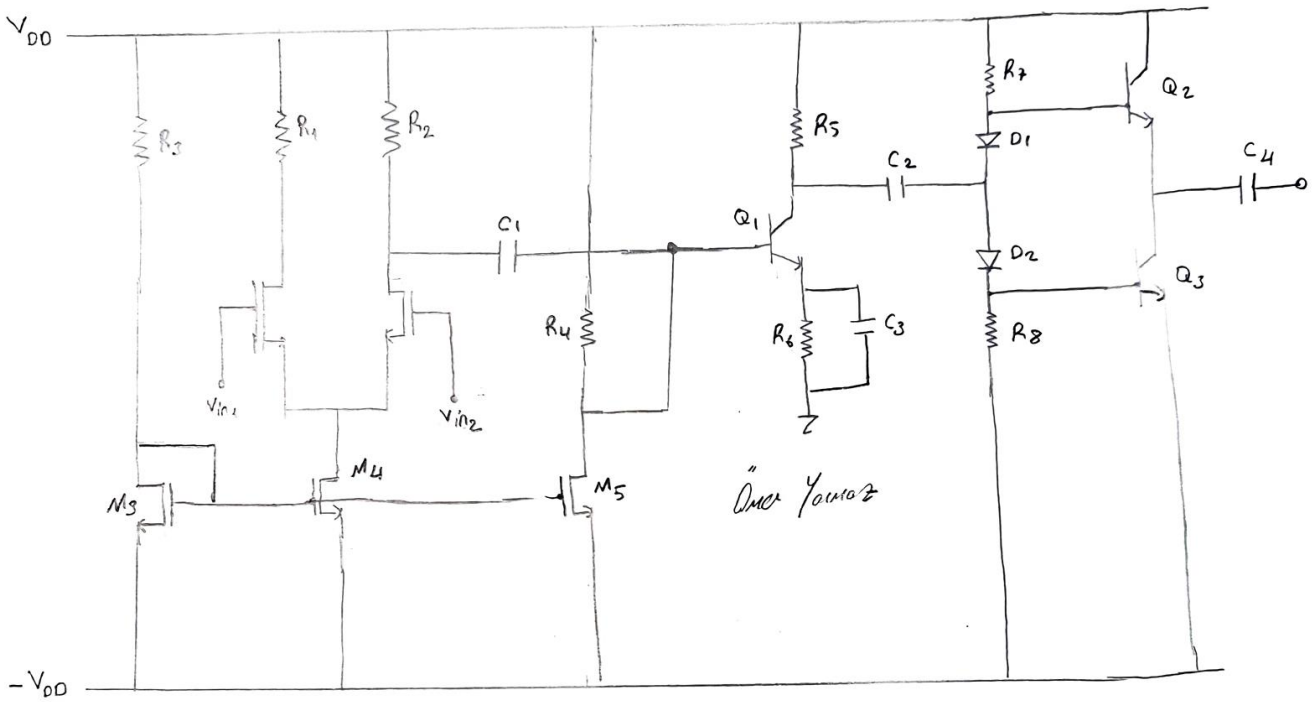
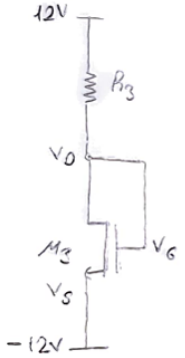
Theorotical Calculations



Current Mirror Design

Current mirror calculations:

Desired current for diff amp: 1.1mA $K_p = 0.78\ mA/V^2$



M_3 model: 2N7000 $V_{TH} = 1.6V$

$12 - I_3 R_3 = V_D = V_G$

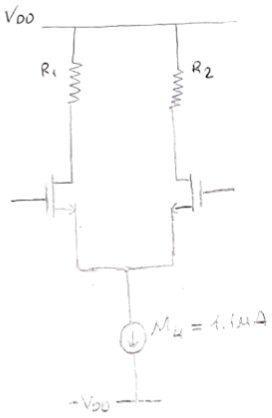
$12 - 1.1mA\, R_3 = V_G$

$R_3 = 20k$

$V_G \cong -10V$

$I_D = \frac{K_p}{2} (V_{GS} - V_{TH})^2$

Diff Amp Design



$V_{TO} = 1.6V$ $\quad K_P = 17\mu A/V^2$

$I_{D1} = 550\mu A$

$A_v = -g_m R_D \Rightarrow g_m = \sqrt{2K_P \cdot I_D} = \sqrt{18.7 \cdot 10^{-3}} = 4.33mA/V$

R_1 choosed as 22k

$A_v = (R_D \| r_o) \times 4.33mA/V$

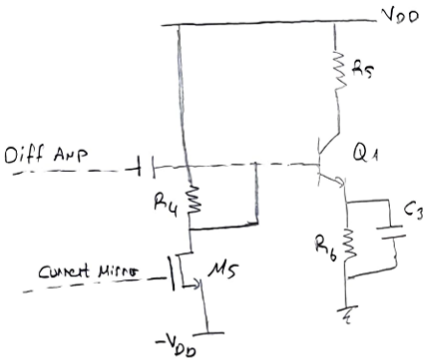
$r_o = \frac{1}{\lambda \cdot I_D} = \frac{1}{0.01 \cdot 0.55} \cong 182k\Omega$

$R_{eff} \cong 19.7k\Omega$

$A_v = g_m \cdot R_{eff} = 4.33mA/V \cdot 19.7k$

$= 85$

Gain Stage Design



I_Q = 1. fourth (Current Mirror)

Gain calculations for Q_1:

R_S is choosed as 1.2k $\quad \beta = 100 \quad V_{BE} = 0.7$

$V_{DD} = 12V$

$I_{C(max)} = \frac{V_{CC} - V_{R6}}{V_{RS}} = \frac{12-1}{1200} = 9.2mA$

$I_{CQ} = \frac{I_{Cmax}}{2} = 4.58mA$

then $I_B = \frac{I_C}{\beta} = 45.8\mu A \approx 46\mu A$

$V_{BE} = V_B - V_E \Rightarrow V_{BE} + V_E = V_B$

$V_{BE} = 1.7V \Rightarrow$ changed to 1.4 V

$R_6 = \frac{1V}{4.63mA} = 216\Omega \cong 220\Omega$

$A_v = \frac{-R_S}{\frac{1}{g_m} + R_6}$

$A_v = 5.44$

$g_m = \frac{I_C}{V_T} = \frac{4.75mA}{0.026mV} = 187.7$

For Bias

$R_4 = 9.k$

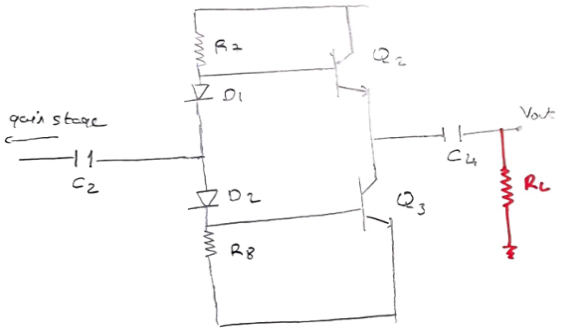
$12V - 9k \cdot 1.14mA = 1.74V$

* In Simulation

When V_B increased to 1.74V

gain increased to 7.5

Output Stage Design



Aim: I wanna deliver at least 100mA to R_L load when it varies 20Ω.

$\beta = 200$ for Q_2 and Q_3

$100mA \cdot 20\Omega = 2V = V_L$

$V_{R7} + V_{R8} = V_{CC} - V_{out}$

$= 10V$

$V_{R7} = V_{R8} = 5V$

$\beta \cdot I_B = I_C$

$200 \cdot I_B = 50mA$ (balanced)

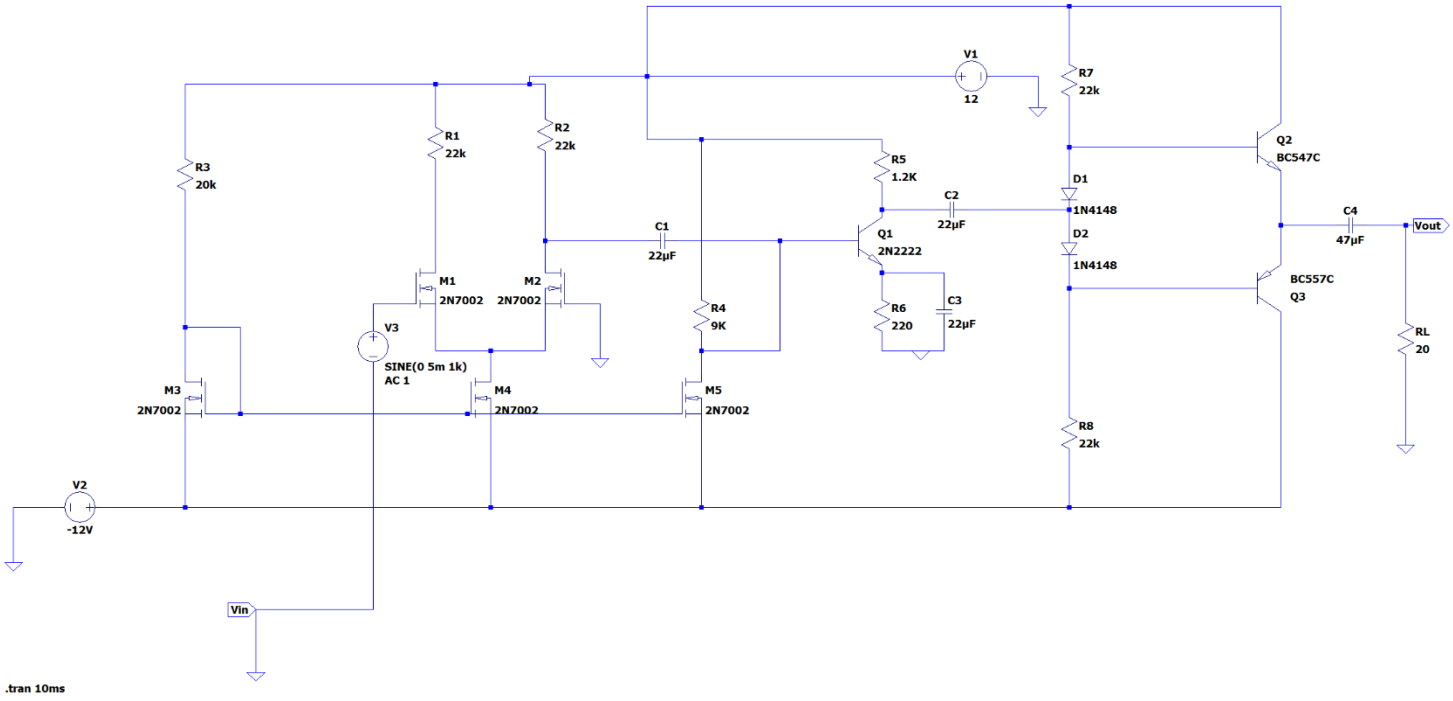
$I_B = \frac{1}{4} mA = 0.25mA$

$I_B = \frac{5V}{R_7}$

$R_8 = R_7 = \frac{5}{0.25mA} = 5 \cdot \frac{1}{4} \cdot 103 = 20k$

R_7 and R_8 choosed 22k

Lt Spice Simulation And Conclusions



Circuit DC Analysis Summary

Operating Point Data

MOSFET Voltages and Currents

Node/Device	Value	Units
Id(M1)	0.000558071	Current (A)
Ig(M1)	-6.07079e-11	Current (A)
Is(M1)	-0.000558071	Current (A)
Id(M2)	0.000558071	Current (A)
Ig(M2)	-6.07079e-11	Current (A)
Is(M2)	-0.000558071	Current (A)
Id(M3)	0.00111614	Current (A)
Ig(M3)	-5.35491e-11	Current (A)
Is(M3)	-0.00111614	Current (A)
Id(M4)	0.00111614	Current (A)
Ig(M4)	-1.5027e-11	Current (A)
Is(M4)	-0.00111614	Current (A)
Id(M5)	0.00111614	Current (A)
Ig(M5)	-1.41865e-11	Current (A)
Is(M5)	-0.00111614	Current (A)

BJT Voltages and Currents

Node/Device	Value	Units
Ic(Q1)	0.00475463	Current (A)
Ib(Q1)	2.30841e-05	Current (A)
Ie(Q1)	-0.00477771	Current (A)
Ic(Q2)	0.000113256	Current (A)
Ib(Q2)	2.05498e-07	Current (A)
Ie(Q2)	-0.000113461	Current (A)
Ic(Q3)	-0.000113286	Current (A)
Ib(Q3)	-1.75769e-07	Current (A)
Ie(Q3)	0.000113461	Current (A)

Source Voltages and Currents :

Node/Device	**Value**	**Units**
V(n001)	12.000000	Voltage (V)
V(n014)	-12.000000	Voltage (V)
I(V1)	-0.00875964	Current (A)
I(V2)	0.00398193	Current (A)
I(V3)	0.000000	Current (A)

Circuit Functional Analysis

Component	Observation
Q1	Active region, amplifies the signal. Ic=4.75 mA, Ib=23.08 µA, indicating proper operation.
Q2 & Q3	Functioning near linear/active region, for signal rectification or balancing.
MOSFETs	Operate in active region; involved in signal amplification.
Resistors	Current values consistent with expected signal pathways; e.g., R5 handles 4.75 mA from Q1.
Capacitors	Minimal current, used for filtering or coupling in signal processing.
Diodes (D1, D2)	Conducting current (520 µA each), used for biasing.
Output (Vout)	Voltage near 0 (-2.3 µV); circuit functions correctly as a low-output signal processor.

Power Consumption Calculations(No-Load):

Source V1 (12V):

Voltage: 12 V

Current: -0.00875964 A

Power: 12 × -0.00875964 = -0.1051 W

Source V2 (-12V):

Voltage: -12 V

Current: 0.00398193 A

Power: -12 × 0.00398193 = -0.0478 W

Total Power Consumption

Total power consumption is the sum of all power sources:

Total Power = -0.1051 W + -0.0478 W + 0 W = -0.1529 W

Small Signal Gain Analysis and Gain Variations:

Simulation of Gain (Under No-Load):

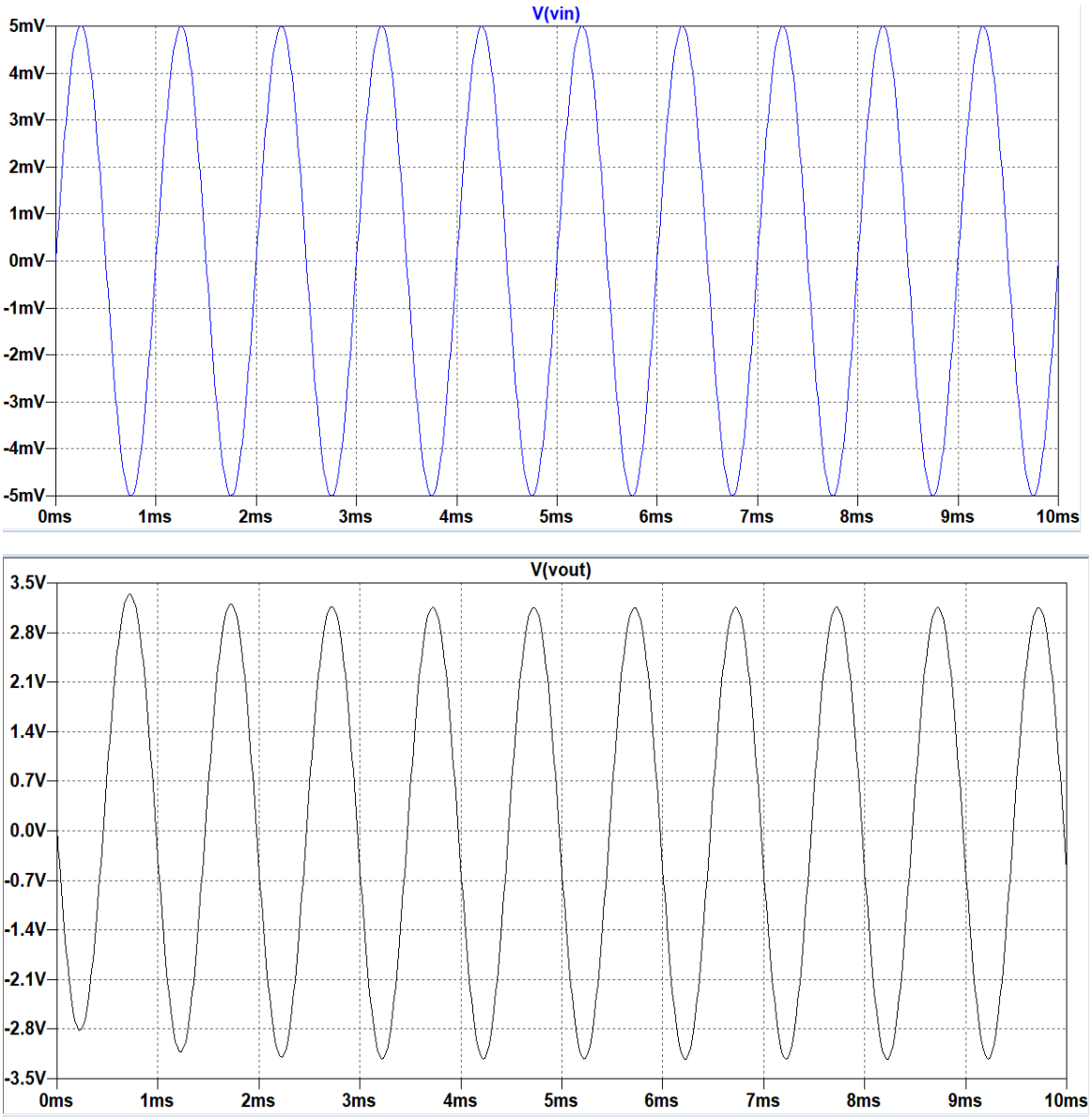


Figure 1.

Gain Calculation:

The gain of a circuit is calculated as the ratio of the output voltage amplitude to the input voltage amplitude:

Gain = Vout_peak / Vin_peak

From the graphs:

Input Voltage (Vin) Amplitude: ±5 mV (peak)

Output Voltage (Vout) Amplitude: ±3.5 V (peak)

Using the formula: Gain = 3.5 V / 0.005 V = **700**

Comment for Gain Calculations:

The simulation(Figure1) shows that the circuit amplifies the input signal significantly, achieving a gain of approximately 700 under no-load conditions. The input sine wave, with an amplitude of ±5 mV, is amplified to an output sine wave with an amplitude of ±3.5 V. This high gain indicates that the circuit operates effectively in its linear region without visible distortion. However, additional analysis is needed to verify whether the gain remains consistent under varying load conditions or higher input signal levels.

Gain Variation via Input Voltage Change:

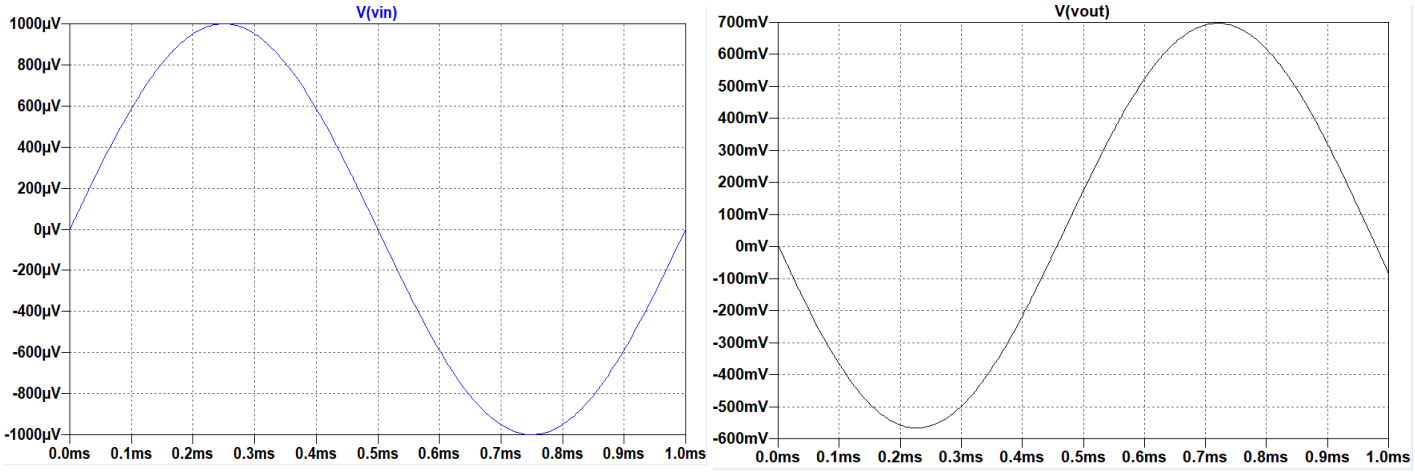


Figure 2

Comment For Gain Variaton with Voltage Change:

The simulation results(**figure 1, figure 2**) show how the circuit behaves under different conditions. In the first set of graphs, the gain remains consistent, as the input signal is a small ±5 mV sine wave, and the output signal is amplified to about ±3.5 V without any visible distortion, indicating the circuit is operating in its linear region. However, in the second set of graphs, as the input voltage increases to ±1 V, the output signal shows signs of non-linearity, with the gain decreasing and potential saturation occurring. This suggests that the circuit's linear operating range is limited, and the input signal must be kept within this range to avoid distortion in the output.

Load Variation:

20Ω load is connected. Vin = 5mV

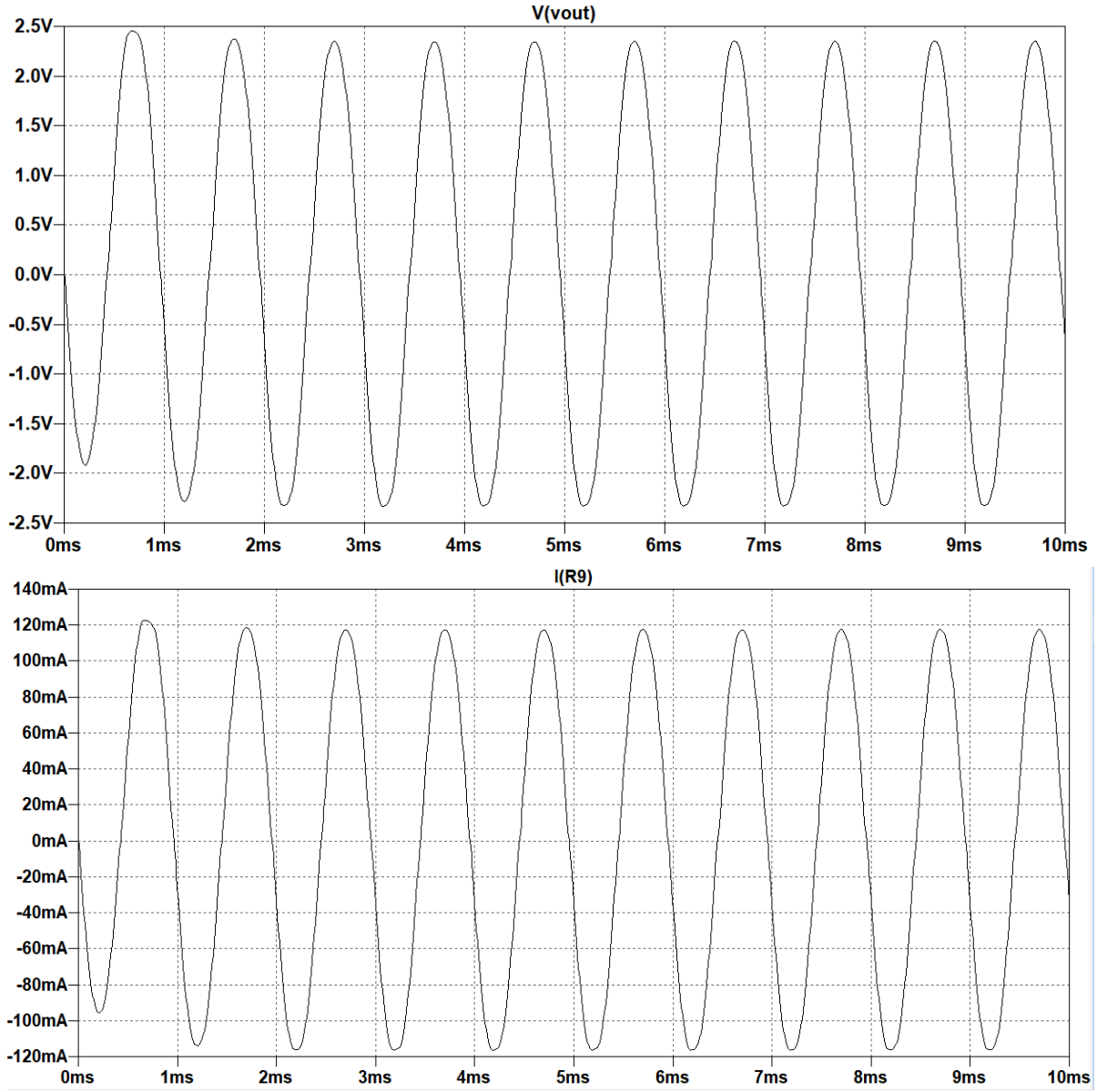


Figure 3

5kΩ load is connected. Vin = 5mV

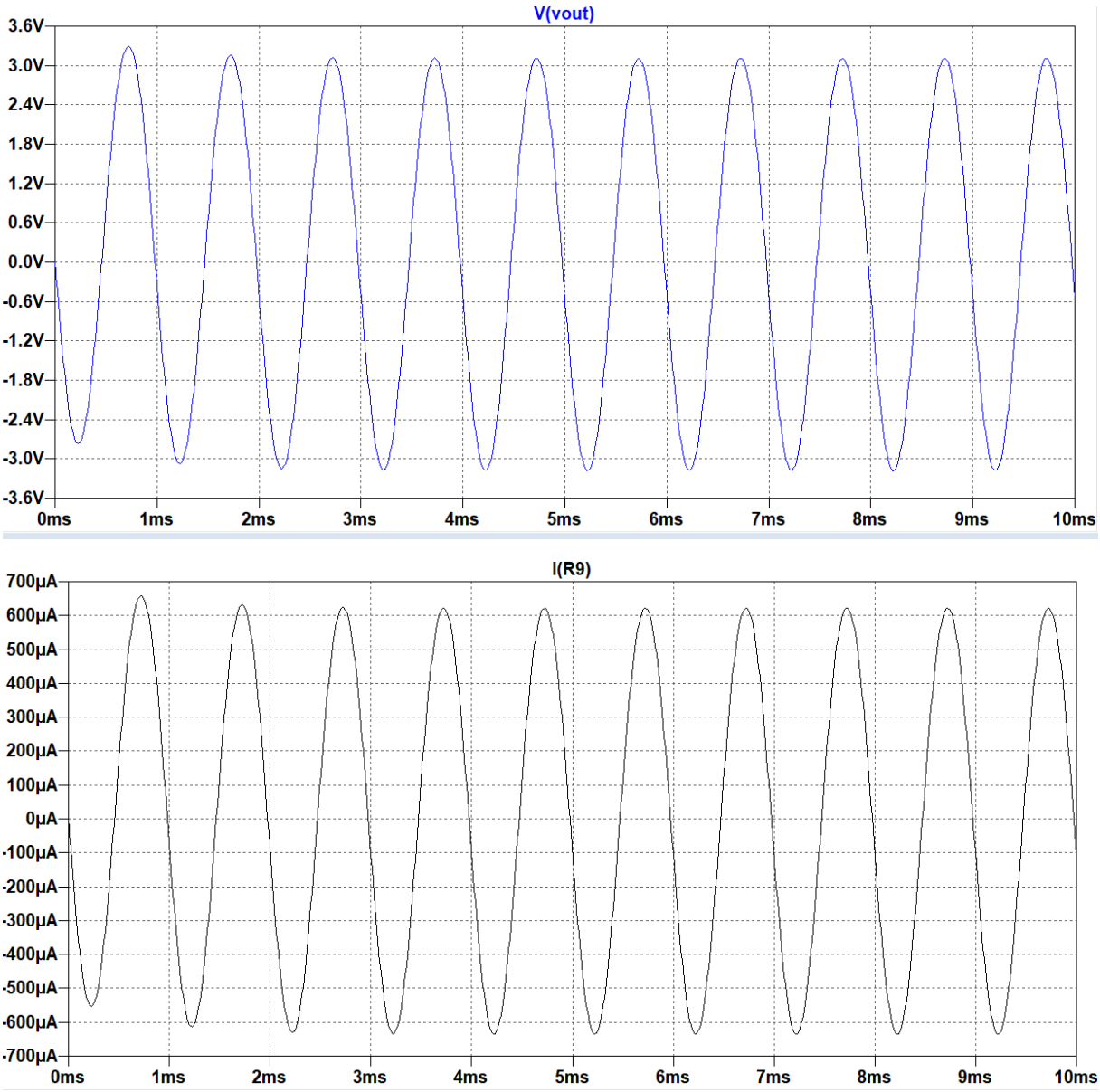


Figure 4

Comment on Load Variation :

The simulation results(**figure 3 , figure 4**) show that the circuit maintains the waveform integrity of the output signal under varying load conditions. With a 20 Ω load, the circuit delivers high current levels (up to approximately 120 mA) without any visible distortion in the output signal. However, the amplitude of the output voltage drops to ±2.5 V compared to the no-load condition, where it was ±3.5 V, indicating a reduction in gain. This drop in gain is expected due to the increased current demand and the associated voltage drop across the internal resistance of the circuit.

In contrast, with a 5 kΩ load, the output signal amplitude remains close to ±3.5 V, with minimal gain reduction and significantly lower current (approximately ±700 µA). These results demonstrate that while the output stage is capable of delivering high currents for low-impedance loads, there is a trade-off in terms of gain. The robust design of the output stage ensures that it can handle significant current demands, making it suitable for low-resistance applications, but the gain performance should be carefully considered when designing for such conditions.

Feedback Resistors:

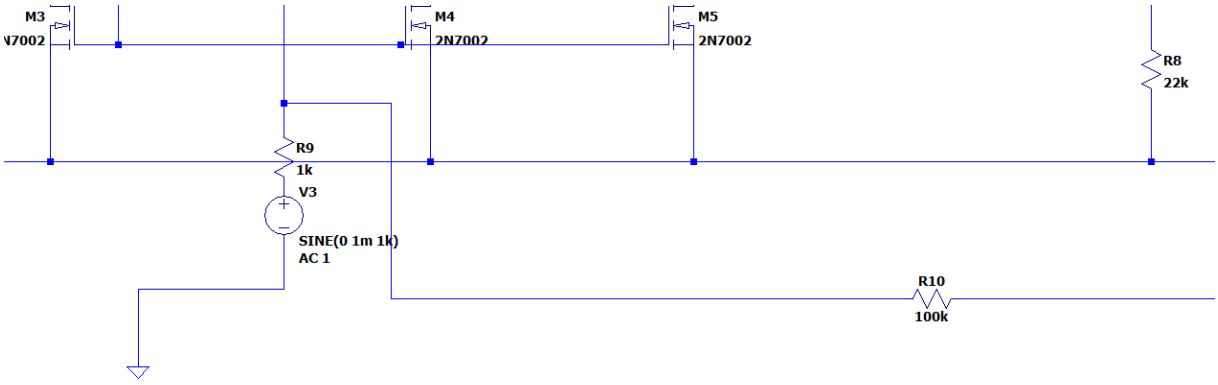


Figure 5

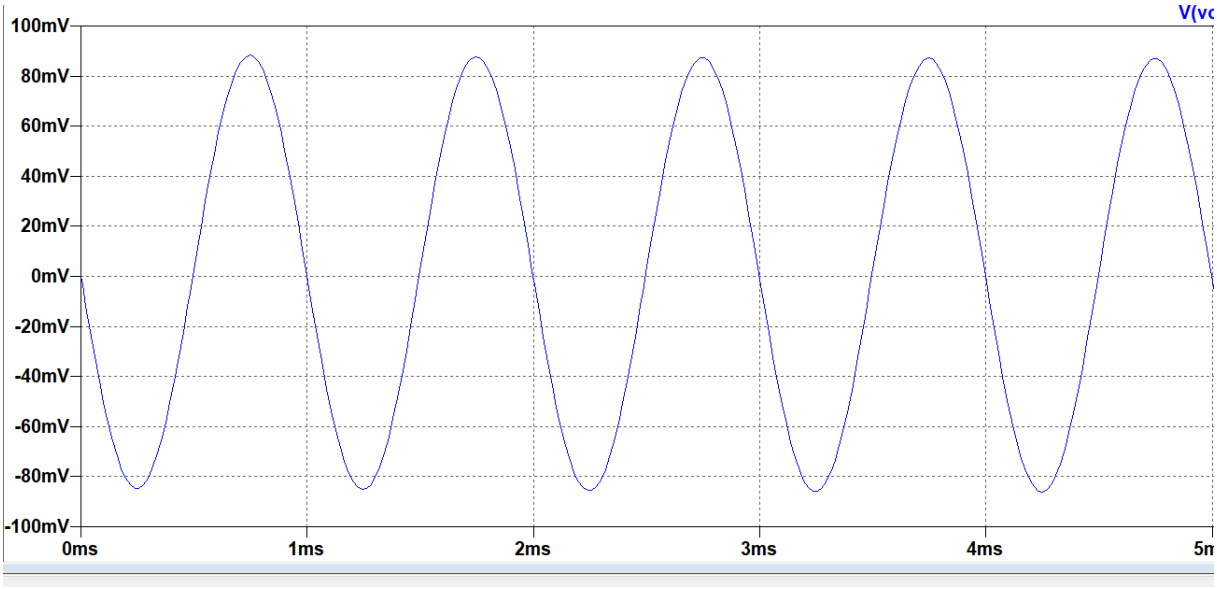


Figure 5

Comment on Feedback:

This circuit is a feedback network connected to an op-amp that I designed and analyzed. The graph shows a clean sinusoidal output signal at 1 kHz with an amplitude of approximately ±100 mV, matching the input frequency. This indicates that the feedback loop is functioning properly and stabilizing the op-amp.

The resistors R9 (1 kΩ) and R10 (100 kΩ) set the feedback ratio, controlling the gain and ensuring stability. The MOSFETs in their linear region, maintaining signal integrity without introducing distortion. The output being in-phase with the input confirms that the circuit is stable and well-designed.

Overall, the circuit performs as expected.

Frequency response analysis with Feedback:

I also analyzed the circuit's frequency response using LTSpice and observed the Bode plot. The circuit appears to function across wide frequencies, as indicated by the datas(Figure 6). To test the bandwidth, I adjusted the frequency of my sinusoidal voltage source and observed that the bandwidth increased. However, as expected, there was a trade-off: the gain decreased as the bandwidth expanded. This is consistent with the gain-bandwidth trade-off inherent to feedback systems.

x = 35.370Hz y = 35.893dB, -189.791°

x = 1.835KHz y = 38.761dB, -157.015°

x = 221.671KHz y = 35.501dB, -194.269°

Figure 6

PSRR and CMRR Calculations:

CMRR

for 1V in V_{in1} and V_{in2}

$$A_{CM} = \frac{30 \times 10^{-3}}{1} = 0.03$$

A_{DM} is 600

$$CMRR = 20 \log\left(\frac{600}{0.03}\right)$$

$$= 20 \log(20000) = 86.02\ db$$

PSRR

$$20 \log\left(\frac{V_{PS,ripple}}{V_{out,ripple}}\right)$$

$V_{PS\,rip} = 0.1$

$V_{out\,rip} = 1.2$

$$20 \log\left(\frac{0.1}{1.2}\right) = -21.58\ db$$

- PSRR value is very low, capacitor gone be added power lines.

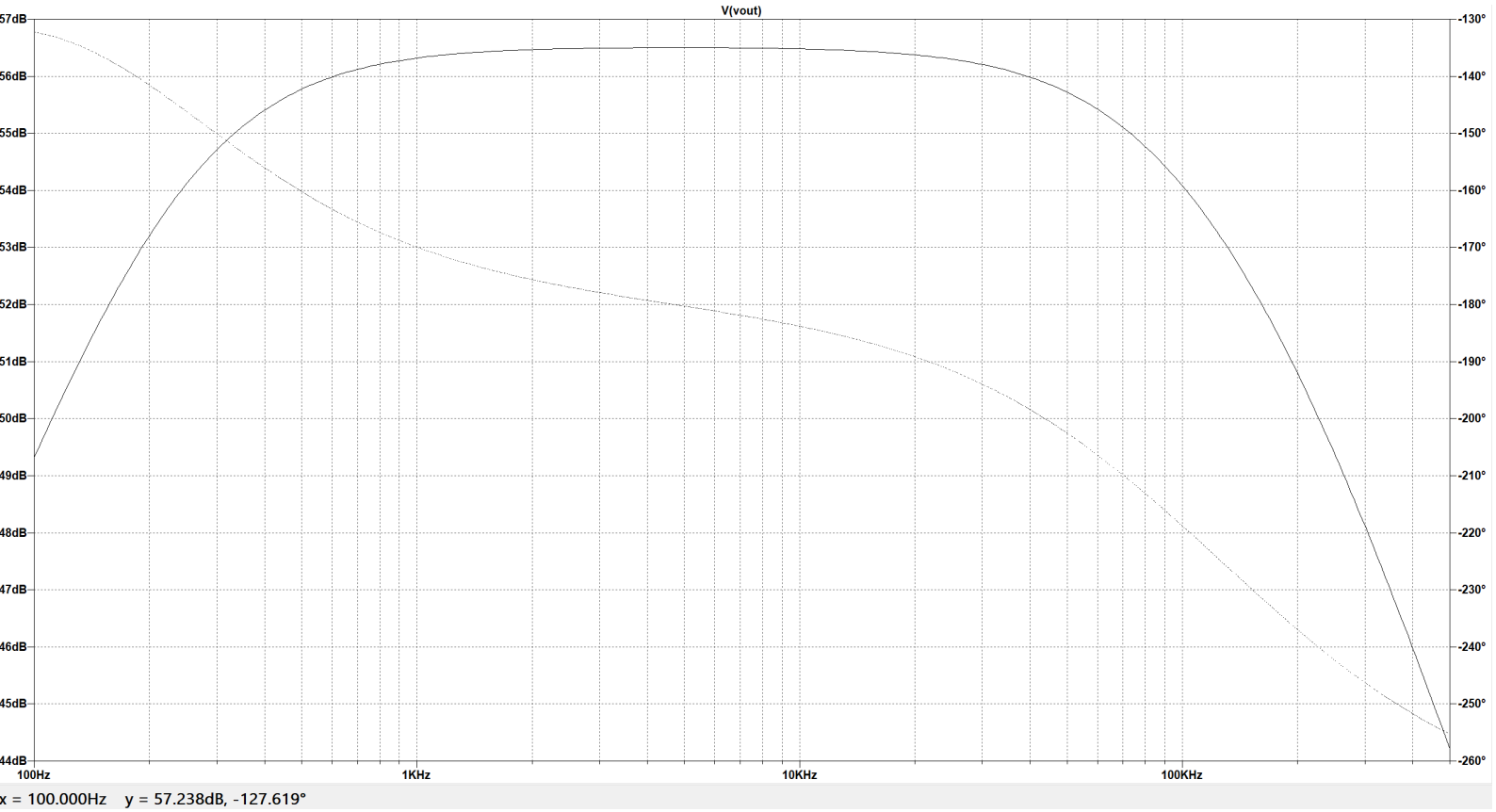
Figure 6

Comment on PSRR and CMRR :

The calculations show a CMRR of 86.02 dB, indicating excellent rejection of common-mode signals, making the op-amp suitable for precision applications. However, the PSRR is low at -21.58 dB, highlighting sensitivity to power supply variations. To calculate CMRR, the differential gain was measured by applying a sinusoidal input to one terminal while grounding the other, and the common-mode gain was obtained using a 1V input to both terminals. PSRR was determined by adding a 0.1V sinusoidal ripple to the power supply (+12V) and measuring the output ripple. The low PSRR suggests adding capacitors to the power supply lines to filter ripples and improve stability, ensuring better performance in noisy environments.

Frequency Analysis

Bode plot:



x = 2.413KHz y = 56.462dB, -135.382°

x = 108.817KHz y = 53.750dB, -162.500°

x = 215.868Hz y = 53.626dB, -163.742°

The provided Bode plot illustrates the magnitude and phase response of the circuit:

1. **Magnitude Analysis**:

   At **215.868 Hz**, the gain is **53.626 dB**, indicating the circuit's low-frequency response where the gain is relatively stable and flat.

   The maximum gain of **56.462 dB** occurs at **2.413 kHz**, suggesting this is the frequency where the circuit operates most effectively in terms of amplification.

   Beyond **2.413 kHz**, the gain gradually decreases, with a significant drop observed at **108.817 kHz**, where the gain is reduced to **53.750 dB**.

2. **Phase Analysis**:

   At **low frequencies (e.g., 215.868 Hz)**, the phase shift is **-163.742°**, indicating that the output signal is slightly lagging the input.

   As the frequency increases to the peak gain at **2.413 kHz**, the phase shift becomes **-135.382°**.

   At higher frequencies (e.g., 108.817 kHz), the phase shift further increases to **-162.500°**, showing significant phase lag due to the circuit's characteristics.

3. **Bandwidth**:

   The circuit operates effectively within a range close to the peak gain frequency (2.413 kHz). Frequencies significantly beyond this point show a reduction in gain, suggesting the bandwidth is relatively narrow.

Comment on frequency response:

The analysis shows that the circuit achieves its maximum gain of 56.462 dB at 2.413 kHz, indicating the optimal operating frequency. The gain remains stable at low frequencies but starts to decrease beyond the peak, which is expected for most amplifiers due to the limitations of the frequency response. The phase shift also increases with frequency, reaching -162.500° at higher frequencies, indicating significant lag. Overall, the circuit performs well within its operational range, but improvements could be considered to extend the bandwidth or reduce phase lag for applications requiring higher frequency performance.

"Challenges and Gains"

During the design and analysis of my circuit, I developed a series of ideas and made iterative improvements based on both theoretical concepts and practical testing. Here is the timeline of my design journey:

Initial Design and Rationale

My initial design for the differential stage utilized an **N-MOS differential amplifier (2N7000)** with a **load P-MOS** instead of a resistor. This decision was motivated by the goal of achieving higher gain and maintaining a compact, efficient design. I aimed to leverage the MOSFET's characteristics for improved linearity and performance compared to traditional resistive loads. However, in the simulation I coludn't achive at least 100 gain, therefore I replaced the load P-MOS with a resistor to simplify the design and improve performance.

In the gain stage, I initially considered using a **Darlington pair** to maximize amplification, but I encountered difficulties in achieving stable operation due to impedance mismatches. To address this, I used commen emitter bjt ampifier and replaced the voltage divider with a **current mirror**, which provided a stable base voltage and ensured better resilience to current variations. This approach, coupled with using a resistor to supply the gain stage, improved the overall reliability of the design.

In the output stage, I designed the circuit with BJTs to handle high current loads while maintaining low output impedance. This decision was driven by the need for a robust output capable of delivering sufficient current to low-resistance loads.

Challenges During Testing and Simulation

Despite resolving some theoretical challenges, I encountered several issues during practical testing:

Issues:

1. The differential amplifier (initially designed with an N-MOS) displayed improper operation on the oscilloscope, with the output resembling the **horizontal projection of a sine wave**. Upon investigation, I attributed this to the lack of a well-defined Id-Vgs relationship for low currents in the 2N7000, as it was designed for higher current applications. During this process, I also researched alternatives like the **BSH103**, which offered better low-current characteristics and lower Vgs thresholds. However, due to availability issues and long shipping times, I was unable to source these MOSFETs. The problem persisted until I replaced the N-MOS with an **NPN transistor (2N2222)**, which retained similar characteristics and resolved the gain issue.
2. For the gain stage, design failed to provide the expected performance due to difficulties in ensuring stability and defecction of BJT's.

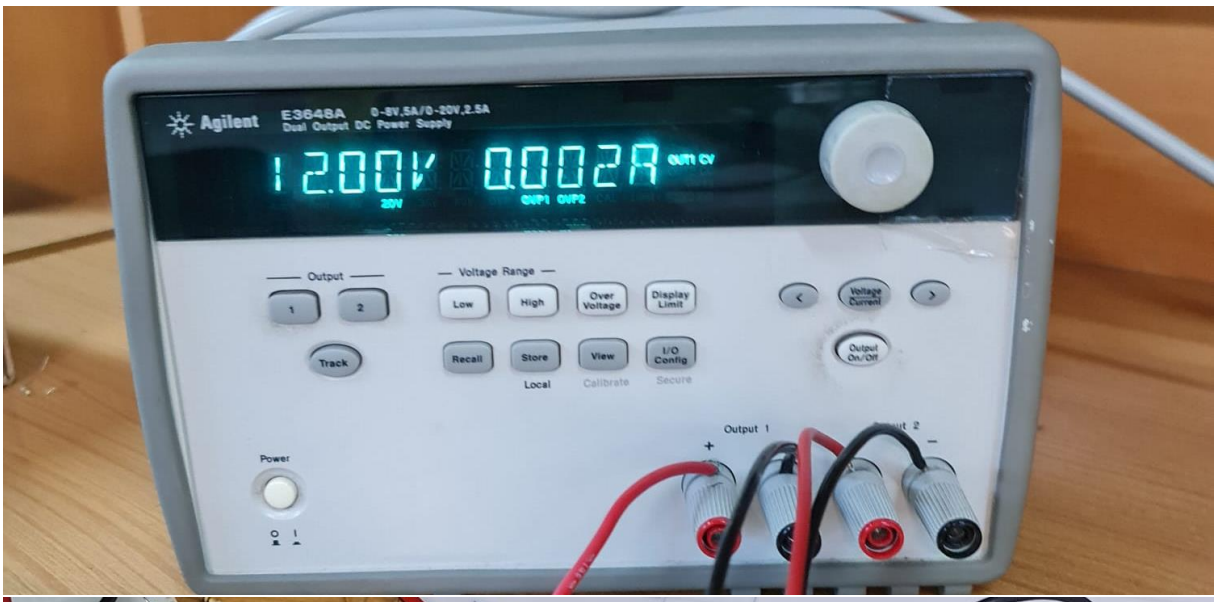
3. In the output stage, designed to handle high currents with BJTs, I observed that the output still displayed the **horizontal projection of a sine wave**, likely due to improper biasing or stage impedance mismatches. While the differential amplifier functioned correctly, the output stage required further refinement to deliver a clean sinusoidal waveform.
4. During the simulation process in LTSpice, I encountered unexpected issues related to the accuracy of the predefined component libraries. Some components within the standard library did not accurately represent real-world behavior, leading to discrepancies between **simulation** and **laboratory** results. Additionally, third-party models used for MOSFETs and BJTs were not thoroughly verified for accuracy, which further contributed to these inconsistencies. For example, certain parameters critical to the differential amplifier's operation, such as characteristics, were either missing or inaccurately modeled. This mismatch likely explains why some designs that appeared functional in simulation performed poorly in practical testing. These insights highlighted the importance of verifying component models before relying on them in simulations and reinforced the need for cross-referencing simulation results with **real-world** measurements.

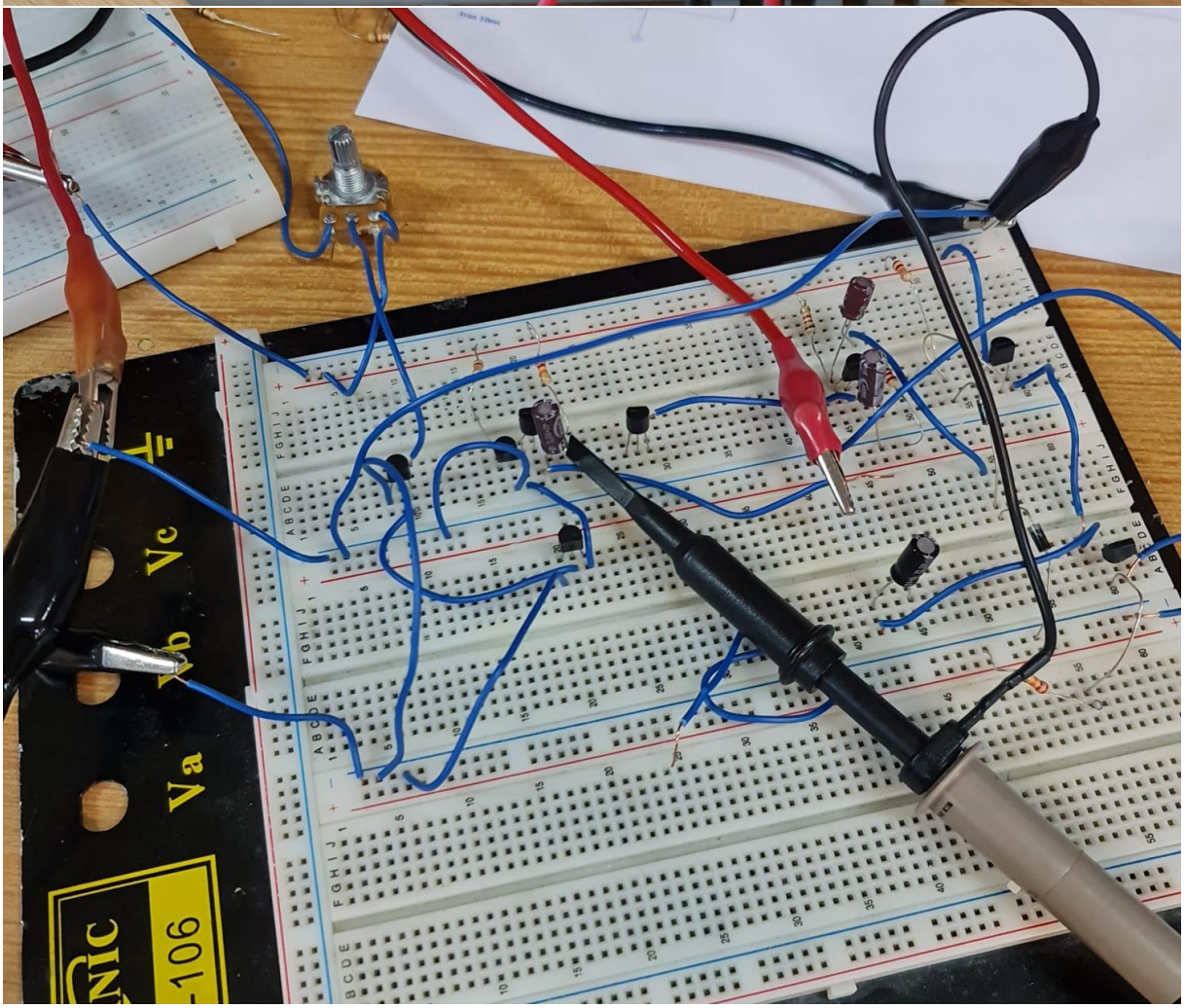
Insights

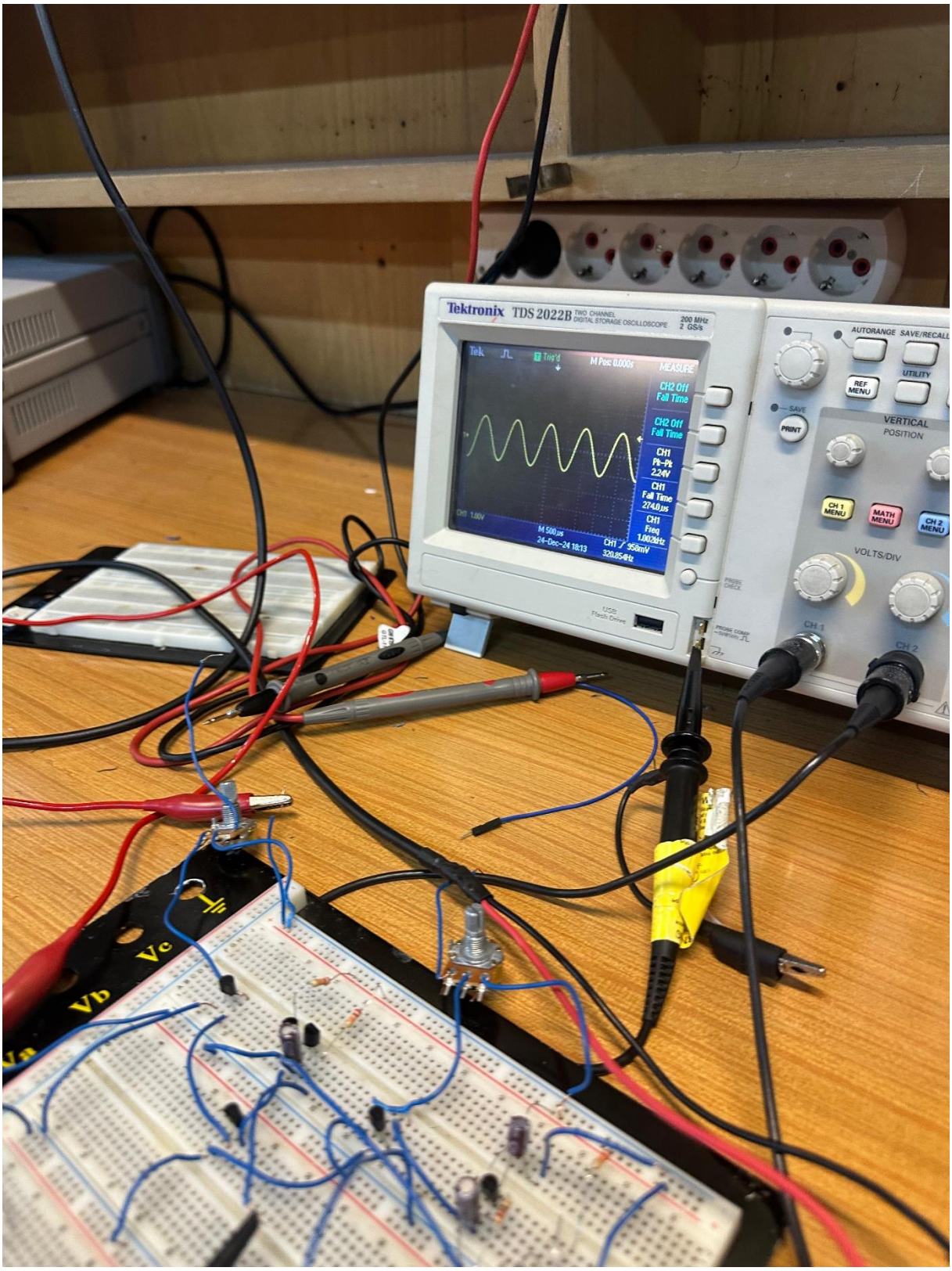
This project was a significant learning experience, showcasing the importance of iterative design and practical testing. In the lab, challenges like transistor failures and time constraints required multiple redesigns and adjustments. Despite these setbacks, the final design operated successfully in simulation and highlighted the potential of a well-thought-out structure.

“Development Journey in Pictures”

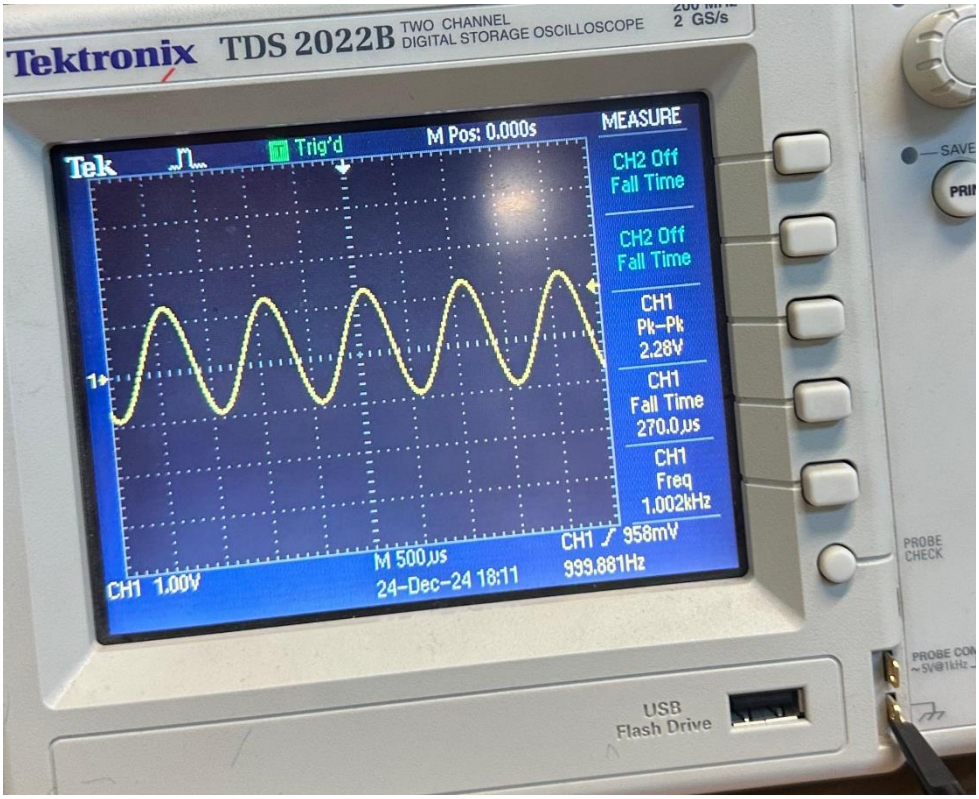
Lab Tests:





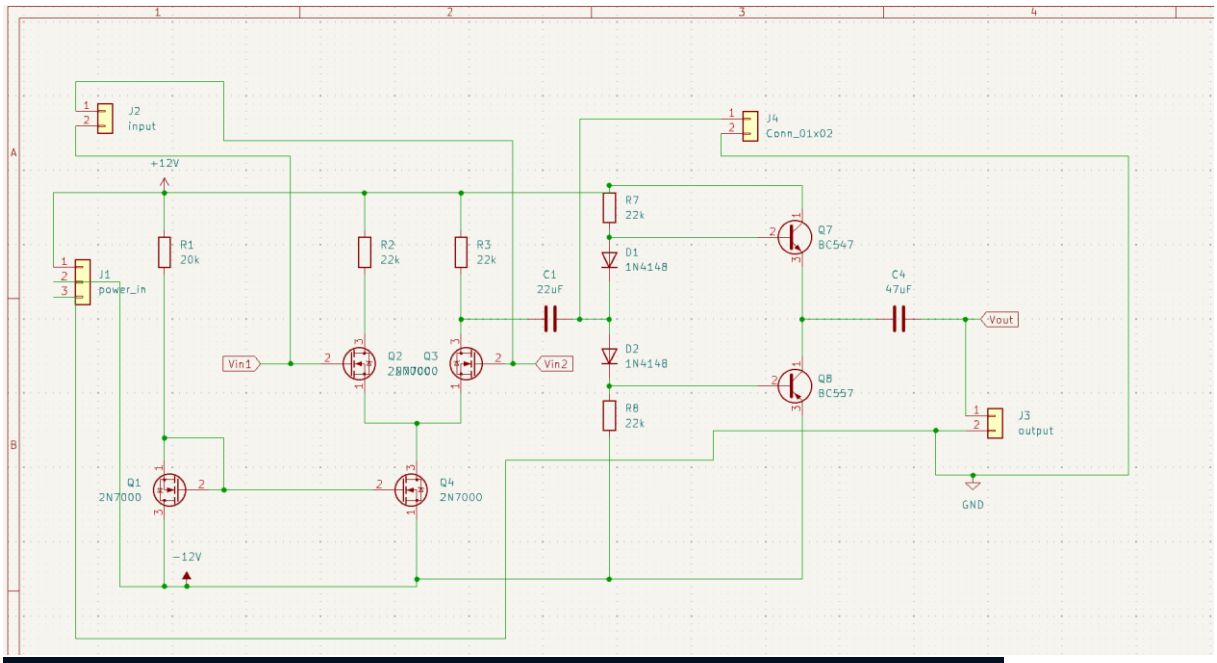

Tektronix TDS 2022B TWO CHANNEL DIGITAL STORAGE OSCILLOSCOPE
200 MHz 2 GS/s
AUTORANGE
SAVE/RECALL
UTILITY
REF MENU
SAVE
PRINT
VERTICAL
POSITION
CH 1 MENU
MATH MENU
CH 2 MENU
VOLTS/DIV
CH 1
CH 2
MEASURE
CH2 Off Fall Time
CH2 Off Fall Time
CH1 Pk-Pk 2.24V
CH1 Fall Time 274.0ns
CH1 Freq 1.0026kHz
M 500µs
24-Dec-24 18:13
CH1 ∕ 958mV
320.854Hz
USB Flash Drive
Vc
Vb

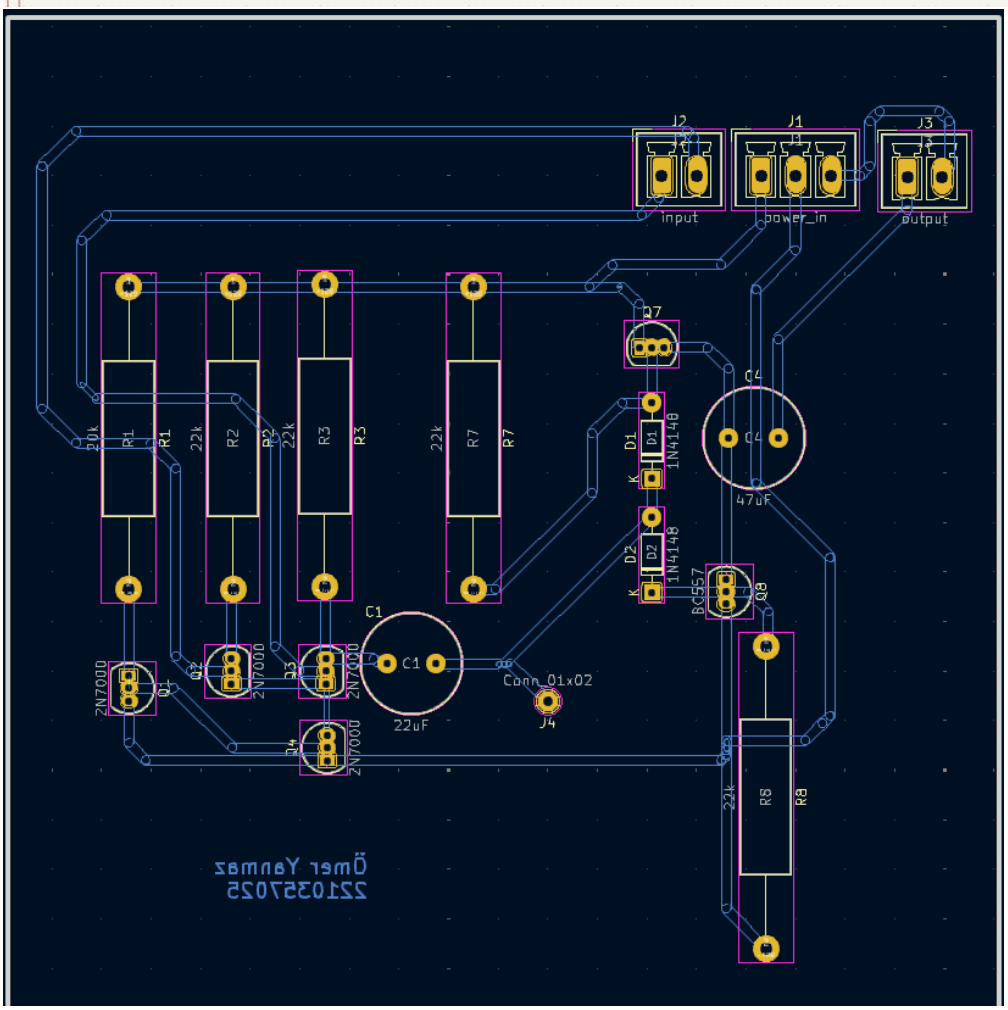
1Khz



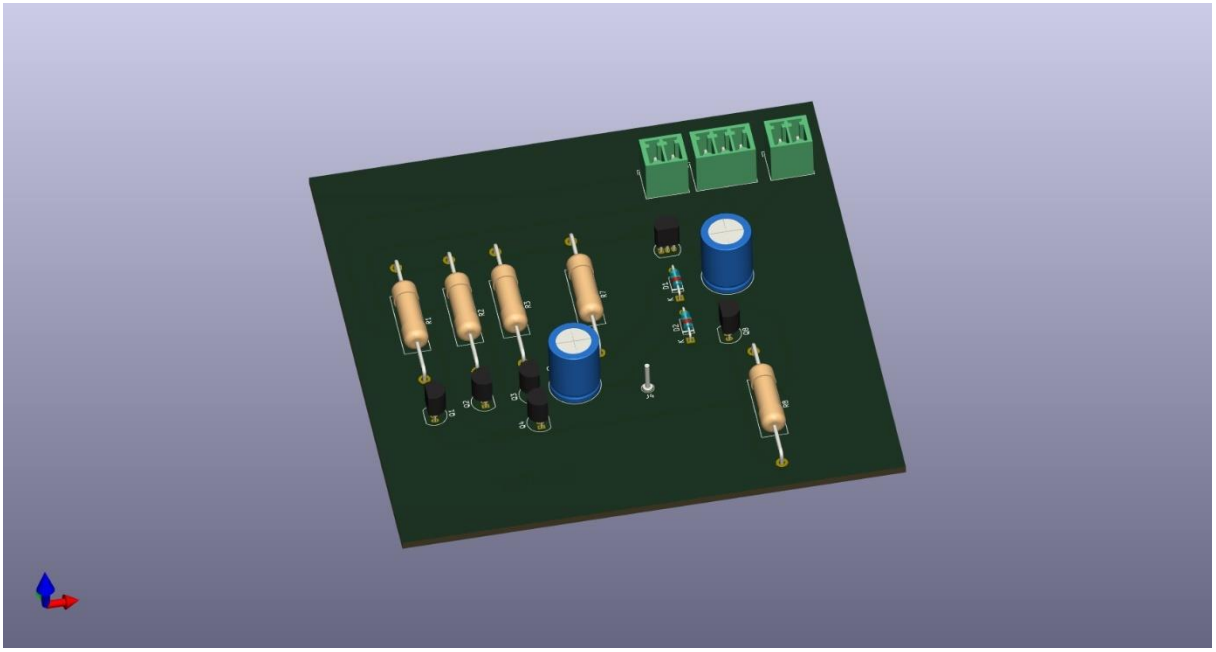
Gain stage removed. It shows at least 100 gain.

KiCad Schematic and PCB Layout:





3D View:



Resources :

Behzad Razavi - Fundamentals of Microelectronics

Adel S. Sedra & Kenneth C. Smith - Microelectronic Circuits

Robert F. Coughlin & Frederick F. Driscoll - Operational Amplifiers and Linear Integrated Circuits

LM358 Datasheet