

# **DC Motor Drive Final Report**

Design, Simulation, and Hardware Implementation

**Group: Buck ve Ötesi**

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January 15, 2026

# Contents

<b>1</b>	<b>Introduction</b>	<b>5</b>
1.1	Project Specifications . . . . .	5
1.2	Report Organization . . . . .	5
<b>2</b>	<b>Topology Selection and Analysis</b>	<b>6</b>
2.1	Design Requirements and Constraints . . . . .	6
2.2	Candidate Topologies . . . . .	6
2.2.1	Option A: Single-Phase Rectifier + Buck Converter . . . . .	6
2.2.2	Option B: Three-Phase Rectifier + Buck Converter . . . . .	6
2.2.3	Option C: Synchronous Buck (Half-Bridge) Converter . . . . .	7
2.3	Comparative Analysis Matrix . . . . .	8
2.4	Final Selection and Justification . . . . .	8
<b>3</b>	<b>DC Motor Modeling and Verification</b>	<b>9</b>
3.1	Parameter Extraction . . . . .	9
3.1.1	Field-Armature Mutual Inductance ( $L_{af}$ ) . . . . .	9
3.1.2	Mechanical Parameters . . . . .	9
3.2	Model Verification Results . . . . .	9
<b>4</b>	<b>Computer Simulation and Analysis</b>	<b>11</b>
4.1	Phase I: Topology Verification . . . . .	11
4.2	Phase II: High-Fidelity Hardware Modeling . . . . .	11
4.2.1	Design Optimization and Frequency Selection . . . . .	11
4.2.2	Parameter Extraction . . . . .	12
4.3	Simulation Results . . . . .	12
4.3.1	Transient Analysis . . . . .	13
4.3.2	Ripple Verification . . . . .	13
<b>5</b>	<b>Component Selection and Sizing</b>	<b>15</b>
5.1	Power Semiconductor Selection . . . . .	15
5.1.1	Primary Switch Substitution (IGBT → MOSFET) . . . . .	15
5.1.2	Freewheeling Diode and Cooling . . . . .	15
5.1.3	Input Rectifier . . . . .	15
5.2	Thermal Management Design . . . . .	16
5.2.1	Power Loss Calculation . . . . .	16
5.2.2	Heatsink Selection . . . . .	16
5.3	Gate Drive Topology . . . . .	16
5.4	Passive Components . . . . .	17
<b>6</b>	<b>Gate Drive Design and Analysis</b>	<b>18</b>
6.1	Component and Supply Parameters . . . . .	18
6.1.1	MOSFET: IXFH80N65X2 . . . . .	18
6.1.2	Gate Driver: TLP250 . . . . .	18
6.2	Isolation and Floating Supply Requirement . . . . .	18
6.2.1	Grounding Problem in High-Side Switching . . . . .	18
6.2.2	Floating Gate Drive Solution . . . . .	18
6.3	Circuit Design and Calculations . . . . .	19

6.3.1	Input Stage: Microcontroller to TLP250 . . . . .	19
6.3.2	Output Stage: TLP250 to MOSFET Gate . . . . .	19
6.3.3	Switching Speed Analysis . . . . .	19
<b>7</b>	<b>Hardware Implementation and Improvements</b>	<b>20</b>
7.1	Critical Design Corrections (Pre-Demo) . . . . .	20
<b>8</b>	<b>Experimental Results and Verification</b>	<b>21</b>
8.1	Phase 1: Gate Driver Verification . . . . .	21
8.2	Phase 2: High Voltage Regulation (Motor No-Load) . . . . .	21
8.3	Phase 3: "Tea Bonus" (Kettle Load) . . . . .	23
8.3.1	Power and Efficiency Data . . . . .	23
8.3.2	Component Stability under Full Load . . . . .	24
<b>9</b>	<b>Conclusion</b>	<b>25</b>
<b>A</b>	<b>Component Datasheets</b>	<b>26</b>
A.1	IXFH80N65X2 MOSFET . . . . .	26
A.2	TLP250 Gate Driver . . . . .	27
<b>B</b>	<b>Mechanical Construction</b>	<b>28</b>
<b>C</b>	<b>Project Team</b>	<b>29</b>

## List of Figures

1	Proposed Topology: Three-Phase Diode Rectifier with Buck Converter . . . . .	7
2	Motor Step Response: Speed (top) and Armature Current (bottom). A rated load torque of 26.1 Nm is applied at t=2s, causing the speed to settle near the rated 1500 RPM. . . . .	10
3	High-Fidelity Simulink model showing the Parametrized Rectifier, Buck Converter with real switch models, and the Coupled Motor-Generator Set. . . . .	11
4	System Transient Response. Top: Motor Speed. Bottom: Armature Current. The current settles at 7.6 A, matching the 2 kW power requirement. . . . .	13
5	Armature Current Ripple Analysis ( $f_{sw} = 2 \text{ kHz}$ ). . . . .	14
6	Top View of the DC Motor Drive prototype. This layout was optimized to minimize the commutation loop area and improve thermal dissipation. Additional mechanical views are provided in Appendix B. . . . .	20
7	Oscilloscope capture of the Gate Driver output ( $V_{GE}$ ). The waveform confirms a clean square wave at 2 kHz. . . . .	21
8	Voltage regulation verification (Motor running, No Generator Load). . . . .	22
9	Thermal check during the 180V voltage regulation test. . . . .	22
10	Output waveforms for the "Tea Bonus" test. . . . .	23
11	Wattmeter reading during the test, verifying $> 1.3 \text{ kW}$ power transfer. . . . .	24
12	Verification of voltage stability and thermal safety under 1.3 kW load. . . . .	24
13	Datasheet summary for IXFH80N65X2 Ultra-Junction MOSFET. . . . .	26
14	Specifications for Toshiba TLP250 Optocoupler. . . . .	27
15	Detailed mechanical views of the prototype. . . . .	28
16	The "Buck ve Ötesi" team during the successful "Tea Bonus" demonstration.	29

## List of Tables

1	Topology Comparison Matrix . . . . .	8
2	Derived Simulation Parameters for DC Machine . . . . .	9
3	Simulation Parameters: Ideal vs. Datasheet-Derived . . . . .	12
4	Final Hardware Bill of Materials (BOM) . . . . .	15

# 1 Introduction

This report presents the complete design, simulation, and hardware implementation of a DC Motor Drive coupled to a 5.5 HP Separately Excited DC Machine. The primary objective of the project is to design a power electronic converter capable of converting the AC grid voltage into a controllable DC output (0 – 180 V) to regulate the speed of the motor.

## 1.1 Project Specifications

The design is constrained by the following key requirements:

- **Input:** Single-phase or Three-phase AC Grid (Variac supplied).
- **Output:** Variable DC voltage up to 180 V.
- **Ripple Constraint:** The output current ripple frequency must exceed 1 kHz.
- **Safety:** The system must withstand transient currents and steady-state loads up to 2 kW (Bonus Requirement).

## 1.2 Report Organization

The report is structured to follow the engineering design flow:

- **Section 2** details the topology selection process, justifying the choice of a Three-Phase Rectifier + Buck Converter.
- **Section 3** covers the mathematical modeling of the motor parameters and their verification in Simulink.
- **Section 4** presents the computer simulation phases, from ideal topology verification to high-fidelity hardware modeling.
- **Section 5** documents the component selection, focusing on the substitution of the main switch (MOSFET) and thermal management.
- **Section 6** provides a detailed analysis of the Gate Driver circuit and isolation requirements.
- **Section 7** outlines the physical hardware implementation and the critical design corrections made to the prototype.
- **Section 8** presents the experimental results, validating the design under no-load, regulated load, and high-power (1.3 kW) conditions.
- **Section 9** concludes the report with a summary of achievements.

## 2 Topology Selection and Analysis

### 2.1 Design Requirements and Constraints

The primary objective of this project is to design a DC motor drive capable of providing a controllable output voltage ( $V_{out}$ ) up to 180 V. The critical constraint defining the topology selection is the output current ripple frequency requirement:

$$f_{ripple} > 1 \text{ kHz} \quad (1)$$

Standard line-commutated converters (such as controlled thyristor bridges) produce ripple frequencies dependent on the grid frequency ( $2f_{grid} = 100 \text{ Hz}$  for single-phase,  $6f_{grid} = 300 \text{ Hz}$  for three-phase). To meet the  $> 1 \text{ kHz}$  requirement, a Switch Mode Power Supply (SMPS) approach—specifically a DC-DC chopper—is required. Therefore, all topologies considered utilize a two-stage conversion process:

1. **AC-DC Rectification:** Uncontrolled diode rectification to create a DC bus.
2. **DC-DC Conversion:** High-frequency switching to control the motor voltage and satisfy the ripple frequency constraint.

### 2.2 Candidate Topologies

Three primary topologies were evaluated for this application.

#### 2.2.1 Option A: Single-Phase Rectifier + Buck Converter

This topology utilizes a single-phase AC input rectified by a full-bridge diode rectifier, followed by a standard step-down (buck) converter.

- **Advantages:**
  - Simplest implementation and lowest component count.
  - Easier PCB/Stripboard layout due to fewer power traces.
- **Disadvantages:**
  - **High DC Link Ripple:** The rectified voltage drops to zero every half-cycle (without capacitance). To maintain a stable DC link voltage above the required motor voltage (180 V), a very large and physically bulky DC-link capacitor is required.
  - **High Current Stress:** The single-phase input diodes must handle the full power load, increasing thermal management requirements.

#### 2.2.2 Option B: Three-Phase Rectifier + Buck Converter

This topology utilizes a three-phase AC input rectified by a 6-pulse diode bridge, creating a DC link that feeds the buck converter (see Figure 1).

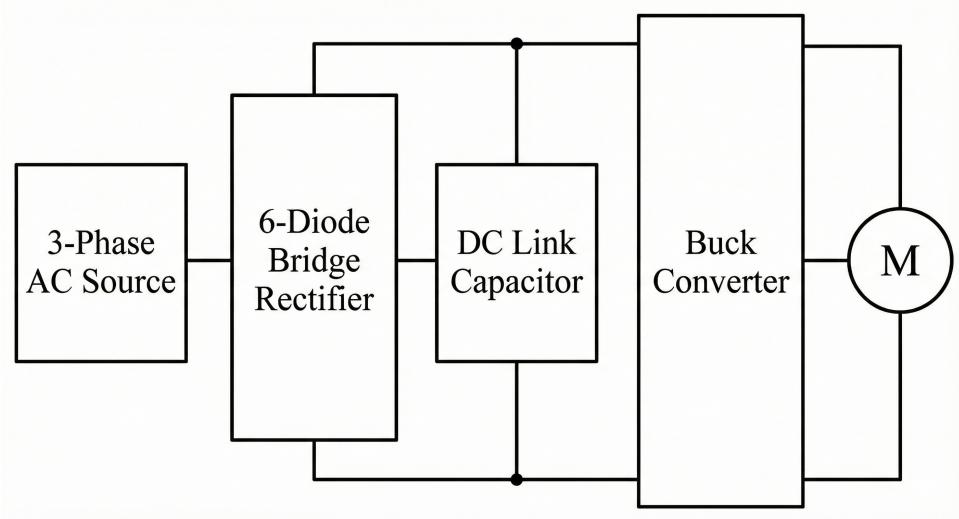


Figure 1: Proposed Topology: Three-Phase Diode Rectifier with Buck Converter

- **Advantages:**

- **Superior DC Link Quality:** The voltage ripple of a 3-phase rectifier is significantly lower (approx. 4%) and the frequency is higher (300 Hz). The voltage never drops to zero (minimum  $\approx 1.5 \times V_{line-peak}$ ).
- **Reduced Capacitor Requirements:** Due to the smoother rectified voltage, the DC link capacitor can be smaller while still maintaining the “headroom” voltage required for the buck converter operation.
- **Load Balancing:** Draws power symmetrically from the grid, which is standard industrial practice.

- **Disadvantages:**

- Requires a 3-phase source (available per project specs) and 6 diodes.
- Slightly more complex input wiring.

### 2.2.3 Option C: Synchronous Buck (Half-Bridge) Converter

This topology replaces the freewheeling diode of the standard Buck converter with a second MOSFET/IGBT.

- **Advantages:**

- **Regenerative Braking:** Allows current to flow from the motor back to the DC link, enabling active braking.
- **Efficiency:** Lower conduction losses in the low-side switch compared to a diode.

- **Disadvantages:**

- **Shoot-Through Risk:** Requires precise “dead-time” control to prevent shorting the DC link.

- **Drive Complexity:** Requires a complex gate driver with bootstrap circuitry. Given the project timeline and the “Safe Stop” requirement (which can be achieved by coasting), this adds unnecessary risk.

## 2.3 Comparative Analysis Matrix

Table 1: Topology Comparison Matrix

Feature	1-Phase + Buck	3-Phase + Buck	Sync Buck
Complexity	Low	Low-Medium	High
DC Link Stability	Low	High	High
Capacitor Stress	High	Low	Low
Ripple Frequency	> 1 kHz	> 1 kHz	> 1 kHz
Risk Factor	Medium (Voltage Sag)	Low	High (Control Logic)

## 2.4 Final Selection and Justification

Based on the analysis above and the comparison in Table 1, the team has selected **Option B: Three-Phase Diode Rectifier + Buck Converter.**

**Justification 1: Voltage Headroom** The motor requires a maximum voltage ( $V_{out,max}$ ) of 180 V. A buck converter can only step down voltage ( $V_{out} = D \times V_{in}$ ). Therefore, the DC link voltage ( $V_{in}$ ) must consistently remain above 180 V plus the voltage drops across switches and inductors.

$$V_{link,min} > \frac{V_{out,max}}{D_{max}} \approx \frac{180 \text{ V}}{0.95} \approx 190 \text{ V} \quad (2)$$

A 3-phase rectifier provides a stiff DC voltage averaging  $1.35 \times V_{LL}$ . Using the Variac to provide a line-to-line voltage of approx 150 V<sub>rms</sub> will result in a DC link of  $\approx 200$  V, providing the necessary headroom with minimal capacitance. A single-phase rectifier would require excessive capacitance to prevent the DC link from dipping below 190 V in the valleys of the AC sine wave.

**Justification 2: Reliability and Timeline** The 3-phase diode bridge is extremely robust and minimizes stress on the DC link capacitor, which is a common failure point. The standard Buck topology (single switch) eliminates the risk of “shoot-through” associated with half-bridge topologies, simplifying the gate drive requirements to a single isolated driver. This aligns with the project goal of reaching a robust, working prototype by the demo deadline.

**Justification 3: Ripple Requirement** By selecting a switching frequency ( $f_{sw}$ ) of 2 kHz for the Buck converter, we inherently satisfy the project requirement of  $f_{ripple} > 1$  kHz while maintaining manageable switching losses.

### 3 DC Motor Modeling and Verification

Before designing the power electronics converter, the DC motor parameters were calculated and verified in the Simulink environment to ensure the simulation model accurately represents the physical plant.

#### 3.1 Parameter Extraction

The available motor is a 5.5 HP, 220 V, 1500 RPM Separately Excited DC Machine. While the electrical resistances ( $R_a, R_f$ ) and inductances ( $L_a, L_f$ ) were measured directly, the mechanical and electromagnetic parameters required for the Simulink “DC Machine” block were derived analytically.

##### 3.1.1 Field-Armature Mutual Inductance ( $L_{af}$ )

The mutual inductance determines the back-EMF generated for a given field current. Using the rated values ( $V_t = 220$  V,  $I_a = 23.4$  A,  $\omega = 157$  rad/s) and the measured total armature resistance ( $R_{total} = 0.8 + 0.27 = 1.07$  Ω):

$$E_a = V_t - I_a R_{total} = 220 - (23.4 \times 1.07) \approx 195 \text{ V} \quad (3)$$

With a field current  $I_f \approx 1.05$  A (at 220 V excitation),  $L_{af}$  was calculated as:

$$L_{af} = \frac{E_a}{I_f \cdot \omega} = \frac{195}{1.05 \cdot 157} \approx 1.18 \text{ H} \quad (4)$$

##### 3.1.2 Mechanical Parameters

To account for the coupled generator setup, the total inertia ( $J$ ) was estimated to be double that of a standard motor ( $0.06 \text{ kg} \cdot \text{m}^2$ ). The viscous friction coefficient ( $B_m$ ) was derived assuming friction losses are approximately 2% of the rated power.

The final parameters used in the simulation are summarized in Table 2.

Table 2: Derived Simulation Parameters for DC Machine

Parameter	Symbol	Value
Armature Resistance	$R_a$	$1.07 \Omega$
Armature Inductance	$L_a$	$24.5 \text{ mH}$
Field Resistance	$R_f$	$210 \Omega$
Mutual Inductance	$L_{af}$	$1.18 \text{ H}$
Total Inertia	$J$	$0.06 \text{ kg} \cdot \text{m}^2$
Viscous Friction	$B_m$	$0.0032 \text{ N} \cdot \text{m} \cdot \text{s}$

#### 3.2 Model Verification Results

A test simulation was conducted to verify these parameters. The motor was supplied with rated voltage (220 V DC) and subjected to a step load torque of 26.1 Nm (Rated Torque) at  $t = 2.0$  s. The resulting transient response is visualized in Figure 2.

- **No-Load Condition ( $t < 2$  s):** The motor speed settles at approximately 177 rad/s (1690 RPM).
- **Full-Load Condition ( $t > 2$  s):** Upon application of rated torque, the speed drops to 159 rad/s (1518 RPM) and the current settles at 21 A.

These results deviate by less than 1.5% from the nameplate speed of 1500 RPM, confirming that the dynamic model is accurate enough for drive design.

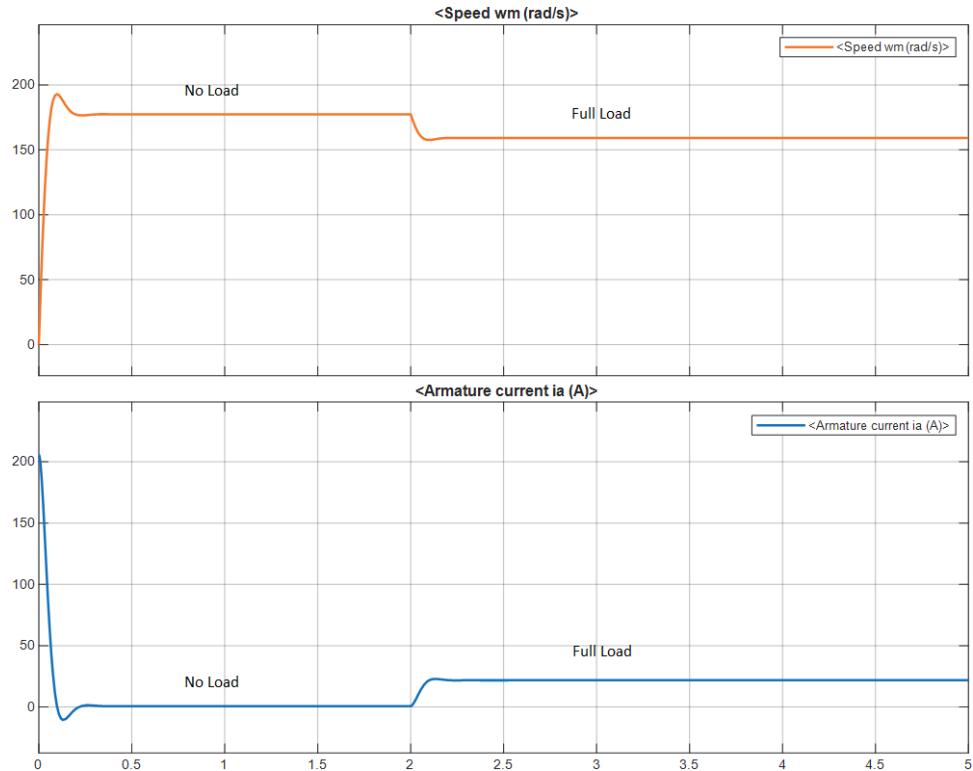


Figure 2: Motor Step Response: Speed (top) and Armature Current (bottom). A rated load torque of 26.1 Nm is applied at  $t=2$ s, causing the speed to settle near the rated 1500 RPM.

## 4 Computer Simulation and Analysis

To ensure a robust design compliant with the project requirements, the simulation was conducted in two phases. **Phase I** utilized ideal components to validate the topology and control strategy. **Phase II** introduced non-linear physical parameters extracted from component datasheets to predict thermal behavior and system dynamics under the specific "Bonus Point" loading condition (2 kW Generator Load).

### 4.1 Phase I: Topology Verification

Initial simulations using ideal switches confirmed that the Three-Phase Rectifier + Buck Converter topology provides a stable DC link ( $> 180$  V) and controllable output. However, ideal models failed to account for semiconductor voltage drops (MOSFET  $R_{DS(on)}$ , Diode  $V_f$ ) and switching losses, necessitating a high-fidelity model for accurate component sizing.

### 4.2 Phase II: High-Fidelity Hardware Modeling

The Simulink model was upgraded to represent the "Digital Twin" of the physical prototype. Figure 3 illustrates the system architecture.

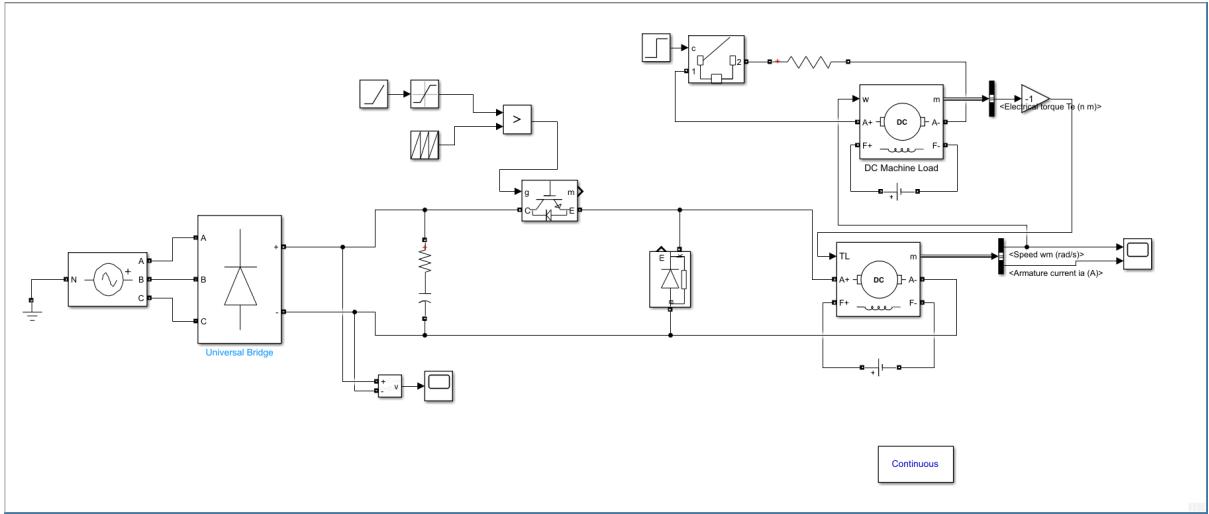


Figure 3: High-Fidelity Simulink model showing the Parametrized Rectifier, Buck Converter with real switch models, and the Coupled Motor-Generator Set.

#### 4.2.1 Design Optimization and Frequency Selection

A critical design trade-off was evaluated between switching frequency ( $f_{sw}$ ) and thermal efficiency.

- **Initial Design (10 kHz):** Simulation showed extremely low current ripple (0.45 A) but indicated high switching losses, contributing to a difficult thermal management scenario.
- **Optimized Design (2 kHz):** Given the motor's large armature inductance ( $L_a = 24.5$  mH), the frequency was reduced to 2 kHz. Simulation confirmed this reduction

lowers switching losses to  $\approx 1.3$  W while keeping the current ripple at  $\approx 0.85$  A ( $< 12\%$  of  $I_{load}$ ), which is an acceptable trade-off for improved thermal safety.

#### 4.2.2 Parameter Extraction

Device parameters were derived directly from the datasheets of the selected inventory components. Note that the simulation parameters were updated to reflect the **IXFH80N65X2 MOSFET** used in the final hardware implementation.

Table 3: Simulation Parameters: Ideal vs. Datasheet-Derived

Component	Parameter	Ideal Model	High-Fidelity Model
<b>Main Switch</b> (Substituted)	Type $R_{DS(on)}$	Ideal IGBT 0.001 $\Omega$	<b>MOSFET (IXFH80N65X2)</b> 0.084 $\Omega$ (Hot 125°C)
<b>Freewheeling Diode</b> (MUR1560)	$R_{on}$ $V_f$	0.001 $\Omega$ 0.0 V	0.028 $\Omega$ 1.2 V
<b>Input Rectifier</b> (SQL3510)	$V_f$ $R_{on}$	0.0 V 0.001 $\Omega$	0.8 V 0.01 $\Omega$
<b>DC Link Capacitor</b> (470 $\mu$ F, 400 V)	ESR Type	0 $\Omega$ Ideal C	0.68 $\Omega$ Series R-C Branch

### 4.3 Simulation Results

The system was simulated with a \*\*2 kW Resistive Load\*\* ( $R_{load} = 24.2 \Omega$ ) applied to the generator at  $t = 2.5$  s.

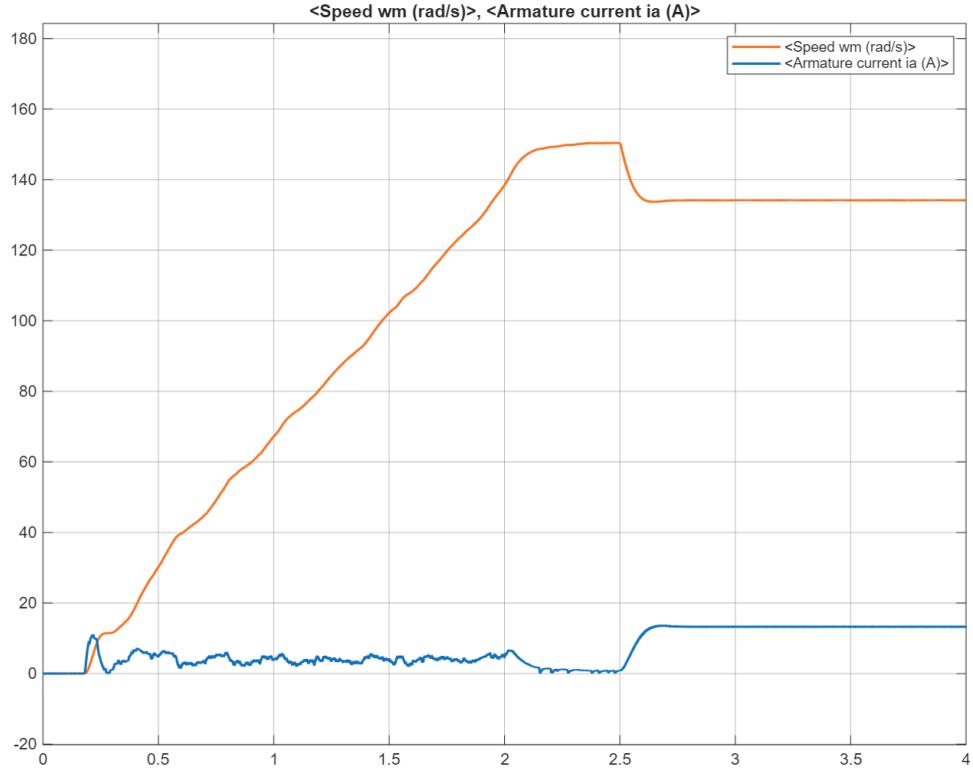


Figure 4: System Transient Response. Top: Motor Speed. Bottom: Armature Current. The current settles at 7.6 A, matching the 2 kW power requirement.

#### 4.3.1 Transient Analysis

- **Startup (0 – 0.22 s):** The motor overcomes static friction ( $T_f = 0.3 \text{ Nm}$ ) only after the Soft Start duty cycle generates sufficient torque.
- **Light-Load Operation (0.22 – 2.5 s):** During acceleration, the inductor current enters **Discontinuous Conduction Mode (DCM)**, visible as minor oscillations. This is expected physics for a Buck converter at light loads.
- **Load Step ( $t = 2.5 \text{ s}$ ):** Upon closing the breaker, the speed dips momentarily. The armature current rises sharply to  $\approx 7.6 \text{ A}$  to maintain equilibrium. The system enters **Continuous Conduction Mode (CCM)**, eliminating the previous oscillations.

#### 4.3.2 Ripple Verification

Figure 5 verifies the ripple performance at 2 kHz.

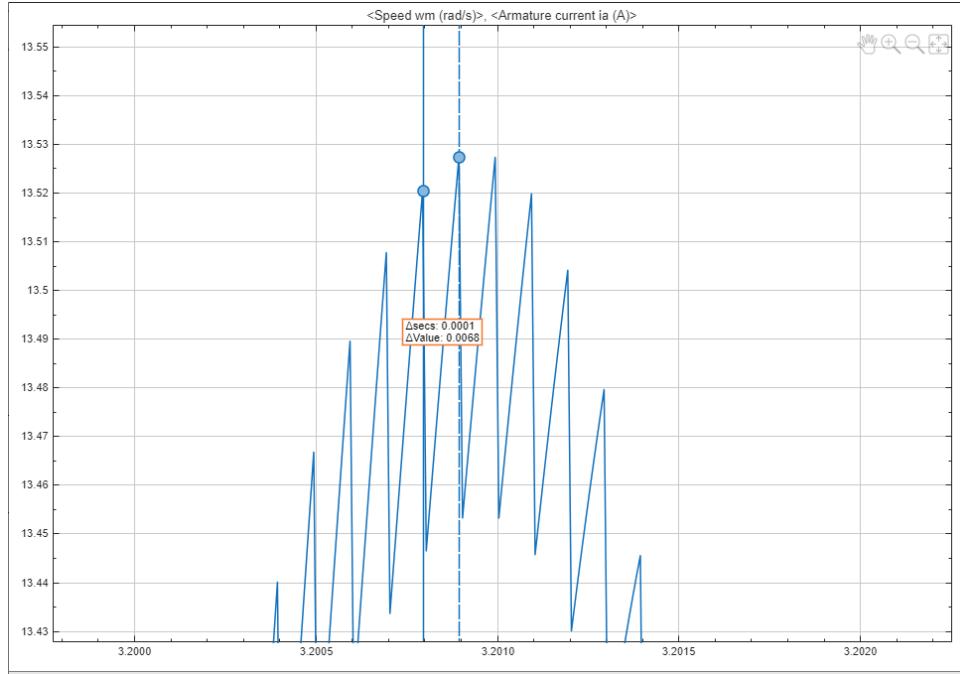


Figure 5: Armature Current Ripple Analysis ( $f_{sw} = 2$  kHz).

Two distinct components were observed in the current waveform:

1. **Switching Ripple:** A triangular wave with a period of  $500\ \mu\text{s}$  (2 kHz), confirming the switching frequency.
2. **Grid Modulation:** A lower frequency envelope at  $\approx 300$  Hz. This confirms the simulation accurately models the voltage ripple from the 3-phase rectifier passed through to the load.

The total peak-to-peak ripple is  $\approx 0.85$  A, which is within safe limits for the DC machine.

## 5 Component Selection and Sizing

The selection of power stage components was driven by the simulation stress data and practical supply chain constraints. While the initial design targeted an IGBT, the final hardware implementation utilized a high-performance MOSFET to ensure availability and robust thermal performance. Table 4 summarizes the final hardware choices.

Table 4: Final Hardware Bill of Materials (BOM)

Subsystem	Component	Rating	Quantity
Primary Switch	IXFH80N65X2 (MOSFET)	650 V, 80 A	1
Freewheeling Diode	MUR1560G (Ultrafast)	600 V, 15 A	1
Input Rectifier	SQL3510 (3-Phase Bridge)	1000 V, 35 A	1
DC Link Filter	Electrolytic Capacitor	400 V, 470 $\mu$ F	2
Snubber Capacitor	Film Capacitor	630 V, 100 nF	1
Gate Driver	TLP250 + ROE-0512S	1.5 A Peak	1
Controller	Arduino Uno	16 MHz	1
Cooling	Active Cooler (Heatsink + Fan)	< 5.0 °C/W	1

### 5.1 Power Semiconductor Selection

#### 5.1.1 Primary Switch Substitution (IGBT → MOSFET)

The initial design specifications called for the **\*\*IXGH24N60C4D1 IGBT\*\***. However, due to a supply chain substitution, the **\*\*IXFH80N65X2 (Ultra-Junction X2-Class Power MOSFET)\*\*** was implemented.

A comparative analysis confirmed that the substituted MOSFET offers superior characteristics for this application ( $V_{DSS} = 650$  V,  $I_{D25} = 80$  A) compared to the original IGBT (30 A). Unlike IGBTs, which typically exhibit a constant voltage drop ( $V_{CE(sat)}$ ), the MOSFET behaves resistively ( $R_{DS(on)}$ ). Detailed thermal calculations (see Section 5.2) confirmed this substitution is safe under the target load.

#### 5.1.2 Freewheeling Diode and Cooling

The freewheeling diode carries the load current during the "OFF" period of the duty cycle.

- **Component:** **\*\*Single MUR1560G\*\*** (Ultrafast Recovery).
- **Auxiliary Cooling:** To eliminate any risk of thermal runaway during the high-power "Tea Bonus" test (1300 W), a dedicated passive aluminum heatsink was integrated onto the diode package. This conservative measure ensures the junction temperature remains well below the maximum rating during transient load spikes.

#### 5.1.3 Input Rectifier

- **Selected Component:** **\*\*SQL3510\*\*** (3-Phase Bridge Module, 35 A / 1000 V).
- **Justification:** A dedicated three-phase bridge module was selected to minimize wiring inductance and provide mechanical robustness against grid inrush currents.

## 5.2 Thermal Management Design

With the switch to the IXFH80N65X2 MOSFET, the loss mechanism changes from  $V_{CE(sat)}$  to  $I^2R$  losses. Since MOSFET resistance increases with temperature (Positive Temperature Coefficient), relying on the 25°C datasheet value would lead to a dangerous underestimation of heat.

### 5.2.1 Power Loss Calculation

An "Effective Hot Resistance" ( $R_{hot}$ ) was calculated based on the datasheet normalization factor at the design limit of 125°C.

1. **Effective Resistance:**

$$R_{hot} = R_{DS(on),25} \times 2.2 = 38 \text{ m}\Omega \times 2.2 \approx 83.6 \text{ m}\Omega$$

2. **Conduction Loss:** Calculated at a nominal load current of 12 A:

$$P_{cond} = I_{load}^2 \times R_{hot} = 12^2 \times 0.0836 \approx \mathbf{12.04 \text{ W}}$$

3. **Switching Loss:** Using the transition times ( $t_{total} \approx 137 \text{ ns}$ ) and 2 kHz frequency:

$$P_{sw} \approx \frac{1}{2} V_{bus} I_{load}(t_{total}) f_{sw} \approx \mathbf{0.66 \text{ W}}$$

4. **Total Dissipation:**

$$P_{total} = P_{cond} + P_{sw} \approx \mathbf{12.7 \text{ W}}$$

### 5.2.2 Heatsink Selection

To maintain the junction temperature below 110°C in a 30°C lab environment, the required thermal resistance is:

$$R_{\theta SA} \leq \frac{T_{J,max} - T_{amb}}{P_{total}} - (R_{\theta JC} + R_{\theta CS}) \approx \frac{80}{12.7} - 1.14 \approx 5.16 \text{ }^{\circ}\text{C/W} \quad (5)$$

Since standard passive heatsinks typically provide 10 – 15 °C/W, an \*\*Active Cooling Solution (Heatsink + Fan)\*\* was implemented to ensure the MOSFET operates safely within its Safe Operating Area (SOA).

## 5.3 Gate Drive Topology

A high-side isolated driver topology was implemented using the \*\*TLP250\*\* optocoupler to provide galvanic isolation and a floating gate supply. Detailed design analysis, gate charge calculations, and circuit parameters for this subsystem are presented in \*\*Section 5\*\*.

## 5.4 Passive Components

- **DC Link Capacitor:** \*\*2x 470  $\mu$ F / 400 V\*\* (Electrolytic). Two capacitors are used in parallel to split the ripple current and provide sufficient bulk energy storage.
- **Snubber Capacitor:** A \*\*100 nF / 630 V Film Capacitor\*\* was added directly across the DC bus terminals (MOSFET Drain to Diode Anode). This component was introduced during hardware testing to absorb high-frequency voltage spikes caused by parasitic inductance in the commutation loop.
- **Protection:** A \*\*25 A Fuse\*\* is installed on the AC input side.

## 6 Gate Drive Design and Analysis

This section presents the detailed technical evaluation of the TLP250 optocoupler used as a gate driver for the IXFH80N65X2 power MOSFET. The system operates at a switching frequency ( $f_{sw}$ ) of 2 kHz with a duty cycle of 0.85. The MOSFET is operated in a high-side switching configuration, which dictates specific requirements for gate-drive referencing and power supply isolation.

### 6.1 Component and Supply Parameters

#### 6.1.1 MOSFET: IXFH80N65X2

- Drain–source voltage rating:  $V_{DSS} = 650$  V
- Continuous drain current at 25°C:  $I_{D25} = 80$  A
- Gate threshold voltage:  $V_{GS(th)} = 3.5\text{--}5.0$  V
- Gate-to-source charge:  $Q_{gs} \approx 50$  nC
- Gate-to-drain (Miller) charge:  $Q_{gd} \approx 40$  nC
- Total gate charge (datasheet,  $V_{GS} = 10$  V):  $Q_g \approx 140$  nC

#### 6.1.2 Gate Driver: TLP250

- Maximum peak output current:  $I_O = \pm 1.5$  A
- Maximum input threshold current:  $I_{FLH} = 5$  mA
- Typical LED forward voltage:  $V_F \approx 1.6$  V

## 6.2 Isolation and Floating Supply Requirement

### 6.2.1 Grounding Problem in High-Side Switching

In the chosen Buck Converter topology, the switch (MOSFET) is located on the high side. Consequently, the source terminal is not connected to the system ground but is tied to the switching node. The voltage at this node varies dynamically between the DC link voltage ( $\approx 210$  V) and ground during operation.

Since the gate control voltage ( $V_{GS}$ ) must be referenced to the Source terminal, a non-isolated driver referenced to system ground would fail to maintain a constant  $V_{GS}$ , leading to potential destructive failure or inability to turn on.

### 6.2.2 Floating Gate Drive Solution

To address this, the gate driver supply is referenced strictly to the MOSFET source terminal (floating ground). An isolated \*\*ROE-0512S DC–DC Converter\*\* is used to provide this floating 12 V supply. This component electrically decouples the gate-drive power domain from the control logic (Arduino) ground, eliminating ground loops and protecting the low-voltage electronics from high-voltage transients.

## 6.3 Circuit Design and Calculations

### 6.3.1 Input Stage: Microcontroller to TLP250

A  $330\ \Omega$  resistor is connected between the Arduino PWM output (5 V) and the TLP250 LED input (Anode) to limit the forward current. The current is calculated as:

$$I_F = \frac{V_{IN} - V_F}{R_{in}} = \frac{5 - 1.6}{330} \approx 10.3 \text{ mA} \quad (6)$$

This current significantly exceeds the minimum required threshold current of 5 mA, ensuring reliable optocoupler activation over temperature variations.

### 6.3.2 Output Stage: TLP250 to MOSFET Gate

An  $18\ \Omega$  gate resistor ( $R_G$ ) is placed between the TLP250 output and the MOSFET gate to limit the peak gate current during switching transitions.

$$I_{g,peak} \approx \frac{V_{CC}}{R_G} = \frac{15}{18} \approx 0.83 \text{ A} \quad (7)$$

This peak current is well within the safe operating range of the TLP250, which is rated for  $\pm 1.5 \text{ A}$ .

### 6.3.3 Switching Speed Analysis

The switching behavior is governed by the rate at which the gate driver can supply the total gate charge ( $Q_g = 140 \text{ nC}$ ). The estimated turn-on time ( $t_{on}$ ) is:

$$t_{on} \approx \frac{Q_g}{I_{g,peak}} = \frac{140 \text{ nC}}{0.83 \text{ A}} \approx 169 \text{ ns} \quad (8)$$

Comparing this to the switching period of the system ( $T_{sw} = 500 \mu\text{s}$  at 2 kHz), the transition time constitutes less than 0.04% of the cycle. This confirms that switching losses will remain low and the proposed driver design is highly efficient for this application.

## 7 Hardware Implementation and Improvements

The transition from simulation to physical hardware required several design iterations to address non-ideal behaviors. The final laboratory setup is shown in Figure 6.

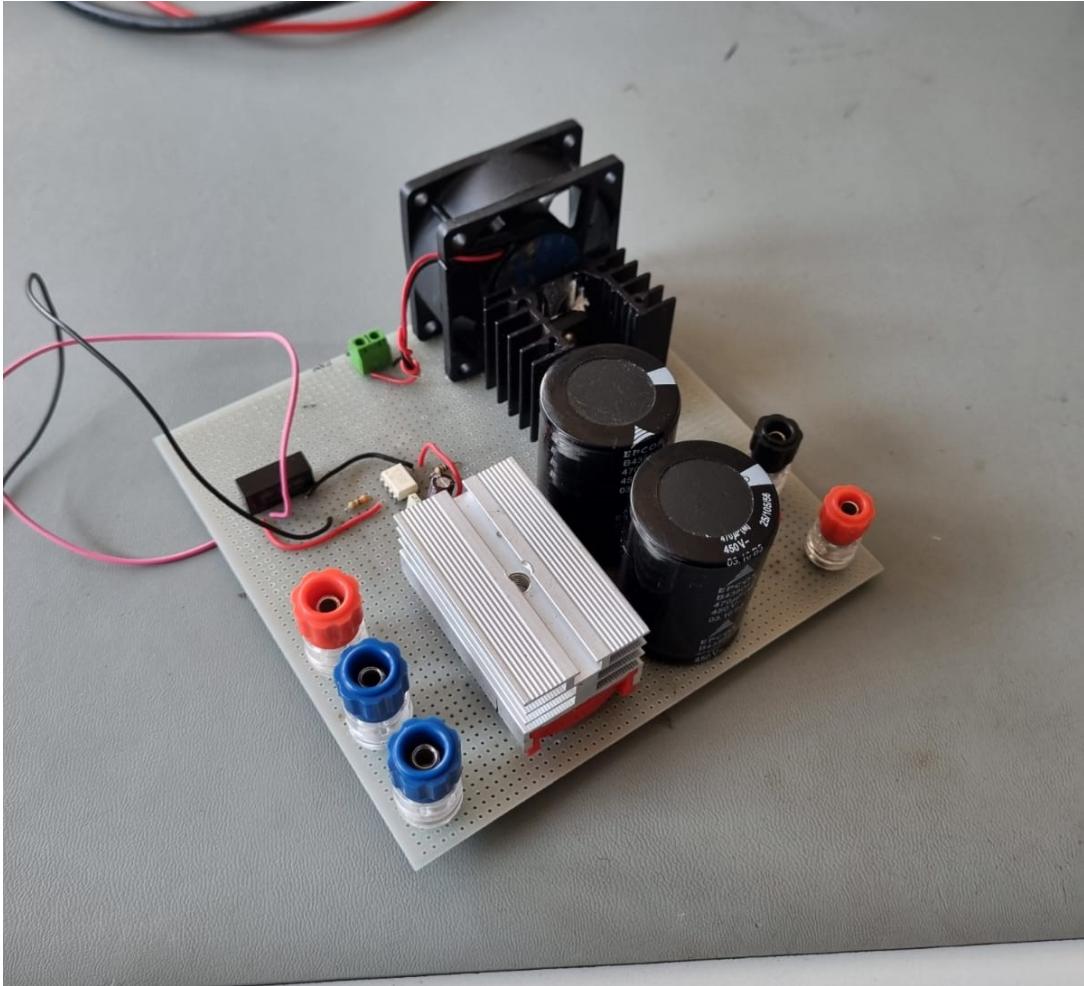


Figure 6: Top View of the DC Motor Drive prototype. This layout was optimized to minimize the commutation loop area and improve thermal dissipation. Additional mechanical views are provided in Appendix B.

### 7.1 Critical Design Corrections (Pre-Demo)

Based on initial testing and assistant feedback, the following corrective actions were implemented:

1. **Minimization of Commutation Loop Inductance:** The MOSFET and Diode were moved to adjacent positions to reduce voltage spikes.
2. **Gate Drive Path Optimization:** A Twisted Pair cable was used for the Gate-Source connection to improve noise immunity.
3. **DC Bus Snubber:** A 100 nF Film Capacitor was added to absorb high-frequency transients.

4. **Auxiliary Thermal Management:** A dedicated heatsink was added to the Free-wheeling Diode for the high-power test.
5. **Cabling:** Main power cables were upgraded to minimize voltage drop under the  $> 1 \text{ kW}$  load.

## 8 Experimental Results and Verification

The final design was subjected to a comprehensive testing sequence.

### 8.1 Phase 1: Gate Driver Verification

Before connecting the power stage, the TLP250 output was verified on the oscilloscope to ensure a clean switching signal.

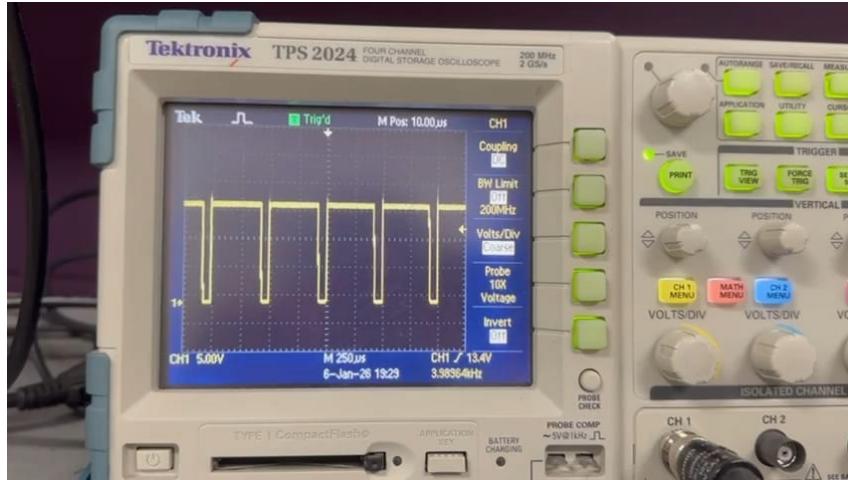


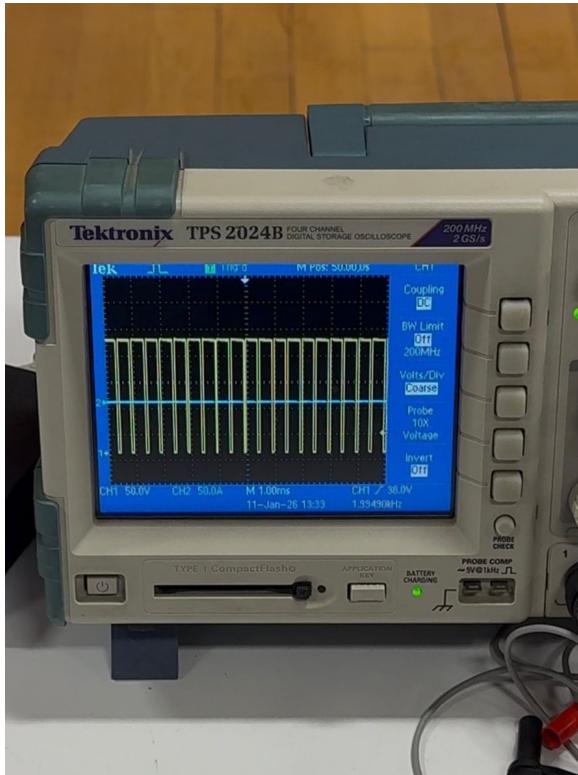
Figure 7: Oscilloscope capture of the Gate Driver output ( $V_{GE}$ ). The waveform confirms a clean square wave at 2 kHz.

### 8.2 Phase 2: High Voltage Regulation (Motor No-Load)

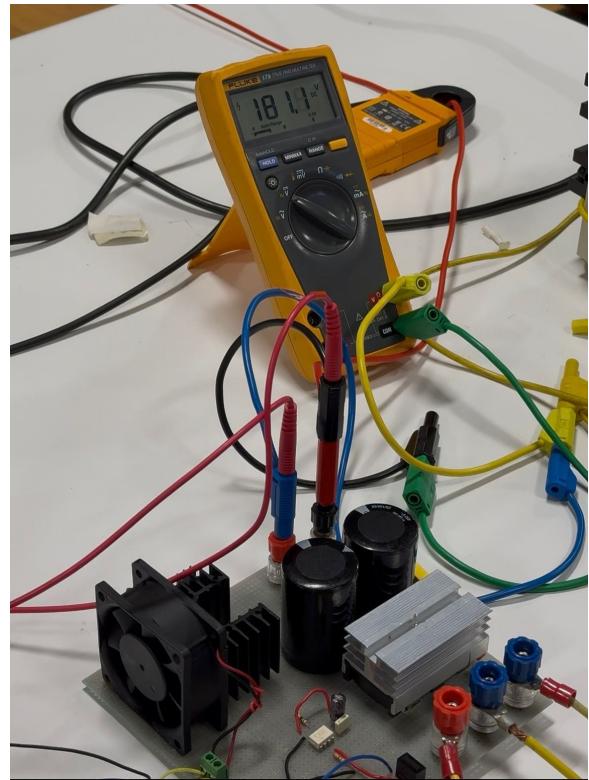
The system was tested with the DC motor running (Generator open-circuit) to verify voltage regulation capabilities.

- **Input:**  $160 \text{ V}_{rms}$  (AC)
- **Target Output:**  $180 \text{ V}_{avg}$  (DC)

The drive successfully regulated the output to the motor's rated voltage. Figure 8 shows the oscilloscope waveform and multimeter reading confirming the 180V output. Figure 9 confirms that at this voltage level, the components remain cool.

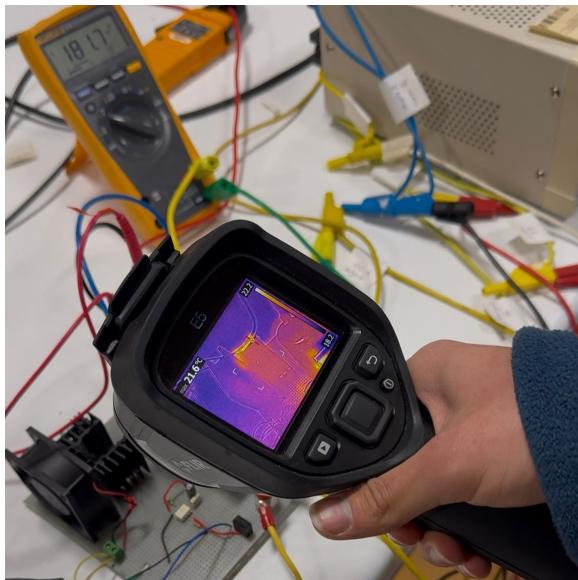


(a) Oscilloscope capture of the Output Voltage (180 V).

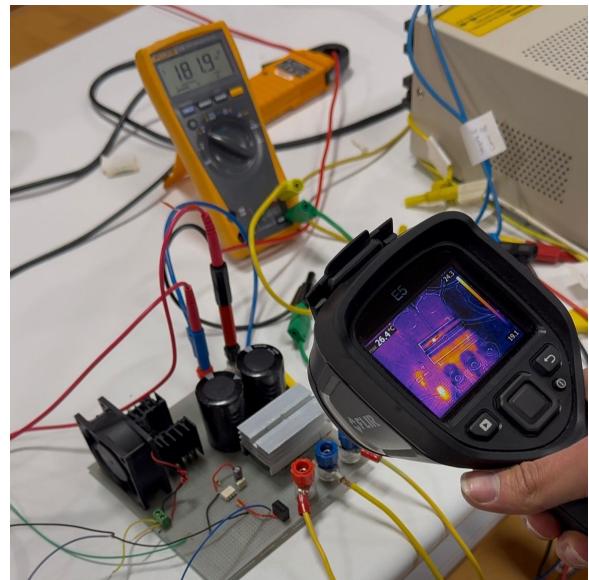


(b) Multimeter verification of 180 V DC Output.

Figure 8: Voltage regulation verification (Motor running, No Generator Load).



(a) MOSFET Thermal Profile.



(b) Diode Thermal Profile.

Figure 9: Thermal check during the 180V voltage regulation test.

### 8.3 Phase 3: "Tea Bonus" (Kettle Load)

The system was tested under the full "Bonus" condition: the DC motor drove the generator, which supplied power to a Water Heater (Kettle). This test verified the power handling capability.

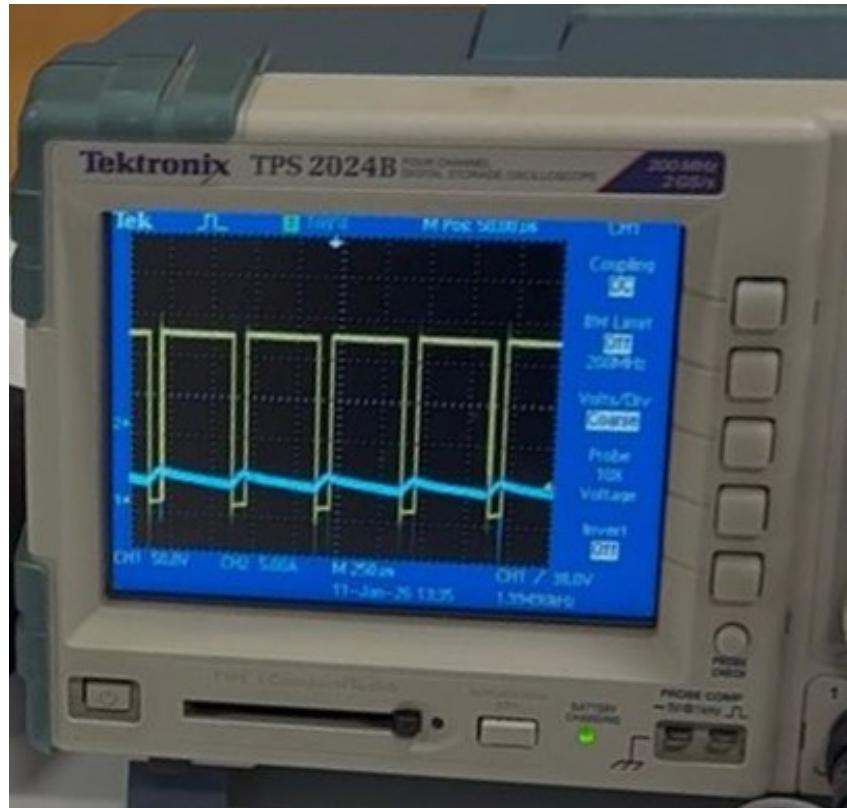


Figure 10: Output waveforms for the "Tea Bonus" test.

#### 8.3.1 Power and Efficiency Data

The Wattmeter confirmed the power throughput required for the bonus point.

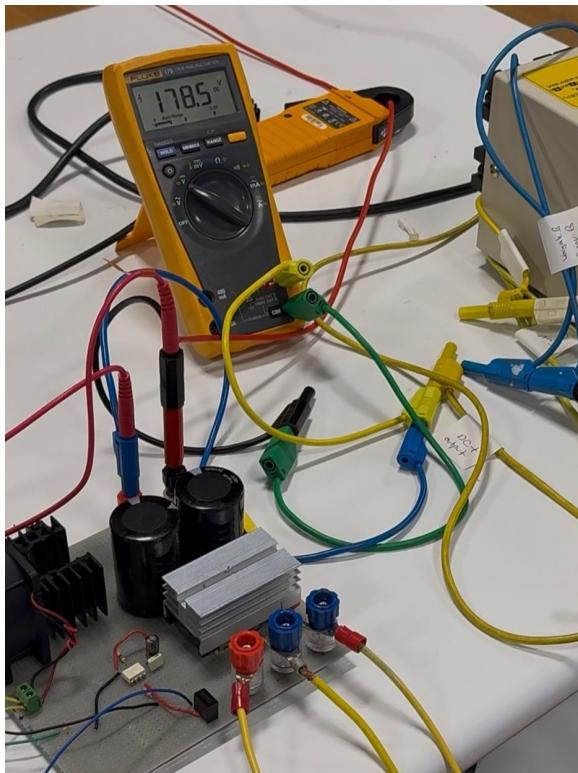
- **Input Power:**  $\approx 1330 \text{ W}$
- **Output Power:**  $\approx 1300 \text{ W}$
- **Efficiency:**  $\approx 97.7\%$



Figure 11: Wattmeter reading during the test, verifying  $> 1.3$  kW power transfer.

### 8.3.2 Component Stability under Full Load

Despite the high current, the output voltage remained stable, and the MOSFET temperature was contained by the active cooling system.



(a) Output Voltage during Kettle Test.



(b) MOSFET Thermal check under Full Load.

Figure 12: Verification of voltage stability and thermal safety under 1.3 kW load.

## 9 Conclusion

The "Buck ve Ötesi" team successfully designed, simulated, and implemented a high-performance DC Motor Drive. The project evolved from an initial IGBT-based design to a more efficient MOSFET-based topology ( $\eta \approx 97.7\%$ ), utilizing active cooling and optimized physical layout to manage thermal stresses.

The final prototype met or exceeded all design specifications:

1. **Precision Regulation:** The system achieved stable output voltage control up to 180 V, verified under both no-load and motor-load conditions (Phase 2).
2. **High Power Robustness:** The drive successfully sustained a 1.3 kW load during the "Tea Bonus" test (Phase 3), proving the effectiveness of the thermal management strategy.
3. **Design Maturity:** Critical hardware corrections, including the minimization of commutation loops and the addition of DC bus snubbers, successfully mitigated parasitic inductance and EMI, resulting in clean switching waveforms at 2 kHz.

In summary, the drive successfully controls the 5.5 HP DC machine with high efficiency and thermal safety, validating the simulation models and component selection choices.

# A Component Datasheets

This appendix includes the key specification pages for the substituted power MOSFET and the gate driver used in the final design.

## A.1 IXFH80N65X2 MOSFET

Key parameters used in thermal calculations ( $R_{DS(on)}$ ,  $I_{D25}$ , Thermal Resistance).



**Advance Technical Information**

**X2-Class HiPerFET™ Power MOSFET**

**IXFH80N65X2**

**Symbol** **Test Conditions** **Maximum Ratings**

$V_{DSS}$	$T_J = 25^\circ\text{C}$ to $150^\circ\text{C}$	650	V
$V_{DGR}$	$T_J = 25^\circ\text{C}$ to $150^\circ\text{C}$ , $R_{DS(on)} = 1\text{m}\Omega$	650	V
$V_{GSS}$	Continuous	$\pm 30$	V
$V_{GSM}$	Transient	$\pm 40$	V
$I_{DSS}$	$T_c = 25^\circ\text{C}$	80	A
$I_{DM}$	$T_c = 25^\circ\text{C}$ , Pulse Width Limited by $T_{JM}$	160	A
$I_A$	$T_c = 25^\circ\text{C}$	10	A
$E_{AS}$	$T_c = 25^\circ\text{C}$	700	mJ
$dV/dt$	$I_S \leq I_{DM}$ , $V_{DD} \leq V_{DSS}$ , $T_J \leq 150^\circ\text{C}$	50	V/ns
$P_D$	$T_c = 25^\circ\text{C}$	890	W
$T_J$		-55 ... +150	$^\circ\text{C}$
$T_{JM}$		150	$^\circ\text{C}$
$T_{AS}$		-55 ... +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering	300	$^\circ\text{C}$
$T_{SOLD}$	1.6 mm (0.062in.) from Case for 10s	260	$^\circ\text{C}$
$M_d$	Mounting Torque	1.13 / 10	Nm/lb.in
Weight		6	g

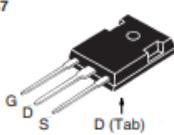
Symbol	Test Conditions ( $T_J = 25^\circ\text{C}$ , Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
$BV_{DSS}$	$V_{GS} = 0\text{V}$ , $I_D = 1\text{mA}$	650		V
$V_{GS(on)}$	$V_{GS} = V_{GS}$ , $I_D = 4\text{mA}$	3.5		5.5 V
$I_{GSS}$	$V_{GS} = \pm 30\text{V}$ , $V_{DS} = 0\text{V}$			$\pm 100$ nA
$I_{GSM}$	$V_{GS} = V_{DS(on)}$ , $V_{GS} = 0\text{V}$ $T_J = 125^\circ\text{C}$			50 $\mu\text{A}$ 3 mA
$R_{DS(on)}$	$V_{GS} = 10\text{V}$ , $I_D = 0.5 * I_{DSS}$ , Note 1			40 m $\Omega$

**N-Channel Enhancement Mode Avalanche Rated Fast Intrinsic Diode**

**Symbol**



**TO-247**



G = Gate      D = Drain  
S = Source      Tab = Drain

**Features**

- International Standard Package
- Low  $R_{DS(on)}$  and  $C_o$
- Avalanche Rated
- Low Package Inductance

**Advantages**

- High Power Density
- Easy to Mount
- Space Savings

**Applications**

- Switch-Mode and Resonant-Mode Power Supplies
- DC-DC Converters
- PFC Circuits
- AC and DC Motor Drives
- Robotics and Servo Controls

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DS100673(7/15)

Figure 13: Datasheet summary for IXFH80N65X2 Ultra-Junction MOSFET.

## A.2 TLP250 Gate Driver

Key parameters used in the gate resistor selection ( $I_{peak}$ ,  $V_{CC}$  range).

**TOSHIBA** **TLP250**

TOSHIBA Photocoupler GaAlAs Ired & Photo-IC

**Transistor Inverter**  
**Inverter For Air Conditionor**  
**IGBT Gate Drive**  
**Power MOS FET Gate Drive**

The TOSHIBA TLP250 consists of a GaAlAs light emitting diode and a integrated photodetector.  
This unit is 8-lead DIP package.  
TLP250 is suitable for gate driving circuit of IGBT or power MOS FET.

- Input threshold current:  $I_F=5\text{mA}(\text{max.})$
- Supply current ( $I_{CC}$ ):  $11\text{mA}(\text{max.})$
- Supply voltage ( $V_{CC}$ ):  $10\text{-}35\text{V}$
- Output current ( $I_O$ ):  $\pm 1.5\text{A}$  (max.)
- Switching time ( $t_{PLH}/t_{PHL}$ ):  $1.5\mu\text{s}(\text{max.})$
- Isolation voltage:  $2500\text{VRms}(\text{min.})$
- UL recognized: UL1577, file No.E67349
- Option (D4) type  
VDE approved: DIN VDE0884/06.92,certificate No.76823  
Maximum operating insulation voltage:  $630\text{VPK}$   
Highest permissible over voltage:  $4000\text{VPK}$

(Note) When a VDE0884 approved type is needed,  
please designate the "option (D4)"

- Creepage distance:  $6.4\text{mm}(\text{min.})$
- Clearance:  $6.4\text{mm}(\text{min.})$

**Schematic**

A  $0.1\mu\text{F}$  bypass capacitor must be connected between pin 8 and 5 (See Note 5).

**Pin Configuration (top view)**

1	N.C.
2	Anode
3	Cathode
4	N.C.
5	GND
6	$V_O$ (Output)
7	$V_O$
8	$V_{CC}$

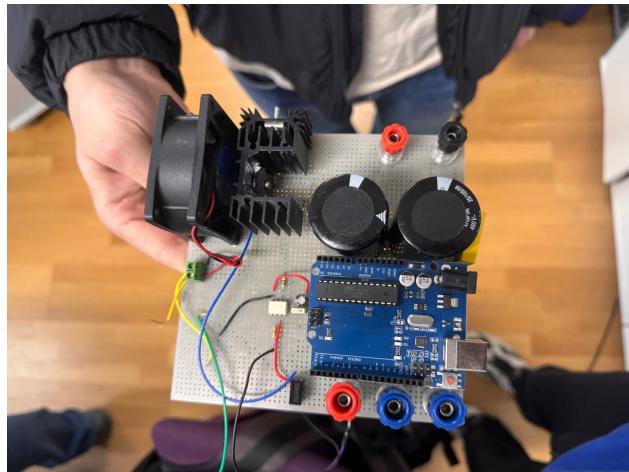
**Truth Table**

	Tr1	Tr2
Input LED	On	On
Off	Off	On

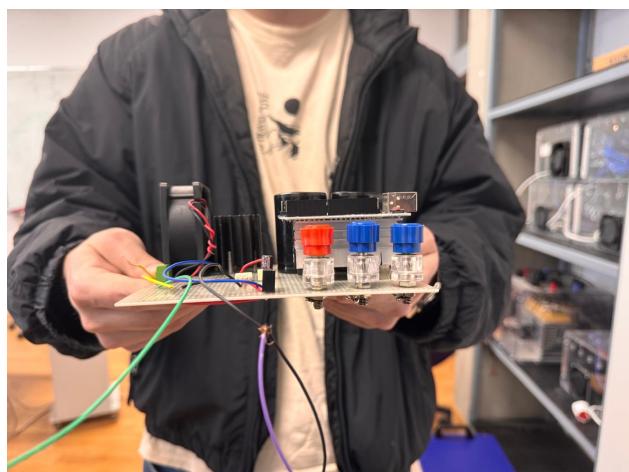
Figure 14: Specifications for Toshiba TLP250 Optocoupler.

## B Mechanical Construction

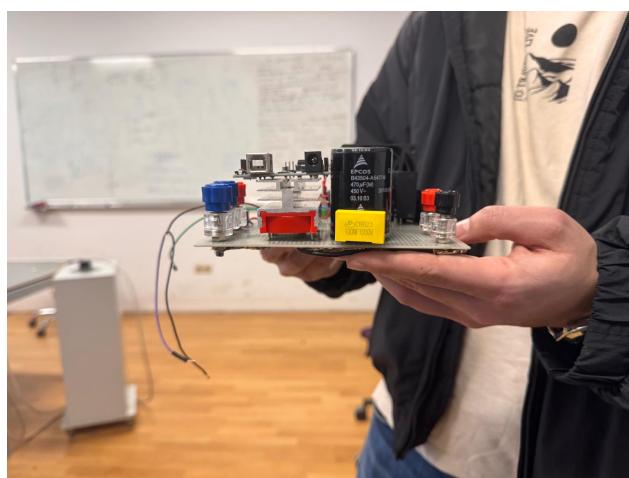
Additional views of the prototype hardware.



(a) Top View



(b) Front View



(c) Side View

Figure 15: Detailed mechanical views of the prototype.

## C Project Team



Figure 16: The "Buck ve Ötesi" team during the successful "Tea Bonus" demonstration.