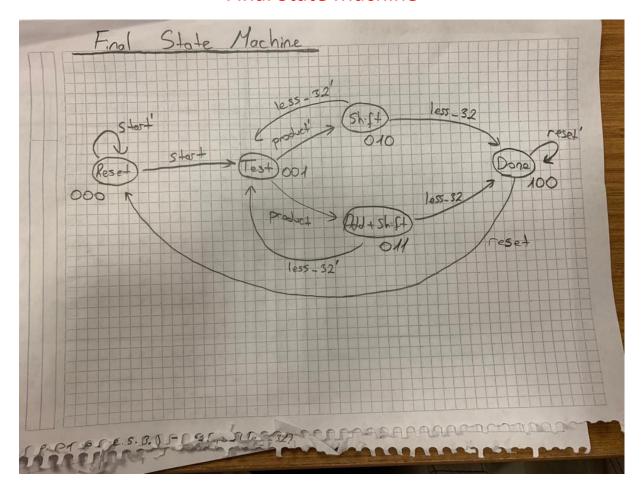
#### **Final State Machine**



# **Missing Part**

In the 1st part, I designed the control and datapath components. However, I couldn't make the connection. However, I done separate testbenches of control and dataPath components.

That's why there is no MULT on the ALU.

# **Truth Table**

52 51	Sol	0.1.	Maria de la companya della companya					Ve	stput	
The second secon		Product	less_32	reset	Stort	N <sub>2</sub>	NA	No	Shift Right	Write
0 0	0	X	×	×	0	0	0	0	0	0
0 0	0	X	×	×	1	0	0	1	0	0
0 0	1	0	X	×	X	0	1	0	0	0
0 0	1	1	X	X	X	0	1	1	0	0
)   1	0	X	0	×	X	0	0	1	1	0
) 1	0	X	1	X	Х	1	0	0	1	0
1	1	×	0	X	X	0	0	1	1	1
0 1	1	X	1.	X	X	1	0	0	1	1
0	0	X	X	0	X	1	0	0	0	0
10	0	X	X	1	X	0	0	01	0	0

# Karnough Maps

S2, S1, S0	product, less,_32, reset, start	0000	0001	0011	0010	0110	0111	0101	0100	1100	1101	1111	1110	1010	1011	1001	1000
000		0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
001		0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
011		1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1
010		1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1
100		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
101		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
111		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
110		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

N0= S2' S1' S0' (start) + S2' S1' S0 (product) + S2' S1 (less\_32)'

S2, S1, S0	product, less,_32, reset, start	0000	0001	0011	0010	0110	0111	0101	0100	1100	1101	1111	1110	1010	1011	1001	1000
000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
001		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
011		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
010		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
100		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
101		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
111		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
110		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

N1 = S2' S1' S0

	product, less,_32, reset, start	0000	0001	0011	0010	0110	0111	0101	0100	1100	1101	1111	1110	1010	1011	1001	1000
S2, S1, S0																	
000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
001		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
011		0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
010		0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
100		1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1
101		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
111		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
110		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

#### **Test Benches**

#### Half Adder (1 bit)

```
# Loading work.half adder testbench
# Loading work.half_adder
add wave -position insertpoint \
sim:/half_adder_testbench/A \
sim:/half_adder_testbench/B \
sim:/half_adder_testbench/R \
sim:/half_adder_testbench/carry_out
# ** Warning: (vsim-WLF-5000) WLF file currently in use: vsim.wlf
            File in use by: Yunus Emre Hostname: DESKTOP-E04VNT1 ProcessID: 16260
            Attempting to use alternate WLF file "./wlft3we6ga".
# ** Warning: (vsim-WLF-5001) Could not open WLF file: vsim.wlf
            Using alternate file: ./wlft3we6ga
VSIM 6> step -current
# time = 0, A =1, B=0, Sum=1, carry Out=0
# time = 20, A =0, B=0, Sum=0, carry Out=0
VSIM 7>
```

#### Full Adder (1 bit)

```
Transcript
# Loading work.half_adder
add wave -position insertpoint \
sim:/full_adder_testbench/A \
sim:/full_adder_testbench/B \
sim:/full_adder_testbench/carry_in \
sim:/full_adder_testbench/R \
sim:/full_adder_testbench/carry_out
# ** Warning: (vsim-WLF-5000) WLF file currently in use: vsim.wlf
             File in use by: Yunus Emre Hostname: DESKTOP-E04VNT1 ProcessID: 16260
             Attempting to use alternate WLF file "./wlft4xdhw4".
# ** Warning: (vsim-WLF-5001) Could not open WLF file: vsim.wlf
             Using alternate file: ./wlft4xdhw4
VSIM 7> step -current
# time = 0, A =1, B=0, Sum=0, carry In=1, carry Out=1
# time = 20, A =1, B=1, Sum=0, carry In=0, carry Out=1
VSIM 8>
```

#### MyAdder (32 bit)

#### Full Sub (1 bit)

```
# Loading work.full_Sub
add wave -position insertpoint \
sim:/full_Sub_testbench/A \
sim:/full_Sub_testbench/B \
sim:/full_Sub_testbench/carry_in \
sim:/full_Sub_testbench/carry_out

# ** Warning: (vsim-WLF-5000) WLF file currently in use: vsim.wlf

# File in use by: Yunus Emre Hostname: DESKTOP-E04VNT1 ProcessID: 16260

# Attempting to use alternate WLF file "./wlft8sht64".

# ** Warning: (vsim-WLF-5001) Could not open WLF file: vsim.wlf

# Using alternate file: ./wlft8sht64

# Using alternate file: ./wlft8sht64
```

#### MySubber (32 bit)

### Xor4x1 (8 bit)

```
# vsim work.Xor4xl_testbench

# Loading work.Xor4xl_testbench

# Loading work.Xor4xl_testbench

# Loading work.Xor4xl_testbench/A \

sim:/Xor4xl_testbench/A \

sim:/Xor4xl_testbench/B \

sim:/Xor4xl_testbench/B \

sim:/Xor4xl_testbench/R

# ** Warning: (vsim-WLF-5000) WLF file currently in use: vsim.wlf

# File in use by: Yunus Emre Hostname: DESKTOP-E04VNT1 ProcessID: 16260

# Attempting to use alternate WLF file "./wlftc2tzxs".

# ** Warning: (vsim-WLF-5001) Could not open WLF file: vsim.wlf

# Using alternate file: ./wlftc2tzxs

# VSIM 5> step -current

# time = 0, A =00001111, B=00000001, R=00001110

# time = 20, A =00000000, B=00001111, R=00001111

VSIM 6>
```

#### MyXor (32 bit)

#### Nor4x1 (8 bit)

## MyNor (32 bit)

#### And4x1 (8 bit)

```
transcript

f vsim work.And4xl_testbench

f Loading work.And4xl_testbench

f Loading work.And4xl
    add wave -position insertpoint \
    sim:/And4xl_testbench/A \
    sim:/And4xl_testbench/B \
    sim:/And4xl_testbench/R

    ** Warning: (vsim-WLF-5000) WLF file currently in use: vsim.wlf

f    ** File in use by: Yunus Emre Hostname: DESKTOP-E04VNT1 ProcessID: 16260

f    Attempting to use alternate WLF file "./wlft0ckhbf".

f ** Warning: (vsim-WLF-5001) Could not open WLF file: vsim.wlf

f    Using alternate file: ./wlft0ckhbf

f    Using alternate file: ./
```

#### MyAnd (32 bit)

#### Or4x1 (8 bit)

```
# vsim work.Or4xl_testbench

# Loading work.Or4xl_testbench

# Loading work.Or4xl_testbench

# Loading work.Or4xl_testbench/B 

sim:/Or4xl_testbench/B \

sim:/Or4xl_testbench/B \

sim:/Or4xl_testbench/R

# ** Warning: (vsim-WLF-5000) WLF file currently in use: vsim.wlf

# File in use by: Yunus Emre Hostname: DESKTOP-E04VNT1 ProcessID: 16260

# Attempting to use alternate WLF file "./wlftnlv3rq".

# ** Warning: (vsim-WLF-5001) Could not open WLF file: vsim.wlf

# Using alternate file: ./wlftnlv3rq

# VSIM 5> step -current

# time = 0, A =00001111, B=00000001, R=00001111

# time = 20, A =00000000, B=00001111, R=00000111
```

#### MyOr (32 bit)

## Mux2x1 (1 bit)

# Mux32x1 (32 bit)

#### Mux8x3 (1 bit)

```
| Sim:/mux8x3_testbench/R

VSIM 6> step -current

# time = 0, D0 =1, D1=0, D2=0, D3=0, D4=0, D5=0, D6=0, D7=0, S=000, R=1

# time = 20, D0 =0, D1=1, D2=0, D3=0, D4=0, D5=0, D6=0, D7=0, S=001, R=1

# time = 40, D0 =0, D1=0, D2=1, D3=0, D4=0, D5=0, D6=0, D7=0, S=010, R=1

# time = 60, D0 =0, D1=0, D2=0, D3=1, D4=0, D5=0, D6=0, D7=0, S=011, R=1

# time = 80, D0 =0, D1=0, D2=0, D3=0, D4=1, D5=0, D6=0, D7=0, S=100, R=1

# time = 100, D0 =0, D1=0, D2=0, D3=0, D4=1, D5=0, D6=0, D7=0, S=101, R=1

# time = 120, D0 =0, D1=0, D2=0, D3=0, D4=0, D5=1, D6=0, D7=0, S=101, R=1

# time = 140, D0 =0, D1=0, D2=0, D3=0, D4=0, D5=0, D6=1, D7=0, S=110, R=1

# time = 140, D0 =0, D1=0, D2=0, D3=0, D4=0, D5=0, D6=0, D7=1, S=111, R=1
```

#### Mux32bit8x3 (32 bit)

#### ALU (32 bit)

### SetLessThan (32 bit)

# 1.Part Test Benches

#### Control

```
# time = 0, S=xxx, N=xxx, ShitfRight=x, Write=x
# time = 5, S=000, N=000, ShitfRight=0, Write=0
# time = 10, S=000, N=001, ShitfRight=0, Write=0
# time = 15, S=001, N=001, ShitfRight=0, Write=0
# time = 25, S=001, N=100, ShitfRight=0, Write=1
# time = 35, S=000, N=000, ShitfRight=0, Write=1
# time = 35, S=000, N=000, ShitfRight=0, Write=0
# ** Note: $finish : D:/Emre/OneDrive - GTÜ/Masaüstü/ALU/control_testbench.v(44)
# Time: 40 ps Iteration: 0 Instance: /control_testbench
# 1
# Break in Module control_testbench at D:/Emre/OneDrive - GTÜ/Masaüstü/ALU/control_testbench.v line 44
```

# Right Shift (64 bit)

# Less32Bit (check if the product less 32 bit)

# Set64bit (create a product with multiplier)