Assignment 21: Generate Half Wave rectifier signal using Single Port ROM, using a given COE file.

Code

```
(* CORE_GENERATION_INFO = "design_1,IP_Integrator,{x_ipVendor=xilinx.com,x_ipLibrary=BlockDiagram,x_ipName=design_1,x_ipVersion=1.00.a,x_ipLanguage=VERILOG,numBlks=2,numReposBlks=2,numNonXlnx
module design_1
   (clk,
    douta_0,
    en);
  (* X_INTERFACE_INFO = "xilinx.com:signal:clock:1.0 CLK.CLK CLK" *) (* X_INTERFACE_PARAMETER = "XIL_INTERFACENAME CLK.CLK, CLK_DOMAIN design_1_clka_0, FREQ_HZ 100000000, FREQ_TOLERANCE_HZ 0,
  output [7:0]douta_0;
  input en;

  wire [7:0]blk_mem_gen_0_douta;
  wire [9:0]c_counter_binary_0_Q;
  wire clka_0_1;
  wire ena_0_1;

  assign clka_0_1 = clk;
  assign douta_0[7:0] = blk_mem_gen_0_douta;
  assign ena_0_1 = en;
  design_1_blk_mem_gen_0_1 blk_mem_gen_0
       (.addra(c_counter_binary_0_Q),
        .clka(clka_0_1),
        .douta(blk_mem_gen_0_douta),
        .ena(ena_0_1));
  design_1_c_counter_binary_0_1 c_counter_binary_0
       (.CE(ena_0_1),
        .CLK(clka_0_1),
        .Q(c_counter_binary_0_Q));
endmodule
```

Simulation