Assignment 14: Design a Full Subtractor with Gate Level Modeling Style.

Code

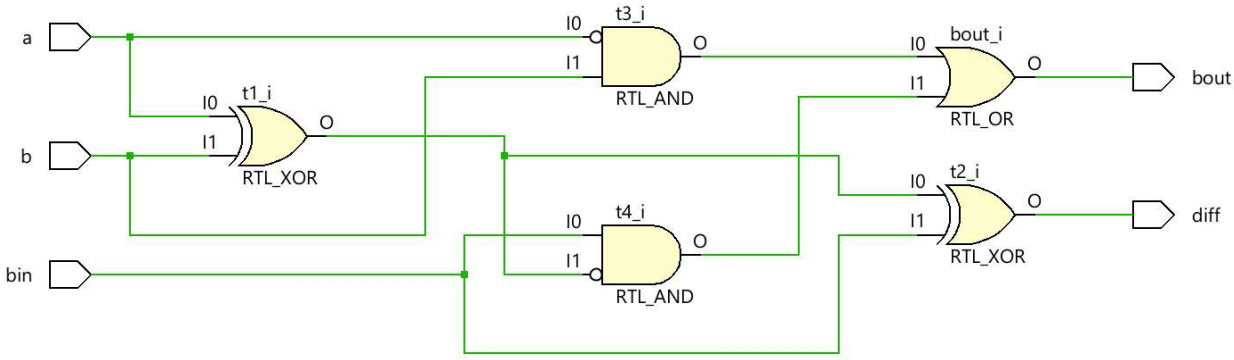
ELABORATED DESIGN - xc7z010clg400-1

Project Summary | top.v | Schematic | Schematic (2)

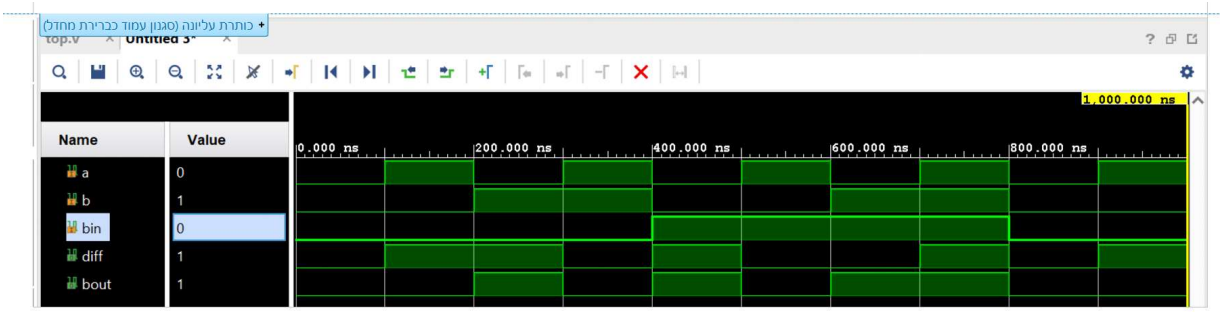
E:/XLINIX/viv_projects/assigment_a132/assigment_a132.srcs/sources_1/new/top.v

```
1  `timescale 1ns / 1ps
2
3
4  module top(
5      input a,b ,bin,
6      output diff, bout
7      );
8
9  wire t1, t2, t3, t4, t5;
10
11 assign t1   = a ^ b;
12 assign t2   = t1 ^ bin;
13 assign diff = t2;
14 assign t3   = ~a & b;
15 assign t4   = bin & ~t1;
16 assign bout = t3 | t4 ;
17
18 endmodule
19
```

Schematic



Simulation and Full Subtractor Truth table



								y
a	0	1	0	1	0	1	0	1
b	0	0	1	1	0	0	1	1
bin	0	0	0	0	1	1	1	1
Diff	0	1	1	0	1	0	0	1
bout	0	0	1	0	1	0	1	1