

## Assignment 24: Design FSM for Moore Machine.

Code:

```
1 timescale 1ns / 1ps
2
3 module moo(
4     input clk, rst, din,
5     output reg dout
6 );
7     parameter idle = 0;
8     parameter s0 = 1;
9     parameter s1 = 2;
10    parameter s2 = 3;
11    parameter s3 = 4;
12    parameter s4 = 5;
13
14    reg [2:0] state=idle,nstate=idle;
15
16    always@(posedge clk)
17    begin
18        if(rst == 1'b1)
19            state <= idle;
20        else
21            state <= nstate;
22        end
23
24    always@(state,din)
25    begin
26        case(state)
27            idle : begin
28                nstate = s0; // Corrected transition
29                dout = 1'b0;
30            end
31            s0: begin
32                nstate = (din == 1'b1) ? s1 : s0;
33                dout = 1'b0;
34            end
35            s1: begin
36                nstate = (din == 1'b0) ? s2 : s1;
37                dout = 1'b0;
38            end
39            s2: begin
40                nstate = (din == 1'b0) ? s3 : s1;
41                dout = 1'b0;
42            end
43            s3: begin
44                nstate = (din == 1'b1) ? s4 : s0;
45                dout = 1'b0;
46            end
47            s4: begin
48                nstate = (din == 1'b0) ? s1 : s0;
49                dout= 1'b1;
50            end
51            default : nstate = idle;
52        endcase
53    end
54
55 endmodule
```

Simulation:

