

Assignment 6: Write a Verilog Code to Initialize Variable a to decimal value of 12, b to octal value of 345 and c to binary value of 100.

The image shows a Verilog code editor window and a Tcl console window. The Verilog code defines a testbench module 'tb' with three registers: 'a' (4-bit), 'b' (8-bit), and 'c' (3-bit). Register 'a' is initialized to decimal 12, 'b' to octal 345, and 'c' to binary 100. The code includes three \$display statements to show the values of 'a', 'b', and 'c' in decimal, octal, and binary formats respectively, along with the current time.

```
1 module tb;
2
3 // Declare a 4-bit register 'a' with an initial value of 0
4 reg [7:0] a; // decimal value of 12
5 reg [7:0] b; // octal value of 354
6 reg [2:0] c; // binary value of 100
7
8
9 initial begin
10     a = 8'd12; // Set 'a' to binary 1001
11     b = 8'o345; // Set 'a' to binary 0001
12     c = 3'b100; // Set 'a' to binary 1010
13     #1
14     $display("Value of a_d : %d @ %0t",a, $time); // Display the value of 'a' in decimal format, along with the current time
15     $display("Value of b_d : %o @ %0t",b, $time); // Display the value of 'a' in decimal format, along with the current time
16     $display("Value of c_d : %b @ %0t",c, $time); // Display the value of 'a' in decimal format, along with the current time
17 end
18
19 endmodule
20
21
```

The Tcl console window shows the simulation results, including warnings, completion messages, and the final values of 'a', 'b', and 'c' in decimal, octal, and binary formats respectively, along with the current time.

```
Tcl Console x Messages Log
WARNING: [XSIM 43-4100] "E:/XLINIX/viv_projects/tb_test/tb_test.sim/sim_1/behav/xsim/glbl.v" Line 6. Module glbl has a timescale but at least one module in design does not.
WARNING: [XSIM 43-4100] "E:/XLINIX/viv_projects/tb_test/tb_test.sim/sim_1/behav/xsim/glbl.v" Line 6. Module glbl has a timescale but at least one module in design does not.
Completed simulation data flow analysis
Time Resolution for simulation is 1ps
Compiling module xil_defaultlib.tb
Compiling module xil_defaultlib.glbl
Built simulation snapshot tb_behav
INFO: [USF-XSim-69] 'elaborate' step finished in '2' seconds
Time resolution is 1 ps
Value of a_d : 12 @ 1000
Value of b_d : 345 @ 1000
Value of c_d : 100 @ 1000
relaunch_sim: Time (s): cpu = 00:00:01 ; elapsed = 00:00:07 . Memory (MB): peak = 1694.977 ; gain = 0.000
Type a Tcl command here
```

21:1 Insert Verilog