## Assignment 28: Implement 4-bit Down counter with Reset and Load Control pin

1) When user apply active high to reset counter output must be 4'b0000
2) Counter should work when Reset is having value of Active Low
3) When user apply active high to load it should start counting from the user loaded value 4) If user have not loaded any value then it should start counting from 0

## Code:

```
1  `timescale 1ns / 1ps
2
3  module counter(
4      input rst, clk, ld, [3:0] ldvalue,
5      output [3:0] res);
6
7  reg [3:0] temp;
8
9  always@(posedge clk or posedge rst) begin
10     if(rst == 1'b1)
11         begin
12             temp <= 4'b0000;
13         end
14     else
15         begin
16         if (ld == 1'b1)
17             temp <= ldvalue;
18         else
19             begin
20                 temp <= temp - 1'b1;
21             end
22         end
23     end
24
25 assign res = temp;
26
27 endmodule
28
```

## Simulation: