Assignment_18: Design 8:1 Mux using 2:1 Mux

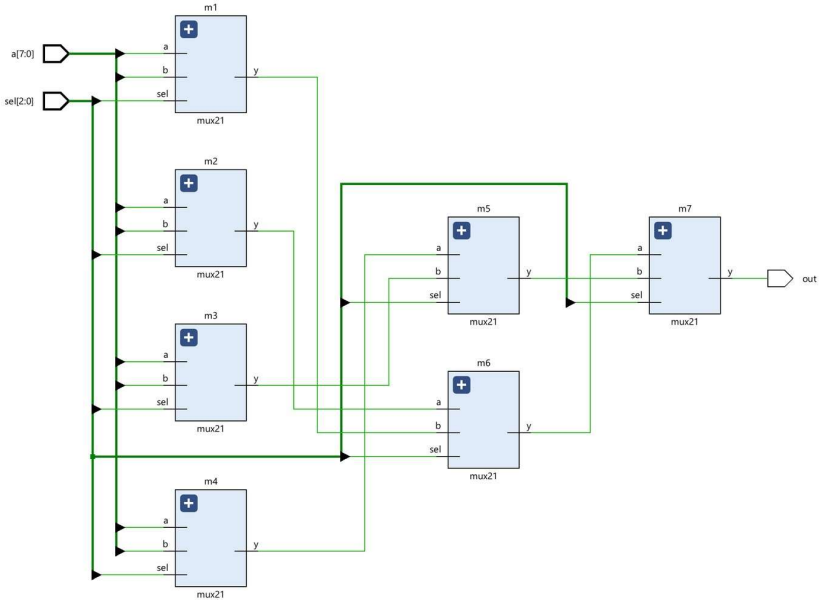
code

top.v | tb.v | Untitled 6*

E:/XLINIX/viv_projects/project_11/project_11.srcs/sources_1/new/top.v

```
module mux21
(
input a,b,sel,
output y
);

assign y = (sel == 1'b0) ? a : b;


endmodule


module top(
input [7:0] a,
input [2:0] sel,
output out
);

wire [3:0] t0;
wire [1:0] t1;
/// mux 8 to 4
mux21 m1 (.a(a[7]), .b(a[6]), .sel(sel[2]),.y(t0[0]));
mux21 m2 (.a(a[5]), .b(a[4]), .sel(sel[2]),.y(t0[1]));
mux21 m3 (.a(a[3]), .b(a[2]), .sel(sel[2]),.y(t0[2]));
mux21 m4 (.a(a[1]), .b(a[0]), .sel(sel[2]),.y(t0[3]));
/// mux 4 to 2
mux21 m5 (.a(t0[3]), .b(t0[2]), .sel(sel[1]),.y(t1[0]));
mux21 m6 (.a(t0[1]), .b(t0[0]), .sel(sel[1]),.y(t1[1]));
// mux 2 to 1
mux21 m7 (.a(t1[1]), .b(t1[0]), .sel(sel[0]),.y(out));

endmodule
```

Structural Schematic



Simulation