Assignment 30: Design a 4-bit Ring Counter such that MSB bit first becomes 1 instead of LSB.

Refer Ring Counter Circuit and Implement 4-bit Ring Counter such that MSB bit is set to 1 (HIGH) instead of LSB. so sequenc of values at Ring counter output must be 1000, 0100, 0010, 0001.

Code:

```
`timescale 1ns / 1ps

module ring_counter_4bit (
    input clk,
    input reset,
    output reg [3:0] q
);

  always @(posedge clk) begin
    if (reset) begin
      q <= 4'b1000; // Initial state on reset
    end else begin
      q <= {q[0], q[3], q[2], q[1]}; // Shift left
    end
  end

endmodule
```

Test Bench

```
`timescale 1ns / 1ps

module tb;

  reg clk, reset;
  wire [3:0] q;

  ring_counter_4bit dut (
    .clk(clk),
    .reset(reset),
    .q(q)
  );

  always #5 clk = ~clk;

  initial begin
    reset = 1'b1;
    clk   = 1'b0;
    #10;
    reset = 1'b0;
    #40;
    $finish;
  end

endmodule
```

Simulation