Assignment_12: Design a RTL for 8 x 3 Priority encoder whose truth table is mentioned in the Instructions tab.

code

```
module top (
  input  [7:0] D,  // Data inputs (D7 is MSB, D0 is LSB)
  output reg  [2:0] Q   // Encoded output (highest priority encoded)
);

  // Case statement for priority encoding
  always @(D) begin
    case (D)
      8'b00000000: Q <= 3'b000;  // No active bits (default)
      8'b00000000_10000000: Q <= 3'b000;  // D0 active
      8'b00000000_01000000: Q <= 3'b001;  // D1 active
      8'b00000000_00100000: Q <= 3'b010;  // D2 active
      8'b00000000_00010000: Q <= 3'b011;  // D3 active
      8'b00000000_00001000: Q <= 3'b100;  // D4 active
      8'b00000000_00000100: Q <= 3'b101;  // D5 active
      8'b00000000_00000010: Q <= 3'b110;  // D6 active
      8'b00000000_00000001: Q <= 3'b111;  // D7 active
      default: Q <= 3'bX;  // Unexpected input (optional - for debugging)
    endcase
  end

endmodule
```

Simulation