Assignment 16: Design 4-bit Johnson Counter using Structural Modeling style.

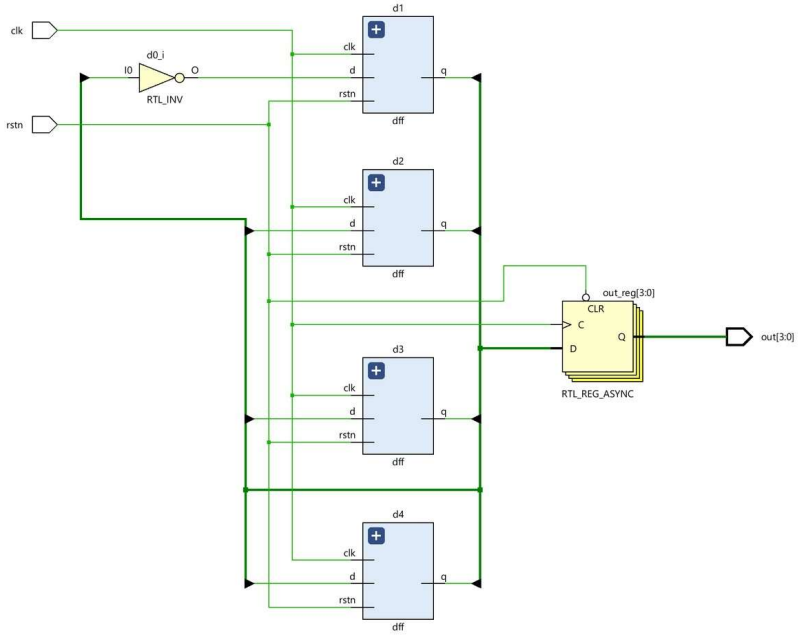
Code:

top.v | tb.v | Untitled 2*

E:/XILINIX/viv_projects/project_9/project_9.srcs/sources_1/new/top.v

```
module dff (
    input clk, rstn, d,
    output reg q
);
    always @(posedge clk or negedge rstn)
    begin
        if (~rstn)  // Note: Correcting the negation of rstn
            q <= 1'b0;
        else
            q <= d;
    end
endmodule

module top (
    input clk, rstn,
    output reg [3:0] out
);

    wire t0, t1, t2, t3;

    dff d1 (.clk(clk), .rstn(rstn), .d(~t3), .q(t0));
    dff d2 (.clk(clk), .rstn(rstn), .d(t0), .q(t1));
    dff d3 (.clk(clk), .rstn(rstn), .d(t1), .q(t2));
    dff d4 (.clk(clk), .rstn(rstn), .d(t2), .q(t3));

    always @(posedge clk or negedge rstn)
    begin
        if (~rstn)
            out <= 4'b0000;
        else
            out <= {t0, t1, t2, t3};  // Concatenate outputs of D flip-flops
    end

endmodule


}
```

Structural Schematic



Simulation