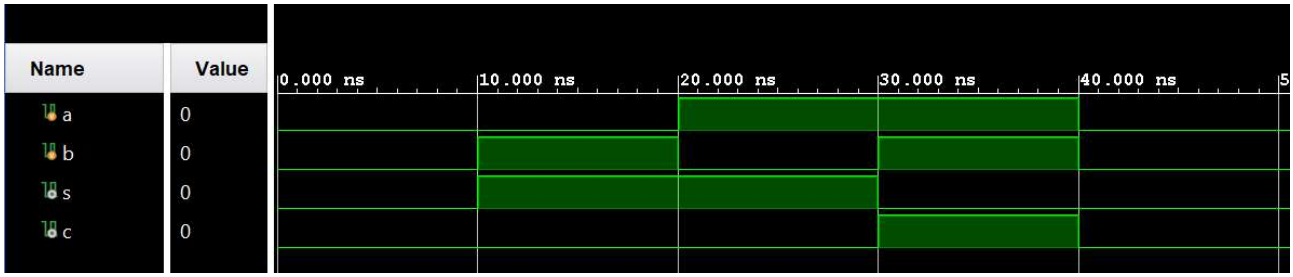
Assignment 1: Assume our half adder has input ports a, b, and Output ports as s,c. Use these ports to implement a Half adder in Verilog.

Code:

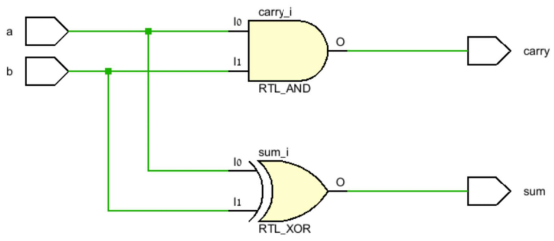
```
module half_addr(
input a,b,

output s, c

);

assign s = a ^ b;

assign c = a & b;

endmodule
```

Assignment 2: Use half adder code designed in the previous assignment and apply the manual stimulus to verify the functional behavior of the Design.



Assignment 3: Perform RTL analysis and Synthesis on the Half adder code designed in the Previous assignment and share your RTL and Technology Schematic.

RTL Schematic



Technology Schematic