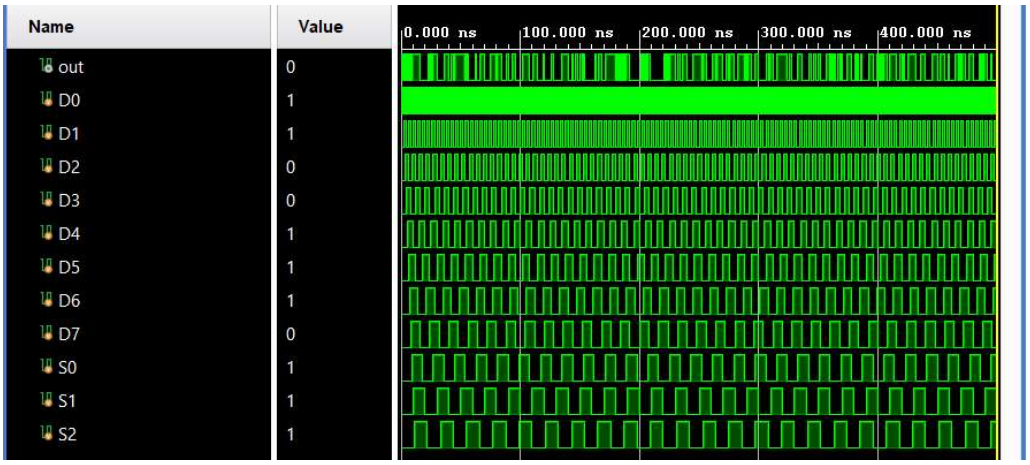
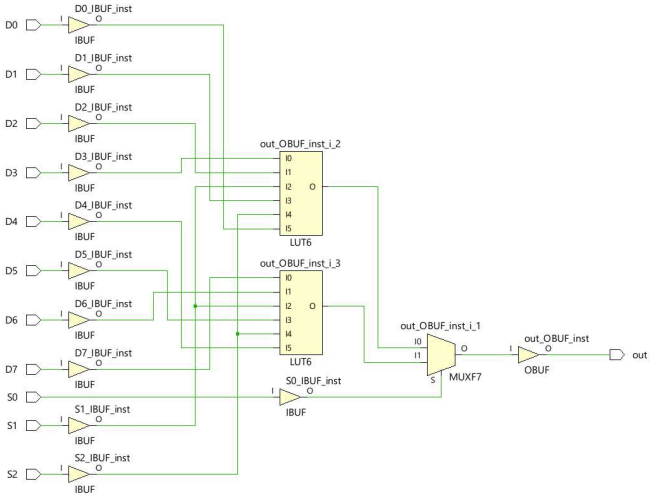
Assignment 5: Use the Design Code and Testbench code mentioned in the Instructions tab to demonstrate complete FPGA design flow. Perform each step such as Behavioral Simulation, I/O planning, Synthesis, Functional simulation after synthesis, perform Implementation

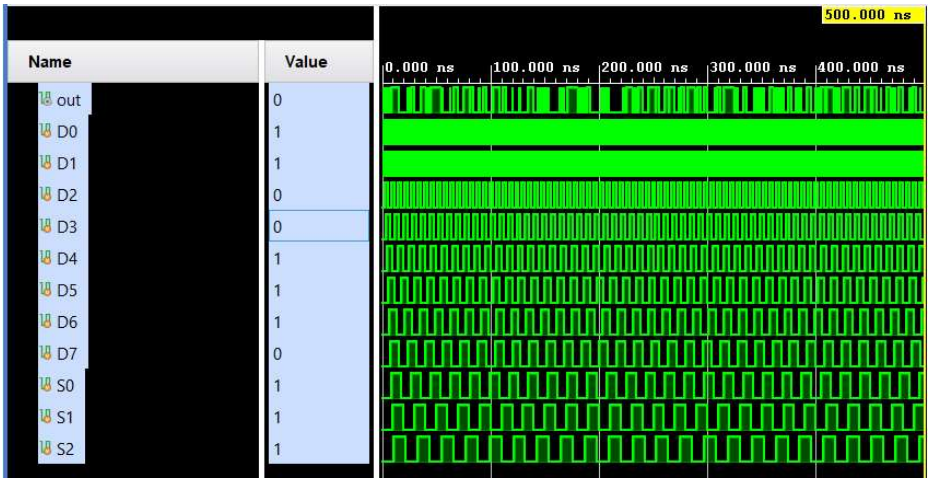
Behavioral Simulation



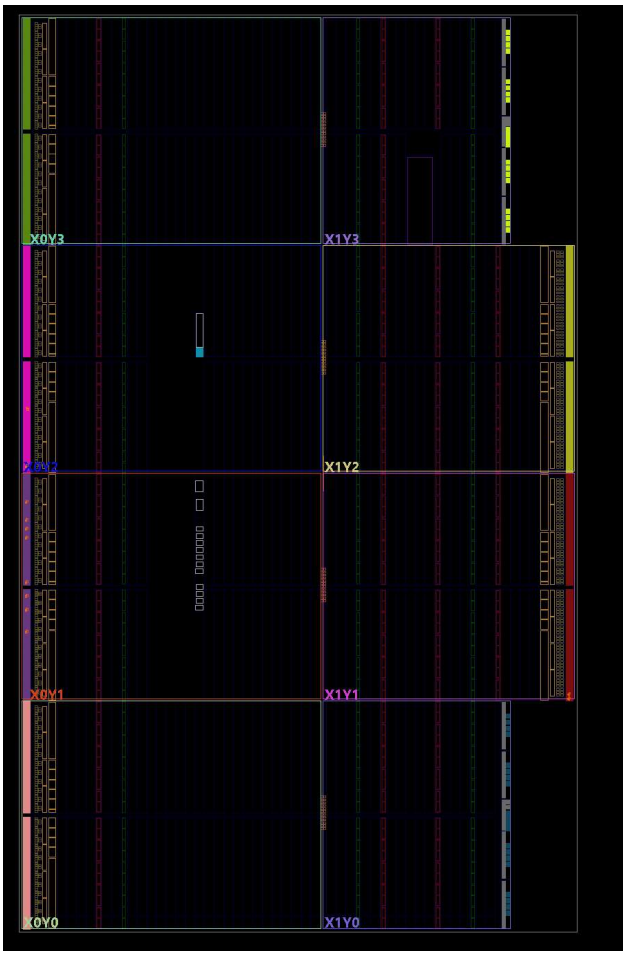
Technology Schematic



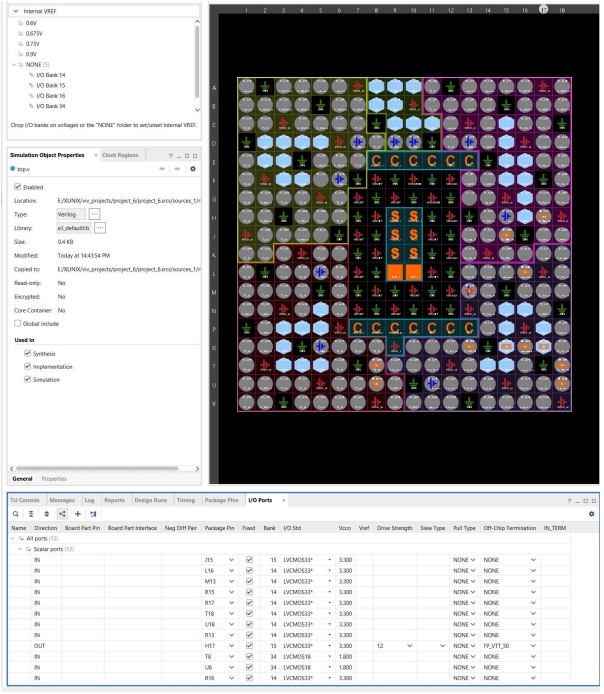
Post Analysis functional simulation



Implementation



I/O planning



Post Implementation functional simulation