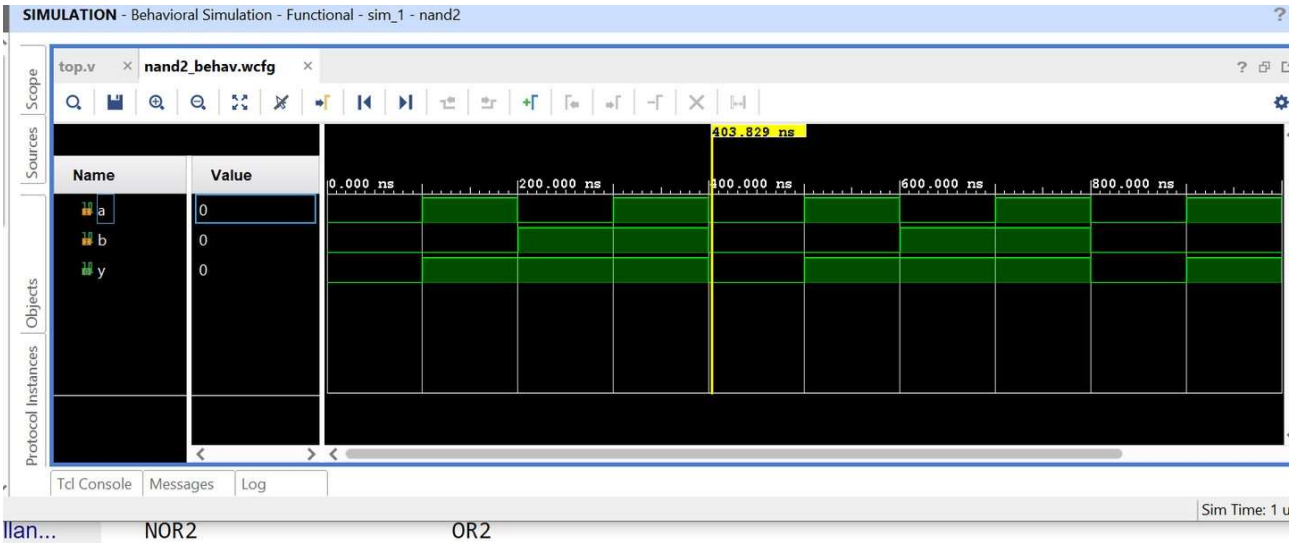
Assignment 15: Design 2-input OR gate with Switch Level Modeling Style.

1. Code

```
module nand2 (
input a,b,
output y
);

supply1 vdd;
supply0 gnd;
wire t1;
wire t2;

pmos p1 (t1, vdd, a);
pmos p2 (t2, t1,  b);

nmos n1 (t1, gnd, a);
nmos n2 (t2, gnd, b);

pmos p3 (y, vdd, t2);
nmos n3 (y, gnd, t2);

endmodule
```

2. waveform with or truth table for comparison



NOR2

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

OR2

A	B	Z
0	0	0
0	1	1
1	0	1
1	1	1