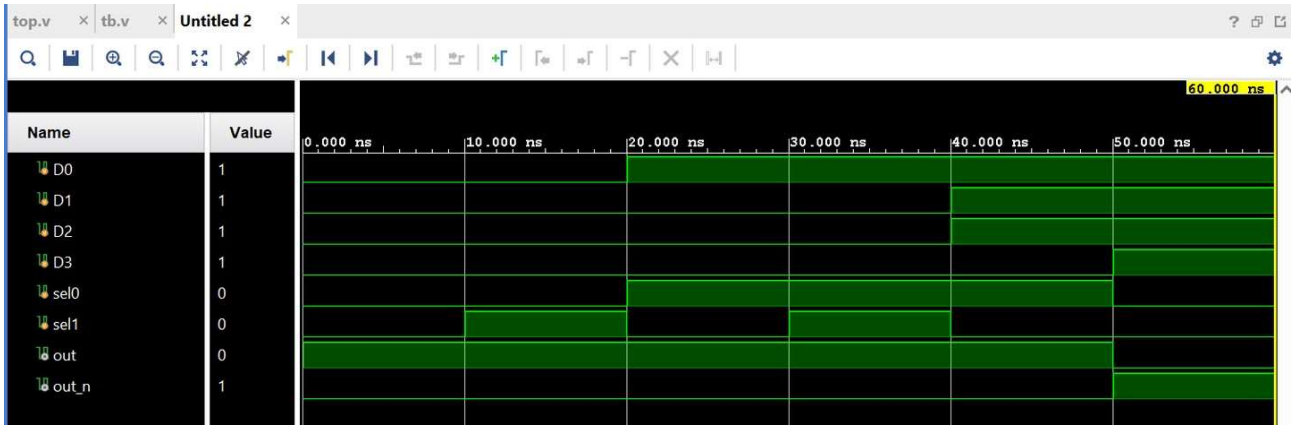
Assignment_10:

Take a help of the 2:1 Mux with complemented output design and try to implement 4:1 Mux with True and Complemented output.

Code:

```
`timescale 1ns / 1ps


module top(
    input D0,D1,D2,D3,sel0, sel1,
    output out, out_n
    );

wire y1, y2;

    assign y1    = ~(~sel0 & D0) | (sel0 & D1);
    assign y2    = ~(~sel0 & D2) | (sel0 & D3);
    assign out   = sel1 ? y2 : y1;
    assign out_n = ~out;

endmodule
```

Simulation



we can see that according to the selection switches, we can get the desired output, and complemented output as follows