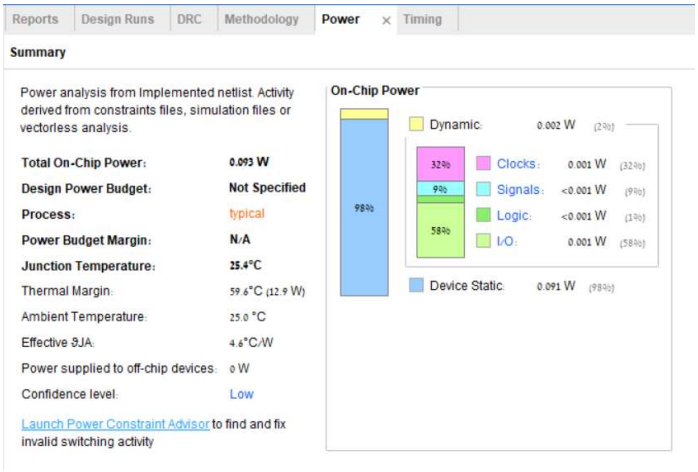
Assignment 4: Use the HDL code mentioned in the Instruction tab and add Power Optimization strategy before placement in the Implementation to observe changes in the Synthesized Schematic and Implemented Schematic. Share the Report Power Snapshot of both Synthesize and Implemented design. Use necessary Clock XDC.

Understanding of the Implementation Strategies.

Synthesis power consumption – Before optimization



Implementation power consumption – After optimization