

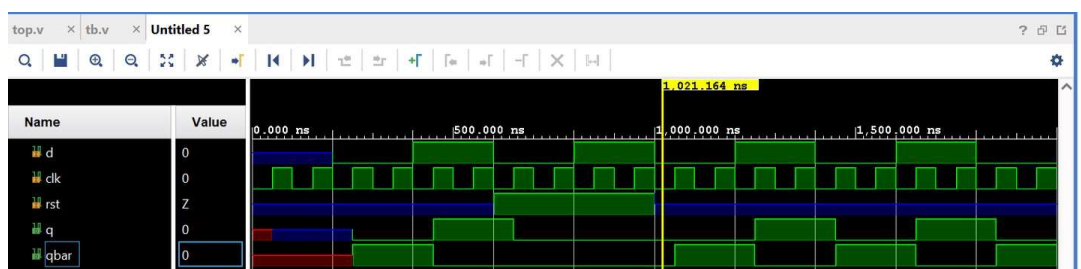
Assignment_11:

Implement D-Flipflop with Synchronous and Asynchronous Reset. Assume both True and complemented output pins are available in the D-Flipflop and it should send a value of '0' on the true output pin when the user applies Active High reset onto Flipflop.

code

```
SIMULATION - Behavioral Simulation - Functional - sim_1 - top
top.v x tb.v x Untitled 5 x
E:/XILINX/viv_projects/project_4/project_4_srcs/sources_1/new/top.v
1 timescale 1ns / 1ps
2
3 module top(
4     input d, clk, rst,
5     output reg q, reg qbar
6 );
7
8
9
10 always@(posedge clk or negedge rst) // asynchronous reset
11 begin
12     if (rst)
13     begin
14         q <= 1'b0;
15     end
16     else
17     begin
18         q <= d;
19         qbar <= ~d;
20     end
21 end
22
23
24 always@(posedge clk) // synchronous reset
25 begin
26     if (rst)
27     begin
28         q <= 1'b0;
29     end
30     else
31     begin
32         q <= d;
33         qbar <= ~d;
34     end
35 end
36
37 endmodule
```

Synchronous simulation



asynchronous simulation

