Assignment_9:

Create verilog code without I/O ports. Add two four bit reg variable in the code. Initialize the variable of 7 and F in hexadecimal format using blocking assignmnet operator. Add four bit reg type variable "res", store the result of xoring two reg variables initialized above in "res" using blocking assignment operator and always block. Make sure that you have added correct sensitivity list for always block. Perform Simulation and observe "res" has value of 8 in hexadecimal.