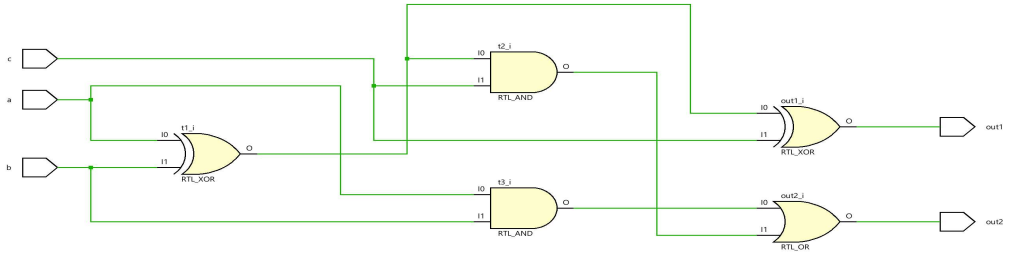
Assignment 13: Design a Circuit mentioned in the figure with Gate Level Modeling Style. Identify the Name of the Circuit by performing Behavioral Simulation.

The circuit in the task is a full adder

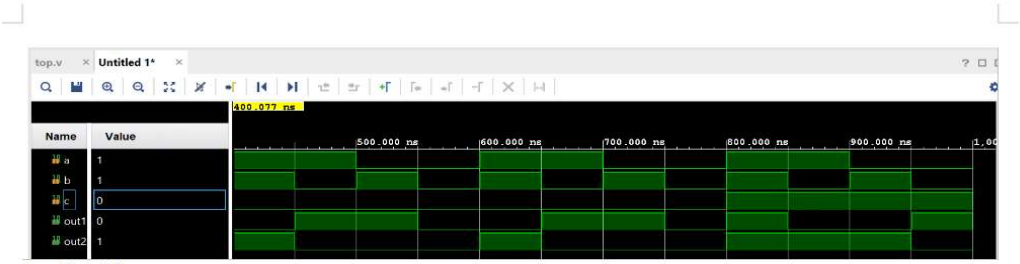
Code

```
`timescale 1ns / 1ps

module top(
    input a,b,c,
    output out1, out2
    );

wire t1, t2, t3;

assign t1 = a ^ b;
assign t2 = t1 & c;
assign t3 = a & b;
assign out1 = t1 ^ c;
assign out2 = t3 | t2;

endmodule
```

Gate Level Schematic



Simulation



Truth table

A	0	1	0	1	0	1	0	1
B	0	0	1	1	0	0	1	1
C	0	0	0	0	1	1	1	1
Out1	0	1	1	0	1	0	0	1
Out 2	0	0	0	1	0	1	1	1

and as it can be seen from the simulation the circuit functions as a full adder