Assignment 24: Design FSM for Moore Machine.

Code:

```
`timescale 1ns / 1ps

module moo(
  input clk, rst, din,
  output reg dout
  );
parameter idle = 0;
parameter s0 = 1;
parameter s1 = 2;
parameter s2 = 3;
parameter s3 = 4;
parameter s4 = 5;

reg [2:0] state=idle,nstate=idle;

always@(posedge clk)
begin
  if(rst == 1'b1)
    state <= idle;
  else
    state <= nstate;
end

always@(state,din)
begin
  case(state)
  idle : begin
    nstate = s0; // Corrected transition
    dout = 1'b0;
  end
  s0: begin
    nstate = (din == 1'b1) ? s1 : s0;
    dout = 1'b0;
  end
  s1: begin
    nstate = (din == 1'b0) ? s2 : s1;
    dout = 1'b0;
  end
  s2: begin
    nstate = (din == 1'b0) ? s3 : s1;
    dout = 1'b0;
  end
  s3: begin
    nstate = (din == 1'b1) ? s4 : s0;
    dout = 1'b0;
   end
  s4: begin
    nstate = (din == 1'b0) ? s1 : s0;
    dout= 1'b1;
  end
  default : nstate = idle;
  endcase
end

endmodule
```

Simulation: