**COMPHY\_112G**

**Calibration Top**

**R1.0**

**Macro Architecture Specification**

For Internal Use Only

Design Version V1.0

**Revision History**

|  |  |  |  |
| --- | --- | --- | --- |
| **Revision** | **Author** | **Change List** | **Date** |
| V1.0 |  |  |  |
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# **Introduction**

This document describes the firmware of calibration top.

# **2. Interafces**

## **2.1 Firmware Interface Signal**

|  |  |  |
| --- | --- | --- |
| **Port Name** | **Dir** | **Description** |
| cmx\_CAL\_DONE | O | Calibration done. |
| cmx\_EXT\_FORCE\_CAL\_DONE | I/O | Force to skip calibration. |
| cmx\_CAL\_START | I/O | Calibration start. |

## 

## **2.2 Digital Interface Signal**

|  |  |  |
| --- | --- | --- |
| **Port Name** | **Dir** | **Description** |
| PHY\_STATUS | O | The running status of PHY. |
| reg\_PIN\_PHY\_MODE\_RD\_2\_0 | I/O | PHY mode. |
| reg\_RX\_INIT\_DONE\_LANE | I/O | RX INIT done. |
| reg\_EOM\_CLK\_EN\_LANE | I/O | EOM CLK enable. |
| reg\_TSEN\_ADC\_RD\_REQ | I/O | TSEN RD request. |
| reg\_TSEN\_ADC\_RDY | I/O | TSEN ADC ready. |
| reg\_DTL\_FLOOP\_FREEZE\_LANE | I/O | DTL FLOOP Freeze. |
| reg\_PWRON\_SEQ\_LANE | I/O | Power On sequence. |
| reg\_RST\_FRAME\_SYNC\_DET\_CLK\_LANE | I/O | Reset Frame SYNC Detect. |
| reg\_PIN\_PLL\_READY\_RX\_LANE | I/O | PLL Ready RX. |
| reg\_PIN\_PLL\_READY\_TX\_LANE | I/O | PLL Ready TX. |
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## **2.3 Analog Interface Signal**

|  |  |  |
| --- | --- | --- |
| **Port Name** | **Dir** | **Description** |
| reg\_ANA\_TX\_IDLE\_FORCE\_LANE | I/O | TX IDLE force. |
| reg\_ANA\_TX\_IDLE\_LANE | I/O | TX IDKE. |
| reg\_ANA\_RX\_DTL\_LOOP\_FREEZE\_LANE | I/O | RX DTL Loop Freeze. |
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## **2.4 Time Flow**

Timing flow

# **Block Diagram**

## **Power On Calibration**



## **Cont Calibration**



# **FW Handling**

The calibration majorly is done in hard ware. The firmware does the PLL power on calibration and the VDD calibration. For the other calibrations, firmware only initializes for the calibration and starts unified core to do the calibration.

## **4.1** **Flow Chart**



## **4.2 Code Size**

# **Features**

The calibration top function has the following features.

1. Start calibrations;
2. Set registers.

# **Test Plan**

| **No** | **Description** |
| --- | --- |
| **1** | **Calibration starts.** |
| 1-1 | **Verify the calibration starts.**  Check the cmx\_CAL\_START. Covered by local test. |
| **2** | **Calibration done.** |
| 2-1 | **Verify the calibration done.**  Check the cmx\_CAL\_DONE. Covered by local test. |
| **3** | **Verify the registers** |
| 3-1 | **Verify the related registers programming properly**  Check the registers. Covered by local test. |
| **4** | **Verify the calibration after manually cal\_start and speed change** |
| 4-1 | **Verify the calibration after manually cal\_start.**  Check the calibration can start and finish after manually set cal\_start. Expect to be covered by DV test. |
| 4-2 | **Verify the calibration after speed change.**  Check the calibration can start and finish after speed change. Expect to be covered by DV test. |