**COMPHY\_112G**

**Speed Control**

**R1.0**

**Macro Architecture Specification**

For Internal Use Only

Design Version V1.0

**Revision History**

|  |  |  |  |
| --- | --- | --- | --- |
| **Revision** | **Author** | **Change List** | **Date** |
| Rev 1.0 | echeng | Initial draft | 03/26/2018 |
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# **Introduction**

This document describes the structure of speed table and how the firmware programs the speed table related register fields and perform speed change.

# **2. Interafces**

## **2.1 Firmware Interface Signal**

|  |  |  |
| --- | --- | --- |
| **Port Name** | **Dir** | **Description** |
| cmx\_PHY\_GEN\_MAX\_4\_0 | I/O | Max Gen speed |
| BYPASS\_SPDTBL\_LOAD | I/O | Bypass speed table load |
| lnx\_RXDCLK\_NT\_SEL\_LANE\_1\_0 | I/O | PIN\_RXDCLK\_NT Selection |

## 

## **2.2 Digital Interface Signal**

|  |  |  |
| --- | --- | --- |
| **Port Name** | **Dir** | **Description** |
| PHY\_STATUS | O | The running status of PHY. |
| reg\_ANA\_TRX\_PLL\_FBCK\_SEL\_LANE | I/O | PLL Feedback Clock Selection. |
| reg\_INIT\_TXFOFFS\_LANE\_12\_0\_b0 | I/O | Initial TX Frequency Offset Low Byte |
| eg\_INIT\_TXFOFFS\_LANE\_12\_0\_b1 | I/O | Initial TX Frequency Offset High Byte |
| reg\_SSC\_ACC\_FACTOR\_LANE | I/O | SSC Accumulator Factor internal |
| reg\_SSC\_STEP\_125PPM\_LANE\_3\_0 | I/O | SSC Step Value For 125PPM |
| reg\_SSC\_M\_LANE\_12\_0\_b0 | I/O | This field indicates how many clock cycles are contained in one 31.5 KHz period of SSC. Firmware sets this register based on value in speed table. |
| reg\_SSC\_M\_LANE\_12\_0\_b1 | I/O | This field indicates how many clock cycles are contained in one 31.5 KHz period of SSC. Firmware sets this register based on value in speed table. |
| reg\_TX\_PAM2\_EN\_LANE | I/O | Tx PAM2 Enable |
| reg\_TX\_HALFRATE\_EN\_LANE | I/O | Tx Half Rate Enable |
| reg\_TRAIN\_PAT\_NUM\_LANE\_9\_0\_b0 | I/O | Training Patten Number Including Frame Marker Low Byte. |
| reg\_TRAIN\_PAT\_NUM\_LANE\_9\_0\_b1 | I/O | Training Patten Number Including Frame Marker High Byte. |
| reg\_TX\_TRAIN\_PAT\_TOGGLE\_LANE | I/O | Toggle TX Training Pattern In Each Training Frame. |
| reg\_TX\_TRAIN\_PAT\_SEL\_LANE\_1\_0 | I/O | TX Training Pattern Select. |
| reg\_ETHERNET\_MODE\_LANE\_1\_0 | I/O | Ethernet Mode Enable. |
| reg\_TX\_TRAIN\_PAT\_MODE\_LANE | I/O | TX Training Pattern Mode |
| reg\_RX\_SELMUFI\_LANE\_3\_0 | I/O | Select Initial Multiple Frequency. |
| reg\_RX\_SELMUFF\_LANE\_3\_0 | I/O | Select Final Multiple Frequency. |
| reg\_DTL\_CLK\_MODE\_LANE\_1\_0 | I/O | DTL Clock Mode |
| reg\_RX\_FOFFSET\_EXTRA\_M\_LANE\_13\_0\_b0 | I/O | RX Frequency Offset Extraction SSC Frequency Low Byte. |
| reg\_RX\_FOFFSET\_EXTRA\_M\_LANE\_13\_0\_b1 | I/O | RX Frequency Offset Extraction SSC Frequency High Byte. |
| reg\_INIT\_RXFOFFS\_LANE\_12\_0\_b0 | I/O | Initial RX Frequency Offset Low Byte. |
| reg\_INIT\_RXFOFFS\_LANE\_12\_0\_b1 | I/O | Initial RX Frequency Offset High Byte. |
| reg\_DFE\_RATE\_MODE\_LANE\_1\_0 | I/O | DFE Full Rate Mode |
| reg\_DFE\_TAP\_SETTLE\_SCALE\_LANE\_1\_0\_b0 | I/O | Select Tap Settling Time Scale Factor Low Bit. |
| reg\_DFE\_TAP\_SETTLE\_SCALE\_LANE\_1\_0\_b1 | I/O | Select Tap Settling Time Scale Factor High Bit. |
| reg\_RX\_PAM2\_EN\_LANE | I/O | Rx PAM2 Enable. |
| reg\_RX\_HALFRATE\_EN\_LANE | I/O | Rx Half Rate Enable. |
| reg\_DFE\_PAM2\_MODE\_LANE | I/O | DFE PAM2 Mode. |
| reg\_DFE\_EN\_LANE | I/O | DFE Enable. |
| reg\_DFE\_DIS\_LANE | I/O | Disable DFE From Speed Table. |

## **2.3 Analog Interface Signal**

|  |  |  |
| --- | --- | --- |
| **Port Name** | **Dir** | **Description** |
| reg\_PLL\_REG\_SEL\_LANE\_2\_0 | I/O | Regulator Output Voltage High/low Speed Mode Selection. |
| reg\_FBDIV\_LANE\_7\_0 | I/O | PLL Feed-back Divider Ratio Low Byte. |
| reg\_FBDIV\_LANE\_9\_8 | I/O | PLL Feed-back Divider Ratio High Byte. |
| reg\_REFDIV\_LANE\_3\_0 | I | PLL Reference Divider Ratio. |
| reg\_VIND\_BAND\_SEL\_LANE | I/O | LC Tank Inductor Frequency Band Select. |
| reg\_DIV\_1G\_LANE\_7\_0 | I/O | ADC CLK Divider Ratio Low Byte. |
| reg\_DIV\_1G\_LANE\_9\_8 | I/O | ADC CLK Divider Ratio High Byte. |
| reg\_PLL\_ICP\_LANE\_4\_0 | I/O | PLL Charge Pump Current Control. |
| reg\_PLL\_LPFR\_LANE\_1\_0 | I/O | PLL Loop R Value Selection. |
| reg\_PLL\_LPFC\_LANE\_1\_0 | I/O | PLL Loop C2 Value Selection. |
| reg\_LCCAP\_USB\_LANE | I/O | LCVCO Capacitance USB. |
| reg\_TXSPEED\_DIV\_LANE\_2\_0 | I/O | Control TX Speed Divider. |
| reg\_TXREG\_SPEEDTRK\_CLK\_LANE\_2\_0 | I/O | Select Slave Regulator Size For TX Clock Path. |
| reg\_TXREG\_SPEEDTRK\_DATA\_LANE\_2\_0 | I/O | Select Slave Regulator Size For TX Data Path. |
| reg\_RXSPEED\_DIV\_LANE\_2\_0 | I/O | Control RX Speed Divider. |
| reg\_DTL\_CLK\_SPEEDUP\_LANE\_2\_0 | I/O | Controls Up-conversion Or Down-conversion Of DTL UP/DN Signals. |
| reg\_RXINTPI\_LANE\_3\_0 | I/O | Select RX Phase Interpolator Bias Current. |
| reg\_INTPR\_LANE\_1\_0 | I/O | Select RX Phase Interpolator Resistor. |
| reg\_DLL\_FREQ\_SEL\_LANE\_1\_0 | I/O | Coarse Control Of The Delay Of DLL. |
| reg\_EOM\_DLL\_FREQ\_SEL\_LANE\_1\_0 | I/O | Coarse Control Of The Delay Of EOM DLL. |
| reg\_RXREG\_SPEEDTRK\_CLK\_LANE\_2\_0 | I/O | Select Slave Regulator Size For RX Clock Path. |
| reg\_RXREG\_SPEEDTRK\_CLK\_HALF\_LANE | I/O | Reduce Slave Regulator Size When Clock Speed Is Halved. |
| reg\_RXREG\_SPEEDTRK\_DATA\_LANE\_2\_0 | I/O | Select Slave Regulator Size For RX Data Path. |
| reg\_RXCLK\_25M\_CTRL\_LANE\_1\_0 | I/O | Select Divider For 25MHz Clock Path. |
| reg\_RXCLK\_25M\_DIV1P5\_EN\_LANE | I/O | Enable Divide By 1.5 For 25MHz Clock Path. |
| reg\_RXCLK\_25M\_DIV\_LANE\_7\_0 | I/O | Select 25MHz N-Divider (N=32~255). |
| reg\_RXCLK\_25M\_FIX\_DIV\_EN\_LANE | I/O | Select Divider Operation for 25MHz N-Divider. |
| reg\_RXCLK\_NT\_FIX\_DIV\_EN\_LANE | I/O | Select Divider Operation for NT Clock N-Divider. |
| reg\_REG\_SELMUPI\_LANE\_3\_0 | I/O | Phase Loop Initial Coefficient. |
| reg\_REG\_SELMUPF\_LANE\_3\_0 | I/O | Phase Loop Final Coefficient. |
|  |  |  |

## **2.4 Time Flow**

Signals

|  |  |  |  |
| --- | --- | --- | --- |
| **Signal Name** | **Register** | **Read/Write** | **Interrupt?** |
| PIN\_PU\_PLL | reg\_rd\_pin\_pu\_pll\_lane | r | yes |
| PIN\_PU\_TX | reg\_rd\_pin\_pu\_tx\_lane | r | yes |
| PIN\_PU\_RX | reg\_rd\_pin\_pu\_rx\_lane | r | yes |
| PU\_PLL | reg\_ana\_pu\_pll\_lane | w | NA |
| PU\_RX | reg\_ana\_pu\_rx\_lane | w | NA |
| PU\_RX\_DLY | reg\_ana\_pu\_rx\_dly\_lane | w | NA |
| PU\_TX | reg\_ana\_pu\_tx\_lane | w | NA |
| PLL\_CLK\_READY | reg\_ana\_pll\_clk\_ready\_lane | w | NA |
| PIN\_PLL\_READY\_RX | reg\_pin\_pll\_ready\_rx\_lane | w | NA |
| PIN\_PLL\_READY\_TX | reg\_pin\_pll\_ready\_tx\_lane | w | NA |
| DTL\_FLOOP\_FREEZE | reg\_dtl\_floop\_freeze\_lane | w | NA |
| DTL\_LOOP\_FREEZE | reg\_ana\_rx\_dtl\_loop\_freeze\_lane | w | NA |
| DTL\_CLK\_OFF | reg\_dfe\_clk\_off\_lane | w | NA |
| DFE\_CLK\_OFF | reg\_dfe\_clk\_off\_lane | w | NA |
| DTX\_CLK\_OFF | reg\_dtx\_clk\_off | w | NA |
| RESET\_DTL | reg\_reset\_dtl\_lane | w | NA |
| RESET\_DTX | reg\_reset\_dtx\_lane | w | NA |
| RESET\_DFE | reg\_reset\_dfe\_lane | w | NA |
| phy\_cal\_done | Firmware variable | NA | NA |

Timing flow



# **Speed Table Structure**

The speed table data includes the data for PLL at one reference frequency and the data for all GENs. The speed table data is located in the last 1.5K address range of the xdata which is 4K bytes long.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Start address |  |  | |  |  |  |
| 0x6500 | lc\_pll\_PI0\_R0 | | | | | LC PLL\_PI0 |
|  | : | | | | |
|  | lc\_pll\_PI0\_R9 | | | | |
|  | lc\_pll\_PI1\_R0 | | | | | LC PLL\_PI1 |
|  | : | | | | |
|  | lc\_pll\_PI1\_R9 | | | | |
|  |  | | | | |
| 0x6750 | phy\_mode\_cmn | | | | |
|  | 0 | | | | | Null |
| 0x6770 | max\_gen | | min\_gen | 0 | 0 | Header |
|  | tx/rx | | | | | G0  …  G16 |
|  | 0 | | | | | Null |
| 0x6eb0 | phy\_mode\_lane | | | | | LANE CAL |
|  | 0 | | | | | Null |
|  |  |  | |  |  |  |

# **Interrupt Handling**

## **Interrupts**

|  |  |
| --- | --- |
| **Interrupt** | **Events** |
| Int2 | Speed change |

## **Sources**

The speed change interrupt is triggered by the signals PHY\_GEN\_TX/RX.

## **Mechanism**



# **FW Handling**

The FW programs the speed related register fields during power on process and speed change. The speed table data are loaded into memory at the corresponding addresses. The FW will read out the data and program the corresponding registers. The indices of speed table data are given in the file spdtb\_oft.h.

## **5.1** **Flow Chart**



## **5.2 Code Size**

The speed related FW size is 2.8k bytes.

# **Features**

The speed change function has the following features.

1. Handle the speed change request interrupt;
2. Program the control signals;
3. Program the speed related registers;
4. Calibrate PLL in the fast start mode.

# **Test Plan**

| **No** | **Description** |
| --- | --- |
| **1** | **PLL speed table load** |
| 1-1 | **Verify the data programmed correctly into the registers.**  Check the programmed values. Covered by local test. |
| **2** | **Gen speed table load** |
| 2-1 | **Verify the data programmed correctly into the registers.**  Check the programmed values. Covered by local test. |
| **3** | **Speed change** |
| 3-1 | **Verify the speed change interrupt handling**  Check the interrupt handling flow and timing. Covered by local test. |
| 3-2 | **Verify the speed change timing flow**  Check the timing in the flow chart in the section 2.4. Expect to be covered by DV test. |
| 3-3 | **Verify the TX/RX speed after speed change**  Check the registers after the speed change. Covered by local test. |
| 3-4 | **Verify speed change values for different TX and RX rate combinations**  Check the speed for TX and RX. Expected to be covered by DV test. |
|  |  |