**COMPHY\_112G**

**DLL Calibration**

**R1.0**

**Macro Architecture Specification**

For Internal Use Only

Design Version V1.0

**Revision History**

|  |  |  |  |
| --- | --- | --- | --- |
| **Revision** | **Author** | **Change List** | **Date** |
| V1.0 |  |  |  |
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# **Introduction**

This document describes the firmware of TX Align90 DCC calibration.

# **2. Interafces**

## **2.1 Firmware Interface Signal**

|  |  |  |
| --- | --- | --- |
| **Port Name** | **Dir** | **Description** |
| cmx\_DLL\_CAL\_EXT\_EN | O | External enable. |
| cmx\_EXT\_FORCE\_CAL\_DONE | I/O | Force to skip calibration. |
| lnx\_DLL\_CAL\_DONE\_LANE | I/O | TXDCC Calibration done. |
| lnx\_DLL\_CAL\_PASS\_LANE | I/O | TXDCC Calibration pass. |

## 

## **2.2 Digital Interface Signal**

|  |  |  |
| --- | --- | --- |
| **Port Name** | **Dir** | **Description** |
| PHY\_STATUS | O | The running status of PHY. |
| TXDCC\_EN\_LANE | I/O | TXDCC enable. |
| TX\_BYPASS\_ALIGN90 | I/O | TX bypass align90. |
| TX\_BYPASS\_DCC3 | I/O | TX bypass DCC3. |
| TX\_SPEED\_DIV\_LOCAL | I/O | TX speed DIV local. |
| TX\_ALIGN90\_DCC\_CAL\_TOP\_START | I/O | TX ALIGN90 DCC CAL start. |
| TX\_ALIGN90\_DCC\_CAL\_TOP\_DONE | I/O | TX ALIGN90 DCC CAL done. |
| TXDCC\_PDIV\_EN\_LANE | I/O | TXDCC PDIV Enable. |
| TX\_BYPASS\_DCC2 | I/O | TX bypass DCC2. |
|  |  |  |

## **2.3 Analog Interface Signal**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Port Name** | **Dir** | | **Default** | | **Description** | |
| RXDCC\_DLLCLK[6:0] | I | | 0 | | RXDCC\_DLLCLK[6] is sign bit:  1 -> VDCCP>VDCCN  0 -> VDCCP<VDCCN  RXDCC\_DLLCLK[5:0] is amplitude:  000000 -> smallest  …..  111111-> largest | |
| RXDCC\_EN\_DLLCLK | I | | 0 | | Enable the DCC resistor DAC  0 : disable  1 : enable | |
| CK\_CMPCAL\_DLL | I | | 0 | | Comparator auto zero clock  Its rising edge is also used to update the RXDCC\_DLLCLK[6:0] to the resistor DAC. | |
| DLL\_FREQ\_SEL[2:0] | I | | 111 | | DLL\_FREQ\_SEL[2:0] or EOM\_DLL\_FREQ\_SEL[2:0] is for frequency selection.  111: 14GHz  101: 12.5GHz  100: 10.3GHz  000: 8GHz | |
| EOM\_DLL\_FREQ\_SEL[2:0] |
| DLL\_GMSEL[2:0] | I | | 100 | | GMSEL[2:0] is for process calibration.  GMSEL[2:0]=111 initially and decrease by the state machine until the right GMSEL code is found. | |
| EOM\_DLL\_GMSEL[2:0] |
| SELLV\_RXDLL\_CH0/1/2/3[5:0] | I | | NA | | VDDA\_DLL or VDDA\_DLL\_EOM is continuously tracking for temperature variation by changing SELLV\_RXDLL\_CH0/1/2/3 (or SELLV\_RXEOMDLL\_CH0/1/2/3) code at VDDA\_DLL (or VDDA\_DLL\_EOM) regulator. If temperature is held constant, then SELLV\_RXDLL\_CH0/1/2/3 (or SELLV\_RXEOMDLL\_CH0/1/2/3) code will toggle between two fixed adjacent values. | |
| SELLV\_RXEOMDLL\_CH0/1/2/3[5:0] | |  | |  | |  |
| DLL\_PD\_SEL[2:0] | | I | | 000 | | Input CLK DCC, DLL and DLL\_EOM VDDA calibration input, and  DLL and DLL\_EOM phase detector outputs select  1xx: select input CLK DCC  000: select DLL phase detector output  001: select DLL\_EOM phase detector output  010: select DLL VDDA calibration input  011: select DLL\_EOM VDDA calibration input |
| EOM\_CLK\_EN | | I | | 0 | | This signal is not the direct input to DLL\_EOM. But is required for DLL\_EOM calibration.  0: Power off DLL\_EOM  1: Power on DLL\_EOM |
| VREF\_VDDADLL\_HALF\_SEL[3:0] | | I | | 0 | | reference voltage that is half of the DLL supply voltage , used to calibrate Gm with the temperature input:  4'b0000 --> 360mV  4'b0001 --> 370mV  ...  4'b1110 --> 500mV  4'b1111 --> 510mV |
| SHRTR\_TRXPLL | | I | | 0 | | SHRTR\_TRXPLL =1, when the DLL is on initial power up calibration, speed change or fast wake up.  For normal operation and continuous calibration is on for DLL, SHRTR\_TRXPLL =0 |
| DLL\_CAL\_CMP\_OUT | | O | | NA | | The output pin of the comparator  Shared with VCDL Control loop |

## **2.4 Time Flow**

# **Block Diagram**

# **FW Handling**

The firmware first initializes for the calibration, next starts the unicore and wait for the calibration to finish. After the calibration, the FW saves the calibration result.

## **4.1** **Flow Chart**



## **4.2 Code Size**

# **Features**

The calibration function has the following features.

1. Initialize registers;
2. Start the unicore;
3. Wait for the calibration to finish;
4. Save the calibration result.

# **Test Plan**

| **No** | **Description** |
| --- | --- |
| **1** | **Initialization** |
|  | **Verify the initialization.**  Check the registers needed to be initialized. Covered by local test. |
| **2** | **Calibration starts.** |
|  | **Verify the calibration starts.**  Check the TX\_ALIGN90\_DCC\_CAL\_TOP\_START. Covered by local test. |
| **3** | **Calibration done.** |
|  | **Verify the calibration done.**  Check the cmx\_CAL\_DONE. Covered by local test. |