**FFC COMPHY\_112G\_PIPE4**

**Firmware Top**

**Firmware Macro Architecture Specification**

For Internal Use Only

01/08/2018

Design Version: V1

**Revision History**

|  |  |  |  |
| --- | --- | --- | --- |
| **Revision** | **Author** | **Change List** | **Date** |
| V1 | | | |
|  |  | Initial version |  |

**Table of Contents**

[1 Introduction 4](#_Toc504051238)

[2 Features 4](#_Toc504051239)

[3 Interface Signal Definitions 4](#_Toc504051240)

[3.1 Firmware Interface Signal 4](#_Toc504051241)

[3.2 Digital Interface Signal 5](#_Toc504051242)

[3.3 Analog Interface Signal 5](#_Toc504051243)

[4 Block Diagram 6](#_Toc504051244)

[5 Flow Chart 7](#_Toc504051245)

[6 Interface Timing and Sequence 8](#_Toc504051246)

[6.1 Interface Signal Timing 8](#_Toc504051247)

[7 Implementation 8](#_Toc504051248)

[7.1 Simulated Timing 8](#_Toc504051249)

[8 Simulation 8](#_Toc504051250)

[9 Test Plan 9](#_Toc504051251)

# Introduction

This document provides an overview of the firmware for COMPHY­\_112G\_PIPE4. The scope focuses on top level implementation and test plan. The details of individual modules of firmware will be provided in separate documents.

# Features

The FW controls the PHY to realize the following features.

1. Perform the initialization of the MCU and xdata memory;
2. Power up sequence;
3. Perform the power up calibrations;
4. Configure the PHY to correct speed;
5. Speed change;
6. Slumber mode entrance and wake up;
7. RX-init;
8. TX and RX training;
9. DFE adaptation;
10. RTPA;
11. EOM;
12. CLI.

When realizing the above features, the firmware should be implemented in to meet specific timing requirments defined in corresponding design spec.

# Interface Signal Definitions

## Firmware Interface Signal

|  |  |  |  |
| --- | --- | --- | --- |
| **Port Name** | **Dir** | **Default** | **Description** |
| cmx\_CAL\_DONE | O | N/A | Calibration done. |
| cmx\_EXT\_FORCE\_CAL\_DONE | I/O | N/A | Skip calibration and use external calibration values. |
| cmx\_CAL\_START | I/O | N/A | Start the calibration sequence. |
| lnx\_SQ\_AUTO\_TRAIN\_LANE | I/O | N/A | Enable SQ auto train. |
| lnx\_ESM\_EN\_LANE | I/O | N/A | Start EOM function. |
| cmx\_AUTO\_RX\_INIT\_EN | I/O | N/A | Auto RX INIT. |
| cmx\_PHY\_GEN\_MAX\_3\_0 | I | N/A | PHY GEN MAX. |
| cmx\_FORCE\_CONT\_CAL\_SKIP | I | N/A | Skip continuous calibration. |
| To Be Extended |  |  |  |
|  |  |  |  |

## Digital Interface Signal

|  |  |  |  |
| --- | --- | --- | --- |
| **Port Name** | **Dir** | **Default** | **Description** |
| PHY\_STATUS | O | N/A | The running status of PHY. |
| reg\_MCU\_EN\_LANEX | I/O | N/A | Enable MCU\_X. |
| reg\_EN\_LANEX | I/O | N/A | Lane\_X enable. |
| reg\_PIN\_PHY\_GEN\_TX\_RD\_LANE\_3\_0 | I | N/A | PHY GEN TX. |
| reg\_PIN\_PHY\_GEN\_RX\_RD\_LANE\_3\_0 | I | N/A | PHY GEN RX. |
| reg\_MCU\_DEBUGX\_LANE\_7\_0 | I/O | N/A | Lane debug register X. |
| To be extended |  |  |  |

## Analog Interface Signal

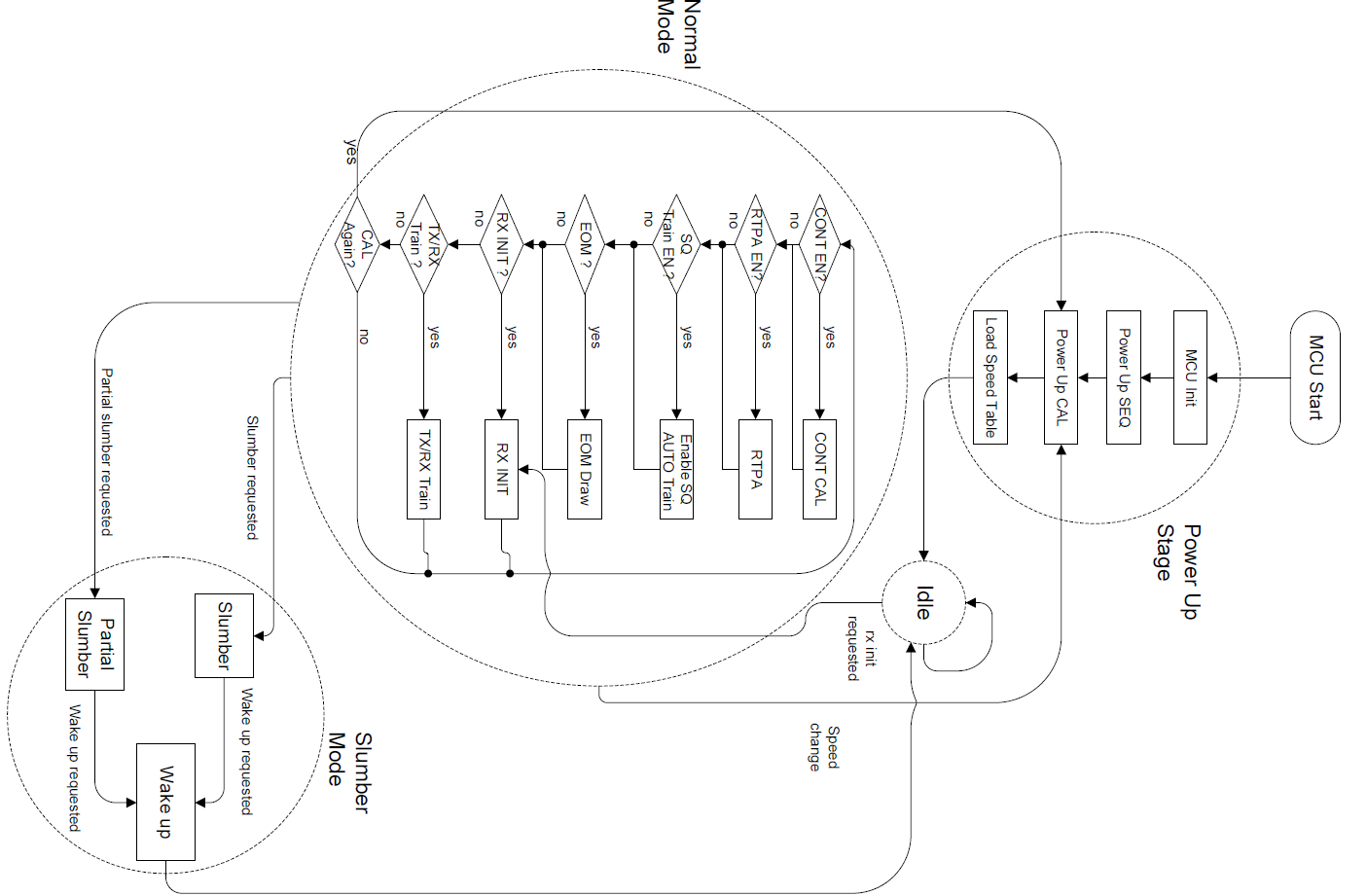
|  |  |  |  |
| --- | --- | --- | --- |
| **Port Name** | **Dir** | **Default** | **Description** |
|  |  |  |  |
| To be extended |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |

# 

# Block Diagram



# Flow Chart



# Interface Timing and Sequence

## Interface Signal Timing

# Implementation

**From the analog design spec**

## Simulated Timing

# Simulation

# Test Plan

| **No** | **Description** |
| --- | --- |
|  |  |
|  | **Power on Seq** |
| The flow defined in power on sequence.  **Checkpoint:**   1. The signals should be correctly programed. 2. Meet timing requirements. |
|  | **Power on calibration** |
| Perform calibrations  **Checkpoint:**   1. Sequnce of calibrations should be correct; |
|  | **Load speed table** |
| Load PLL, TX and RX speed table  **Checkpoint:**   1. Load the speed tables correctly; |
|  | **Continuous calibration** |
| Enter continuous mode  Set force cal done for each calibration  **Checkpoint:**   1. Sequence should be correct; 2. The calibration can be enabled or disabled. |
|  | **RX init** |
| RX init triggering;  RX init correctly.  **Checkpoint:**   1. RX init finishes; 2. Enter normal mode after RX init. |
|  | **EOM draw** |
| EOM function enters and exits correctly;  **Checkpoint:**  EOM function can finish when enabled;  Enter normal mode after EOM. |
|  | **Slumber modes** |
| Slumber mode entering correcly;  Timing requirements.  **Checkpoint:**  Slumber mode enters correctly with timing requirement. |
|  |  |
|  | **Slumber wake up** |
| Slumber wake up correctly;  Timing requirement.  **Checkpoint:**  Slumber mode wakes up correctly with timing requirement. |
|  | **Restart cal** |
| Restart calibration  **Checkpoint:**  Calibrations finish correctly. |
|  | **TX/RX Train** |
|  | TBD |
|  | **RTPA** |
|  | TBD |
|  |  |
|  |  |