**COMPHY\_112G**

**PLL DCC Calibration**

**R1.0**

**Macro Architecture Specification**

For Internal Use Only

Design Version V1.0

**Revision History**

|  |  |  |  |
| --- | --- | --- | --- |
| **Revision** | **Author** | **Change List** | **Date** |
| V1.0 |  |  |  |
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**Table of Contents**

[**1.** **Introduction** 2](#_Toc512591103)

[**2. Interafces** 2](#_Toc512591104)

[**2.1 Firmware Interface Signal** 2](#_Toc512591105)

[**2.2 Digital Interface Signal** 2](#_Toc512591106)

[**2.3 Analog Interface Signal** 3](#_Toc512591107)

[**2.4 Time Flow** 4](#_Toc512591108)

[**3** **Block Diagram** 5](#_Toc512591109)

[**4** **FW Handling** 5](#_Toc512591110)

[**4.1** **Flow Chart** 5](#_Toc512591111)

[**4.2 Code Size** 5](#_Toc512591112)

[**5** **Features** 5](#_Toc512591113)

[**6** **Test Plan** 5](#_Toc512591114)

# **Introduction**

This document describes the firmware of PLL calibration.

# **2. Interafces**

## **2.1 Firmware Interface Signal**

|  |  |  |
| --- | --- | --- |
| **Port Name** | **Dir** | **Description** |
| cmx\_PLL\_DCC\_CAL\_EXT\_EN | O | External enable. |
| cmx\_EXT\_FORCE\_CAL\_DONE | I/O | Force to skip calibration. |
| lnx\_PLL\_DCC\_CAL\_DONE\_LANE | I/O | RX Impedance Calibration done. |
| lnx\_PLL\_DCC\_CAL\_PASS\_LANE | I/O | RX Impedance Calibration pass. |

## 

## **2.2 Digital Interface Signal**

|  |  |  |
| --- | --- | --- |
| **Port Name** | **Dir** | **Description** |
| PHY\_STATUS | O | The running status of PHY. |
| PLL\_DCC\_CAL\_TOP\_START | I/O | PLL DCC Cal top start. |
| PLL\_DCC\_CAL\_TOP\_DONE | I/O | PLL DCC Cal top done. |
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## **2.3 Analog Interface Signal**

|  |  |  |  |
| --- | --- | --- | --- |
| **Port Name** | **Dir** | **Default** | **Description** |
| **LCPLL\_DCC\_EN** | **I** | **1’b0** | **Enable PLL DCC**  **0: Not enable**  **1: Enable**  **If LCPLL\_DCC\_EN=0, the correction code will be ignored.** |
| **LCPLL\_DCC\_CAL\_EN** | **I** | **1’b0** | **Enable PLL\_DCC calibration DN signal output.**  **0: Disable,**  **1: Enable.** |
| **LCPLL\_DCC[5:0]** | **I** | **6’h20** | **Correction code in binary code format. Bit[5] is sign bit. If bit[5]=1, the value is positive.** |
| **LCPLL\_DCC\_HG** | **I** | **1’b0** | **PLL Clock Duty Cycle Correction High Gain. Duty Cycle Correction gain setting.**  **0: regular gain**  **1: 2X gain** |
| **LCPLL\_DCC\_CLK** | **I** |  | **Input clock used to synchronize the offset cancellation circuit of DCC. 100KHz~1M.** |
| **TRX\_IMPCAL\_CLK** | **I** |  | **Input clock used to do auto-zero in comparator 100k~1M.** |
| **CMN\_IMPCAL\_OUT** | **O** |  | **DCC DN flag signal indicating duty cycle.**  **0: duty cycle<50%**  **1: duty cycle>50%**  **Referd as DCC\_DN throughout the spec.** |
|  |  |  |  |
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## **2.4 Time Flow**

# **Block Diagram**



# **FW Handling**

The firmware first initializes for the calibration, next starts the unicore and wait for the calibration to finish. After the calibration, the FW saves the calibration result.

## **4.1** **Flow Chart**



## **4.2 Code Size**

# **Features**

The calibration function has the following features.

1. Initialize registers;
2. Start the unicore;
3. Wait for the calibration to finish;
4. Save the calibration result.

# **Test Plan**

| **No** | **Description** |
| --- | --- |
| **1** | **Initialization** |
|  | **Verify the initialization.**  Check the registers needed to be initialized. Covered by local test. |
| **2** | **Calibration starts.** |
|  | **Verify the calibration starts.**  Check the PLL\_DCC\_CAL\_TOP\_START. Covered by local test. |
| **3** | **Calibration done.** |
|  | **Verify the calibration done.**  Check the lnx\_PLL\_DCC\_CAL\_DONE\_LANE. Covered by local test. |