**COMPHY\_112G**

**DLL Calibration**

**R1.0**

**Macro Architecture Specification**

For Internal Use Only

Design Version V1.0

**Revision History**

|  |  |  |  |
| --- | --- | --- | --- |
| **Revision** | **Author** | **Change List** | **Date** |
| V1.0 |  |  |  |
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# **Introduction**

This document describes the firmware of RXCLK calibration.

# **2. Interafces**

## **2.1 Firmware Interface Signal**

|  |  |  |
| --- | --- | --- |
| **Port Name** | **Dir** | **Description** |
| cmx\_RXCLK\_CAL\_EXT\_EN | O | External enable. |
| cmx\_EXT\_FORCE\_CAL\_DONE | I/O | Force to skip calibration. |
| lnx\_RXCLK\_CAL\_DONE\_LANE | I/O | RXCLK Calibration done. |
| lnx\_RXCLK\_CAL\_PASS\_LANE | I/O | RXCLK Calibration pass. |

## 

## **2.2 Digital Interface Signal**

|  |  |  |
| --- | --- | --- |
| **Port Name** | **Dir** | **Description** |
| PHY\_STATUS | O | The running status of PHY. |
| EOM\_CLK\_EN | I/O | EOM CLK enable. |
| EOM\_RESET\_INTP\_EXT |  |  |
| RXDCC\_HG\_EOMCLK | I/O | RXDCC HG. |
| RXDCC\_EN\_EOMCLK | I/O | RXDCC enable EOMCLK. |
| RX\_CLK\_CAL\_TOP\_START | I/O | RX CLK CAL start. |
| RX\_CLK\_CAL\_TOP\_DONE | O | RX CLK CAL done. |
| PU\_EOM\_ALIGN90\_DCC\_CMP | I/O |  |
|  |  |  |
|  |  |  |

## **2.3 Analog Interface Signal**

|  |  |  |  |
| --- | --- | --- | --- |
| **Port Name** | **Dir** | **Default** | **Description** |
| RX­DCC\_GM\_P1P3\_CCLK[1:0] | I | 2’b00 | MSB for the segments control in DCCP13.  Gray code  2’b00:All branches VP[1:0] ON, DCC OFF.  2’b01:VP[0], Branch[0] bias voltage.  2’b11:VP[1], Branch[1] bias voltage  2’b10:Not Allowed. |
| RX­DCC\_GM\_P1P3\_ECLK[1:0] | I | 2’b00 | MSB for the segments control in DCCP13E.  Gray code  2’b00:All branches VP[1:0] ON, DCC OFF.  2’b01:VP[0], Branch[0] bias voltage.  2’b11:VP[1], Branch[1] bias voltage  2’b10:Not Allowed. |
| RX­DCC\_GM\_P2P4\_CCLK[1:0] | I | 2’b00 | MSB for the segments control in DCCP24.  Gray code  2’b00:All branches VP[1:0] ON, DCC OFF.  2’b01:VP[0], Branch[0] bias voltage.  2’b11:VP[1], Branch[1] bias voltage  2’b10:Not Allowed. |
| RX­DCC\_GM\_P2P4\_ECLK[1:0] | I | 2’b00 | MSB for the segments control in DCCP24E.  Gray code  2’b00:All branches VP[1:0] ON, DCC OFF.  2’b01:VP[0], Branch[0] bias voltage.  2’b11:VP[1], Branch[1] bias voltage  2’b10:Not Allowed. |
| RX­DCC\_DAC\_P1P3\_CCLK[6:0] | I | 0x0 | Bit[6] is polarity control for DCCP13.  0: Decrease duty cycle of CLKP  1: Increase duty cycle of CLKP  Bit[5:0] is LSB for the voltage control in DCCP13. Binary code  Max:0d47  Min: 0 |
| RX­DCC\_DAC\_P1P3\_ECLK[6:0] | I | 0x0 | Bit[6] is polarity control for DCCP13E.  0: Decrease duty cycle of CLKP  1: Increase duty cycle of CLKP  Bit[5:0] is LSB for the voltage control in DCCP13E. Binary code  Max:0d47  Min: 0 |
| RX­DCC\_DAC\_P2P4\_CCLK[6:0] | I | 0x0 | Bit[6] is polarity control for DCCP24.  0: Decrease duty cycle of CLKP  1: Increase duty cycle of CLKP  Bit[5:0] is LSB for the voltage control in DCCP24. Binary code  Max:0d47  Min: 0 |
| RX­DCC\_DAC\_P2P4\_ECLK[6:0] | I | 0x0 | Bit[6] is polarity control for DCCP24E.  0: Decrease duty cycle of CLKP  1: Increase duty cycle of CLKP  Bit[5:0] is LSB for the voltage control in DCCP24E. Binary code  Max:0d47  Min: 0 |
| RXDCC­\_ DMCLK\_P1P3\_CCLK | I |  | Dummy clock cycle for DCCP13.  1:Inactive  0:Active |
| RXDCC­\_ DMCLK\_P1P3\_ECLK | I |  | Dummy clock cycle for DCCP13E.  1:Inactive  0:Active |
| RXDCC­\_ DMCLK\_P2P4\_CCLK | I |  | Dummy clock cycle for DCCP24.  1:Inactive  0:Active |
| RXDCC­\_ DMCLK\_P2P4\_ECLK | I |  | Dummy clock cycle for DCCP24E.  1:Inactive  0:Active |
| ALIGN90\_DCC\_REF[7:0] | I |  | Reference for Align90\_DD/EE/DE/DE\_H and DCC1-DCC5 calibration comparator.  “0d0-0d192”: for Align90 phase detector range 27-123deg with 0.5deg/step. Code 0d126=>90deg.  “0d193”: invalid  “0d194-0d254”: for DCC detector range with +-0.14%/step. Code 0d224=50% duty cycle. |
| EOM\_ALIGN90\_DCC\_REF [6:0] | I |  | Reference for Align90\_EOMEOM/EEOM\_H/DEOM and DCC6 calibration comparator.  “0d0-0d40”: for Align90 phase detector range 80-100deg with 0.5deg/step. Code 0d20=>90deg.  “0d41”: invalid  “0d42-0d102”: for DCC6 detector range with +-0.14%/step. Code 0d224=50% duty cycle. Code 0d72=50% duty cycle. |
| RX\_Align90\_DCC\_CMP\_OUT | O |  | The output pin of the comparator  For duty cycle P>N, RX\_ALIGN90\_DCC\_CMP\_OUT=1  For duty cycle P<N, RX\_ALIGN90\_DCC\_CMP\_OUT=0  Shared with RX ALIGN90 |
| ALIGN90\_DCC\_PD\_EN | I |  | Enable the mux between phase detector/DCC detector outputs and comparator input for calibration. |
| ALIGN90\_DCC\_PD\_SEL[2:0] | I |  | Phase detector/DCC detector output selection for comparator input.  0x0: DCC\_P1P3\_CCLK(DCC4)  0x1: DCC\_P2P4\_CCLK(DCC1)  0x2: DCC\_P2P4\_ECLK(DCC2)  0x3: DCC\_P1P3\_ECLK(DCC3)  0x4: PD\_DE  0x5: PD\_EE  0x6: PD\_DD  0x7: PD\_DEH |
| EOM\_ALIGN90\_DCC\_PD\_EN | I |  | Enable the mux between phase detector/DCC detector outputs and EOM comparator input for calibration. |
| EOM\_ALIGN90\_DCC\_PD\_SEL[2:0] | I |  | Phase detector/DCC detector output selection for comparator input.  0x0: PD\_EEOM\_H  0x1: DCC\_EOM (DCC6)  0x2: PD\_DEOM  0x3: PD\_EOMEOM  Other: not valid. |
| RXDCC\_CMN\_CAL\_EN | I | 0 | Enable common mode DCC5 calibration.  0: Disable DCC5 calibration  1: Enable DCC5 calibration |
| RX\_HALFRATE\_EN | I |  | Half rate enable bit.  0: Quad rate 112G  1: Half rate 56G |

## **2.4 Time Flow**

# **Block Diagram**



# **FW Handling**

The firmware first initializes for the calibration, next starts the unicore and wait for the calibration to finish. After the calibration, the FW saves the calibration result.

## **4.1** **Flow Chart**



## **4.2 Code Size**

# **Features**

The calibration function has the following features.

1. Initialize registers;
2. Start the unicore;
3. Wait for the calibration to finish;
4. Save the calibration result.

# **Test Plan**

| **No** | **Description** |
| --- | --- |
| **1** | **Initialization** |
|  | **Verify the initialization.**  Check the registers needed to be initialized. Covered by local test. |
| **2** | **Calibration starts.** |
|  | **Verify the calibration starts.**  Check the TX\_ALIGN90\_DCC\_CAL\_TOP\_START. Covered by local test. |
| **3** | **Calibration done.** |
|  | **Verify the calibration done.**  Check the cmx\_CAL\_DONE. Covered by local test. |