**COMPHY\_112G**

**TX IMP Calibration**

**R1.0**

**Macro Architecture Specification**

For Internal Use Only

Design Version V1.0

**Revision History**

|  |  |  |  |
| --- | --- | --- | --- |
| **Revision** | **Author** | **Change List** | **Date** |
| V1.0 |  |  |  |
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# **Introduction**

This document describes the firmware of RXCLK calibration.

# **2. Interafces**

## **2.1 Firmware Interface Signal**

|  |  |  |
| --- | --- | --- |
| **Port Name** | **Dir** | **Description** |
| cmx\_TXIMP\_CAL\_EXT\_EN | O | External enable. |
| cmx\_EXT\_FORCE\_CAL\_DONE | I/O | Force to skip calibration. |
| lnx\_TXIMP\_CAL\_DONE\_LANE | I/O | TX IMP Calibration done. |
| lnx\_TXIMP\_CAL\_PASS\_LANE | I/O | TX IMP Calibration pass. |

## 

## **2.2 Digital Interface Signal**

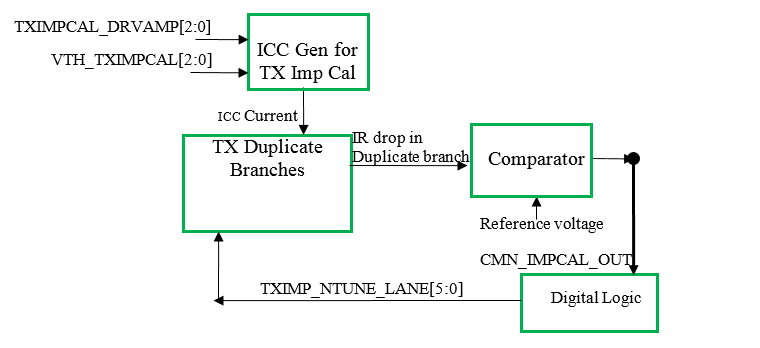
|  |  |  |
| --- | --- | --- |
| **Port Name** | **Dir** | **Description** |
| PHY\_STATUS | O | The running status of PHY. |
| TX\_IMP\_CAL\_TOP\_START | I/O | TX IMP Calibration Top Start. |
| TX\_IMP\_CAL\_TOP\_DONE | I/O | TX IMP Calibration Top Done. |
|  |  |  |

## **2.3 Analog Interface Signal**

|  |  |  |
| --- | --- | --- |
| **Port Name** | **Dir** | **Description** |
| PU\_DRVREG\_LANE | IR | Previous description: TX output driver power down control signal. 0=power down 1=power up |
| PU\_TX\_LANE | IR | TX power control 0=power down 1=active |
| TXIMPCAL\_EN | IR | TX Impedance calibration enable signal for CMN  1= enable TX impedance cali. 0= disable TX impedance cali. |
| TX\_IMPCAL\_EN\_LANE | IR | TX Impedance calibration enable signal. 1= enable impedance cali for corresponding lane 0= disable impedance cali for corresponding lane |
| TX\_IMPCAL\_BOT\_LANE | IR | Control Signal in TX impedance calibration.  0=Calibrate the impedance of PMOS (top) branches  1=calibrate the impedance of NMOS (bottom) branches. |
| TX\_IMPCAL\_SIDE\_LANE | IR | Switch the side during impedance calibration, either for PMOS (top) or NMOS (bottom). Because each time, only half of the PMOS branches (or NMOS branches) will be used during calibration.  0=Calibrate the first half of PMOS or NMOS branches  1=Calibrate the other half of PMOS or NMOS branches. |
| RCAL\_2ND\_EN\_LANE | IR | Perform impedance calibration for PMOS side twice, switch main branch and mirrored current in between. |
| TXIMP\_PTUNE\_LANE[5:0] | IR | Binary code. TX impedance setting for PMOS side, default ~42ohm without Tcoil. TXIMP\_PTUNE\_LANE[0] is 1LSB. |
| TXIMP\_NTUNE\_LANE[5:0] | IR | Binary code. TX impedance setting for NMOS side, default ~42ohm without Tcoil. TXIMP\_NTUNE\_LANE[0] is 1LSB. |
| TRX\_IMPCAL\_CLK | IR | Tx & Rx impedance calibration input clock |
| VREF\_TXDRV\_SEL[2:0] | IR | TX amplitude setting, which are sent to Ivref. [2:1] are used to adjust common mode voltage for hiz common mode voltage holding.  For each lane, there is separate VREF\_TXDRV\_SEL[2:0]  000: TX amp=0.88V  001: 0.9V  010: 0.92V  011: 0.94V  100: 0.96V (default)  101: 0.98V  110: 1.00V  111: 1.02V |
| TXIMPCAL\_DRVAMP[2:0] | IR | Control the value of tx impedance calibration current, which should match tx amplitude setting.  TXIMPCAL\_DRVAMP[2:0] is sent to Ivref and shared for all the lanes.  During each lane’s tx impedance calibration,  TXIMPCAL\_DRVAMP[2:0] follow the setting of VREF\_TXDRV\_SEL[2:0] of the lane.  For example, during tx impedance calibration of lane0,  TXIMPCAL\_DRVAMP[2:0]= VREF\_TXDRV\_SEL[2:0]\_CH0 |
| VTH\_TXIMPCAL[2:0] | IR | Impedance target setting for TX Impedance calibration, with T-coil excluded. With T-coil included, 2~3 ohm will be added.  000: Reserved  001: Reserved  010: Reserved  011: 42.3 ohm (default)  100: 44.7 ohm  101: 46.2 ohm  110: Reserved  111: Reserved |
| CMN\_IMPCAL\_OUT | O | Impedance calibration comparator output. |

## **2.4 Time Flow**

# **Block Diagram**



# **FW Handling**

The firmware first initializes for the calibration, next starts the unicore and wait for the calibration to finish. After the calibration, the FW saves the calibration result.

## **Flow Chart**

The FW does the TXIMP\_N\_1, TXIMP\_N\_2 and TXIMP\_P\_1, TXIMP\_P\_2, TXIMP\_P\_3 and TXIMP\_P\_4 calibration. The flow chart of each stage is similar. The flow chart is plotted below.



## **4.2 Code Size**

# **Features**

The calibration function has the following features.

1. Initialize registers;
2. Start the unicore;
3. Wait for the calibration to finish;
4. Save the calibration result.

# **Test Plan**

| **No** | **Description** |
| --- | --- |
| **1** | **Initialization** |
|  | **Verify the initialization.**  Check the registers needed to be initialized. Covered by local test. |
| **2** | **Calibration starts.** |
|  | **Verify the calibration starts for each stage.**  Check the TX\_IMP\_CAL\_TOP\_START. Covered by local test. |
| **3** | **Calibration done.** |
|  | **Verify the calibration done.**  Check the lnx\_TXIMP\_CAL\_DONE\_LANE. Covered by local test. |