**COMPHY\_112G**

**Training**

**R1.0**

**Macro Architecture Specification**

For Internal Use Only

Design Version V1.0

**Revision History**

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| --- | --- | --- | --- |
| **Revision** | **Author** | **Change List** | **Date** |
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# **Introduction**

This document describes the firmware of TRX train. The current train FW is based on the train FW on 28G design.

# **2. Interafces**

## **2.1 Firmware Interface Signal**

|  |  |  |
| --- | --- | --- |
| **Port Name** | **Dir** | **Description** |
| lnx\_RX\_TRAIN\_ONLY\_DFE\_LANE | I/O | RX train only. |
| lnx\_TRAIN\_DONE\_LANE | I/O | Train done. |
| lnx\_TRAIN\_PASS\_LANE | I/O | Train pass. |
| lnx\_PATTERN\_PROTECT\_EN\_LANE | I/O | Pattern protect switch. |
| lnx\_TX\_NO\_INIT\_LANE | I/O | No TX train init. |
| lnx\_RX\_NO\_INIT\_LANE | I/O | No RX train init. |
| lnx\_THRE\_EXCELLENT\_LANE\_5\_0 | I/O | RX train excellent F0D threshold. |
| lnx\_THRE\_GOOD\_LANE\_4\_0 | I/O | RX train good F0D threshold. |
| lnx\_THRE\_POOR\_LANE\_2\_0 | I/O | RX train poor F0D threshold. |
| lnx\_EYE\_CHECK\_BYPASS\_LANE | I/O | Eye check pass. |
| lnx\_SATURATE\_DISABLE\_LANE | I/O | Saturate disable. |
| lnx\_CDRPHASE\_OPT\_EN\_LANE | I/O | CDR phase optimization enable. |
| lnx\_TX\_TRAIN\_P2P\_HOLD\_LANE | I/O | TX train P2P hold. |
| lnx\_TRAIN\_USE\_S\_LANE | I/O | Train use S path. |
| lnx\_TRAIN\_USE\_D\_LANE | I/O | Train use D path. |
| lnx\_TRAIN\_PH\_CONTROL\_MODE\_LANE\_1\_0 | I/O | Train phase control mode. |
|  | I/O |  |
|  | I/O |  |

## 

## **2.2 Digital Interface Signal**

| Signal Name | Dir | Description |
| --- | --- | --- |
| System signals | | |
| clk | I | treed\_tx\_train\_if\_tx\_clk\_lane  Per lane tx clock. Derived from ANA\_TX\_TXCLK |
| reset | I | Per lane tx clock domain reset |
| int\_pin\_txdata[39:0] | I | Data from SoC, optional training payload used to bypass data from PT |
| txdata\_fm\_tx\_train\_en | O | Indicate data from training is ready to use, high to bypass SoC txdata |
| txdata\_fm\_tx\_train[39:0] | O | Tx Data with framemarker, TTIU and package. Used only during Tx training |
| int\_sel\_bits | I | Select whether is 32bit or 40bit mode  0: 40bit  1: 32bit |
| int\_tx\_train\_enable | I | Tx Train Enable from PIN\_TX\_TRAIN\_ENABLE or reg\_tx\_train\_enable. During auto mode (reg\_link\_train\_mode = 1’b0), asserting this bit will package TTIU with framemarker and phyload from phytest. Asserting this bit will send interrupt tx\_train\_enable\_irq to MCU interrupt |
| int\_rx\_train\_enable | I | Rx Train Enable from PIN\_RX\_TRAIN\_ENABLE or reg\_rx\_train\_enable. Asserting this bit will send interrupt rx\_train\_enable\_irq to MCU interrupt |
| int\_tx\_train\_frame\_lock\_enable |  | Transmitter Train Frame Lock Enable.  This signal notifies the local PHY to begin looking for TX training frame markers.  0h: Not enabled 1h: Enabled  Use this signal for link layer TX training mode only. In non-link layer Tx training, frame lock is auto enabled.  In this module, when frame lock is enabled, hardware will package the received link train command and status with frame marker and payload and send out. If disabled, this module will not be activated.  If int\_tx\_train\_enable is not activated, enabling this bit can still send out frame marker and TTIU command. And payload instead of coming from phytest, will be coming from fm\_pin\_txdata[39:0] by setting reg\_tx\_train\_pat\_link to high. |
| reg\_pin\_train\_complete\_type | I | PIN\_TX\_TRAIN\_COMPELTE and PIN\_RX\_TRAIN\_COMPLETE type  0: deassert PIN\_TX\_TRAIN\_COMPLETE, PIN\_RX\_TRAIN\_COMPLETE, PIN\_TX\_TRAIN\_FAILED and PIN\_RX\_TRAIN\_FAILED when tx\_train\_enable is low  1: PIN\_TX\_TRAIN\_COMPLETE, PIN\_RX\_TRAIN\_COMPLETE, PIN\_TX\_TRAIN\_FAILED and PIN\_RX\_TRAIN\_COMPLETE only have one clock cycle |
| PIN\_TX\_TRAIN\_COMPLETE | O | Transmitter Train Complete.  In non-link layer TX train mode, when asserted, this signal indicates that the transmitter training process of the local PHY and remote PHY is completed.  In link layer TX train mode, when asserted, this signal indicates that the transmitter training process of the local PHY is completed. This signal is asserted when TX training is complete, and it is de-asserted when PIN\_TX\_TRAIN\_ENABLE is low. |
| PIN\_TX\_TRAIN\_FAILED | O | Transmitter Train Failed.  This signal is valid when PIN\_TX\_TRAIN\_COMPLETE is asserted. It indicates that the local PHY has encountered a problem during training or could not converge. PIN\_TX\_TRAIN\_FAILED deasserts when PIN\_TX\_TRAIN\_ENABLE=0.  PIN\_TX\_TRAIN\_ERROR[2:0] determines which of the four error cases for Tx training failure has occured:   * Pattern lock lost timer expires * There are no additional, untried, or commonly supported settings for the local PHY * MTTT timer expires for local PHY * No remote PHY complete status within MTTT timer |
| PIN\_TX\_TRAIN\_ERROR[2:0] | O | Valid when PIN\_TX\_TRAIN\_COMPLETE is asserted.  Indicates which error occurs when PIN\_TX\_TRAIN\_FAILED is high. This signal will go to low when PIN\_TX\_TRAIN\_ENABLE is low. There are three error cases which can cause TX train failed. This is only for SAS application.  0h: Pattern lock lost timer expires (only in auto mode)  1h: there are no additional, untried, commonly supported settings for local PHY  2h: MTTT timer expires for local PHY  3h: does not get remote PHY's complete status within MTTT timer |
| PIN\_RX\_TRAIN\_COMPLETE | O | Receiver Train Complete.  When this singal asserted, it indicates when local PHY has completed receiver adaptation process. This signal is asserted when RX training is complete and it is de-asserted when PIN\_RX\_TRAIN\_ENABLE is de-asserted. |
| PIN\_RX\_TRAIN\_FAILED | O | Receiver Train Failed.  This signal is valid when PIN\_RX\_TRAIN\_COMPLETE is asserted. This signal indicates that the local PHY has encountered a problem during training or that the PHY could not converge. |
| Emphasis Ctrl | | |
| to\_ana\_vref\_txdrv\_sel |  | TX amplitude setting. Are used to adjust common mode voltage for hiz common mode voltage holding. Used in PCIe G1, G2.  000: TX amp=0.88V  001:0.9V  010: 0.92V  011: 0.94V  100: 0.96V (default)  101: 0.98V  110: 1.00V  111: 1.02V |
| to\_ana\_tx\_em\_peak\_en | O | Enable analog peak amplitude control |
| reg\_ana\_tx\_em\_peak\_en\_lane | I | Enable analog peak amplitude control |
| to\_ana\_tx\_em\_peak\_ctrl | O | Analog Emphasis Peak Ctrl  0000: 0, Nominal amplitude 0001: (1-1/45) of nominal amp. ... 1110: (1-14/45) of nominal amp. |
| reg\_tx\_em\_ctrl\_reg\_en\_lane | I | Speed Table. Decides whether tx emphasis it is register Ctrl or PCIe PIN Ctrl  0: PCIe PIN Ctrl  1: Register Ctrl |
| reg\_tx\_em\_peak\_ctrl\_lane | I | Register Ctrl for Emphasis Peak Ctrl  0000: 0, Nominal amplitude 0001: (1-1/45) of nominal amp. ... 1110: (1-14/45) of nominal amp. |
| reg\_tx\_em\_ctrl\_pipe\_sel\_lane |  | Speed table. Decides whether PCIe is in Gen1,2 or Gen 3,4  0: Gen1, 2  1: Gen3, 4 |
| Options Signals (Located in midas xdata\_lane) | | |
| reg\_status\_det\_timer\_lane[7:0] |  | status detection maximum time  unit is 0.5ms, use (n+1)/2 ms |
| reg\_tx\_train\_status\_det\_timer\_enable\_lane |  | tx train status detection timeout enable |
| reg\_rx\_train\_timer\_lane[9:0] |  | RX train maximum time  unit is 1ms |
| reg\_rx\_train\_timer\_enable\_lane |  | rx train timeout enable |
| reg\_trx\_train\_timer[9:0] |  | TX trainning maximum time  unit is 1ms |
| reg\_trx\_train\_timer\_enable\_lane |  | tx train timeout enable |
| reg\_frame\_det\_timer[3:0] |  | framemarker detection maximum wait during trx training  unit is 0.5ms, timeout duration is (n+1)\*0.5ms |
| reg\_frame\_lock\_sel\_lane |  | Frame lock select timeout signals  0: use internal generated frame lock signal to start trx train frame detection timers  1: use PIN\_TX\_TRAIN\_ENABLE as frame\_lock to start trx train frame detection timers |
| MCU Ctrl Related | | |
| mcu\_clk | I | MCU clock. Used to synchronize |
| mcu\_clk\_reset | I | MCU clock domain reset |
| reg\_tx\_train\_complete | I | Asserted by MCU  In non-link layer TX train mode, when asserted, this signal indicates that the transmitter training process of the local PHY and remote PHY is completed.  In link layer TX train mode, when asserted, this signal indicates that the transmitter training process of the local PHY is completed |
| reg\_tx\_train\_failed |  | Asserted by MCU  It indicates that the local PHY has encountered a problem during training or could not converge. |
| reg\_tx\_train\_error[1:0] |  | 0h: Pattern lock lost timer expires (only in auto mode)  1h: there are no additional, untried, commonly supported settings for local PHY  2h: MTTT timer expires for local PHY  3h: does not get remote PHY's complete status within MTTT timer |
| reg\_rx\_train\_complete |  | When this singal asserted, it indicates when local PHY has completed receiver adaptation process. This signal is asserted when RX training is complete |
| reg\_rx\_train\_failed |  | This signal indicates that the local PHY has encountered a problem during training or that the PHY could not converge. |
| reg\_local\_ctrl\_field\_valid | I | Rising edge.  To indicate full local control field is ready to send to remote PHY |
| reg\_local\_ctrl\_field[15:0] | I | Full local ctrl word. Including Pattern Type, Control Setting and Coefficient Request  [13:10] is PCIe Reset  [13:12] is Ethernet Ctrl Reset  [11:10] is SAS Ctrl Reset  [5:4] G1 Ctrl  [3:2] G0 Ctrl  [1:0] Gn1 Ctrl |
| reg\_local\_status\_field\_valid | I | Rising Edge  To indicate full local status field is ready to send to remote PHY |
| reg\_local\_status\_field[15:0] | I | Full local status word. Including Train Comp, Tx Init, Balance Bit and Coefficient Status  [5:4] G1 Status  [3:2] G0 Status  [1:0] Gn1 Status |
| pin\_tx\_train\_enable\_irq\_lane | O | Pulse in MCU clock domain  IRQ to register to indicate Tx Train has started |
| pin\_rx\_train\_enable\_irq\_lane | O | Pulse in MCU clock domain  IRQ to register to indicate Rx Train has started |
| remote\_ctrl\_valid\_irq\_lane | O | Pulse in MCU clock domain  IRQ to register to indicate Remote Ctrl is valid |
| reg\_rd\_remote\_ctrl\_field[15:0] | O | Remote ctrl field.  [13:10] is PCIe Reset  [13:12] is Ethernet Ctrl Reset  [11:10] is SAS Ctrl Reset  [5:4] G1 Ctrl  [3:2] G0 Ctrl  [1:0] Gn1 Ctrl |
| remote\_status\_valid\_irq\_lane | O | Pulse in MCU clock domain  IRQ to register to indicate Remote Status is valid |
| reg\_rd\_remote\_status\_field[15:0] | O | Remote status field.  [5:4] G1 Status  [3:2] G0 Status  [1:0] Gn1 Status |
| Link Interface Signals (All Synced to Tx Clock Domain)  For/from SoC or PIPE, valid when reg\_link\_train\_mode is high. | | |
| reg\_link\_train\_mode | I | Special TX training mode  0: TX training control pins are not used; COMPHY will take care of TX training protocol.  1: TX training control pins are used by link layer (SoC or PIPE) |
| reg\_link\_train\_mode\_lpbk | I | loop back mode when link\_train\_mode is high  0: Controlled by internal logic  1: All TX training related pins are connected to link interface RX status results. This is for test and debug only. |
| fm\_pin\_local\_ctrl\_field\_ready | I | To indicate remote status have responded local control request, local PHY can send another control field when ready |
| PIN\_REMOTE\_CTRL\_FIELD\_READY | O | The local PHY is ready to receive Tx coefficient update requests from the remote PHY or not. |
| PIN\_LOCAL\_CTRL\_FIELD\_VALID | O | To indicate local control field and reset is ready to latch into SoC/PIPE by this pulse. |
| PIN\_LOCAL\_CTRL\_FIELD[5:0] | O | Local ctrl field. [5:4] is post emphasis command, [3:2] is amplitude command, [1:0] is pre emphasis command |
| PIN\_LOCAL\_CTRL\_FIELD\_RESET[3:0] | O | Preset value. Used in |
| PIN\_LOCAL\_STATUS\_FIELD\_VALID | O | To indicate local status field is ready to send to remote PHY |
| PIN\_LOCAL\_STATUS\_FIELD[5:0] | O | Local status field. [5:4] is post emphasis status, [3:2] is amplitude status, [1:0] is pre emphasis status |
|  |  |  |

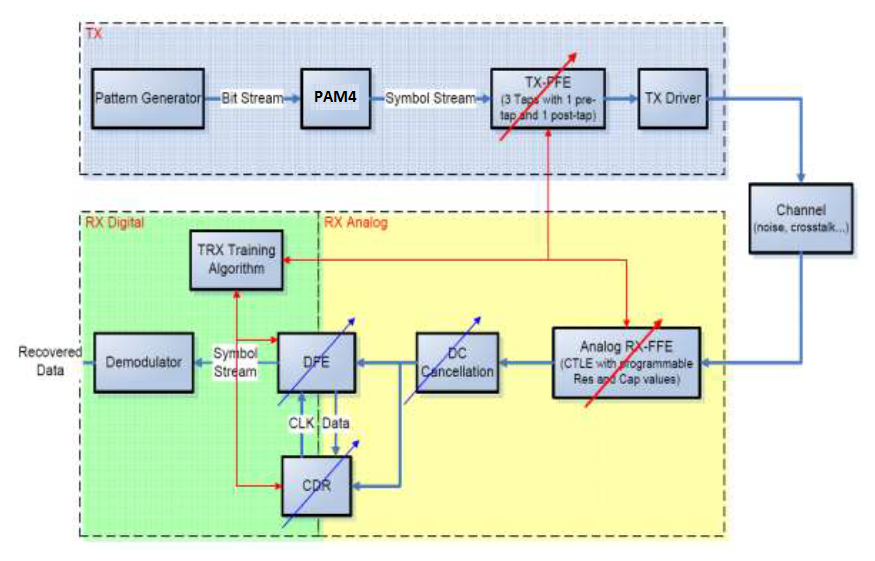
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## **2.3 Analog Interface Signal**

|  |  |  |
| --- | --- | --- |
| **Port Name** | **Dir** | **Description** |
| reg\_CTLE\_RES1\_SEL\_LANE\_3\_0 | IR | CTLE RES1. |
| reg\_CTLE\_RES2\_SEL\_LANE\_3\_0 | IR | CTLE RES2. |
| reg\_CTLE\_CAP1\_SEL\_LANE\_3\_0 | IR | CTLE CAP1. |
| reg\_CTLE\_CAP2\_SEL\_LANE\_3\_0 | IR | CTLE CAP2. |
| reg\_CTLE\_CURRENT1\_SEL\_LANE\_3\_0 | IR | CTLE CURRENT1. |
| reg\_CTLE\_CURRENT2\_SEL\_LANE\_3\_0 | IR | CTLE CURRENT2. |
| reg\_CTLE\_RL1\_SEL\_LANE\_3\_0 | IR | CTLE RL1. |
| reg\_CTLE\_RL2\_SEL\_LANE\_3\_0 | IR | CTLE RL2. |

## **2.4 Time Flow**

# **Block Diagram**



# **FW Handling**

The firmware first initializes for the TRX train, next starts the TX train and do the RX train. The TRX train does the training 3 times for the TX presets.

## **Flow Chart**

The FW does the TX and RX train. The flow chart of the TRX train is plotted below.



## **TX Train**

The TX train adjusts the TX parameters. The flow chart is plotted below.



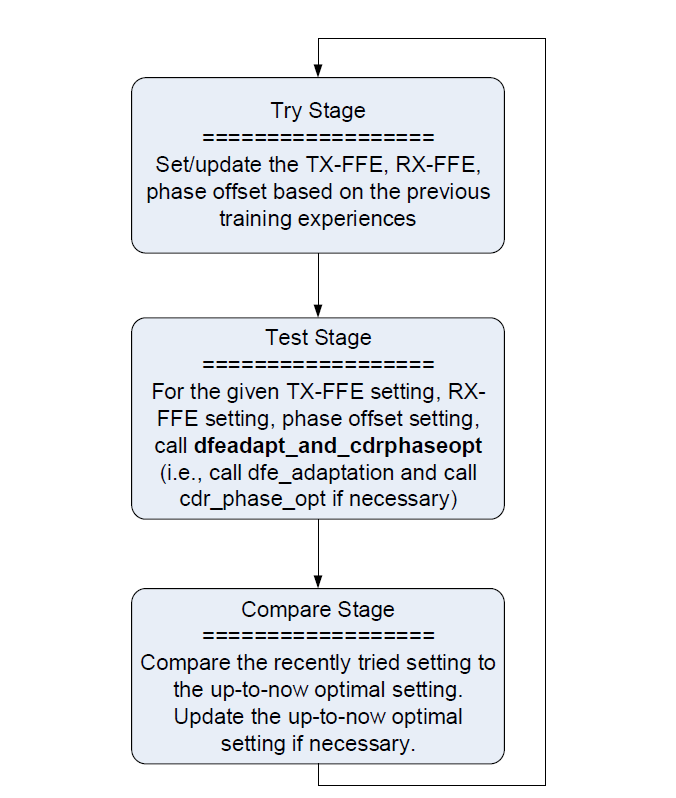
## **RX Train**

The RX train adjusts the RX parameters based on DFE taps. The flow chart is plotted below.



## **Training Process**

The training consists of 3 stages, try, test and compare.



## **Code Size**

# **Features**

The calibration function has the following features.

1. Initialize registers;
2. The TX train;
3. RX train;
4. Gain train and Res train.

# **Test Plan**

| **No** | **Description** |
| --- | --- |
| **1** | **Initialization** |
|  | **Verify the initialization.**  Check the registers needed to be initialized. Covered by local test. |
| **2** | **TX train.** |
|  | **Verify the TX train for each stage.**  Check the TX train signals. Covered by local test. |
| **3** | **RX Train.** |
|  | **Verify the RX train for each stage.**  Check the RX train signals. Covered by local test. |
| **4** | **Gain Train.** |
|  | **Verify the Gain train for each stage.**  Check the RX train signals. Covered by local test. |
| **5** | **Res Train.** |
|  | **Verify the Res train for each stage.**  Check the Res train signals. Covered by local test. |