**COMPHY\_112G\_FW**

**Power Management**

**R1.0**

**Macro Architecture Specification**

For Internal Use Only

Design Version V1.0

**Revision History**

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| --- | --- | --- | --- |
| **Revision** | **Author** | **Change List** | **Date** |
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**Table of Contents**

[**1.** **Introduction** 2](#_Toc509822774)

[**2.** **Power States** 2](#_Toc509822775)

[**3.** **Interface Signal Definitions** 3](#_Toc509822776)

[**3.1 Firmware Interface Signal** 3](#_Toc509822777)

[**3.2 Digital Interface Signal** 3](#_Toc509822778)

[**3.3 Analog Interface Signal** 3](#_Toc509822779)

[**3.4 Timing flow** 3](#_Toc509822780)

[**Signals** 3](#_Toc509822781)

[**Timing flow: slumber** 5](#_Toc509822782)

[**Timing flow: Partial TX** 6](#_Toc509822783)

[**Timing flow: Partial RX** 7](#_Toc509822784)

[**4.** **Interrupt Handling** 8](#_Toc509822785)

[**4.1** **Interrupts** 8](#_Toc509822786)

[**4.2** **Sources** 8](#_Toc509822787)

[**4.3** **Mechanism** 9](#_Toc509822788)

[**5.** **FW Flow** 9](#_Toc509822789)

[**5.1 Flow Chart** 10](#_Toc509822790)

[**5.2 Code Size** 11](#_Toc509822791)

[**6.** **Features** 11](#_Toc509822792)

[**7.** **Test Plan** 11](#_Toc509822793)

# **Introduction**

This document describes the power states of 112G PHY and how the firmware manages the entrance and exit of power states.

# **Power States**

The power states are in the following table.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Power Mode** | **PIN\_PU\_PLL** | **PIN\_PU\_TX** | **PIN\_PU\_RX** | **Description** |
| Normal | 0x1 | 0x1 | 0x1 | PLL, TX and RX are powered up |
| Slumber | 0x0 | 0x0 | 0x0 | PLL, TX and RX are powered off |
| Partial | 0x1 | 0x0 | 0x0 | PLL is on, TX and RX are powered off |

# **Interface Signal Definitions**

## **3.1 Firmware Interface Signal**

|  |  |  |
| --- | --- | --- |
| **Port Name** | **Dir** | **Description** |
| cmx\_AUTO\_RX\_INIT\_EN | I/O | Auto RX init |
| PHY\_STATUS | O | The running status of PHY. |
|  |  |  |

## 

## **3.2 Digital Interface Signal**

|  |  |  |
| --- | --- | --- |
| **Port Name** | **Dir** | **Description** |
| reg\_DFE\_ADAPT\_CONT\_LANE | I/O | DFE adapt continuous. |
| reg\_DFE\_START\_LANE | I/O | DFE start. |
| reg\_DFE\_CLK\_OFF\_LANE | I/O | DFE clock off. |
| reg\_RESET\_DFE\_LANE | I/O | Reset DFE. |
| reg\_PIN\_REFCLK\_DIS\_RD | I | PIN Referece Clock Disable Value. |
| reg\_INT\_REFCLK\_DIS\_CHG\_ISR\_LANE | I/O | Refclk\_dis\_chg Interrupt. |
| reg\_INT0\_REFCLK\_DIS\_EN\_INT\_EN\_LANE | I/O | Enable Refclk\_dis\_en\_int For INT0. |
| reg\_PU\_IVREF\_FELL | I/O | PU\_ivref Fell. |
| reg\_PU\_BG\_FELL | I/O | PU\_BG Fell. |
| reg\_RESET\_DTL\_LANE | I/O | Reset DTL. |
| reg\_DTL\_CLK\_OFF\_LANE | I/O | DTL clock off. |
| reg\_PIN\_PLL\_READY\_TX\_LANE | I/O | PLL Ready Tx |
| reg\_PIN\_PLL\_READY\_RX\_LANE | I/O | PHY Output Port PIN\_PLL\_READY\_RX |
| reg\_RESET\_ANA\_LANE | I/O | Reset Analog Circuitry |
|  |  |  |

## **3.3 Analog Interface Signal**

|  |  |  |
| --- | --- | --- |
| **Port Name** | **Dir** | **Description** |
| reg\_ANA\_PU\_TX\_LANE | I/O | Powre Up TX. |
| reg\_ANA\_PU\_SQ\_LANE | I/O | Analog Power Up Squetch Detector. |
| reg\_ANA\_PU\_PLL\_LANE | I/O | Power Up Analog PLL. |
| reg\_ANA\_PU\_RX\_LANE | I/O | Powre Up RX. |
| reg\_ANA\_PU\_RX\_DLY\_LANE | I/O | Power Up RX Delay. |
| reg\_ANA\_PU\_IVREF\_DLY1 | I/O | Analog Input ANA\_PU\_IVREF\_DLY1 Control |
| reg\_ANA\_PU\_IVREF\_DLY2 | I/O | Analog Input ANA\_PU\_IVREF\_DLY2 Control |
| reg\_ANA\_PU\_IVREF\_DLY3 | I/O | Analog Input ANA\_PU\_IVREF\_DLY3 Control |
| reg\_ANA\_LD\_CAL\_DATA\_LANE | I/O | Analog Load Calibration Data |
|  |  |  |

## **3.4 Timing flow**

## **Signals**

|  |  |  |  |
| --- | --- | --- | --- |
| **Signal Name** | **Register** | **Read/Write** | **Interrupt?** |
| PIN\_PU\_IVREF | reg\_rd\_pin\_pu\_ivref | r | yes; masked |
| PIN\_TX\_IDLE | reg\_rd\_pin\_tx\_idle\_lane | r | yes; masked |
| PIN\_PU\_SQ | reg\_rd\_pin\_pu\_sq\_lane | r | yes; masked |
| PIN\_PU\_PLL | reg\_rd\_pin\_pu\_pll\_lane | r | yes |
| PIN\_PU\_TX | reg\_rd\_pin\_pu\_tx\_lane | r | yes |
| PIN\_PU\_RX | reg\_rd\_pin\_pu\_rx\_lane | r | yes |
| PIN\_REFCLK\_DIS | reg\_rd\_pin\_refclk\_dis | r | yes |
| PIN\_RESET | ASIC | NA | NA |
| PU\_IVREF | reg\_ana\_pu\_ivref | w | NA |
| PU\_IVREF\_DLY1 | reg\_ana\_pu\_ivref\_dly1 | w | NA |
| PU\_IVREF\_DLY2 | reg\_ana\_pu\_ivref\_dly2 | w | NA |
| PU\_IVREF\_DLY3 | reg\_ana\_pu\_ivref\_dly3 | w | NA |
| PU\_PLL | reg\_ana\_pu\_pll\_lane | w | NA |
| PU\_PLL\_DLY | reg\_ana\_pu\_pll\_dly\_lane | w | NA |
| PU\_RX | reg\_ana\_pu\_rx\_lane | w | NA |
| PU\_RX\_DLY | reg\_ana\_pu\_rx\_dly\_lane | w | NA |
| PU\_TX | reg\_ana\_pu\_tx\_lane | w | NA |
| PU\_BG | ASIC | NA | NA |
| PU\_SQ | reg\_ana\_pu\_sq\_lane | w | NA |
| PLL\_CLK\_READY | reg\_ana\_pll\_clk\_ready\_lane | w | NA |
| PIN\_PLL\_READY\_RX | reg\_pin\_pll\_ready\_rx\_lane | w | NA |
| PIN\_PLL\_READY\_TX | reg\_pin\_pll\_ready\_tx\_lane | w | NA |
| DTL\_CLK\_OFF | reg\_dfe\_clk\_off\_lane | w | NA |
| DFE\_CLK\_OFF | reg\_dfe\_clk\_off\_lane | w | NA |
| DTX\_CLK\_OFF | reg\_dtx\_clk\_off | w | NA |
| RESET\_DTL | reg\_reset\_dtl\_lane | w | NA |
| RESET\_DTX | reg\_reset\_dtx\_lane | w | NA |
| RESET\_DFE | reg\_reset\_dfe\_lane | w | NA |
| TX\_IDLE | ASIC | NA | NA |
| RESET\_INTP\_EXT\_EOM | reg\_eom\_reset\_intp\_ext | w | NA |
| TXINTP\_RESET\_EXT | reg\_tx\_intpreset\_ext | w | NA |
| PIN\_REFCLK\_DIS\_ACK | ASIC | NA | NA |

## **Timing flow: slumber**



## **Timing flow: Partial TX**



## **Timing flow: Partial RX**



# **Interrupt Handling**

## **Interrupts**

|  |  |
| --- | --- |
| **Interrupt** | **Events** |
| Int9 | Slumber entrance, Partial(TX/RX) entrance, Wake up |
| Int3 | Slumber.NoClk/NoIVREF |

## **Sources**

**Isolation mode**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | **PLL\_PU** | **TX\_PU\_TX** | **RX\_PU\_RX** | **IDLE** | **PU\_IVREF** | **MCU CLK** |
| **Partial(TX/RX)** | 1 | (0/1) | (1/0) | (1/0) | 1 | ON |
| **slumber** | 0 | 0 | 0 | 1 | 1 | ON |
| **slumber.NoIVREF** | 0 | 0 | 0 | 1 | 0 | ON |
| **slumber.NoClk** | 0 | 0 | 0 | 1 | 1 | OFF |
| **slumber.NoClkNoIVREF** | 0 | 0 | 0 | 1 | 0 | OFF |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **SoC mode** |  |  |  |  |  |  |
|  | **PIN\_PU\_PLL** | **PIN\_PU\_TX** | **PIN\_PU\_RX** | **PIN\_TX\_IDLE** | **PIN\_PU\_IVREF** | **PIN\_REFCLK\_**  **DIS** |
| **Partial(TX/RX)** | 1 | (0/1) | (1/0) | (1/0) | 1 | 0 |
| **slumber** | 0 | 0 | 0 | 1 | 1 | 0 |
| **slumber.NoIVREF** | 0 | 0 | 0 | 1 | 0 | 0 |
| **slumber.NoClk** | 0 | 0 | 0 | 1 | 1 | 1 |
| **slumber.NoClkNoIVREF** | 0 | 0 | 0 | 1 | 0 | 1 |

## **Mechanism**





# **FW Flow**

The entering and exit the power states are triggered by interrupts (e.g., 3 and 9). The FW programs the corresponding register fields when requests of entering or exiting power stare are received.

## **5.1 Flow Chart**



## **5.2 Code Size**

The code size corresponding to power management functions is about 1.2k bytes.

# **Features**

1. Slumber entering;
2. Partial slumber entering;
3. Slumber wake up;
4. Handling corresponding signals defined in the spec.

# **Test Plan**

| **No** | **Description** |
| --- | --- |
| 1 | **Entering/exiting slumber, partial TX/RX** |
| 1-1 | **Verify the FW flow.**  PHY\_STATUS. Covered by local test bench.  Verify Slumber entrance, Slumber partial TX/RX entrance and Wake Up. Triggered by signals in 4.2. |
| 1-2 | **Verify the timing flow for slumber mode.**  Based on the flow chart in section 3.4. Expected to be covered by DV test.  Verify that the signals programmed correctly with proper timing requirements. |
| 1-3 | **Verify the timing flow for Partial TX mode.**  Based on the flow chart in section 3.4. Expected to be covered by DV test.  Verify that the signals programmed correctly with proper timing requirements. |
| 1-4 | **Verify the timing flow for Partial RX mode.**  Based on the flow chart in section 3.4. Expected to be covered by DV test.  Verify that the signals programmed correctly with proper timing requirements. |
| 2 | **Slumber, partial TX/RX entrance followed by wake up immediately** |
| 2-1 | **Verify that the slumber request and the wake up request is received and handled properly.**  Expected to be covered by DV test.  The PHY should either ignore the slumber request or wake up successfully. The successful operation should end up to by in normal mode.  Verify the wake up sequence based on the spec. |
| 3 | **Partial TX followed by Partial RX** |
| 3-1 | **Verify that the requests are received and handle properly.**  Expected to be covered by DV test.  The PHY should be in slumber mode eventually.  Verify the required signal status defined in the spec for slumber mode. |
|  |  |
|  |  |