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| 12FFC COMPHY\_28G\_PIPE4\_X4 |
|  |
| FW Application Note |
| Central Engineering Applications Group |

INTERNAL

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| Doc Status: Preliminary | | Technical Publication: Int. Rev. x.xx |
| This document is based on template# MV-S200005-05. | | |

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# Lane Selection

|  |  |  |  |
| --- | --- | --- | --- |
| BROADCAST | LANE\_SEL[1:0] | Lane Write Operation | Comments |
| 0x1 | x | All lanes | LANE\_SEL is ignored, all lanes registers can be programmed to the same value at once. |
| 0x0 | 0 | Lane 0 | Program lane 0 registers or data RAM |
| 0x0 | 1 | Lane 1 | Program lane 1 registers or data RAM |
| 0x0 | 2 | Lane 2 | Program lane 2 registers or data RAM |
| 0x0 | 3 | Lane 3 | Program lane 3 registers or data RAM |

# CALIBRATION

## Calibration Blocks Summary

* Process Calibration
* Impedance Calibration
* LCPLL Calibration
* Ring PLL Calibration
* PLL DCC Calibration
* Tx DCC Calibration
* Rx DCC Calibration
* Phase Align90 Calibration
* Squelch Detector Calibration
* Sampler Calibration
* VDD Calibration

## Calibration Blocks

### Process Calibration

|  |  |  |
| --- | --- | --- |
| **Register Name** | **R/W** | **Description** |
| CAL\_PROC\_SUBSS[7:0]  (RE620h[23:16]) | R/W | Process Threshold SUBSS[4:0]. |
| CAL\_PROC\_SS2TT[7:0]  (RE620h[15:8]) | R/W | Process Threshold SS2TT[4:0]. |
| CAL\_PROC\_TT2FF[7:0]  (RE620h[7:0]) | R/W | Process Threshold TT2FF[4:0]. |
| ANA\_PROCESS\_VALUE[3:0]  (RA330h[7:4]) | R/W | Result of process calibration to analog |
| process\_cal\_done  (RE64Ch[5]) | R | Calibration done flag |

### Impedance Calibration

|  |  |  |
| --- | --- | --- |
| **Register Name** | **R/W** | **Description** |
| vth\_tximpcal[2:0]  (R8204h[4:2]) | R/W | Tx impedance threshold value |
| vth\_rximpcal[2:0]  (R8228h[4:2]) | R/W | Rx impedance threshold value |
| impcal\_rx\_lane[4:0]  (R0008h[6:2]) | R/W | Rx impedance calibration result for different lanes |
| tximp\_tunep\_lane[3:0]  (R0240h[7:4]) | R/W | Tx impedance setting for PMOS side |
| tximp\_tunen\_lane[3:0]  (R0240h[3:0]) | R/W | Tx impedance setting for NMOS side |
| cal\_tximp\_tunep\_lane[7:0]  (R6018h[23:16]) | R/W | FW saves Tx impedance calibration result for PMOS side. |
| cal\_tximp\_tunen\_lane[7:0]  (R6018h[7:0]) | R/W | FW saves Tx impedance cal result for NMOS side. |
| cal\_rx\_imp\_lane[7:0]  (R6014h[15:8]) | R/W | FW saves Rx calibrated impedance result |
| tximp\_cal\_timeout\_lane  (R6008h[22]) | R/W | Tx impedance calibration timeout indicator |
| rximp\_cal\_timeout\_lane  (R6008h[23]) | R/W | Rx impedance calibration timeout indicator |
| rximp\_cal\_done\_lane  (R6000h[14]) | R | Rx Impedance Calibration Done. |
| tximp\_cal\_done\_lane  (R6000h[13]) | R | Tx Impedance Calibration Done. |

### LCPLL Calibration

|  |  |  |
| --- | --- | --- |
| **Register Name** | **R/W** | **Description** |
| lcvco\_dac\_msb[2:0]  (R82B4h[2:0]) | R/W | MSB of VCO swing amplitude. Higher value means larger amplitude. This field control the VCO supply voltage for the DAC around 80 mV per MSB. |
| lcvco\_dac\_lsb[4:0]  (R82B4h[7:3]) | R/W | LSB of VCO swing amplitude. Higher value means larger amplitude. Around 2.5 mv per LSB. |
| lccap\_usb  (R82C0h[4]) | R/W | Control the capacitance of LC tank 🡪 VCO frequency |
| lccap\_msb[3:0]  (R82C8h[7:4]) | R/W |
| lccap\_lsb[4:0]  (R82C4h[7:3]) | R/W |
| icp\_lc[4:0]  (R8334h[4:0]) | R/W | Control the charge pump current |
| ANA\_FBCK\_SEL  (RA318h[9]) | R/W | Choose whether the signal before or after PI will go FBDIV. Setting to 0 means PI OFF, FBDIV needs to be set as 4 times as when it’s set to 1 |
| pll\_cal\_done  (RE64Ch[16]) | R | PLL calibration is done |

### Ring PLL

|  |  |  |
| --- | --- | --- |
| **Register Name** | **R/W** | **Description** |
| PLL\_SPEED\_RING[4:0]  (R8300h[7:3]) | R/W | Ring PLL speed selection |
| PLL\_SLLP\_DAC\_COARSE\_RING[3:0]  (R8304h[3:0]) | R/W | Control VDDVCO coarse tuning |
| PLL\_SLLP\_DAC\_FINE\_RING[10:0]  (R8308h[7:5]+R830Ch[7:0]) | R/W | Control VDDVCO fine tuning |
| icp\_ring[3:0]  (R82F8h[7:4]) | R/W | Control the charge pump current |
| ANA\_FBCK\_SEL\_RING  (RA318h[2]) | R/W | Choose whether the signal before or after PI will go FBDIV. Setting to 0 means PI OFF, FBDIV needs to be set as 4 times as when it’s set to 1 |
| pll\_cal\_ring\_done  (RE64Ch[24]) | R | Ring PLL calibration is done |

### PLL DCC Calibration

|  |  |  |
| --- | --- | --- |
| **Register Name** | **R/W** | **Description** |
| lcpll\_dcc[5:0]  (R82D8h[7:2]) | R/W | LCPLL DCC DAC code |
| plldcc\_cal\_done  (RE64Ch[1]) | R | PLL DCC calibration is done |

### Tx DCC Calibration

|  |  |  |
| --- | --- | --- |
| **Register Name** | **R/W** | **Description** |
| txdcc\_cnt\_lane[5:0]  (R024Ch[6:1]) | R/W | Correction code in binary code format. Bit[5] is sign bit. If bit[5]=1, the value is positive. |
| txdcccal\_pdiv\_cnt\_lane[5:0]  (R025Ch[7:2]) | R/W | Tx post divider correction code in binary code format. |
| txdcc\_cal\_cont\_en  (RE60Ch[23]) | R/W | Tx DCC Calibration Continuous Enable |
| txdcc\_cal\_done\_lane  (R6000h[16]) | R | Tx DCC calibration done indicator. |

### Rx DCC Calibration

|  |  |  |
| --- | --- | --- |
| **Register Name** | **DIR** | **Description** |
| rxdcc\_eomclk\_lane[5:0]  (R0040h[7:2]) | R/W | Rx EOM clock DCC code in binary format. Bit[5] is sign bit. If bit[5]=1, the value is positive. |
| rxdcc\_dataclk\_lane[5:0]  (R0220h[7:2]) | R/W | Rx DATA clock DCC code in binary code format. Bit[5] is sign bit. If bit[5]=1, the value is positive. |
| rxdcc\_eom\_cal\_done\_lane  (R6000h[8]) | R | RX DCC EOM Calibration Done. |
| rxdcc\_data\_cal\_done\_lane  (R6000h[7]) | R | Rx DCC Center Calibration Done. |

### Align90 Calibration

|  |  |  |
| --- | --- | --- |
| **Register Name** | **R/W** | **Description** |
| ALIGN90\_REF\_LANE[5:0]  (R0038h[7:2]) | R/W | Selection for phase shift. Control from the DSP side.  ALIGN90\_REF will change when align 90 or phase selection happen, ALIGN90\_REF is controlled by the DSP side. |
| align90\_gm\_lane[2:0]  (R0030h[3:1]) | R/W | Control Gate Bias Voltage of Phase Shifter. |
| align90\_dac\_lane[5:0]  (R0034h[7:2]) | R/W | Control Gate Bias Voltage of Phase Shifter. |
| rxalign90\_cal\_done\_lane  (R6000h[9]) | R | Rx Align90 calibration done. |

### Squelch Calibration

|  |  |  |
| --- | --- | --- |
| **Register Name** | **R/W** | **Description** |
| cal\_sq\_offset\_lane[7:0]  (R6010h[23:16]) | R/W | FW saves SQ calibration offset result. |
| cal\_sq\_thresh\_lane[7:0]  (R6010h[31:24]) | R/W | FW saves SQ calibration threshold result. |
| PIN\_RX\_SQ\_OUT\_RD\_LANE  (R2170h[15]) | R | Internal Analog Portion Rx Sq Output Read. |
| sq\_cal\_done\_lane  (R6000h[18]) | R | Squelch Calibration Done. |

### Sampler Calibration

|  |  |  |  |
| --- | --- | --- | --- |
| **Register Name** | | **R/W** | **Description** |
| ofst\_f1p\_pos\_d\_e\_lane[4:0]  (R0478h[4:0]) | | R/W | Controls offset for even F1P data sampler. Decode from OFST\_F1P\_D\_E[6:0] in digital |
| ofst\_f1p\_neg\_d\_e\_lane[4:0]  (R047Ch[4:0]) | | R/W | Controls offset for even F1P data sampler. Decode from OFST\_F1P\_D\_E[6:0] in digital |
| ofst\_f1n\_pos\_d\_e\_lane[4:0]  (R0480h[4:0]) | | R/W | Controls offset for even F1N data sampler. Decode from OFST\_F1N\_D\_E[6:0] in digital |
| ofst\_f1n\_neg\_d\_e\_lane[4:0]  (R0484h[4:0]) | | R/W | Controls offset for even F1N data sampler. Decode from OFST\_F1N\_D\_E[6:0] in digital |
| ofst\_f1p\_pos\_d\_o\_lane[4:0]  (R0878h[4:0]) | | R/W | Controls offset for odd F1P data sampler. Decode from OFST\_F1P\_D\_O[6:0] in digital |
| ofst\_f1p\_neg\_d\_o\_lane[4:0]  (R087Ch[4:0]) | | R/W | Controls offset for odd F1P data sampler. Decode from OFST\_F1P\_D\_O[6:0] in digital |
| ofst\_f1n\_pos\_d\_o\_lane[4:0]  (R0880h[4:0]) | | R/W | Controls offset for odd F1N data sampler. Decode from OFST\_F1N\_D\_O[6:0] in digital |
| ofst\_f1n\_neg\_d\_o\_lane[4:0]  (R0884h[4:0]) | | R/W | Controls offset for odd F1N data sampler. Decode from OFST\_F1N\_D\_O[6:0] in digital |
| ofst\_f1p\_pos\_s\_e\_lane[4:0]  (R0488h[4:0]) | | R/W | Controls offset for even F1P slicer sampler. Decode from OFST\_F1P\_D\_E[6:0] in digital |
| ofst\_f1p\_neg\_s\_e\_lane[4:0]  (R048Ch[4:0]) | | R/W | Controls offset for even F1P slicer sampler. Decode from OFST\_F1P\_D\_E[6:0] in digital |
| ofst\_f1n\_pos\_s\_e\_lane[4:0]  (R0490h[4:0]) | | R/W | Controls offset for even F1N slicer sampler. Decode from OFST\_F1N\_D\_E[6:0] in digital |
| ofst\_f1n\_neg\_s\_e\_lane[4:0]  (R0494h[4:0]) | | R/W | Controls offset for even F1N slicer sampler. Decode from OFST\_F1N\_D\_E[6:0] in digital |
| ofst\_f1p\_pos\_s\_o\_lane[4:0]  (R0888h[4:0]) | | R/W | Controls offset for odd F1P slicer sampler. Decode from OFST\_F1P\_D\_O[6:0] in digital |
| ofst\_f1p\_neg\_s\_o\_lane[4:0]  (R088Ch[4:0]) | | R/W | Controls offset for odd F1P slicer sampler. Decode from OFST\_F1P\_D\_O[6:0] in digital |
| ofst\_f1n\_pos\_s\_o\_lane[4:0]  (R0890h[4:0]) | | R/W | Controls offset for odd F1N slicer sampler. Decode from OFST\_F1N\_D\_O[6:0] in digital |
| ofst\_f1n\_neg\_s\_o\_lane[4:0]  (R0894h[4:0]) | | R/W | Controls offset for odd F1N slicer sampler. Decode from OFST\_F1N\_D\_O[6:0] in digital |
| cal\_ofst\_edge\_e\_lane[7:0]  (R2520h[6:0]) | R/W | FW saves each sampler result. |
| cal\_ofst\_edge\_o\_lane[7:0]  (R2520h[14:8]) | R/W | FW saves each sampler result. |
| sampler\_cal\_done\_lane  (R6000h[11]) | R | Sampler calibration done. |

### VDD Calibration

|  |  |  |
| --- | --- | --- |
| **Register Name** | **R/W** | **Description** |
| sellv\_txclk\_ch0/1/2/3[3:0]  (R8270h-R8274h) | R/W | TX clock voltage regulator control value. Unsigned binary |
| sellv\_txdata\_ch0/1/2/3[3:0]  (R8278h-R827Ch) | R/W | TX data voltage regulator control value. Unsigned binary |
| sellv\_txpre\_ch0/1/2/3[3:0]  (R8280h-R8284h) | R/W | TX pre-driver voltage regulator control value. Unsigned binary |
| sellv\_rxeomclk\_ch0/1/2/3[3:0]  (R8240h-R8244h) | R/W | RX EOM clock routing voltage regulator control value. Unsigned binary |
| sellv\_rxdataclk\_ch0/1/2/3[3:0]  (R8238h-R823Ch) | R/W | RX data clock voltage regulator control value. Unsigned binary |
| sellv\_rxsampelr\_ch0/1/2/3[3:0]  (R8248h-R824Ch) | R/W | RX sampler voltage regulator control value. Unsigned binary |
| vdd\_cal\_done\_lane  (R6000h[15]) | R | VDD calibration done indicator. |

## Other Calibration Registers

|  |  |  |
| --- | --- | --- |
| **Register Name** | **R/W** | **Description** |
| CAL\_DONE  (RE604h[8]) | R | Calibration done. |
| EXT\_FORCE\_CAL\_DONE  (RE604h[17]) | R | External force calibration done |

# TRX TRAIN

## TRX Train Flow Chart



|  |  |  |
| --- | --- | --- |
| **Bypass Register** | **Default** | **Description** |
| TX\_TRAIN\_ENABLE\_LANE  (R2010h[5]) | 1’b0 | TRx training enable in Isolation mode. |
| TX\_NO\_INIT\_LANE  (R604Ch[2]) | 1’b0 | No Tx initial during Tx train.  1’b0: TX preset commands are sent to remote PHY. Which preset command is used is determined by the register tx\_preset\_index\_lane[7:0].  1’b1: (Bypass) TX preset commands are not sent to remote PHY at the beginning of the TX training. |
| RX\_NO\_INIT\_LANE  (R604Ch[1]) | 1’b0 | No Rx initial during Rx train.  1’b0: initialize and reset R\_INI and C\_INI of Rx FFE settings at the beginning of TX/RX training.  1’b1: (Bypass) RX FFE settings are not reset at the beginning of the TX/RX training. |
| GAIN\_TRAIN\_INIT\_EN\_LANE  (R6038h[18]) | 1’b1 | 0: [GAIN TRAIN] DFE resolution training disable during Tx/Rx train initialize state. |
| RX\_TRAIN\_ENABLE\_LANE  (R210Ch[3]) | 1’b0 | TRx training enable in Isolation mode. |
| bypass\_rxtrain\_lane  (R6098h[6]) | 1’b0 | 1: Bypass Rx Train during TRx train for test. |
| GAIN\_TRAIN\_END\_EN\_LANE  (R6038h[17]) | 1’b1 | 0: [GAIN TRAIN] DFE resolution training disable during Tx/Rx train end state. |

## Tx Train Flow Chart



|  |  |  |
| --- | --- | --- |
| **Bypass Registers** | **Default** | **Description** |
| TX\_ADAPT\_G0\_EN\_LANE  (R6058h[23]) | 1’b0 | Tx FFE adapt G0 enable. |
| TX\_ADAPT\_GN1\_EN\_LANE  (R6058h[22]) | 1’b0 | Tx FFE adapt Gn1 enable. |
| TX\_ADAPT\_G1\_EN\_LANE  (R6058h[21]) | 1’b0 | Tx FFE adapt G1 enable. |

## Rx Train Flow Chart

|  |  |  |
| --- | --- | --- |
| **Bypass Registers** | **Default** | **Description** |
| bypass\_ctle\_train\_lane  (by MCU-FW control) | 1’b0 | 1: Bypass Rx CTLE train for test. |
| CDRPHASE\_OPT\_EN\_LANE  (R604Ch[15]) | 1’b0 | 0: Bypass Rx phase train for test. |

### Train Algorithm Control

#### **Tx Train**

|  |  |
| --- | --- |
| **Register Name** | **Description** |
| TX\_ADAPT\_G0\_EN\_LANE  (R6058h[23]) | Tx FFE adapt G0 enable. |
| TX\_ADAPT\_GN1\_EN\_LANE  (R6058h[22]) | Tx FFE adapt Gn1 enable. |
| TX\_ADAPT\_G1\_EN\_LANE  (R6058h[21]) | Tx FFE adapt G1 enable. |
| TRAIN\_G0\_LANE[7:0]  (R6030h[23:16]) | Tx Train G0 Value. |
| TRAIN\_G1\_LANE[7:0]  (R6030h[15:8]) | Tx Train G1 Value. |
| TRAIN\_GN1\_LANE[7:0]  (R6030h[7:0]) | Tx Train GN1 Value. |
| TX\_G0\_STEP\_SIZE\_LANE[1:0]  (R60A4h[23:22]) | Tx G0 step size |
| TX\_G1\_STEP\_SIZE\_LANE[1:0]  (R60A4h[25:24]) | Tx G1 step size |
| TX\_GN1\_STEP\_SIZE\_LANE[1:0]  (R60A4h[21:20]) | Tx Gn1 step size |
| TX\_G0\_STEP\_NUM\_LANE[3:0]  (R60A4h[19:16]) | Number of Tx G0 steps to be searched. |
| TX\_G1\_STEP\_NUM\_LANE[4:0]  (R608Ch[7:3]) | Number of Tx G1 steps to be searched. |
| TX\_GN1\_STEP\_NUM\_LANE[4:0]  (R60A4h[30:26]) | Number of Tx GN1 steps to be searched. |
| TX\_G1\_MAXF0T\_EN\_LANE  (R60A4h[7]) | Tx G1 Max F0t train enable |
| TX\_GN1\_MAXF0T\_EN\_LANE  (R60A4h[6]) | Tx GN1 Max F0t train enable |
| TX\_G1\_MIDPOINT\_EN\_LANE  (R6030h[25]) | TX G1 mid-point train enable |
| TX\_GN1\_MIDPOINT\_EN\_LANE  (R6038h[5]) | TX GN1 mid-point train enable |
| tx\_gn1\_midpoint\_thres\_k\_lane[7:0]  (R6050h[15:8]) | Tx Gn1 midpoint threshold K |
| tx\_gn1\_midpoint\_thres\_c\_lane[7:0]  (R6050h[7:0]) | Tx Gn1 midpoint threshold C (2's Complement) |
| tx\_g1\_midpoint\_thres\_k\_lane[7:0]  (R6084h[15:8]) | Tx G1 midpoint threshold K |
| tx\_g1\_midpoint\_thres\_c\_lane[7:0]  (R6084h[7:0]) | Tx G1 midpoint threshold C (2's Complement) |
| cfg\_cursor\_preset0\_lane[5:0]  (R402Ch[5:0]) | Cursor coefficient of preset0 |
| cfg\_cursor\_preset1\_lane[5:0]  (R402Ch[11:6]) | Cursor coefficient of preset1 |
| cfg\_cursor\_preset2\_lane[5:0]  (R402Ch[21:16]) | Cursor coefficient of preset2 |
| cfg\_cursor\_preset3\_lane[5:0]  (R402Ch[27:22]) | Cursor coefficient of preset3 |
| cfg\_cursor\_preset4\_lane[5:0]  (R4030h[5:0]) | Cursor coefficient of preset4 |
| cfg\_cursor\_preset5\_lane[5:0]  (R4030h[11:6]) | Cursor coefficient of preset5 |
| cfg\_cursor\_preset6\_lane[5:0]  (R4030h[21:16]) | Cursor coefficient of preset6 |
| cfg\_cursor\_preset7\_lane[5:0]  (R4030h[27:22]) | Cursor coefficient of preset7 |
| cfg\_cursor\_preset8\_lane[5:0]  (R4034h[5:0]) | Cursor coefficient of preset8 |
| cfg\_cursor\_preset9\_lane[5:0]  (R4034h[11:6]) | Cursor coefficient of preset9 |
| cfg\_cursor\_preset10\_lane[5:0]  (R4034h[21:16]) | Cursor coefficient of preset10 |
| cfg\_post\_cursor\_preset0\_lane[5:0]  (R4038h[11:6]) | Post-Cursor coefficient of preset0 |
| cfg\_post\_cursor\_preset1\_lane[5:0]  (R4038h[27:22]) | Post-Cursor coefficient of preset1 |
| cfg\_post\_cursor\_preset2\_lane[5:0]  (R403Ch[11:6]) | Post-Cursor coefficient of preset2 |
| cfg\_post\_cursor\_preset3\_lane[5:0]  (R403Ch[27:22]) | Post-Cursor coefficient of preset3 |
| cfg\_post\_cursor\_preset4\_lane[5:0]  (R4040h[11:6]) | Post-Cursor coefficient of preset4 |
| cfg\_post\_cursor\_preset5\_lane[5:0]  (R4040h[27:22]) | Post-Cursor coefficient of preset5 |
| cfg\_post\_cursor\_preset6\_lane[5:0]  (R4044h[11:6]) | Post-Cursor coefficient of preset6 |
| cfg\_post\_cursor\_preset7\_lane[5:0]  (R4044h[27:22]) | Post-Cursor coefficient of preset7 |
| cfg\_post\_cursor\_preset8\_lane[5:0]  (R4048h[11:6]) | Post-Cursor coefficient of preset8 |
| cfg\_post\_cursor\_preset9\_lane[5:0]  (R4048h[27:22]) | Post-Cursor coefficient of preset9 |
| cfg\_post\_cursor\_preset10\_lane[5:0]  (R404Ch[11:6]) | Post-Cursor coefficient of preset10 |
| cfg\_pre\_cursor\_preset0\_lane[5:0]  (R4038h[5:0]) | Pre-Cursor coefficient of preset0 |
| cfg\_pre\_cursor\_preset1\_lane[5:0]  (R4038h[21:16]) | Pre-Cursor coefficient of preset1 |
| cfg\_pre\_cursor\_preset2\_lane[5:0]  (R403Ch[5:0]) | Pre-Cursor coefficient of preset2 |
| cfg\_pre\_cursor\_preset3\_lane[5:0]  (R403Ch[21:16]) | Pre-Cursor coefficient of preset3 |
| cfg\_pre\_cursor\_preset4\_lane[5:0]  (R4040h[5:0]) | Pre-Cursor coefficient of preset4 |
| cfg\_pre\_cursor\_preset5\_lane[5:0]  (R4040h[21:16]) | Pre-Cursor coefficient of preset5 |
| cfg\_pre\_cursor\_preset6\_lane[5:0]  (R4044h[5:0]) | Pre-Cursor coefficient of preset6 |
| cfg\_pre\_cursor\_preset7\_lane[5:0]  (R4044h[21:16]) | Pre-Cursor coefficient of preset7 |
| cfg\_pre\_cursor\_preset8\_lane[5:0]  (R4048h[5:0]) | Pre-Cursor coefficient of preset8 |
| cfg\_pre\_cursor\_preset9\_lane[5:0]  (R4048h[21:16]) | Pre-Cursor coefficient of preset9 |
| cfg\_pre\_cursor\_preset10\_lane[5:0]  (R404Ch[5:0]) | Pre-Cursor coefficient of preset10 |
| CFG\_EQ\_FS\_LANE[5:0]  (R4024h[21:16]) | Local transmitter full swing parameter (FS). |
| CFG\_EQ\_16G\_FS\_LANE[5:0]  (R4058h[5:0]) | Local transmitter full swing parameter (FS). |
| CFG\_EQ\_LF\_LANE[5:0]  (R4024h[27:22]) | Local transmitter low frequency Parameter (LF). |
| CFG\_EQ\_16G\_LF\_LANE[5:0]  (R4058h[11:6]) | Local transmitter low frequency parameter (LF). |
| cfg\_tx\_coeff\_max0\_lane[11:0]  (R4050h[11:0]) | Local Tx transmitter coefficient maximum value.  Bit[5:0]: C-1  Bit[11:6]:C0 |
| cfg\_tx\_coeff\_max1\_lane[5:0]  (R4050h[21:16]) | Local Tx transmitter coefficient maximum value.  Bit[5:0]: C+1 |
| TX\_EM\_PRE\_MAX\_LANE[3:0]  (R600Ch[31:28]) | Tx pre emphasis maximum in SAS/Ethernet mode |
| TX\_EM\_PO\_MAX\_LANE[3:0]  (R600Ch[27:24]) | Tx post emphasis maximum in SAS/Ethernet mode |
| TX\_EM\_PEAK\_MIN\_LANE[3:0]  (R600Ch[23:20]) | Tx peak emphasis minimum in SAS/Ethernet mode |
| TX\_EM\_PEAK\_MAX\_LANE[3:0]  (R600Ch[19:16]) | Tx Peak Emphasis Maximum in SAS/Ethernet mode |
| TX\_TRAIN\_P2P\_HOLD\_LANE  (R6044h[3]) | Tx train peak to peak hold enable.  1'b0: Tx coefficient control separately.  1'b1: Hold the range of peak to peak range. The coefficient changes of G0, G1 and Gn1 impact each other. |

#### **Rx Train**

CDR TRAIN

|  |  |
| --- | --- |
| **Register Name** | **Description** |
| CDRPHASE\_OPT\_EN\_LANE  (R604Ch[15]) | 0: CDR phase optimization train bypass  1: CDR phase optimization train enable. |
| CDR\_MAXF0P\_EN\_LANE  (R60A0h[6]) | CDR max F0p train enable |
| CDR\_MIDPOINT\_EN\_LANE  (R6038h[0]) | CDR midpoint train enable |
| CDR\_STEP\_NUM\_LANE[3:0]  (R60A4h[15:12]) | CDR step number |
| midpoint\_small\_thres\_k\_lane[3:0]  (R6050h[23:20]) | CDR midpoint small threshold k. |
| midpoint\_small\_thres\_c\_lane[3:0]  (R6050h[19:16]) | CDR midpoint small threshold c. |
| midpoint\_large\_thres\_k\_lane[3:0]  (R6050h[31:28]) | CDR midpoint large threshold k. |
| midpoint\_large\_thres\_c\_lane[3:0]  (R6050h[27:24]) | CDR midpoint large threshold c. |

FFE TRAIN

|  |  |
| --- | --- |
| **Register Name** | **Description** |
| DFE\_F0\_SAT\_THRES\_LANE[7:0]  (R6064h[31:24]) | DFE F0 Saturation Threshold (0~63) => To avoid saturated F0A. |
| RX\_RXFFE\_R\_INI\_LANE[3:0]  (R6058h[31:28]) | Rx FFE Resistor Initial. |
| RX\_RXFFE\_C\_INI\_LANE[3:0]  (R608Ch[31:28]) | Rx FFE Capacitor Initial. |
| FFE\_DATA\_RATE\_LANE[3:0]  (R0208h[7:4]) | FFE Data Rate Selection.  Downloaded from the speed table. |

GAIN TRAIN

|  |  |
| --- | --- |
| **Register Name** | **Description** |
| gain\_train\_init\_en\_lane  (R6038h[18]) | DFE resolution training enable during Tx/Rx train initialize state. |
| gain\_train\_end\_en\_lane  (R6038h[17]) | DFE resolution training enable during Tx/Rx train end state. |
| GAIN\_TRAIN\_WITH\_C\_LANE  (R6038h[16]) | FFE capacitor enable during gain train.  1’b0: FFE\_CAP will be swept in the search table.  1’b1: FFE\_CAP will not be swept in the search table. |
| rxffe\_r\_gain\_train\_lane[3:0]  (R6058h[27:24]) | FFE resistor gain train. |
| DFE\_RES\_F0A\_HIGH\_THRES\_INIT\_LANE[7:0]  (R602Ch[31:24]) | DFE resolution F0a high threshold for train initial stage |
| DFE\_RES\_F0A\_HIGH\_THRES\_END\_LANE[7:0]  (R606Ch[7:0]) | DFE resolution F0a high threshold for train end stage |
| DFE\_RES\_F0A\_LOW\_THRES\_01\_INIT\_LANE[7:0]  (R6078h[7:0]) | DFE resolution F0a low threshold 01 for gain train in train initial stage. |
| DFE\_RES\_F0A\_LOW\_THRES\_2\_INIT\_LANE[7:0]  (R6078h[15:8]) | DFE resolution F0a low threshold 2 for gain train in train initial stage. |
| DFE\_RES\_F0A\_LOW\_THRES\_3\_INIT\_LANE[7:0]  (R6078h[23:16]) | DFE resolution F0a low threshold 3 for gain train in train initial stage. |
| DFE\_RES\_F0A\_LOW\_THRES\_01\_END\_LANE[7:0]  (R6078h[31:24]) | DFE resolution F0a low threshold 01 for gain train in train end stage. |
| DFE\_RES\_F0A\_LOW\_THRES\_2\_END\_LANE[7:0]  (R6074h[7:0]) | DFE resolution F0a low threshold 2 for gain train in train end stage. |
| DFE\_RES\_F0A\_LOW\_THRES\_3\_END\_LANE[7:0]  (R6074h[15:8]) | DFE resolution F0a low threshold 3 for gain train in train end stage. |

#### **Others**

|  |  |
| --- | --- |
| **Register Name** | **Description** |
| CFG\_RX\_EQ\_CTRL\_LANE  (R4010h[18]) | PHY Rx training enable while in USB3 LTSSM Polling.RxEQ State, or PCIE LTSSM recovery equalization state. (PIPE lane register)  1'b0: Disable Rx Training.  1'b1: Enable Rx Training. |
| CFG\_UPDATE\_POLARITY\_LANE  (R4028h[12]) | Select polarity of coefficient updates at C-1 and C+1. (PIPE lane register)  1'b0: Increment and decrement with signed value.  1'b1: Increment and decrement with absolute value. |
| cfg\_use\_ctrl\_fld\_rst\_lane  (R4024h[31]) | PHY control field reset command select. This bit enables the reset command for remote Tx training. (PIPE lane register)  1'b0: Do not use PHY remote\_ctrl\_field\_reset\_lane command.  1'b1: Use phy remote\_ctrl\_field\_reset\_lane command. |
| CFG\_CLK\_SRC\_MASK  (RC004h[30]) | Clock source mask for master lane to handle lane turn off signaling.  (PIPE CMN register)  1'b0: When the lane is the master lane, the lane turn off signal does not disable the whole lane.  1'b1: When the lane is the master lane, the lane off signal enables only the power management block, all other blocks of the lane are disabled. |
| thre\_poor\_lane[2:0]  (R604Ch[18:16]) | DFE level check threshold for poor. |
| thre\_good\_lane[4:0]  (R604Ch[12:8]) | DFE level check threshold for good. |
| thre\_excellent\_lane[5:0]  (R604Ch[29:24]) | DFE level check threshold for excellent. |

PIPE Control by MCU

|  |  |  |
| --- | --- | --- |
| **Register Name** | **Value** | **Description** |
| ebuf\_threshold\_wide\_lane  (R400Ch[28]) | 1’b1 | Elastic buffer threshold hysteresis. |

### Training Timer Registers

|  |  |  |
| --- | --- | --- |
| **GPO Signals** | **Default** | **Description** |
| tx\_train\_status\_det\_timer\_enable\_lane  (R6030h[31]) | 1’b1 | Tx Train Status Detection Timeout Enable. |
| RX\_TRAIN\_TIMER\_ENABLE\_LANE  (R6030h[30]) | 1’b1 | Rx Train Timeout Enable. |
| TX\_TRAIN\_TIMER\_ENABLE\_LANE  (R6030h[29]) | 1’b1 | Tx Train Timeout Enable. |
| TX\_TRAIN\_FRAME\_DET\_TIMER\_ENABLE\_LANE  (R6030h[28]) | 1’b1 | Tx Train Frame Detection Timeout Enable. |
| frame\_lock\_sel\_timeout\_lane  (R6030h[27]) | 1’b0 | Frame Lock Select Timeout.  1'b0: Use internal generated frame lock signal to start TRx train frame detection timers.  1'b1: Use PIN\_TX\_TRAIN\_ENABLE as frame lock to start TRx train frame detection timers. |
| tx\_train\_status\_det\_timeout\_int\_lane  (R6030h[26]) | 1’b0 | Tx Train Status Detect Timeout Indicator from MCU. |
| TX\_TRAIN\_FRAME\_DET\_TIMER\_LANE[7:0]  (R6028h[23:16]) | 8’h01 | Frame marker detection maximum wait during TRX. |
| RX\_TRAIN\_TIMER\_LANE[15:0]  (R6028h[15:0]) | 8’h01F3 | Rx train maximum time. |
| TRX\_TRAIN\_TIMER\_LANE[15:0]  (R602Ch[15:0]) | 8’h01F3 | Tx train maximum time. |

### SAS Train Error

TX\_TRAIN\_ERROR\_LANE register values is valid when TX\_TRAIN\_FAILED\_LANE = 1.

|  |  |
| --- | --- |
| **TX\_TRAIN\_ERROR\_LANE[1:0]** | **Description** |
| 0 | Frame lock error |
| 1 | Train Algorithm failed, cannot open Eye. |
| 2 | MTTT (Maximum Transmitter Training Time) expired. |
| 3 | Remote PHY didn't get TRAIN Complete within MTTT not for PCIe mode. |

# Command Interface

## Timing Diagram

## Sequence

### Command Interface Program Sequence

* 1. Set a command by programming PHY\_REMOTE\_CTRL\_COMMAND\_TYPE\_LANE[7:0], PHY\_REMOTE\_CTRL\_COMMAND\_CODE\_LANE[15:0], PHY\_REMOTE\_CTRL\_VALUE\_LANE[31:0] and PHY\_LOCAL\_VALUE\_LANE[31:0] depending on the interface required.
  2. Program PHY\_MCU\_REMOTE\_REQ\_LANE = 1
  3. Wait until PHY\_MCU\_LOCAL\_ACK\_LANE = 1
  4. PHY\_LOCAL\_STATUS\_LANE, PHY\_LOCAL\_VALUE\_LANE can be read at this time
  5. Program PHY\_MCU\_REMOTE\_REQ\_LANE = 0
  6. Wait for PHY\_MCU\_LOCAL\_ACK\_LANE = 0 for the next communication
  7. Repeat above steps.

### Related FW CMD\_IF Registers

|  |  |  |
| --- | --- | --- |
| **Signal Name** | **DIR** | **Description** |
| PHY\_REMOTE\_CTRL\_COMMAND\_TYPE\_LANE[7:0]  (R601Ch[31:24]) | I | PHY Remote Control Type Command. |
| PHY\_REMOTE\_CTRL\_COMMAND\_CODE\_LANE[15:0]  (R601Ch[15:0]) | I | PHY Remote Control Code Command. |
| PHY\_REMOTE\_CTRL\_VALUE\_LANE[31:0]  (R6020h[31:0]) | I | PHY Remote Control Value. |
| PHY\_MCU\_REMOTE\_REQ\_LANE  (R22E4h[0]) | I | PHY MCU Remote Request. |
| PHY\_MCU\_LOCAL\_ACK\_LANE  (R6030h[24]) | O | PHY MCU Local Acknowledge. |
| PHY\_REMOTE\_CTRL\_COMMAND\_TYPE\_LANE[7:0]  (R601Ch[31:24]) | I | PHY Remote Control Type Command. |
| PHY\_REMOTE\_CTRL\_COMMAND\_CODE\_LANE[15:0]  (R601Ch[15:0]) | I | PHY Remote Control Code Command. |
| PHY\_LOCAL\_STATUS\_LANE[7:0]  (R602Ch[23:16]) | O | Command Interface Local Status.  0x0: OK  0x1: Indicated invalid command type or code.  0x2: Not ready to take this command or not valid in this stage  0x3: Reserved  0x4: Invalid remote control value |
| PHY\_LOCAL\_VALUE\_LANE[31:0]  (R6024h[31:0]) | O | PHY LOCAL Value. |

### Firmware Command Tables

1. For all commands in the command tables are valid when PHY\_REMOTE\_CTRL\_VALUE\_LANE[31] = 1 (in debug state for current speed), direct write and read of PHY hardware registers is possible according to PHY\_REMOTE\_CTRL\_VALUE\_LANE[23:0] values for debug purposes, and the PHY\_REMOTE\_CTRL\_VALUE\_LANE[27:24] (GEN number) setting is ignored. When new speed values are entered, the register values which had been programmed when PHY\_REMOTE\_CTRL\_VALUE\_LANE[31] = 1 are overwritten.

#### **Command Type = 0x80**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Command Description** | **PHY\_REMOTE\_CTRL\_COMMAND\_TYPE\_LANE[7:0]** | **PHY\_REMOTE\_CTRL\_COMMAND\_CODE\_LANE[15:0]** | **PHY\_REMOTE\_CTRL\_VALUE\_LANE[31:0]** | **PHY\_LOCAL\_VALUE[31:0]** |
| Set TX FFE control per GEN    OPERATION: MCU-FW loads into GEN table, then sets up circuit on speed-change. Direct Reg: ana\_tx\_em\_peak\_en\_lane  (R2634h[23]) ana\_tx\_em\_pre\_en\_lane  (R2634h[22]) ana\_tx\_em\_po\_en\_lane  (R2634h[21]) | 0x80 | 0x0000 | [31]: Debug for current speed [27:24]: GEN number  [15:12]: Peak amplitude control  [11:8]: Pre emphasis control  [7:4]: Post emphasis control  [3]: Enable peak emphasis control  [2]: Enable pre emphasis control  [1]: Enable post emphasis control  [0]: Force TXFFE control Enable   1: Force to stay on user program value from command interface during training  0: Enable adapted value during training | None |
| Get TX FFE control per GEN | 0x80 | 0x0001 | [31]: Debug for current speed  [27:24]: GEN number | [31]: Debug for current speed  [27:24]: GEN number [15:12]: Peak amplitude control [11:8]: Pre emphasis control [7:4]: Post emphasis control [3]: Enable peak emphasis control [2]: Enable pre emphasis control [1]: Enable post emphasis control [0]: Force TXFFE control Enable |
| Set TX slew rate per GEN    OPERATION: MCU-FW loads into GEN table, then sets up circuit on speed-change. Direct Reg: slewrate\_en\_lane[1:0]  (R004Ch[7:6]) slewctrl0\_lane[1:0]  (R004Ch[5:4]) slewctrl1\_lane[1:0]  (R004Ch[3:2]) | 0x80 | 0x0006 | [31]: Debug for current speed [27:24]: GEN number [17:16]: Slew rate enable 00: Fast Slew Rate 11: slow Slew Rate All others: Not valid [9:8]: Slew control 1 [1:0]: Slew control 0 | None |
| Get TX slew rate per GEN | 0x80 | 0x0007 | [31]: Debug for current speed  [27:24]: GEN number | [31]: Debug for current speed  [27:24]: GEN number [17:16]: Slew rate enable 00: Fast Slew Rate 11: slow Slew Rate All others: Not valid [9:8]: Slew control 1 [1:0]: Slew control 0 |
| Set TX SSC per GEN    OPERATION: MCU-FW loads into GEN table, then sets up circuit on speed-change. Direct Reg: ssc\_en\_lane  (R200Ch[2]) ssc\_step[10:0]  (RA00Ch[10:0]) ssc\_step\_ring[10:0]  (RA014h[10:0]) ssc\_dspread\_tx  (RA008h[30]) ssc\_dspread\_tx\_ring  (RA010h[30]) | 0x80 | 0x0008 | [31]: Debug for current speed  [27:24]: GEN number [16]: SSC enable [14:12] SSC\_STEP[10:8] in 28G X4 R2P1 [8]: SSC down/center spread select 0: Center-Spread 1: Down-Spread [6:0]: SSC AMP in 28G X2 R2P0 [7:0: SSC STEP[7:0] in 28G X4 R2P1 | None |
| Get TX SSC per GEN | 0x80 | 0x0009 | [31]: Debug for current speed  [27:24]: GEN number | [31]: Debug for current speed  [27:24]: GEN number [16]: SSC enable [14:12] SSC\_STEP[10:8] in 28G X4 R2P1 [8]: SSC down/center spread select 0: Center-spread 1: Down-Spread [6:0]: SSC AMP in 28G X2 R2P0 [7:0: SSC STEP[7:0] in 28G X4 R2P1 |
| Set TX margin    OPERATION: MCU-FW sets up circuit immediately. Direct Reg: tx\_margin\_lane[2:0]  (R2010h[31:29]) | 0x80 | 0x000A | [2:0]: TX margin | None |
| Get TX margin | 0x80 | 0x000B | None | [2:0]: TX margin |
|  |  |  |  |  |

#### **Command Type = 0x81**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Command Description** | **PHY\_REMOTE\_CTRL\_COMMAND\_TYPE\_LANE[7:0]** | **PHY\_REMOTE\_CTRL\_COMMAND\_CODE\_LANE[15:0]** | **PHY\_REMOTE\_CTRL\_VALUE\_LANE[31:0]** | **PHY\_LOCAL\_VALUE[31:0]** |
| Set Local-to-Remote TX preset index    OPERATION: MCU-FW saves value, then sets up circuit during Training process. FW Reg control | 0x81 | 0x0000 | [7:0]: Local-to-Remote Local Tx Preset Index In case of PHY\_MODE = SAS  0 : not applicable  1: Refereance 1  2: Refereance 2  3: No Equalization  In case of PHY\_MODE = ETHERNET  0: not applicable  1: Init   2: preset  \* All other phy\_mode is not applicable. | None  Note: This is to control TTIU Tx Preset value for Local to Remote. |
| Get Local-to-Remote TX preset index | 0x81 | 0x0001 | NONE | [7:0]: Local Tx Preset Index |
| Set Local TX presets Table    OPERATION: MCU-FW saves value, then sets up circuit during Training process. FW Reg control | 0x81 | 0x0002 | [27:24]: Tx Preset table select [23:16] Don't care [15:12]: Peak amplitude [11:8]: Pre emphasis [7:4]: Post emphasis [3:0] Don't care | None |
| Get Local TX presets Table | 0x81 | 0x0003 | [27:24]: Tx Preset table slect  In case of PHY\_MODE = SAS  0 : NA  1: Refereance 1  2: Refereance 2  3: No Equalization  In case of PHY\_MODE = ETHERNET  4: Init   5: preset   \* All other phy\_mode is not applicable. | [27:24]: Tx Preset table select [23:16] Don't care [15:12]: Peak amplitude [11:8]: Pre emphasis [7:4]: Post emphasis [3:0] Don't care |
| Set Local TX preset index    OPERATION: MCU-FW saves value, then sets up circuit during Training process. FW Reg control | 0x81 | 0x0004 | [7:0]: Local Tx Preset Index In case of PHY\_MODE = SAS  0 : NA  1: Refereance 1  2: Refereance 2  3: No Equalization  In case of PHY\_MODE = ETHERNET  4: Init   5: preset   \* All other phy\_mode is not applicable. | None   Note: This to to control initial TXFFE select from TxPreset table. It will impact at the beginning of TrxTrain. |
| Get Local TX preset index | 0x81 | 0x0005 | NONE | [7:0]: Local Tx Preset Index |
|  |  |  |  |  |

#### **Command Type = 0x82**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Command Description** | **PHY\_REMOTE\_CTRL\_COMMAND\_TYPE\_LANE[7:0]** | **PHY\_REMOTE\_CTRL\_COMMAND\_CODE\_LANE[15:0]** | **PHY\_REMOTE\_CTRL\_VALUE\_LANE[31:0]** | **PHY\_LOCAL\_VALUE[31:0]** |
| Set RX CDR BW per GEN    OPERATION: MCU-FW loads into GEN table, then sets up circuit on speed-change. Direct Reg: rx\_selmufi\_lane[2:0]  (R2164h[12:10]) rx\_selmuff\_lane[2:0]  (R2164h[15:13]) reg\_selmupi\_lane[3:0]  (R022Ch[3:0]) reg\_selmupf\_lane[3:0]  (R0230h[7:4]) | 0x82 | 0x0000 | [31]: Debug for current speed  [27:24]: GEN number [15:12]: Phase loop final coefficient [11:8]: Phase loop initial coefficient [6:4]: Select final multiple frequency [2:0]: Select initial multiple frequency | None |
| Get RX CDR BW per GEN | 0x82 | 0x0001 | [31]: Debug for current speed  [27:24]: GEN number | [31]: Debug for current speed  [27:24]: GEN number [15:12]: Phase loop final coefficient [11:8]: Phase loop initial coefficient [6:4]: Select final multiple frequency [2:0]: Select initial multiple frequency |
| Set RX FFE resistor selection per GEN    OPERATION: MCU-FW loads into GEN table, then sets up circuit on speed-change. Direct Reg: ffe\_res1\_sel\_lane[3:0]  (R0200h[7:4]) ffe\_res2\_sel\_e\_lane[3:0]  (R0000h[7:4]) ffe\_res2\_sel\_o\_lane[3:0]  (R0204h[7:4]) ffe\_cap1\_sel\_lane[3:0]  (R0200h[3:0]) ffe\_cap2\_sel\_e\_lane[3:0]  (R0000h[3:0]) ffe\_cap2\_sel\_o\_lane[3:0]  (R0204h[3:0]) | 0x82 | 0x0002 | [31]: Debug for current speed  [27:24]: GEN number [23:20]: FFE 2nd stage odd resistor selection [19:16]: FFE 2st stage odd cap selection [15:12]: DON’T CARE [11:8]: DON’T CARE [7:4]: FFE 1st stage resistor selection [3:0]: FFE 1st stage cap selection | None |
| Get RX FFE resistor selection per GEN | 0x82 | 0x0003 | [31]: Debug for current speed  [27:24]: GEN number | [31]: Debug for current speed  [27:24]: GEN number [23:20]: FFE 2nd stage odd resistor selection [19:16]: FFE 2st stage odd cap selection [15:12]: DON’T CARE [11:8]: DON’T CARE [7:4]: FFE 1st stage resistor selection [3:0]: FFE 1st stage cap selection |
| Set RX DFE enable and resolution per GEN    OPERATION: MCU-FW loads into GEN table, then sets up circuit on speed-change. Direct Reg: dfe\_en\_lane  (R2410h[4]) dfe\_res\_f0\_lane[1:0]  (R0050h[4:3]) dfe\_res\_f1\_lane[1:0]  (R0050h[2:1]) dfe\_res\_f234\_lane  (R0050h[0]) dfe\_res\_f567\_lane  (R0054h[7]) dfe\_res\_f8to15\_lane  (R0054h[6]) dfe\_res\_floating\_lane  (R0054h[5]) | 0x82 | 0x0004 | [31]: Debug for current speed  [27:24]: GEN number [9]: DFE enable select 1:from command interface 0: from PIN\_DFE\_EN [8]: DFE enable [7]: F5, F6, F7 resolution [6]: F8 to F15 resolution [5]: Floating tap resolution [4:3]: F0 resolution [2:1]: F1 resolution [0]: F2, F3, F4 resolution | None |
| Get RX DFE enable and resolution per GEN | 0x82 | 0x0005 | [31]: Debug for current speed  [27:24]: GEN number | [31]: Debug for current speed [27:24]: GEN number [9]: DFE enable select 1:from command interface 0: from PIN\_DFE\_EN [8]: DFE enable [7]: F5, F6, F7 resolution [6]: F8 to F15 resolution [5]: Floating tap resolution [4:3]: F0 resolution [2:1]: F1 resolution [0]: F2, F3, F4 resolution |
| Set SQ threshold ratio per GEN    OPERATION: MCU-FW loads into GEN table, then sets up circuit on speed-change. Direct Reg: sq\_thresh\_lane[5:0]  (R0010h[7:2]) | 0x82 | 0x0006 | [31]: Debug for current speed  [27:24]: GEN number [5:0]: Squelch detector threshold ratio | None The squelch threshold = sq\_thresh\_cal\_result \* ratio When sq\_det\_thre\_ratio is not 0, the ratio = sq\_det\_thre\_ratio / 32. When sq\_det\_thre\_ratio is 0, the ratio = 1. \* sq\_det\_thre\_ratio: user defined by Squelch detector threshold ratio  \* sq\_thresh\_cal\_result : SQ threshold calibration result |
| Get SQ threshold ratio per GEN | 0x82 | 0x0007 | [31]: Debug for current speed  [27:24]: GEN number | [31]: Debug for current speed  [27:24]: GEN number [5:0]: Squelch detector threshold ratio |
|  |  |  |  |  |

#### **Command Type = 0x83**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Command Description** | **PHY\_REMOTE\_CTRL\_COMMAND\_TYPE\_LANE[7:0]** | **PHY\_REMOTE\_CTRL\_COMMAND\_CODE\_LANE[15:0]** | **PHY\_REMOTE\_CTRL\_VALUE\_LANE[31:0]** | **PHY\_LOCAL\_VALUE[31:0]** |
| Set bypass CTLE train    OPERATION: MCU-FW saves value, then sets up circuit during Training process. FW Reg control | 0x83 | 0x0000 | [0]: Bypass CTLE train | None |
| Get bypass CTLE train | 0x83 | 0x0001 | None | [0]: Bypass CTLE train |
|  |  |  |  |  |

#### **Command Type = 0x84**

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| **Command Description** | **PHY\_REMOTE\_CTRL\_COMMAND\_TYPE\_LANE[7:0]** | **PHY\_REMOTE\_CTRL\_COMMAND\_CODE\_LANE[15:0]** | **PHY\_REMOTE\_CTRL\_VALUE\_LANE[31:0]** | **PHY\_LOCAL\_VALUE[31:0]** |
| Run RX impedance calibration    OPERATION: MCU-FW performs RX Impedance calibration. FW Reg control | 0x84 | 0x0000 | [0] lane\_sel (0:lane0, 1:lane1) \* NOTE: both lanes cannot be excuted for hardware limitation. | Rx Impedence calibration |
| Run TX impedance calibration    OPERATION: MCU-FW performs TX Impedance calibration. FW Reg control | 0x84 | 0x0001 | [0] lane\_sel (0:lane0, 1:lane1) \* NOTE: both lanes cannot be excuted for hardware limitation. | Tx Impedence calibration |
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1. Reference

| **Ref #** | **Document Name** | **Doc Number** |
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1. Revision History

| **Document No and Revision** | **Int Rev** | **Description** | **Date** |
| --- | --- | --- | --- |
| R1.0 |  | * First Revision | 2018/11/05 |
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