**32G 12FFC XDATA Memory Allocation**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Start address |  |  |  |  |  |
| E000 | lc\_pll\_PI0\_R0 | | | | LC PLL\_PI0 |
|  | : | | | |
|  | lc\_pll\_PI0\_R7 | | | |
|  | lc\_pll\_PI1\_R0 | | | | LC PLL\_PI1 |
|  | : | | | |
|  | lc\_pll\_PI1\_R7 | | | |
|  | ring\_pll\_PI0\_R0 | | | | RING PLL\_PI0 |
|  | : | | | |
|  | ring\_pll\_PI0\_R7 | | | |
|  | ring\_pll\_PI1\_R0 | | | | RING PLL\_PI1 |
|  | : | | | |
|  | ring\_pll\_PI1\_R7 | | | |
|  | ring\_pll\_PI0\_R0 | | | | RING PLL\_PI0 250M |
|  | : | | | |
|  | ring\_pll\_PI0\_R7 | | | |
|  | ring\_pll\_PI1\_R0 | | | | RING PLL\_PI1 250M |
|  | : | | | |
|  | ring\_pll\_PI1\_R7 | | | |
| e5c0 | phy\_mode\_cmn | | | | Common CAL |
|  | 0 | | | | null |
| e600 | xdat\_cmn | | | | Register Midas |
|  |  |  |  |  |  |
|  |  |  |  |  |  |
| 6000 | xdat\_lane | | | | Register Midas |
| 6100 | cds | | | | CDS\_LANE |
| 6300 | max\_gen | min\_gen | 0 | 0 | Header |
| 6304 | tx/rx | | | | g0 |
|  | tx/rx | | | | g1 |
|  | tx/rx | | | | g2 |
|  | tx/rx | | | | g3 |
|  | tx/rx | | | | g4 |
|  | tx/rx | | | | Reserved |
|  | tx/rx | | | | Reserved |
| 6534 | phy\_mode\_lane | | | | LANE CAL |
|  | 0 | | | | Null |
| 6600 |  | | | | firmware Internal |
| 67FC |