Question	Answer	Marks
3(a)	**1 mark** for each completed statement The **Program Counter** holds the address of the next instruction to be loaded. This address is sent to the **Memory Address Register**. The **Memory Data Register** holds the data fetched from this address. This data is sent to the **Current Instruction Register** and the Control Unit decodes the instruction's opcode. The **Program Counter** is incremented.	**5**

<table>
<tr><th>Question</th><th>Answer</th><th>Marks</th></tr>
<tr><td>4(a)</td><td>1 mark for each shaded section / bullet point

• Load 65 into ACC
• Load 100 into ACC, increment and store in 102
• Load 68 into ACC
• Load 101 into ACC, decrement and store in 102

<table>
<tr><th rowspan="2">Instruction address</th><th rowspan="2">ACC</th><th colspan="3">Memory address</th></tr>
<tr><th>100</th><th>101</th><th>102</th></tr>
<tr><td></td><td></td><td>68</td><td>65</td><td>100</td></tr>
<tr><td>70</td><td>65</td><td></td><td></td><td></td></tr>
<tr><td>71</td><td></td><td></td><td></td><td></td></tr>
<tr><td>72</td><td></td><td></td><td></td><td></td></tr>
<tr><td>73</td><td></td><td></td><td></td><td></td></tr>
<tr><td>74</td><td></td><td></td><td></td><td></td></tr>
<tr><td>76</td><td>100</td><td></td><td></td><td></td></tr>
<tr><td>77</td><td>101</td><td></td><td></td><td></td></tr>
<tr><td>78</td><td></td><td></td><td></td><td>101</td></tr>
<tr><td>79</td><td></td><td></td><td></td><td></td></tr>
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<tr><td>71</td><td></td><td></td><td></td><td></td></tr>
<tr><td>72</td><td></td><td></td><td></td><td></td></tr>
<tr><td>80</td><td>101</td><td></td><td></td><td></td></tr>
<tr><td>81</td><td>100</td><td></td><td></td><td></td></tr>
<tr><td>82</td><td></td><td></td><td></td><td>100</td></tr>
<tr><td>83</td><td></td><td></td><td></td><td></td></tr>
<tr><td>(70)</td><td></td><td></td><td></td><td></td></tr>
</table>
</td><td>4</td></tr>
<tr><td>4(b)(i)</td><td>102</td><td>1</td></tr>
<tr><td>4(b)(ii)</td><td>AND</td><td>1</td></tr>
</table>

Question	Answer	Marks
4(b)(iii)	**1 mark** for AND, **1 mark** for #15 AND #15	**2**

Question	Answer	Marks
5(a)	**1 mark** for each term correctly inserted The **control unit/bus** transmits the signals to coordinate events based on the pulses of the (**system) clock**. The **data bus** carries data to components, while the **address bus** carries the address where data is being written to or read from. The **arithmetic logic unit/ALU** performs mathematical operations and logical comparisons.	**5**
5(b)	**1 mark** per bullet point to **max 3** per factor. **max 4** overall. Number of cores: • Each core processes one instruction per clock pulse • More/multiple cores mean that **sequences of instructions** can be split between them • … and so more than one instruction is executed per clock pulse // more **sequences of instructions** can be run at the same time • **More** cores decreases the time taken to complete task Clock speed: • Each instruction is executed on a clock pulse // one F-E cycle is run on each clock pulse • ... so the clock speed dictates the number of instructions that can be run per second • The **faster** the clock speed the more instructions can be run per second	**4**

<table>
<tr><th>Question</th><th>Answer</th><th>Marks</th></tr>
<tr><td>6(a)</td><td>1 mark for identification of line and description of error
1 mark for the correct statement

<table>
<tr><th>Line number</th><th>Description of the error</th><th>Correct statement</th></tr>
<tr><td>2</td><td>Program Counter should be incremented, not decremented</td><td>PC ← [PC] + 1</td></tr>
<tr><td>3</td><td>It should be the contents of the address in the MAR</td><td>MDR ← [[MAR]]</td></tr>
</table>
</td><td>4</td></tr>
</table>

Question	Answer	Marks
6(a)(i)	**1 mark** per bullet point to **max 5** • The Program Counter (PC) holds the **address** of the next instruction … • …and the **contents** are incremented / changed to the next address each cycle • The Memory Address Register (MAR) holds the address to fetch the data (from the PC) • The Memory Data Register (MDR) holds the data at the address in MAR • The instruction is transferred to Current Instruction Register (CIR) for decoding and execution	**5**
6(a)(ii)	**1 mark** for detection • At the start/end of a FE cycle **1 mark** for handling to **max 4** • Priority is checked • If lower priority than current process continue with F-E cycle • If higher priority than current process … • … state of current process is / registers are stored on stack • Location / type of interrupt identified... • …appropriate ISR is called to handle the interrupt • When ISR finished, check for further interrupts (of high priority) / return to step 1 • Otherwise load data from stack and continue with process	**5**
6(b)	**1 mark** for factor **1 mark** for impact e.g. • Clock speed… • …higher clock speed means more FE cycles per second • Number of cores… • …means more instructions can be carried out simultaneously • Bus width … • …allows the transfer of more data each time // allows more memory locations to be directly accessed • Cache … • … the higher capacity the more frequently used instructions it can store for fast access	**2**
6(c)(i)	0000 0000	**1**
6(c)(ii)	0110 1101	**1**
6(c)(iii)	1101 0000	**1**

Question	Answer	Marks
3(d)	**1 mark** per bullet point to **max 3** e.g. • Zero • Carry • Overflow • Sign/negative • Compare results • Parity	**3**

Question	Answer	Marks
6(a)	**One mark** for each term in bold. There are **three** buses that transfer data between components in a computer system. The width of the **address bus** determines the number of directly accessible memory locations. The **control unit** sends signals on the **control bus** to direct the operation of system components. **Clock** pulses are used to synchronise the components on the motherboard.	**5**
6(b)	**One mark** per bullet point to **max 5** • The address in the program counter is the address of next item to be fetched • The address is copied into MAR ... • …using the address bus • The instruction from that address moved/copied from main memory to MDR ... • …using the data bus • The instruction is transferred from MDR to CIR • The processor's instruction set is used to decode the instruction// the instruction is decoded in the CIR • …into op code and operand • The processor executes the instruction // the processor processes the data as required • The address in PC is incremented ready for next loop	**5**

Question	Answer	Marks
6(a)(i)	**1 mark** for each correct answer **A**: The number 193 **B**: The data in memory location 193 **C**: The data in the memory location found by adding the contents of the IX to 193	**3**
6(a)(ii)	**1 mark** each correct answer • Indirect • Relative	**2**

Question	Answer	Marks
6(b)	**1 mark** for correctly naming register, **1 mark** for appropriate role • Program counter // PC • Stores the address of the next instruction to be fetched • Memory address register // MAR • Stores the address where data/instruction is to be read from or saved to • Memory data register // MDR • Stores data that is about to be written to memory // Stores data that has just been read from memory • Current instruction register // CIR • Stores the instruction that is currently being decoded/executed	**4**