3 A processor has one general purpose register, the Accumulator (ACC), and several special purpose registers.

(a) Complete the following description of the role of the registers in the fetch-execute cycle by writing the missing registers.

The ..... holds the address of the next instruction to be loaded. This address is sent to the ..... .

The ..... holds the data fetched from this address. This data is sent to the ..... and the Control Unit decodes the instruction's opcode.

The ..... is incremented.

[5]

4 The table shows part of the instruction set for a processor. The processor has one general purpose register, the Accumulator (ACC), and an Index Register (IX).

Instruction		Explanation
Opcode	**Operand**	
LDM	#n	Immediate addressing. Load the number n to ACC
LDD	<address>	Direct addressing. Load the contents of the location at the given address to ACC
STO	<address>	Store contents of ACC at the given address
ADD	<address>	Add the contents of the given address to the ACC
INC	<register>	Add 1 to the contents of the register (ACC or IX)
DEC	<register>	Subtract 1 from the contents of the register (ACC or IX)
CMP	<address>	Compare the contents of ACC with the contents of <address>
JPE	<address>	Following a compare instruction, jump to <address> if the compare was True
JPN	<address>	Following a compare instruction, jump to <address> if the compare was False
JMP	<address>	Jump to the given address
IN		Key in a character and store its ASCII value in ACC
OUT		Output to the screen the character whose ASCII value is stored in ACC
END		Return control to the operating system
# denotes a denary number, e.g. #123		

The current contents of the main memory and selected values from the ASCII character set are:

Address	Instruction
70	IN
71	CMP 100
72	JPE 80
73	CMP 101
74	JPE 76
75	JMP 80
76	LDD 102
77	INC ACC
78	STO 102
79	JMP 70
80	LDD 102
81	DEC ACC
82	STO 102
83	JMP 70
...	
100	68
101	65
102	100

ASCII code table (selected codes only)

ASCII code	Character
65	A
66	B
67	C
68	D

(a) Complete the trace table for the program currently in main memory when the following characters are input:

```
A D
```

Do not trace the program any further when the third input is required.

Instruction address	ACC	Memory address		
		100	101	102
		68	65	100

[4]

(b) Some bit manipulation instructions are shown in the table:

Instruction		Explanation
Opcode	**Operand**	
AND	#n	Bitwise AND operation of the contents of ACC with the operand
AND	<address>	Bitwise AND operation of the contents of ACC with the contents of <address>
XOR	#n	Bitwise XOR operation of the contents of ACC with the operand
XOR	<address>	Bitwise XOR operation of the contents of ACC with the contents of <address>
OR	#n	Bitwise OR operation of the contents of ACC with the operand
OR	<address>	Bitwise OR operation of the contents of ACC with the contents of <address>
<address> can be an absolute address or a symbolic address # denotes a denary number, e.g. #123		

The contents of the memory address 300 are shown:

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
300	0	1	1	0	0	1	1	0

(i) The contents of memory address 300 represent an unsigned binary integer.

Write the denary value of the unsigned binary integer in memory address 300.

..... [1]

(ii) An assembly language program needs to test if bit number 2 in memory address 300 is a 1.

Complete the assembly language instruction to perform this test.

..... #4

[1]

(iii) An assembly language program needs to set bit numbers 4, 5, 6 and 7 to 0, but keep bits 0 to 3 with their existing values.

Write the assembly language instruction to perform this action.

.....

..... [2]

5 Seth uses a computer for work.

(a) Complete the following descriptions of internal components of a computer by writing the missing terms.

The ..... transmits the signals to coordinate events based on the electronic pulses of the ..... .

The ..... carries data to the components, while the ..... carries the address where data needs to be written to or read from.

The ..... performs mathematical operations and logical comparisons.

[5]

(b) Describe the ways in which the following factors can affect the performance of his laptop computer.

Number of cores

.....

.....

.....

.....

Clock speed

.....

.....

.....

.....

[4]

6 **(a)** There are **two** errors in the following register transfer notation for the fetch-execute cycle.

```
1   MAR ←[PC]

2   PC ← [PC] - 1

3   MDR ← [MAR]

4   CIR ← [MDR]
```

Complete the following table by:

- identifying the line number of each error
- describing the error
- writing the correct statement.

Line number	Description of the error	Correct statement

[4]

6 **(a)** A computer system is designed using the basic Von Neumann model.

(i) Describe the role of the registers in the Fetch-Execute (F-E) cycle.

.....

.....

.....

.....

.....

.....

.....

.....

.....

..... [5]

(ii) Describe when interrupts are detected in the F-E cycle **and** how the interrupts are handled.

Detected .....

.....

Handled .....

.....

.....

.....

.....

.....

.....

.....

.....

.....

.....

[5]

(b) Identify **one** factor that can affect the performance of the computer system **and** state how it impacts the performance.

Factor .....

Impact .....

.....

.....

[2]

(c) The table shows part of the instruction set for a processor. The processor has one general purpose register, the Accumulator (ACC).

Instruction		Explanation
Opcode	**Operand**	
`AND`	`#n`	Bitwise AND operation of the contents of ACC with the operand
`XOR`	`#n`	Bitwise XOR operation of the contents of ACC with the operand
`OR`	`#n`	Bitwise OR operation of the contents of ACC with the operand
`LSL`	`#n`	Bits in ACC are shifted logically n places to the left. Zeros are introduced on the right hand end
`LSR`	`#n`	Bits in ACC are shifted logically n places to the right. Zeros are introduced on the left hand end
# denotes a denary number, e.g. #123		

(i) Complete the register to show the result **after** the instruction `AND #2` is executed.

Register before:	0	1	1	0	1	1	0	1
Register after:								

[1]

(ii) Complete the register to show the result **after** the instruction `OR #8` is executed.

Register before:	0	1	1	0	1	1	0	1
Register after:								

[1]

(iii) Complete the register to show the result **after** the operation `LSL #4` is executed.

Register before:	0	1	1	0	1	1	0	1
Register after:								

[1]

(d) The status register contains condition flags.

Identify **three** condition flags that can be set in the status register.

1 .....

2 .....

3 .....

[3]

6 **(a)** Complete the following sentences that describe parts of a processor in a Von Neumann model for a computer system.

There are ..... buses that transfer data between components in a computer system.

The width of the ..... determines the number of directly accessible memory locations.

The ..... sends signals on the ..... to direct the operation of system components.

..... pulses are used to synchronise the components on the motherboard.
[5]

(b) Describe the stages of the fetch-execute (F-E) cycle.

.....

.....

.....

.....

.....

.....

.....

.....

.....

..... [5]

6 A processor has one general purpose register, the Accumulator (ACC), and an Index Register (IX).

(a) The table gives **three** assembly language instructions for loading data into the ACC. It also identifies the addressing mode used for each instruction.

	Instruction	Addressing mode
A	`LDM #193`	Immediate
B	`LDD 193`	Direct
C	`LDX 193`	Indexed

(i) State the contents of the Accumulator after each of the instructions **A**, **B** and **C** are run.

A .....

.....

B .....

.....

C .....

.....

[3]

(ii) Name **two** other addressing modes.

1 .....

2 .....

[2]

(b) The ACC is a general purpose register. The IX is a special purpose register.

Identify **two** other special purpose registers used in the fetch-execute cycle **and** describe their role in the cycle.

Register 1 .....

Role .....

.....

.....

Register 2 .....

Role .....

.....

.....

[4]