

期末報告

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四位元之全加器設計

1. 原理:

真值表

A	B	C	D	Co1	S1	S0
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	1	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	0	1	0
0	1	1	1	0	1	1
1	0	0	0	0	0	1
1	0	0	1	0	1	0
1	0	1	0	0	1	0
1	0	1	1	0	1	1
1	1	0	0	0	1	0
1	1	0	1	0	1	1
1	1	1	0	0	1	1
1	1	1	1	1	0	0

卡諾圖化簡

CD \ AB	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	0	0	1	0
10	0	0	0	0

$$S1 = A'CD + A'BD + BCD' + AB'D + AB'C + ABC'$$

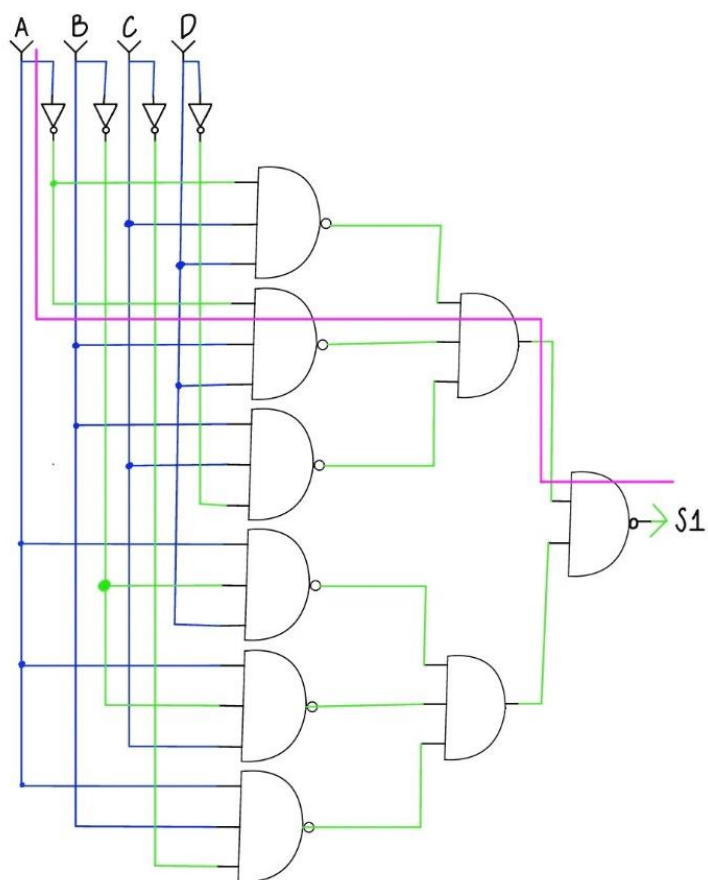
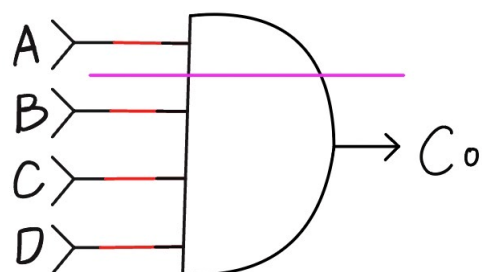
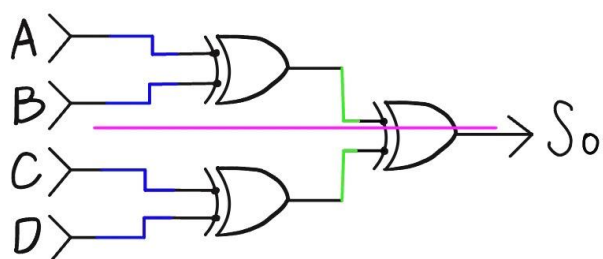
$$= (((A'CD)' (A'BD)' (BCD')') ((AB'D)' (AB'C)' (ABC')'))'$$

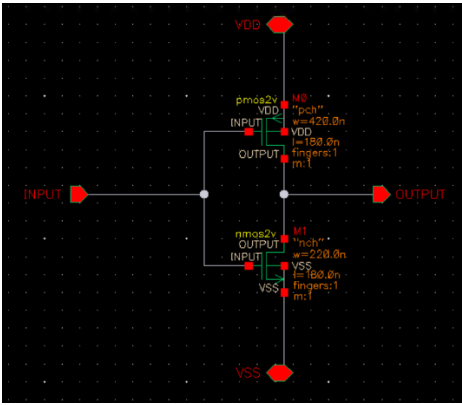
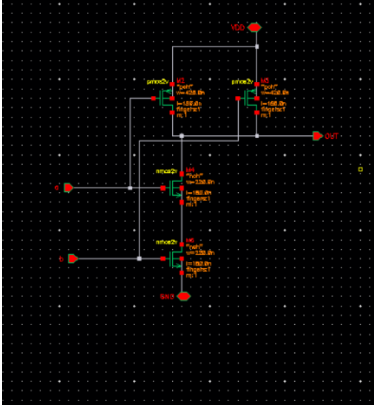
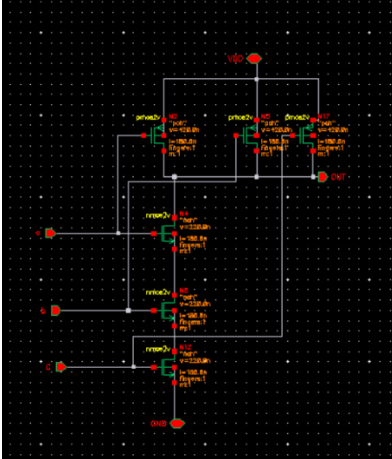
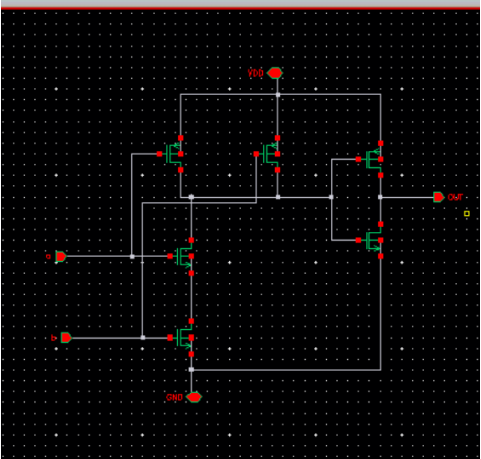
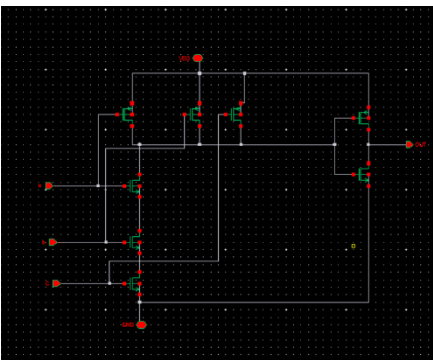
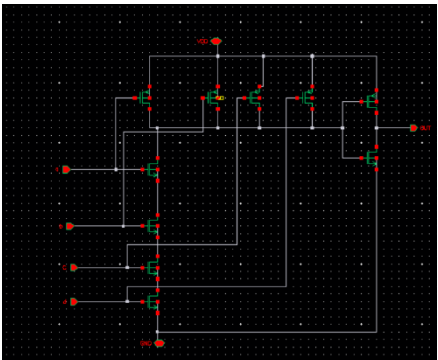
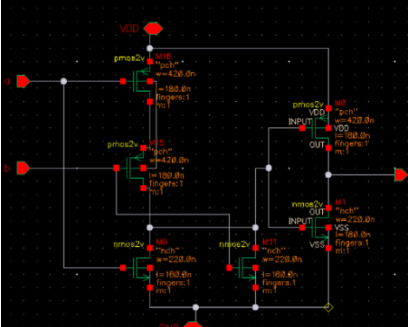
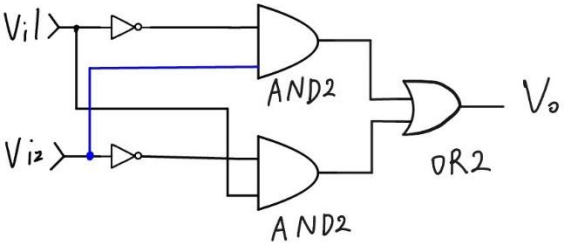
CD \ AB	00	01	11	10
00	0	0	1	0
01	0	1	1	1
11	1	1	0	1
10	0	1	1	1

$$S_0 = A \oplus B \oplus C \oplus D$$

AB \ CD	00	01	11	10
00	0	1	0	1
01	1	0	1	0
11	0	1	0	1
10	1	0	1	0

2. 邏輯閘電路方塊圖:



<p>INV</p>	<p>NAND2</p>
	
<p>NAND3</p>	<p>AND2</p>
	
<p>AND3</p>	<p>AND4</p>
	
<p>OR2</p>	<p>XOR</p>
	

3. 延遲分析:

Co=and4

S1=xor+xor

S0=inv*2 +and*2+or*2

Co 延遲時間 = 164.2ps

S1 延遲時間 = 263.7ps

S0 延遲時間 = 212.1ps

4. 模擬結果:

