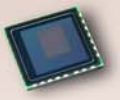
OmniVision



datasheet

PRELIMINARY SPECIFICATION

1/5" CMOS VGA (640 x 480) image sensor
with OmniPixel3-HS™ technology

OV7740

color CMOS VGA (640 x 480) image sensor with OmniPixel3-HS™ technology

datasheet (CSP3)
PRELIMINARY SPECIFICATION

version 1.51
may 2009

To learn more about OmniVision Technologies, visit www.ovt.com.
OmniVision Technologies is publicly traded on NASDAQ under the symbol OVTI.

applications

- PC multimedia

ordering information

- **OV07740-A32A** (color, lead-free)
  32-pin CSP3

features

- support for output formats: RAW RGB and YUV
- support for image sizes: VGA, and QVGA, CIF and any size smaller
- support for black sun cancellation
- support for internal and external frame synchronization
- standard SCCB serial interface
- digital video port (DVP) parallel output interface
- embedded one-time programmable (OTP) memory
- on-chip phase lock loop (PLL)
- embedded 1.5V regulator for core

key specifications

- **active array size:** 656 x 488
- **power supply:**
  core: 1.5VDC ± 5% (internal regulator)
  analog: 3.0 ~ 3.6V
  I/O: 1.7 ~ 3.47V
- **power requirements:**
  active: 48 mA (see **table 8-2** for test conditions))
  standby: 20 µA (see **table 8-2** for test conditions)
- **temperature range:**
  operating: -30°C to 70°C (see **table 8-1**)
  stable image: 0°C to 50°C (see **table 8-1**)
- **output formats:** 8-/10-bit RAW RGB data, 8-bit YUV
- **lens size:** 1/5"
- **lens chief ray angle:** 25°
- **input clock frequency:** 6 ~ 27 MHz
- **S/N ratio:** 38 dB
- **dynamic range:** 71 dB
- **maximum image transfer rate:**
  VGA (640x480): 60 fps for VGA
  QVGA (320x240): 120 fps for QVGA
- **sensitivity:** 6.0 V/(Lux • sec)
- **shutter:** rolling shutter
- **scan mode:** progressive
- **maximum exposure interval:** 502 x t_{ROW}
- **gamma correction:** programmable
- **pixel size:** 4.2 µm x 4.2 µm
- **well capacity:** 13 Ke^-
- **dark current:** 30 mV/sec @ 60°C
- **fixed pattern noise (FPN):** 1% $V_{PEAK-TO-PEAK}$
- **image area:** 2755.2 µm x 2049.6 µm
- **package dimensions:** 4185 µm x 4345 µm

table of contents

list of figures

list of tables

1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pin numbers for the OV7740 image sensor. The package information is shown in **section 9**.

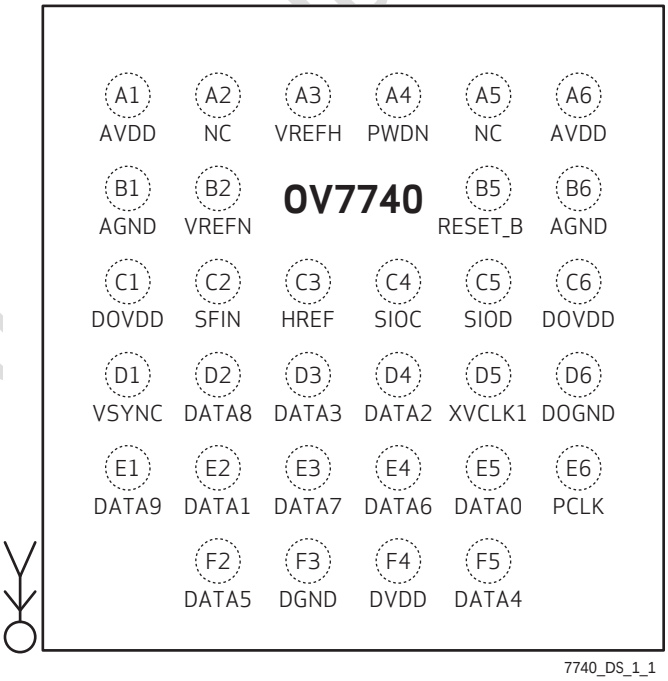
table 1-1 signal descriptions (sheet 1 of 2)

pin number	signal name	pin type	description	default I/O status
A1	AVDD	power	analog power	
A2	NC	–	no connect	
A3	VREFH	reference	reference voltage	
A4	PWDN	input	power down input with pull-down resistor (active high)	
A5	NC	–	no connect	
A6	AVDD	power	analog power	
B1	AGND	ground	analog ground	
B2	VREFN	reference	reference voltage	
B5	RESET_B	input	reset input with pull-up resistor (active low)	
B6	AGND	ground	analog ground	
C1	DOVDD	power	I/O power	
C2	SFIN	input	frame sync input	
C3	HREF	output	horizontal SYNC output	
C4	SIOC	input	SCCB clock	
C5	SIOD	I/O	SCCB data	
C6	DOVDD	power	I/O power	
D1	VSYNC	I/O	vertical SYNC output	output
D2	DATA8	I/O	DV port output[8]	output
D3	DATA3	I/O	DV port output[3]	output
D4	DATA2	I/O	DV port output[2] (LSB in 8-bit mode)	output
D5	XVCLK1	input	input clock	
D6	DOGND	ground	digital ground	
E1	DATA9	I/O	DV port output[9] (MSB)	output
E2	DATA1	I/O	DV port output[1]	output
E3	DATA7	I/O	DV port output[7]	output

table 1-1 signal descriptions (sheet 2 of 2)

pin number	signal name	pin type	description	default I/O status
E4	DATA6	I/O	DV port output[6]	output
E5	DATA0	I/O	DV port output[0] (LSB in 10-bit mode)	output
E6	PCLK	I/O	pixel clock output	output
F2	DATA5	I/O	DV port output[5]	output
F3	DGND	ground	digital ground	
F4	DVDD	power	digital core power (internal regulator)	
F5	DATA4	I/O	DV port output[4]	output

figure 1-1 pin diagram



top view

2 system level description

2.1 overview

The OV7740 (color) image sensor is a high performance VGA CMOS image sensor that provides the full functionality of a single-chip VGA camera using OmniPixel3-HS™ technology in a small footprint package. It provides full-frame, sub-sampled, windowed or scaled 8-bit/10-bit images in various formats via the control of the Serial Camera Control Bus (SCCB) interface.

The OV7740 has an image array capable of operating at up to 60 frames per second (fps) in VGA resolution with complete user control over image quality, formatting and output data transfer. All required image processing functions including exposure control, gamma, white balance, color saturation, hue control, defective pixel canceling, noise canceling, etc., are programmable through the SCCB interface. In addition, OmniVision image sensors use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, etc., to produce a clean, fully stable, color image.

The OV7740 also includes one-time programmable (OTP) memory.

The OV7740 supports a digital video parallel port.

2.2 architecture

The OV7740 sensor core generates stream pixel data at a constant frame rate, indicated by HREF and VSYNC. The maximum pixel rate is 60 frames/second, corresponding to a pixel clock rate of 48 MHz. **figure 2-1** shows the functional block diagram of the OV7740 image sensor.

The timing generator outputs signals to access the rows of the image array, precharging and sampling the rows of array in series. In the time between precharging and sampling a row, the charge in the pixels decreases with the time exposed to the incident light, as known as exposure time.

The exposure time is controlled by adjusting the time interval between precharging and sampling. After the data of the pixels in the row has been sampled, it is processed through a analog circuitry to correct the offset and multiply the data with corresponding gain. Following analog processing is the ADC which outputs a 10-bit data for each pixel in the array.

figure 2-1 OV7740 block diagram

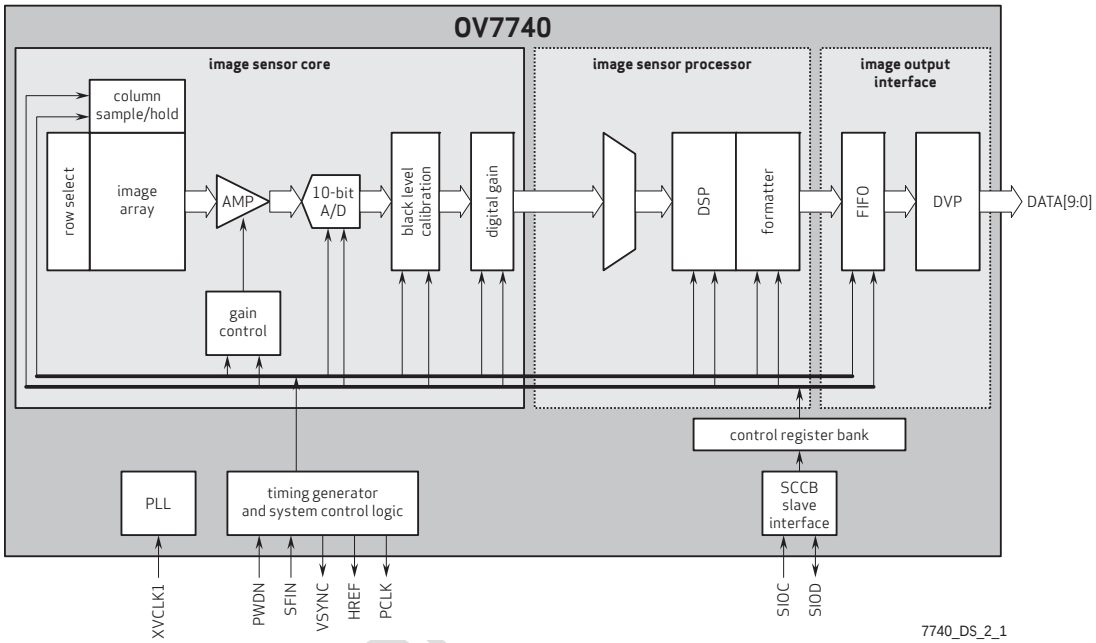
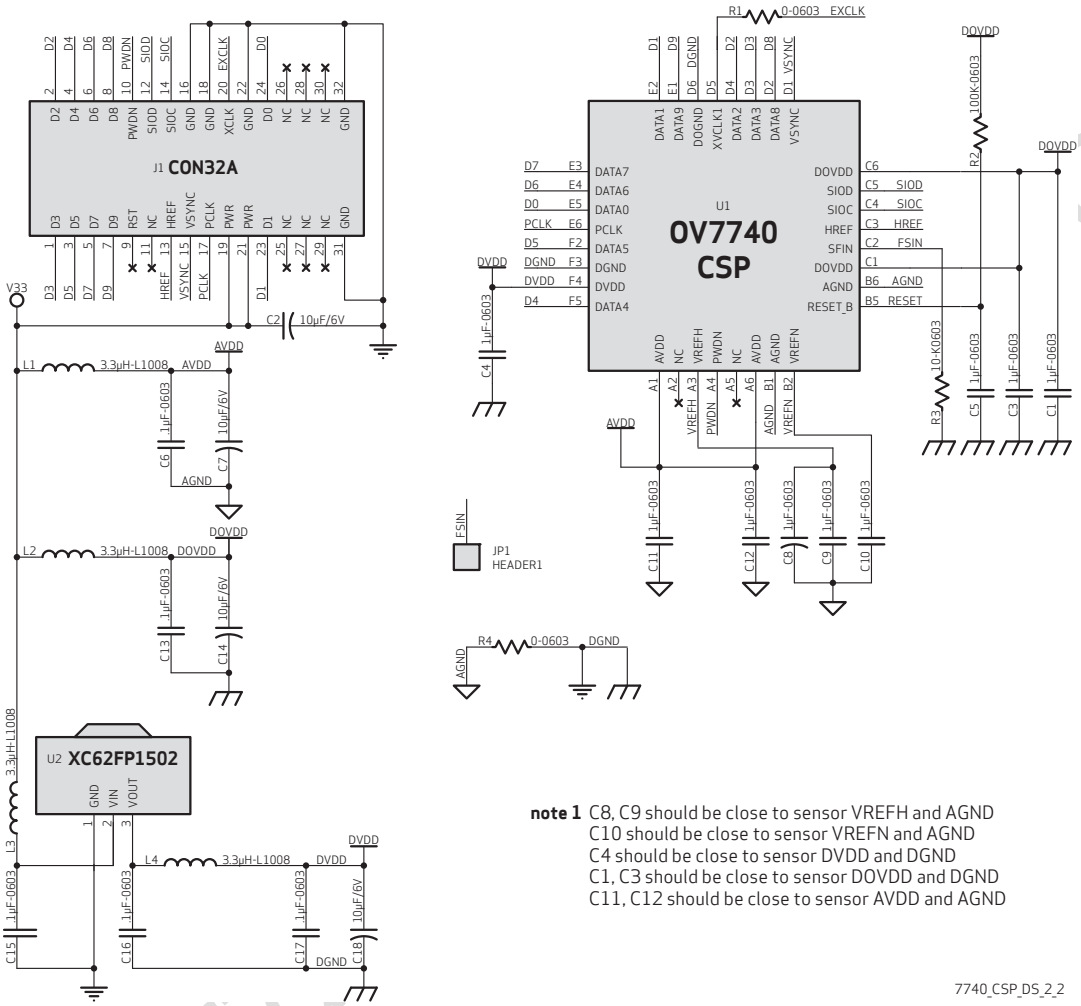


figure 2-2 reference design schematic



note 1 C8, C9 should be close to sensor VREFH and AGND
C10 should be close to sensor VREFN and AGND
C4 should be close to sensor DVDD and DGND
C1, C3 should be close to sensor DOVDD and DGND
C11, C12 should be close to sensor AVDD and AGND

7740_CSP_DS_2_2

2.3 I/O control

The OV7740 I/O pin direction and driving capability can be easily adjusted. **table 2-1** lists the driving capability and direction control registers of the I/O pins.

table 2-1 driving capability and direction control for I/O pads

function	register	description
output drive capability control	0x0E	Bit[1:0]: output driving capability 00: 1x 01: 2x 10: 3x 11: 4x
DATA[9:0] IO control	0x54	Bit[7:5]: input/output selection of the DATA[9:0] pins, 0x54[7] selects DATA[9:2], 0x54[6:5] selects DATA[1:0] 0: input 1: output
HREF IO control	0x54	Bit[4]: input/output selection of the HREF pin 0: input 1: output
VSYNC IO control	0x54	Bit[3]: input/output selection of the VSYNC pin 0: input 1: output
PCLK IO control	0x54	Bit[2]: input/output selection of the PCLK pin 0: input 1: output

2.4 format and frame rate

The OV7740 supports the following output formats: YUV422, RAW RGB and ITU656.

table 2-2 format and frame rate

format	resolution	frame rate	scaling method	pixel clock (YUV/RAW)
VGA	640x480	60 fps	full	48/24 MHz
CIF	352x288	60 fps	scaling down from VGA	48/24 MHz
QVGA	320x240	120 fps	sub sampling from VGA	48/24 MHz
QCIF	176x144	120 fps	scaling down from QVGA	48/24 MHz

2.5 SCCB interface

The Serial Camera Control Bus (SCCB) interface controls the image sensor operation. Refer to the OmniVision Technologies Serial Camera Control Bus (SCCB) Specification for detailed usage of the serial control port.

2.6 group register write

Control values of multiple registers can be written at the same time by using the Group Register Write function. The procedure is as follows:

1. Set the group write enable bit (register 0x54[0] = 1)
2. Write register values (up to 16 registers)
3. Write group write latch register 0xFF = 0xFF
4. The group of registers are updated at the same time.

To disable this function:

1. Clear the group write enable bit (register 0x54[0] = 0)
2. Write group write latch register 0xFF = 0xFF

2.7 power up sequence

Powering up the OV7740 sensor does not require a special power supply sequence. The sensor includes an on-chip initial power-up reset feature. It will reset the whole chip during power up.

2.8 reset

The OV7740 sensor includes an RESET_B pin that forces a complete hardware reset when it is pulled low (GND). The OV7740 clears all registers and resets them to their default values when a hardware reset occurs. A reset can also be initiated through the SCCB interface.

2.9 standby and sleep

Two suspend modes are available for the OV7740:

- hardware standby
- SCCB software sleep

To initiate hardware standby mode, the PWDN pin must be tied to high. When this occurs, the OV7740 internal device clock is halted and all internal counters are reset and registers are maintained.

Executing a software power-down through the SCCB interface suspends internal circuit activity but does not halt the device clock. All register content is maintained.

3 block level description

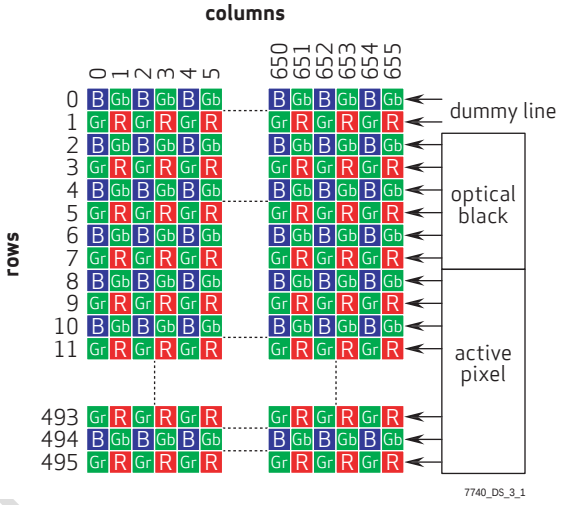
3.1 pixel array structure

The OV7740 sensor has an image array of 656 columns by 496 rows (325,376 pixels). **figure 3-1** shows a cross-section of the image sensor array.

The color filters are arranged in a Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 325,376 pixels, 320,128 (656x488) are active pixels and can be output. The other pixels are used for black level calibration and interpolation.

The sensor array design is based on a field integration read-out system with line-by-line transfer and an electronic shutter with a synchronous pixel read-out scheme.

figure 3-1 sensor array region color filter layout



4 image sensor core digital functions

4.1 mirror and flip

The OV7740 provides Mirror and Flip read-out modes, which respectively reverse the sensor data read-out order horizontally and vertically (see **figure 4-1**). In mirror mode, since the Bayer order changes from BGBG... to GBGB..., the HREF starting point needs to be adjusted, then the ISP block can do color interpolation correctly. In flip mode, the read-out sequence will be adjusted automatically.

figure 4-1 mirror and flip samples

table 4-1 mirror and flip function control

function	register	description
mirror[a]	0x0C	Bit[6]: mirror enable 0: disable mirror 1: enable mirror
flip	0x0C	Bit[7]: flip enable 0: disable flip 1: enable flip

a. when using the mirror function, the start point of HREF, {AHSTART[7:0] (0x17), REG16[1:0] (0x16)}, must be adjusted

4.2 AEC/AGC algorithms

4.2.1 overview

The Auto Exposure Control (AEC) and Auto Gain Control (AGC) allows the image sensor to adjust the image brightness to a desired range by setting the proper exposure time and gain applied to the image. Besides automatic control, exposure time and gain can be set manually from external control. The related registers are listed in **table 4-2**.

table 4-2 AEC/AGC algorithms

function	register	description
AEC enable	0x13	Bit[0]: AEC enable 0: manual 1: auto
AEC (exposure time)	0x10 0x0F	0x10 = AEC[7:0] 0x0F = AEC[15:8]
LAEC (less than 1 row exposure time)	0x30 0x1F	0x30 = LAEC[15:8] 0x1F = LAEC[7:0]
AGC (gain)	0x15[1:0] 0x00[7:0]	AGC[9:8]: digital gain AGC[7:0] analog gain
AGC enable	0x13	Bit[2]: AGC enable 0: manual 1: auto
manual LAEC enable	0x14	Bit[0]: manual LAEC select 0: auto LAEC 1: manual LAEC

4.2.2 average-based algorithm

The average-based AEC controls image luminance using registers **WPT** (0x24) and **BPT** (0x25). In average-based mode, the value of register **WPT** (0x24) indicates the high threshold value and the value of register **BPT** (0x25) indicates the low threshold value. When the target image luminance average value **YAVG** (0x2F) is within the range specified by registers **WPT** (0x24) and **BPT** (0x25), the AEC keeps the image exposure. When register **YAVG** (0x2F) is greater than the value in register **WPT** (0x24), the AEC will decrease the image exposure. When register **YAVG** (0x2F) is less than the value in register **BPT** (0x25), the AEC will increase the image exposure. Accordingly, the value in register **WPT** (0x24) should be greater than the value in register **BPT** (0x25). The gap between the values of registers **WPT** (0x24) and **BPT** (0x25) controls the image stability.

The AEC function supports both normal and fast speed selections in order to bring the image exposure into the range set by the values in registers **WPT** (0x24) and **BPT** (0x25). AEC set to normal mode will allow for single-step increment or decrement in the image exposure to maintain the specified range. A value of "0" in register REG13[7] (0x13) will result in normal speed operation and a "1" will result in fast speed operation.

Register **VPT** (0x26) controls the fast AEC range. If the target image **YAVG** (0x2F) is greater than **VPT**[7:4] × 16, AEC will decrease by 2. If register **YAVG** (0x2F) is less than **VPT**[3:0] × 16, AEC will increase by 2.

As shown in **figure 4-2**, the AEC/AGC convergence uses two regions, the inner stable operating region and the outer control zone, which defines the convergence step size as follows:

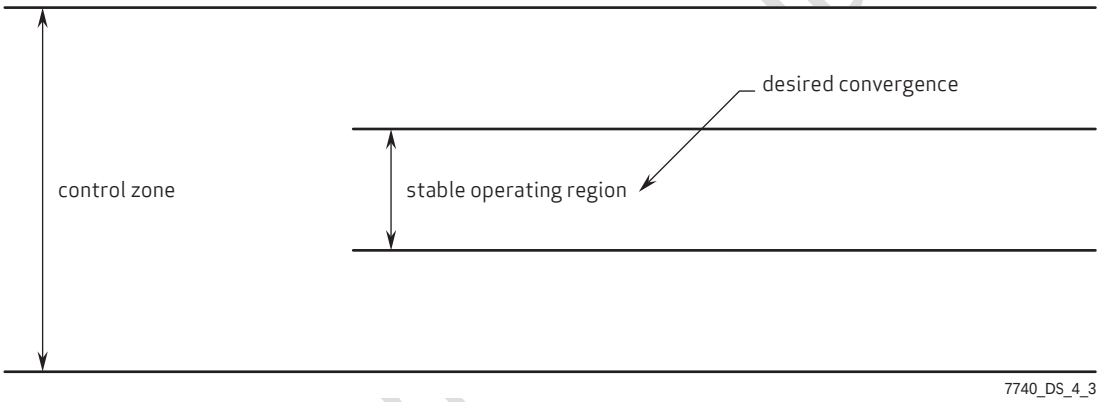
4.2.2.1 outside control zone
step size: AEC[15:0] when increase, AEC[15:0]/2 when decrease
t_{STEP}: t_{ROW} × AEC[15:0] when increase, t_{ROW} × AEC[15:0]/2 when decrease

4.2.2.2 inside control zone
step size: (AEC[15:0]) ÷ 16)

t_{STEP}: t_{ROW} × (AEC[15:0] ÷ 16)

Once the current value is inside the stable operating region, the AEC/AGC value has converged.

figure 4-2 desired convergence



control zone upper limit: {**VPT**[7:4] (0x26[7:4]), 4'b0000}

control zone lower limit: {**VPT**[3:0] (0x26[3:0]), 4'b0000}

stable operating region upper limit: WPT[7:0] (0x24)

stable operating region lower limit: BPT[7:0] (0x25)

For the average-based AEC/AGC algorithm, the measured window is horizontally and vertically adjustable and divided into sixteen (4x4) zones (see **figure 4-3**). Each zone (or block) is 1/16th of the image and has a 2-bit weight in calculating the average luminance (YAVG). The 2-bit weight can be 0x, 1x, 2x, or 4x. The final YAVG is the weighted average of the sixteen zones. For more details on adjusting horizontal and vertical windows and weight for each window, refer to **section 4.2.2.3,** average luminance (YAVG).

4.2.2.3 average luminance (YAVG)

Auto exposure time calculation is based on a frame brightness average value. By properly setting AHS,AVS, AHW, and AVH as shown in **figure 4-3**, a 4x4 grid average window is defined. The average value is the weighted average of the 16 sections. **table 4-3** lists the corresponding registers.

There are two window modes: auto window mode and manual window mode. In auto window mode, the AHS, AVS, AHW and AVH are defined by sizes of output image. In the manual window mode, the window parameters are defined by registers. **table 4-3** lists the corresponding registers. In order to use these register parameters, the yavg_win_man must be set to 1. Auto mode only supports non-scaling and non-subsampling image.

figure 4-3 average-based window definition

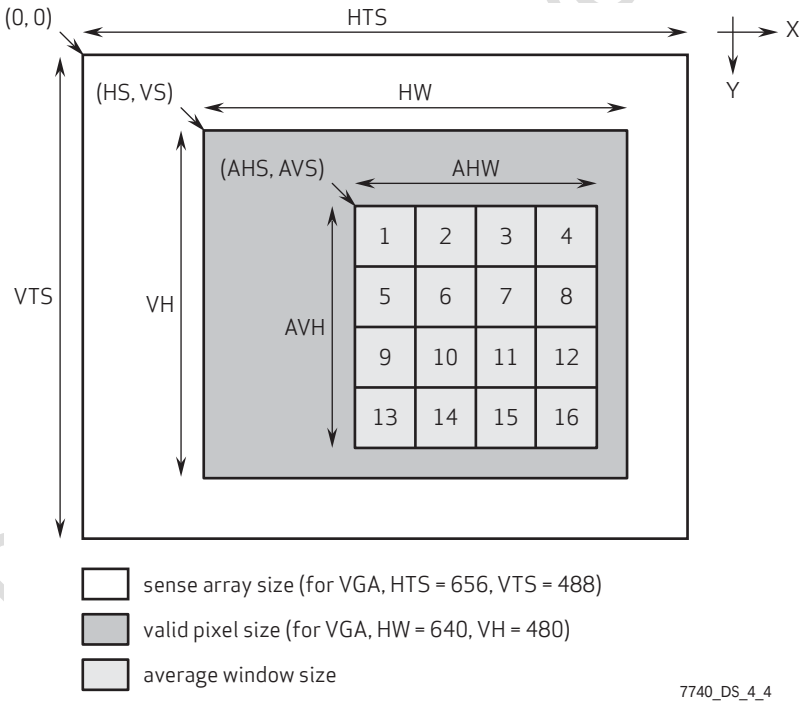


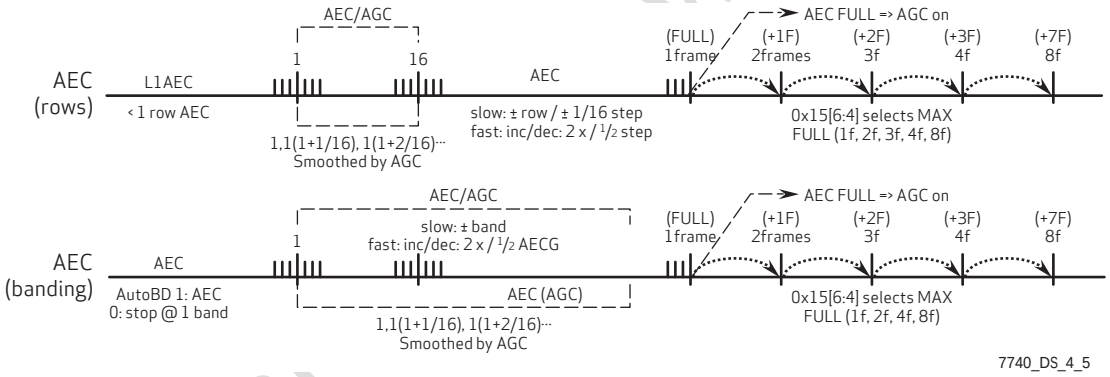
table 4-3 YAVG window registers

function	register	description
AHS (horizontal starting pixel)	{0xE9[1:0] and 0x38[3:0]=4'h4, 0xE9 and 0x38[3:0]=4'h2}	0xE9[1:0] and 0x38[3:0]=4'h4: yavg_winofh[9:8] 0xE9 and 0x38[3:0]=4'h2: yavg_winofh[7:0] Horizontal offset of YAVG window
AVS (vertical starting pixel)	{0xE9[4] and 0x38[3:0]=4'h4, 0xE9 &0x38[3:0]=4'h3}	0xE9[4] and 0x38[3:0]=4'h4: yavg_winofv[8] 0xE9 and 0x38[3:0]=4'h3: yavg_winofv[7:0] Vertical offset of YAVG window
AHW (average section width)	0xE9 sub-address 0x38[3:0]=4'h5	horizontal size of cropping window. It will be multiplied by 8 to be real size.
AVH (average section height)	0xE9 sub-address 0x38[3:0]=4'h6	vertical size of cropping window. It will be multiplied by 4 to be real size.
average section weighting	0x56~0x59	0x56[1:0]: section 1 weight 0x56[3:2]: section 2 weight 0x56[5:4]: section 3 weight 0x56[7:6]: section 4 weight 0x57[1:0]: section 5 weight 0x57[3:2]: section 6 weight 0x57[5:4]: section 7 weight 0x57[7:6]: section 8 weight 0x58[1:0]: section 9 weight 0x58[3:2]: section 10 weight 0x58[5:4]: section 11 weight 0x58[7:6]: section 12 weight 0x59[1:0]: section 13 weight 0x59[3:2]: section 14 weight 0x59[5:4]: section 15 weight 0x59[7:6]: section 16 weight

4.3 AEC/AGC steps

figure 4-4 shows how the AEC and AGC work together to obtain adequate exposure/gain based on the current environment's illumination. The upper one illustrates the non-banding operation which time unit is based on Tline. The lower one shows exposure in banding. The x-axis represents the length of exposure in time scale. In normal light circumstances, the length of exposure will fall into a range from 1 Tline to 1 Tframe. In extremely bright or dark circumstances, exposure time less than 1 Tline/Tband or greater than 1 Tframe may be required accordingly. In order to achieve the best signal-to-noise ratio (SNR), extending the exposure time is always preferred, rather than raising the analog gain, when the current illumination is getting darker. Vice versa, under bright conditions, the action to decrease the gain is always taken prior to shortening the exposure time.

figure 4-4 darker illumination situation / brighter illumination situation



4.3.1 auto exposure control (AEC)

The function of the AEC is to calculate integration time of the next frame and send the information to the timing control block. Based on the statistics of previous frames, the AEC is able to determine whether the integration time should increase, decrease, fast increase, fast decrease, or remain the same.

In extremely bright situations, the LAEC activates, allowing integration time to be less than one row. In extremely dark situations, the VAEC activates, allowing integration time to be larger than one frame.

To avoid image flickering under a periodic light source, the integration time step can be adjusted as an integer multiple of the period of the light source. This new AEC step system is called banding, suggesting that the steps are not continuous but fall within bands.

4.3.1.1 sub-row AEC (LAEC)

If the integration time is only one row but the image is too bright, AEC will enter LAEC mode. Within LAEC, the integration time can be further decreased to a minimum of 1/16 row or so. LAEC can be enabled/disabled by register bit 0x13[3].

4.3.1.2 manual LAEC

LAEC can be in manual mode by setting MLAEC (0x14[0]) to 1. MLAEC exposure is controlled by LAEC[15:0] ({0x30, 0x1F}) as follows:

MLAEC exposure = (CSEND - LAEC) × Tp

where CSEND is register {0x2A, 0x29} and Tp is the pixel period

LAEC should be larger than 0xE0 and less than (CSEND - 0x30)

4.3.1.3 banding mode ON with AEC

When banding mode is ON, AEC step, which is also called 'band', increments by an integer multiple of the period of light intensity. This design is meant to reject image flickering when light source is not steady but periodical.

For a given operating frequency, band step can be expressed in terms of row timing.

Band Step = 'period of light intensity' × 'frame rate' × 'rows per frame'.

The band steps for 50Hz and 60Hz light sources can be set in registers 0x50~0x52.

When auto banding is ON, if the next integration time is less than the minimum band step, banding will automatically turn OFF. It will turn ON again when the next integration time becomes larger than the minimum band. If auto banding is disabled, the minimum integration time is one minimal band. Auto banding can be set in register 0x13[5].

4.3.1.4 banding mode OFF with AEC

When Banding is OFF, integration time increases/decreases by 1/16 of the previous step in slow mode or becomes twice/half of the previous step in fast mode.

4.3.1.5 VAEC (night mode)

In extremely dark situations, the integration time must be longer than one frame.

The OV7740 supports long integration time such as 1 frame, 2 frames, 3 frames and 7 frames. This is achieved by slowing down original frame rate and waiting for exposure. VAEC ceiling can be set in register 0x15[6:4]. VAEC can be disabled by setting register 0x15[7] to 0.

table 4-4 AEC and banding filter registers (sheet 1 of 2)

function	register	description
LAEC enable/disable	**0x13**	Bit[3]: LAEC enable 0: disable 1: enable
banding enable/disable	**0x13**	Bit[5]: banding enable 0: disable 1: enable
VAEC enable/disable (add frame)	**0x15**	Bit[7]: VAEC enable 0: disable 1: enable

table 4-4 AEC and banding filter registers (sheet 2 of 2)

function	register	description
auto banding	0x13	Bit[4]: banding option 0: minimum exposure is limited to 1/120 or 1/100 second when banding filter is enabled 1: minimum exposure is allowed to be less than 1/120 or 1/100 second when banding filter is enabled
VAEC ceiling (max integration time)	0x15	Bit[6:4]: VAEC ceiling 001: 1 frame 010: 2 frames 011: 3 frames 1xx: 7 frames
banding step	0x50~0x52	0x52[7:6]=BD60st[9:8]; 0x51[7:0] = BD60st[7:0] 0x52[5:4]=BD50st[9:8]; 0x50[7:0] = BD50st[7:0]
maximum banding step	{0x20, 0x21}	{0x20[7], 0x21[7:4]}: for 50 Hz {0x20[6], 0x21[3:0]}: for 60 Hz

4.3.2 auto gain control (AGC)

Unlike prolonging integration time, increasing gain will amplify both signal and noise or between two gaps of banding exposure time. Thus, AGC usually starts after AEC is full. However, in same cases where adjacent AEC step changes are too large (>1/16), AGC step should be inserted in between; otherwise, the integration time will keep switching from two adjacent steps and the image flickers.

4.3.2.1 integration time between 1~16 rows

When integration time is less than 16 rows, the changes between adjacent AEC steps are larger than 1/16, which may possibly make the image oscillate between two AEC levels; thus, some AGC steps are added in between. For example, from AEC = 2 rows to AEC = 3 rows, there are 7 more AGC steps (1+ x/16, x=1~7) inserted, which ensures every step change is less than 1/16.

4.3.2.2 gain insertion between AEC banding steps

In Banding ON mode, the minimal integration time change is the period of light intensity (10ms for 50Hz, 8.33ms for 60Hz). For the first 16 band steps, since the change between adjacent steps is larger than 1/16, AGC steps are inserted to ensure image stability.

4.3.2.3 gain insertion between VAEC steps

Between VAEC steps (e.g., integration time = 1 frame and 2 frames), AGC steps are inserted to ensure no adjacent step change is larger than 1/16 (6.25%).

4.4 black level calibration (BLC)

The pixel array contains six optically shielded (black) rows. These rows are used to provide the data for offset cancellation algorithms (black level calibration).

Digital image processing starts with black level subtraction. The BLC algorithm estimates the offset of the black level from the data provided by black rows. These offsets of different color channels will be subtracted from values of the color pixels. If the subtraction produces a negative result for a particular pixel, the value of this pixel is set to "0." By default, BLC will be triggered when gain is changing.

table 4-5 BLC control functions

function	register	description
target	0x67	Bit[5:0]: target black level value
BLC_B, BLC_R	0x0E	Bit[6:5]: BLC line selection 00: use all 4 channel offsets 01: use R/Gr channel offset for all channels 10: use B/Gb channel offset for all channels 11: use all 4 channel offsets
BLC always ON	0x64[5]	Bit[5]: BLC trigger 0: BLC offsets will be adjusted when gain changes 1: BLC offsets be adjusted every frame
MBLC	0x69[3]	Bit[3]: manual BLC trigger Toggling from 0 to 1 triggers BLC manually for 64 frames
Gr offset	0x6E[7:6], 0x6A[7:0]	BLC offset for Gr channel
Gb offset	0x6E[5:4], 0x6B[7:0]	BLC offset for Gb channel
R offset	0x6E[3:2], 0x6C[7:0]	BLC offset for R channel
B offset	0x6E[1:0], 0x6D[7:0]	BLC offset for B channel

4.5 digital gain

After black level subtraction, multiplication may apply to all pixel values based on an optional digital gain. By default, the sensor will use analog gain up to its maximum before applying digital gain to the pixels.

table 4-6 digital gain control functions

function	register	description
DGAIN	0x15	Bit[1:0]: digital gain 00: 1x digital gain 01: 2x digital gain 10: 2x digital gain 11: 4x digital gain

4.6 auto color saturation adjust

The main function of the auto color saturation adjust is to adjust the U/V channel value according to sensor gain. It supports both manual and auto modes.

By setting gth2 {0x5C[7:5], 0x5B[7:6]} to 0, color saturation adjust is in manual mode and the UV adjustment is controlled only by register 0x5C[4:0] for all gains. Otherwise, it is in auto mode and the UV adjust value is controlled by the curve shown in **figure 4-5**.

figure 4-5 UV auto adjust curve

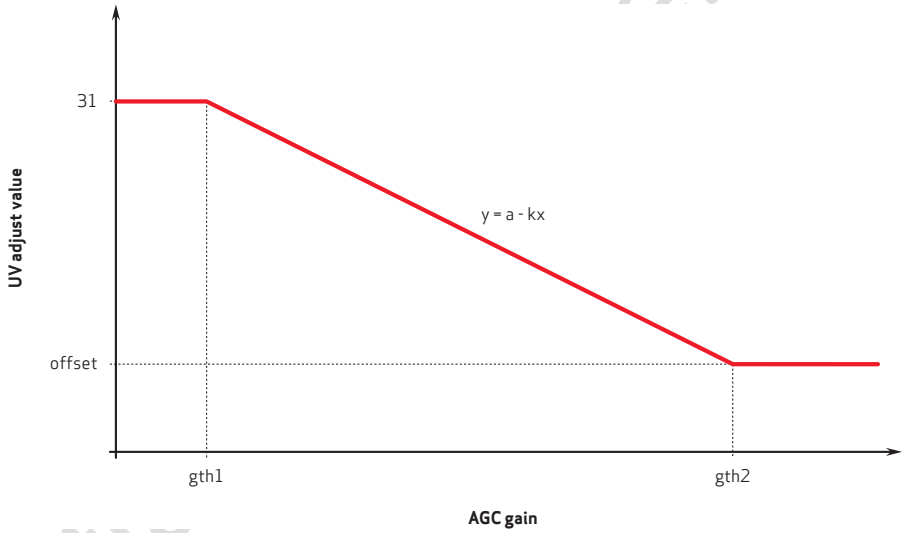


table 4-7 auto color saturation adjust

function	register	description
slope, k	0x5A	slope of UV auto adjust curve, k = {0x5A}/16
intercept, a	0x5B[5:0]	intercept of the UV auto adjust curve (must be set to 0x1F)
gth1	0x5D[7:4]	threshold 1 of UV auto adjust curve
gth2	{0x5C[7:5], 0x5B[7:6]}	threshold 2 of UV auto adjust curve
offset	0x5C[4:0]	auto mode: UV offset of UV auto adjust curve manual mode: manual UV adjust curve

4.7 one-time programmable (OTP) memory

The OV7740 has a one-time programmable (OTP) memory to store chip identification and manufacturing information. This OTP memory is organized as 128-bit by 1 one-time programmable electrical fuse with random access interface. The main function is to store chip identification and manufacturing information.

The OTP has three operation modes: program (PGM), READ, and inactive. Normally, it is in inactive mode. By setting 0xEF to 0xAA, it enters program mode, which will sequentially burn data into the OTP macro. By setting 0xFE to 0x55, the OTP enters read mode, which will load the OTP data into registers. **table 4-8** summarizes the corresponding registers.

table 4-8 OTP registers

function	register	description
OTP program data	0xF0~0xFF	data to be programmed/read into/from OTP memory
OTP program/read enable	0xEF	0x55: read OTP memory 0xAA: program OTP memory

5 image sensor processor digital functions

5.1 ISP general controls

The ISP module provides lens correction, gamma, denoise, sharpness, and other functions. These functions are enabled by registers 0x80 ~ 0x82.

table 5-1 ISP general control registers

address	register name	default value	R/W	description
0x80	ISP CTRL00	0x7F	RW	ISP CONTROL 00 (0: disable; 1: enable) Bit[7]: Not used Bit[6]: Black pixel correction enable Bit[5]: White pixel correction enable Bit[4]: AWB enable Bit[3]: Gamma enable Bit[2]: AWB gain enable Bit[1]: LENC enable Bit[0]: ISP enable
0x81	ISP CTRL01	0x3F	RW	ISP CONTROL 01 (0: disable; 1: enable) Bit[7:6]: Not used Bit[5]: SDE enable Bit[4]: UV adjust enable Bit[3]: YUV422 enable Bit[2]: UV average enable Bit[1]: CMX enable Bit[0]: CIP enable
0x82	ISP CTRL02	0x32	RW	ISP CONTROL 02 (0: disable; 1: enable) Bit[7:6]: Not used Bit[5]: Y average enable Bit[4]: FIFO enable Bit[3]: Vertical scaler enable Bit[2]: Horizontal scaler enable Bit[1]: Window cropping enable Bit[0]: Smooth scale enable

5.2 test pattern

For testing purposes, the OV7740 offers one test pattern type - color bar. There are four color bar modes (see **figure 5-1**). The color bar modes can be set with the register 0x84[5:4] (base address: 0x38[3:0] = 4'h8). In each mode, the color bar can be moved from top to bottom if the moving bar function is enabled by setting signal (0x84[4]: base address: 0x38[3:0] = 4'h7) is 1. The moving step can be configured by setting the register 0x84[3:0] (base address: 0x38[3:0] = 4'h8) (see **table 5-2**).

figure 5-1 test pattern

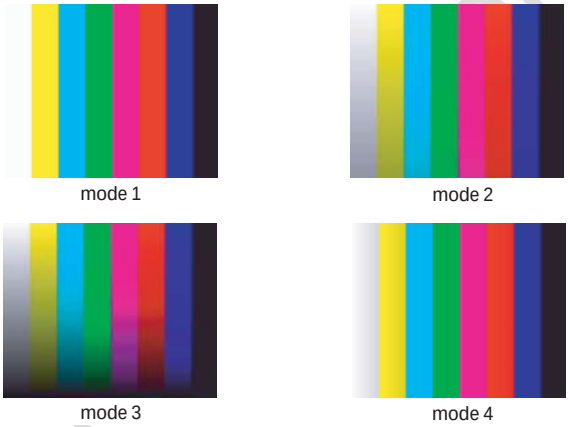


table 5-2 test pattern selection control

address	register name	default value	R/W	description
0x84 0x38[3:0] = 4'h7	PRE CTRL00	0x00	RW	Bit[4]: Moving bar enable 0: Color bar is a still image 1: Color bar is a moving image Bit[1]: Bar enable 0: Output data are normal data 1: Output data are color bar data
0x84 0x38[3:0] = 4'h8	PRE CTRL01	0x00	RW	Bit[5:4]: Bar style Output color bar style Bit[3:0]: Bar step Output color bar step

5.3 lens correction (LENC)

The main purpose of the Lens Correction (LENC) function is to compensate for lens imperfection. According to the radius of each pixel to the lens, the module calculates a gain for the pixel, correcting each pixel with its gain calculated to compensate for the light distribution due to lens curvature.

table 5-3 LENC registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x80	ISP CTRL00	1'b1	RW	Bit[1]: LENC enable 0: Disable LENC 1: Enable LENC
0x84 sub address: 0x38[3:0]=4'h1	BIAS CTRL	1'b1 1'b0	RW	Bit[4]: Lens correction bias enable 0: LENC bias is 0 1: LENC bias is the LENC offset Bit[0]: Manual lens correction offset enable 0: LENC offset is the black level 1: LENC offset is manual offset (refer to **LENC OFF MAN**)
0x84 sub address: 0x38[3:0]=4'h2	LENC OFF MAN	0x00	RW	Bit[7:0]: Manual offset for LENC
0x89	LENC CTRL	0x30	RW	Bit[5]: Lens correction bias handling 0: LENC bias will be not added back to LENC corrected data. 1: LENC bias will be added back to LENC corrected data. Bit[4]: Rounding enable 0: Disable data rounding 1: Enable data rounding Bit[3:2]: Vertical skip 00: Does not skip a pixel 01: Skips 1 pixel every 2 pixels 10: Skips 3 pixels every 4 pixels 11: Skips 7 pixels every 8 pixels Bit[1:0]: Horizontal skip 00: Does not skip a line 01: Skips 1 line every 2 lines 10: Skips 3 lines every 4 lines 11: Skips 7 lines every 8 lines
0x8A	LENC RED X0	0x40	RW	Bit[7:0]: red_x0[7:0] red_x0 is the horizontal coordinate of the lens center with respect to the left_top corner of the image. Range from 0 to 639. See **LENC RED XY0**[1:0] (**0x8C**)

table 5-3 LENC registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x8B	LENC RED Y0	0xF0	RW	Bit[7:0]: red_y0[7:0] red_y0 is the vertical coordinate of the lens center with respect to the left_top corner of the image. Range from 0 to 479. See **LENC RED XY0**[4] (**0x8C**)
0x8C	LENC RED XY0	0x01	RW	Bit[4]: red_y0[8] See **LENC RED Y0**[7:0] (**0x8B**) Bit[1:0]: red_x0[9:8] See **LENC RED X0**[7:0] (**0x8A**)
0x8D	LENC RED A1	0x22	RW	Bit[6:0]: red_a1 The parameter construct the first group of factors used in LENC correction in red color channels.
0x8E	LENC RED B1	0xC2	RW	Bit[7:0]: red_b1 The parameter construct the second group of factors used in LENC correction in red color channels.
0x8F	LENC RED AB2	0x87	RW	Bit[7:4]: red_b2 The parameter construct the second group of factors used in LENC correction in red color channels. Bit[3:0]: red_a2 The parameter construct the first group of factors used in LENC correction in red color channels.
0x90	LENC GRN X0	0x40	RW	Bit[7:0]: grn_x0[7:0] grn_x0 is the horizontal coordinate of the lens center with respect to the left_top corner of the image. Range from 0 to 639. See **LENC GRN XY0**[1:0] (**0x92**)
0x91	LENC GRN Y0	0xF0	RW	Bit[7:0]: grn_y0[7:0] grn_y0 is the vertical coordinate of the lens center with respect to the left_top corner of the image. Range from 0 to 479. See **LENC GRN XY0**[4] (**0x92**)
0x92	LENC GRN XY0	0x01	RW	Bit[4]: grn_y0[8] See **LENC GRN Y0**[7:0] (**0x91**) Bit[1:0]: grn_x0[9:8] See **LENC GRN X0**[7:0] (**0x90**)
0x93	LENC GRN A1	0x22	RW	Bit[6:0]: grn_a1 The parameter construct the first group of factors used in LENC correction in green color channels.

table 5-3 LENC registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x94	LENC GRN B1	0xC2	RW	Bit[7:0]: grn_b1 The parameter construct the second group of factors used in LENC correction in green color channels.
0x95	LENC GRN AB2	0x87	RW	Bit[7:4]: grn_b2 The parameter construct the second group of factors used in LENC correction in green color channels. Bit[3:0]: grn_a2 The parameter construct the first group of factors used in LENC correction in green color channels.
0x96	LENC BLUE X0	0x40	RW	Bit[7:0]: blu_x0[7:0] blu_x0 is the horizontal coordinate of the lens center with respect to the left_top corner of the image. Range from 0 to 639. See **LENC BLUE XY0**[1:0] (**0x98**)
0x97	LENC BLUE Y0	0xF0	RW	Bit[7:0]: blu_y0[7:0] blu_y0 is the vertical coordinate of the lens center with respect to the left_top corner of the image. Range from 0 to 479. See **LENC BLUE XY0**[4] (**0x98**)
0x98	LENC BLUE XY0	0x01	RW	Bit[4]: blu_y0[8] See **LENC BLUE Y0**[7:0] (**0x97**) Bit[1:0]: blu_x0[9:8] See **LENC BLUE X0**[7:0] (**0x96**)
0x99	LENC BLUE A1	0x22	RW	Bit[6:0]: blu_a1 The parameter construct the first group of factors used in LENC correction in blue color channels.
0x9A	LENC BLUE B1	0xC2	RW	Bit[7:0]: blu_b1 The parameter construct the second group of factors used in LENC correction in blue color channels.
0x9B	LENC BLUE AB2	0x87	RW	Bit[7:4]: blu_b2 The parameter construct the second group of factors used in LENC correction in blue color channels. Bit[3:0]: blu_a2 The parameter construct the first group of factors used in LENC correction in blue color channels.

5.4 gamma (GMA)

The main purpose of Gamma (GMA) is to compensate the non-linear of sensor. GMA converts the pixel values according to the Gamma curve to compensate the sensor output in different light strength.

The non-linear gamma curve is approximately constructed with different linear function.

table 5-4 GMA registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x80	ISP CTRL00	1'b1	RW	Bit[3]: Gamma enable 0: Disable gamma 1: Enable gamma
0x84 sub address: 0x38[3:0]=4'h1	BIAS CTRL	1'b1 1'b0	RW	Bit[6]: Gamma bias enable 0: Gamma bias is 0 1: Gamma bias is the gamma offset Bit[2]: Manual gamma offset enable 0: Gamma offset is the black level 1: Gamma offset is manual offset (refer to **GMA OFF MAN**)
0x84 sub address: 0x38[3:0]=4'h4	GMA OFF MAN	0x00	RW	Bit[7:0]: Manual gamma offset
0x9C	GMA YST01	0x0E	RW	Bit[7:0]: YST1 Output value at input = 0x04
0x9D	GMA YST02	0x1A	RW	Bit[7:0]: YST2 Output value at input = 0x08
0x9E	GMA YST03	0x31	RW	Bit[7:0]: YST3 Output value at input = 0x10
0x9F	GMA YST04	0x5A	RW	Bit[7:0]: YST4 Output value at input = 0x20
0xA0	GMA YST05	0x69	RW	Bit[7:0]: YST5 Output value at input = 0x28
0xA1	GMA YST06	0x75	RW	Bit[7:0]: YST6 Output value at input = 0x30
0xA2	GMA YST07	0x7E	RW	Bit[7:0]: YST7 Output value at input = 0x38
0xA3	GMA YST08	0x88	RW	Bit[7:0]: YST8 Output value at input = 0x40

table 5-4 GMA registers (sheet 2 of 2)

address	register name	default value	R/W	description
0xA4	GMA YST09	0x8F	RW	Bit[7:0]: YST9 Output value at input = 0x48
0xA5	GMA YST10	0x96	RW	Bit[7:0]: YST10 Output value at input = 0x50
0xA6	GMA YST11	0xA3	RW	Bit[7:0]: YST11 Output value at input = 0x60
0xA7	GMA YST12	0xAF	RW	Bit[7:0]: YST12 Output value at input = 0x70
0xA8	GMA YST13	0xC4	RW	Bit[7:0]: YST13 Output value at input = 0x90
0xA9	GMA YST14	0xD7	RW	Bit[7:0]: YST14 Output value at input = 0xB0
0xAA	GMA YST15	0xE8	RW	Bit[7:0]: YST15 Output value at input = 0xD0
0xAB	GMA YSLP	0x20	RW	Bit[7:0]: YSLP15 Slope in the range of (0xD1, 0xFF) Slope = (256 - YST15) x 4/3

5.5 auto white balance (AWB)

The main purpose of Auto White Balance (AWB) is to automatically adjust red, green, and blue gain to make the white target be white regardless of the lighting. Two AWB algorithms are supported, simple AWB and advanced AWB. Simple AWB makes the average of red, green, and blue channels equal. Advanced AWB detects the color temperature of the light and adjusts the color gain based on the color temperature. Manual mode is also available to allow the user to set each color gain manually.

table 5-5 AWB registers

address	register name	default value	R/W	description
0x80	ISP CTRL00	1'b1 1'b1	RW	Bit[4]: AWB enable 0: Disable 1: Enable Bit[2]: AWB gain enable 0: Disable 1: Enable
0x84 sub address: 0x38[3:0]=4'h1	BIAS CTRL	1'b1 1'b0	RW	Bit[5]: AWB bias enable 0: AWB bias is 0 1: AWB bias is the AWB offset Bit[1]: Manual AWB offset enable 0: AWB offset is the black level 1: AWB offset is manual offset (refer to **AWB OFF MAN**)
0x84 sub address: 0x38[3:0]=4'h3	AWB OFF MAN	0x00	RW	Bit[7:0]: Manual AWB offset
0x01	BGAIN	0x40	RW	AWB - Blue channel gain setting Blue gain = BGAIN / 0x40 Note: Gain should be ≥ 1x
0x02	RGAIN	0x40	RW	AWB - Red channel gain setting Red gain = RGAIN / 0x40 Note: Gain should be ≥ 1x
0x03	GGAIN	0x40	RW	AWB - Green channel gain setting Green gain = GGAIN / 0x40 Note: Gain should be ≥ 1x
0x13	REG13	0x87	RW	Bit[1]: Auto white balance control selection 0: Manual mode 1: Auto mode
0xAC	AWB CTRL0	0x6D	RW	Bit[6]: Simple AWB mode select 0: Advanced AWB mode 1: Simple AWB mode
0xAD~0xC2	AWB CTRL	–	–	Advanced AWB Parameters

5.6 white black pixel cancellation (WBC)

The main purpose of white/black pixel cancellation (WBC) is removing white/black pixels effect.

table 5-6 WBC registers

address	register name	default value	R/W	description
0x80	ISP CTRL00	1'b1 1'b1	RW	Bit[6]: Black pixel correction enable 0: Disable 1: Enable Bit[5]: White pixel correction enable 0: Disable 1: Enable
0xC3~0xCA	WBC CTRL00~CA	–	RW	WBC Option Changing these values is not recommended

5.7 color interpolation (CIP)

The main purposes of the CIP module includes:

- de-noise RAW data
- interpolate RAW data to RGB data
- sharpness adjustment

There are two methods to set some parameters: auto and manual mode. This module can output RGB data and de-noised RAW data. Setting the register **0xCC** Bit[6]/Bit[5] to 0 will enable auto mode for sharpness/denoise, respectively (see **figure 5-2** and **figure 5-3**, respectively).

figure 5-2 sharpness curve

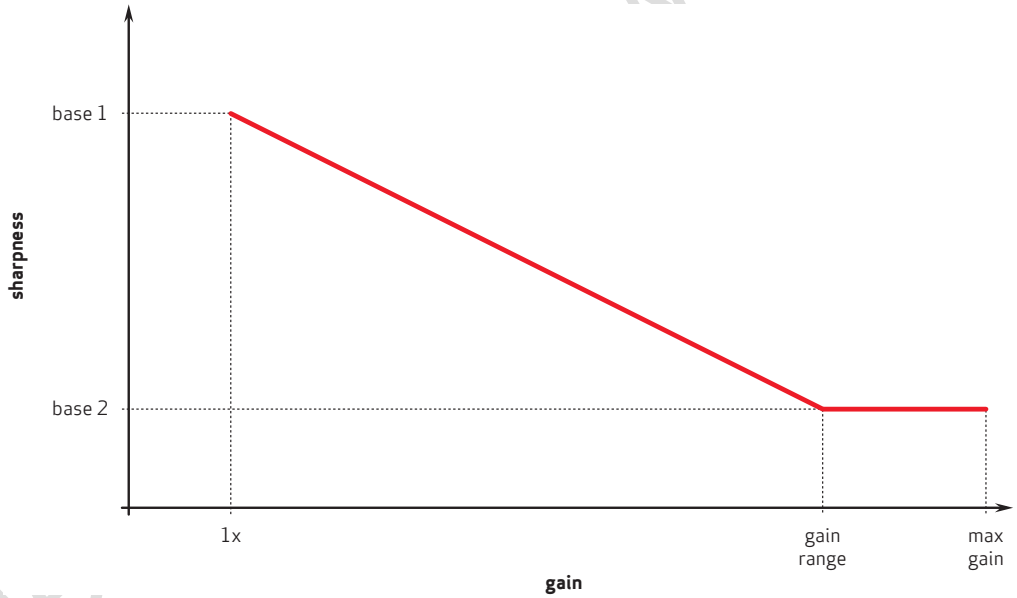


figure 5-3 denoise curve

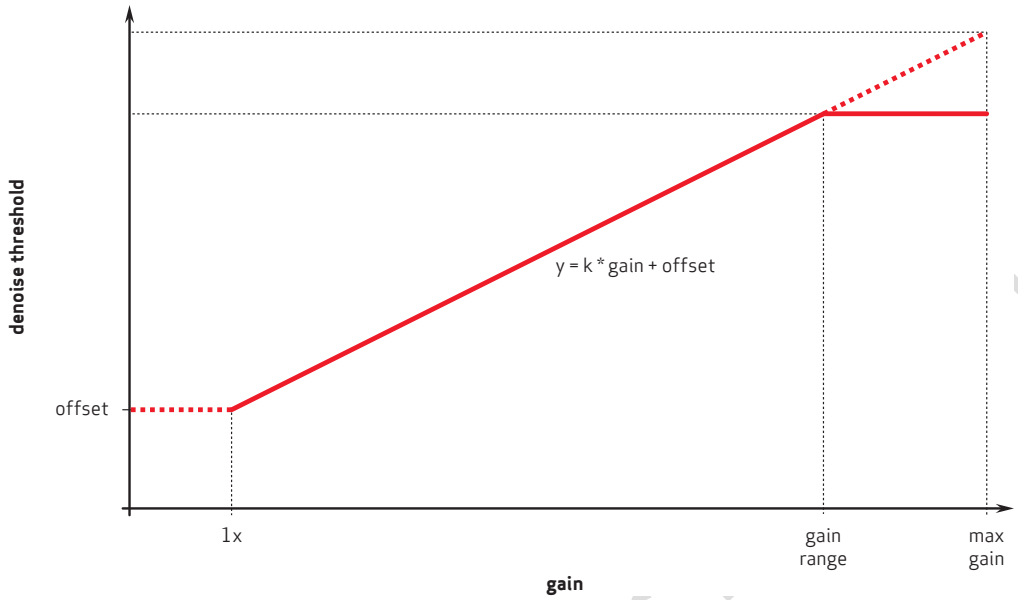


table 5-7 CIP registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x81	ISP CTRL01	1'b1	RW	Bit[0]: CIP enable 0: Disable 1: Enable
0x85	AGC OFFSET	0x00	RW	Bit[7:0]: Lower limit of denoise threshold in auto mode (offset) (see **figure 5-3**)
0x86	AGC BASE1	0x1E	RW	Bit[4:0]: Sharpness upper limit (base 1) (see **figure 5-2**)
0x87	AGC BASE2	0x02	RW	Bit[4:0]: Sharpness lower limit (base 2) (see **figure 5-2**)

table 5-7 CIP registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x88	AGC CTRL	0x00	RW	Bit[6]: Denoise gain range options (see figure 5-3) 0: Gain range is the maximum gain 1: Gain range is determined by bit[5:4] Bit[5:4]: Denoise gain range (see figure 5-3) 00: Gain range = 8 01: Gain range = 16 10: Gain range = 32 11: Gain range = 64 Bit[3:2]: K (slope of denoise curve) (see figure 5-3) 00: K = 1 01: K = 1/2 10: K = 1/4 11: K = 1/8 Denoise threshold = K × gain + offset Bit[1:0]: Sharpness gain range (see figure 5-2) 00: Gain range = 8 01: Gain range = 16 10: Gain range = 32 11: Gain range = 64
0xCB	CIP DNS THRESH MAN	0x08	RW	Bit[7:0]: Manual setting for denoise threshold
0xCC	CIP CTRL	0x04	RW	Bit[6]: Manual mode for sharpness 0: Auto mode 1: Manual mode Bit[5]: Manual mode for denoise 0: Auto mode 1: Manual mode Bit[4:0]: Manual setting for sharpness
0xCD	CIP EDGE THRESHOLD	0x06	RW	Bit[3:0]: Sharpness threshold

5.8 color matrix (CMX)

The main purpose of color matrix (CMX) is converting the image from RGB domain to YUV domain. For different color temperature, the parameters in the transmitting function will be changed.

table 5-8 CMX registers

address	register name	default value	R/W	description
0x81	ISP CTRL01	1'b1	RW	Bit[1]: CMX enable 0: Disable color matrix 1: Enable color matrix
0x84 sub address: 0x38[3:0]=4'h1	BIAS CTRL	1'b1 1'b0	RW	Bit[7]: Color matrix bias enable 0: Color matrix bias is 0 1: Color matrix bias is the color matrix offset Bit[3]: Color matrix manual offset enable 0: Color matrix offset is the black level 1: Color matrix offset is manual offset
0x84 sub address: 0x38[3:0]=4'h5	CMX OFF MAN	0x00	RW	Bit[7:0]: Manual color matrix offset
0xCE	CMX M1	0x41	RW	Bit[7:0]: Color matrix element 1 Coefficient of red to V
0xCF	CMX M2	0x3C	RW	Bit[7:0]: Color matrix element 2 Coefficient of green to V
0xD0	CMX M3	0x06	RW	Bit[7:0]: Color matrix element 3 Coefficient of blue to V
0xD1	CMX M4	0x17	RW	Bit[7:0]: Color matrix element 4 Coefficient of red to U
0xD2	CMX M5	0x3A	RW	Bit[7:0]: Color matrix element 5 Coefficient of green to U
0xD3	CMX M6	0x52	RW	Bit[7:0]: Color matrix element 6 Coefficient of blue to U
0xD4	CMX CTRL	0x5E	RW	Bit[6]: Color matrix doubler 0: Apply color matrix directly 1: Apply double of the color matrix Bit[5]: Sign bit for color matrix element 6 Bit[4]: Sign bit for color matrix element 5 Bit[3]: Sign bit for color matrix element 4 Bit[2]: Sign bit for color matrix element 3 Bit[1]: Sign bit for color matrix element 2 Bit[0]: Sign bit for color matrix element 1 (0: positive; 1: negative)

5.9 window cropping (WINC)

The main purposes of the WINC module is to make the image sizes to the real sizes by removing offsets.

table 5-9 WINC registers

address	register name	default value	R/W	description
0x82	ISP CTRL02	1'b1	RW	Bit[1]: Window cropping enable 0: Disable window cropping 1: Enable window cropping
0x83	ISP CTRL03	1'b0	RW	Bit[2]: Raw data output option 0: Output RAW10 data 1: Output RAW8 data

5.10 image scaler

The main purposes of the image scaler is to scale the array output to any final image size less than CIF. The scaler is composed of two parts, down-sampling and digital zoom out as shown in **figure 5-4**. Down-sampling supports $1/2^n$ scaling ratio and digital zoom out performs fractional scaling. In auto mode, ISP does scaling automatically based on input/output size. In manual mode, H scaling ratio has two registers to be set this way. V scaling ratio has only one register for vertical divider, **0xE5**. For non-$1/2^n$ scaling ratio, use the closest number. The ISP will correct the ratio automatically. For example, QCIF (176 x 144) has a vertical scaling ratio of 1/3.33 so 1/2 should be used in vertical divider and ISP will automatically set the 1/1.665 ratio.

figure 5-4 image scaler circuit

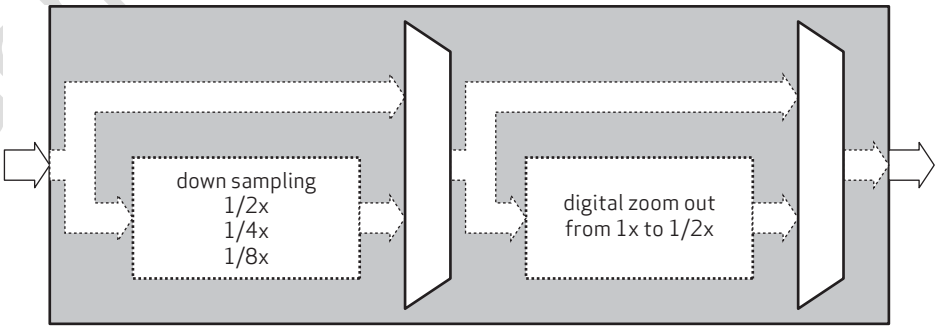


table 5-10 image scaler registers

address	register name	default value	R/W	description
0x82	ISP CTRL02	0x32	RW	Bit[3]: Vertical scaler enable 0: Disable 1: Enable Bit[2]: Horizontal scaler enable 0: Disable 1: Enable
0xD7	SCALEH XSC MAN	0x00	RW	Bit[7:0]: xsc_man[7:0] Manual value of horizontal scale coefficient (see 0xD8[2:0] for xsc_man[10:8]) Down-scaling ratio = 0x200 / xsc_man[10:0] (used for fractional scaling ratio)
0xD8	SCALEH CTRL	0x04	RW	Bit[7]: Horizontal scale option 0: Average mode 1: Skip mode Bit[6]: Horizontal scale mode 0: Auto mode 1: Manual mode Bit[5:4]: h_div_man Manual horizontal divider Down-scaling ratio =1 / 2^h_div_man (used for $1/2^n$ scaling ratio) Bit[3]: Horizontal scaling calculation option 0: Truncate 1: Rounding Bit[2:0]: xsc_man[10:8] Manual value of horizontal scale coefficient (see 0xD7[7:0] for xsc_man[7:0])
0xE5	SCALEV CTRL	0x0C	RW	Bit[7]: Vertical scale mode 0: Auto mode 1: Manual mode Bit[6:4]: Offset for skip mode Bit[3]: Vertical scale option 0: Average mode 1: Skip mode Bit[2]: Manual RAM mode setting Bit[1:0]: v_div Manual vertical divider Down-scaling ratio = 1 / 2^v_div

5.11 special digital effects (SDE)

The main purpose of Special Digital Effects (SDE) is making special digital effect such as hue/saturation etc.

Use SDE_Ctrl to get some special effect of image. Calculate the new U and V from Hue Cos, Hue Sin, and sign of the parameters, or fix the U and V values; Saturate the U and V according to the Sat_u and Sat_v; calculate the Y from Y offset, Y gain, and Y bright, or set the Y value; invert the Y U V values to get a negative image; fixed U and V to 128 (8bit data) resulting in gray image.

Hue control equations are as follows:

$U' = SGNSET[4]\ |Cos(A)| \times C\_U + SGNSET[0] \times |Sin(A)| \times C\_V + 0x80$

$V' = SGNSET[5]\ |Cos(A)| \times C\_V + SGNSET[1] \times |Sin(A)| \times C\_U + 0x80$

where $C\_U = U - 0x80$

$C\_V = V - 0x80$

$|Cos(A)| = HUE\_COS[7:0] / 0x80$

$|Sin(A)| = HUE\_SIN[7:0] / 0x80$

Contrast/Brightness control equation is as follows:

$Y = (Y_0 - Y_{avg}) \times YGAIN / 0x20 + Y_{avg} + SGNSET[3] \times YBRIGHT + SGNSET[2] \times YOFFSET$

where Y_{avg} value is the average image luminance and is automatically calculated by the sensor.

table 5-11 SDE registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x81	ISP CTRL01	1'b1	RW	Bit[5]: SDE enable 0: Disable SDE 1: Enable SDE
0xDA	SDE CTRL	0x00	RW	Bit[7]: Fixed Y enable When it is set, the output Y will be a fixed value. Bit[6]: Negative enable 0: Disable negative color effect 1: Enable negative color effect Bit[5]: Gray enable 0: Disable gray effect 1: Enable gray effect Bit[4]: Fixed V enable When it is set, the output V will be the value set in register **VREG**[7:0] (**0xE0**) Bit[3]: Fixed U enable When it is set, the output U will be the value set in register **UREG**[7:0] (**0xDF**) Bit[2]: Contrast enable 0: Disable contrast/offset /brightness 1: Enable contrast/offset/ brightness Bit[1]: Saturation enable 0: Disable saturation effect 1 Enable saturation effect Bit[0]: Hue enable 0: Disable hue effect 1: Enable hue effect
0xDB	HUE_COS	0x80	RW	Bit[7:0]: Cosine value for hue effect HUE_COS = |cos value| * 0x80
0xDC	HUE_SIN	0x00	RW	Bit[7:0]: Sine value for hue effect HUE_SIN = |sin value| * 0x80
0xDD	USAT	0x40	RW	Bit[7:0]: U saturation Enhancement for U value in saturation effect $U = U_0$ x USAT / 0x40
0xDE	VSAT	0x40	RW	Bit[7:0]: V saturation Enhancement for V value in saturation effect $V = V_0$ x VSAT / 0x40
0xDF	UREG	0x80	RW	Bit[7:0]: Fixed U value U value for fixed U effect
0xE0	VREG	0x80	RW	Bit[7:0]: Fixed V value V value for fixed V effect

table 5-11 SDE registers (sheet 2 of 2)

address	register name	default value	R/W	description
0xE1	YOFFSET	0x00	RW	Bit[7:0]: Y offset for contrast control or Y value for fixed Y effect
0xE2	YGAIN	0x20	RW	Bit[7:0]: Y gain for contrast control Gain = YGAIN / 0x20
0xE3	YBRIGHT	0x00	RW	Bit[7:0]: Brightness
0xE4	SGNSET	0x06	RW	Sign Bit for Hue and Brightness Bit[7:6]: Not used Bit[5]: Sign bit for **HUE_COS** (in V' equation) Bit[4]: Sign bit for **HUE_COS** (in U' equation) Bit[3]: Sign bit for **YBRIGHT** Bit[2]: Sign bit for **YOFFSET** Bit[1]: Sign bit for **HUE_SIN** (in V' equation) Bit[0]: Sign bit for **HUE_SIN** (in U' equation)

5.12 horizontal sub-sample control

table 5-12 horizontal sub-sample control registers

address	register name	default value	R/W	description
0xE6	VAP CTRL	0x10	RW	Bit[4]: Average mode 0: Summation 1: Average Bit[1]: Green channel sub-sample mode 0: Summation or average depending on bit[4] 1: Skip Bit[0]: Blue/red channel sub-sample mode 0: Summation or average depending on bit[4] 1: Skip

6 image sensor output interface digital functions

6.1 digital video port (DVP)

6.1.1 overview

The Digital Video Port (DVP) provides 10-bit parallel data output in all formats supported and extended features including HREF, CCIR656 format, HSYNC mode and test pattern output.

6.1.2 HREF mode

HREF mode is the default mode of the DVP. Each DVP VSYNC indicates the starting of a new frame.

6.1.3 CCIR656 mode

The OV7740 supports standard CCIR656 mode. Instead of using VSYNC to define each frame and HREF to define each row, the CCIR656 mode inserts a 4-byte header before and after the row data as follows:

Active video output period:

SAV: [FF] {00] [00] [80]
EAV: [FF] [00] [00] [9D]

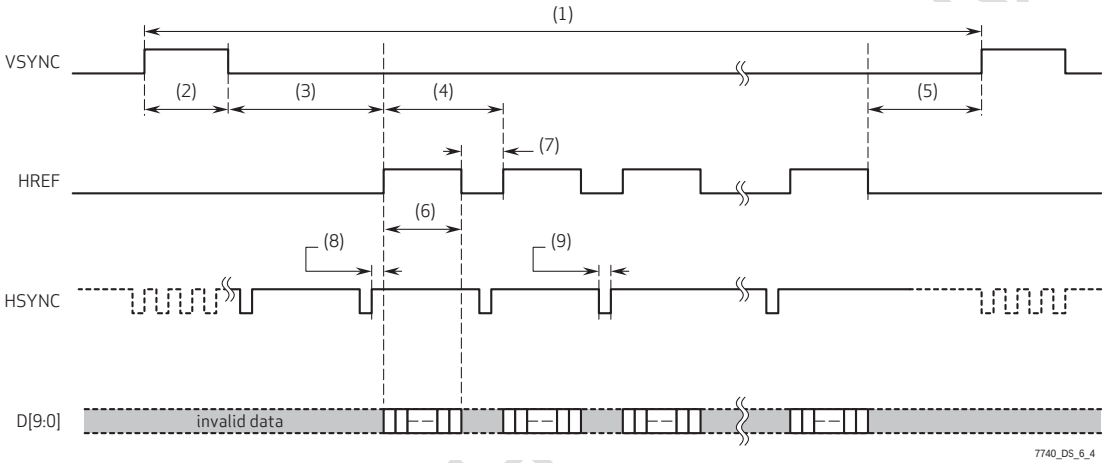
Vertical blanking period:

SAV: [FF] {00] [00] [AB]
EAV: [FF] [00] [00] [B6]

Setting register 0x12[5] = 1 turns ON the CCIR656 mode.

6.1.4 DVP timing

figure 6-1 DVP timing diagram



note
The timing values shown in **table 6-1** may vary depending upon register settings.

table 6-1 DVP timing specifications

mode	timing
VGA 640x480	(1) 399168 = 504 lines (2) 3168 (4 lines) (3) 9674 (4) 792 (5) 6318 (6) 640 (7) 152 (8) 106 (9) 48
QVGA 320x240	(1) 199584 = 252 lines (2) 1584 (2 lines) (3) 6882 (4) 792 (5) 1508 (6) 320 (7) 472 (8) 200 (9) 48

table 6-2 DVP control registers

address	register name	default value	R/W	description
0x12	REG12	0x11	RW	Bit[5]: CCIR656 enable
0x28	REG28	0x00	RW	Bit[7]: Output data bit reverse option Bit[6]: HREF pin output swap 0: HREF 1: HSYNC Bit[5]: HSYNC polarity 0: Positive 1: Negative Bit[4]: HREF polarity 0: Output positive HREF 1: Output negative HREF for data valid Bit[3]: No VSYNC output option 0: Still output VSYNC when frame drop 1: No VSYNC output when frame drop Bit[2]: Control bit Changing this value is not recommended Bit[1]: VSYNC polarity 0: Positive 1: Negative
0x0C	REG0C	0x02	RW	Bit[4]: YUV output Y <-> UV swap 0: YUYVYUYV 1: UYVYUYVY Bit[3]: Output data high 8-bit MSB and LSB swap 0: Output [DATA9,DATA8…DATA3, DATA2,DATA1,DATA0] 1: Output [DATA2,DATA3…DATA8, DATA9,DATA1,DATA0]
0x65	REG65	0x00	RW	Bit[3]: Output data bit swap option 0: Output DATA[9:0] 1: Output DATA[0:9]

7 register tables

The following tables provide descriptions of the device control registers contained in the OV7740. For all register Enable/Disable bits, Enable = 1 and Disable = 0. The device slave addresses are 0x42 for write and 0x43 for read.

table 7-1 system control registers (sheet 1 of 25)

address	register name	default value	R/W	description
0x00	GAIN	0x00	RW	AGC Gain Control LSBs (MSBs in REG15[1:0] (**0x15**)) Bit[7:0]: Analog gain Gain=(GAIN[9] + 1) × (GAIN[8] + 1) × (GAIN[7] + 1) × (GAIN[6] + 1) × (GAIN[5] + 1) × (GAIN[4] + 1) × [(GAIN[3:0])/16 + 1]
0x01	BGAIN	0x40	RW	AWB - Blue channel gain setting Blue gain = BGAIN / 0x40 Note: Gain should be ≥ 1x
0x02	RGAIN	0x40	RW	AWB - Red channel gain setting Red gain = RGAIN / 0x40 Note: Gain should be ≥ 1x
0x03	GGAIN	0x40	RW	AWB - Green channel gain setting Green gain = GGAIN / 0x40 Note: Gain should be ≥ 1x
0x04	REG04	0x00	RW	Analog Setting Changing this value is not recommended
0x05	BAVG	–	R	B Channel Average
0x06	GAVG	–	R	G Channel Average
0x07	RAVG	–	R	R Channel Average
0x08~ 0x09	NOT USED	–	–	Not Used
0x0A	PIDH	0x77	R	Product ID Number MSB (Read only)
0x0B	PIDL	0x40	R	Product ID Number LSB (Read only)

table 7-1 system control registers (sheet 2 of 25)

address	register name	default value	R/W	description
0x0C	REG0C	0x02	RW	Bit[7]: Flip enable 0: Disable flip 1: Enable flip Bit[6]: Mirror enable 0: Mirror disable 1: Mirror enable Bit[5]: Not used Bit[4]: YUV output, Y ↔ UV swap 0: YUYVYUYV 1: UYVYUYVY Bit[3]: High 8-bit MSB and LSB swap 0: Output [Y9,Y8…Y3,Y2,Y1,Y0] 1: Output [Y2,Y3…Y8,Y9,Y1,Y0] Bit[2:1]: Max exposure = frame length – limit × 2 Bit[0]: Not used
0x0D	REG0D	0x34	RW	Analog Setting Changing this value is not recommended
0x0E	REG0E	0xE0	RW	Bit[7]: BLC line selection 0: Electrical BLC 1: Optical BLC Bit[6:5]: BLC line selection 00 Select both blue line and red line as BLC line. 01: Only select red line as BLC line 10: Only select blue line as BLC line. 11: Select both blue line and red line as BLC line Bit[4]: Not used Bit[3]: Sleep mode Bit[2]: Not used Bit[1:0]: Output driving capability 00 1x 01: 2x 10: 3x 11: 4x
0x0F	HAEC	0x00	RW	Automatic Exposure Control Bit[15:8] (LSBs in AEC[7:0] (**0x10**))
0x10	AEC	0xF0	RW	Automatic Exposure Control Bit [7:0] (MSBs in HAEC[7:0] (**0x0F**))

table 7-1 system control registers (sheet 3 of 25)

address	register name	default value	R/W	description
0x11	CLK	0x00	RW	Bit[7:6]: PLL setting Changing these values is not recommended Bit[5:0]: Clock divider sysclk = XVCLK1 × PLLDIV / [(CLK[5:0] + 1) ×2 × PreDiv]
0x12	REG12	0x11	RW	Bit[7]: Soft reset 1: Initiate system reset. All registers are set to factory default value after which the chip resumes normal operation. Bit[6]: Vertical skip mode Bit[5]: CC656 mode Bit[4]: Sensor raw Bit[3:1]: Not used Bit[0]: Output raw data RGB mode
0x13	REG13	0x87	RW	Bit[7]: AEC speed selection 0: Normal 1: Faster AEC correction Bit[6]: Enable frame drop function Bit[5]: Banding enable 0: Disable 1: Enable Bit[4]: Banding option 0: Minimum exposure is limited to 1/120 or 1/100 second when banding filter is enabled 1: Minimum exposure is allowed to be less than 1/120 or 1/100 second when banding filter is enabled Bit[3]: LAEC enable 0: Disable 1: Enable Bit[2]: AGC auto/manual control selection 0: Manual mode 1: Auto mode Bit[1]: Auto white balance control selection 0: Manual mode 1: Auto mode Bit[0]: Exposure auto/manual control selection 0: Manual mode 1: Auto mode

table 7-1 system control registers (sheet 4 of 25)

address	register name	default value	R/W	description
0x14	REG14	0x30	RW	Bit[7]: Analog setting Changing this value is not recommended Bit[6:4]: AGC gain ceiling 000: 2x 001: 4x 010: 8x 011: 16x 100: 32x Bit[3:1]: Analog setting Changing these values is not recommended Bit[0]: Manual LAEC enable
0x15	REG15	0x00	RW	Bit[7]: Enable inserting frames in night mode Bit[6:4]: Ceiling of inserting frames 000: Up to 0 frame 001: Up to 1 frame 010: Up to 2 frames 011: Up to 3 frames 1xx: Up to 7 frames Bit[3:2]: Night mode triggering point 00: 2x gain 01: 4x gain 10: 8x gain 11: 16x gain Bit[1:0]: AGC MSBs (digital gain) (LSBs in GAIN[7:0] (**0x00**))
0x16	REG16	0x00	RW	Bit[7]: Analog setting Changing this value is not recommended Bit[6]: Not used Bit[5]: Sensor vertical output size 1 LSBs Bit[4:3]: Sensor horizontal output size 2 LSB Bit[2]: Sensor vertical output start point 1 LSB Bit[1:0]: Sensor horizontal output start point 2 LSBs
0x17	AHSTART	0x2A	RW	Sensor Horizontal Output Start Point 8 MSBs (LSBs in REG16[1:0] (**0x16**))
0x18	AHSIZE	0xA0	RW	Sensor Horizontal Output size 8 MSBs (LSBs in REG16[4:3] (**0x16**))
0x19	AVSTART	0x05	RW	Sensor Vertical Output Start Point 8 MSBs (LSBs in REG16[2] (**0x16**))

table 7-1 system control registers (sheet 5 of 25)

address	register name	default value	R/W	description
0x1A	AVSIZE	0xF0	RW	Sensor Vertical Output size MSBs (LSB in REG16[5] (**0x16**))
0x1B	PSHFT	0x80	RW	Pixel Shift
0x1C	MIDH	0x7F	R	Manufacturer ID Byte - High
0x1D	MIDL	0xA2	R	Manufacturer ID Byte - Low
0x1E	REG1E	0x11	RW	Bit[7:1]: Analog setting Changing these values is not recommended Bit[0]: AEC step control 0: AEC max increasing step less than vertical blanking 1: AEC max increasing step has no limit
0x1F	REG1F	0x00	RW	LSBs of tp level exposure control when exposure is less than one line (MSBs in REG30 (**0x30**))
0x20	REG20	0x00	RW	Bit[7]: Maximum banding step for 50Hz, 1 MSB Bit[6]: Maximum banding step for 60Hz, 1 MSB Bit[5:0]: Analog setting Changing these values is not recommended
0x21	REG21	0x44	RW	Bit[7:4]: Maximum banding step for 50Hz, 4 LSBs (MSB is in REG20[7] (0x20) Bit[3:0]: Maximum banding step for 60Hz, 4 LSBs (MSB is in REG20[6] (0x20)
0x22~ 0x23	REG22~23	–	RW	Analog Settings Changing these values is not recommended
0x24	WPT	0x78	RW	Luminance Signal High Range for AEC/AGC Operation
0x25	BPT	0x68	RW	Luminance Signal Low Range for AEC/AGC Operation
0x26	VPT	0xD4	RW	Effective only AEC/AGC fast mode
0x27	REG27	0x00	RW	Bit[7]: Black sun cancellation enable Bit[6:0]: Analog setting Changing these values is not recommended

table 7-1 system control registers (sheet 6 of 25)

address	register name	default value	R/W	description
0x28	REG28	0x00	RW	Bit[7]: Output data bit reverse option Bit[6]: HREF pin output swap 0: HREF 1: HSYNC Bit[5]: HSYNC polarity 0: Positive 1: Negative Bit[4]: HREF polarity 0: Output positive HREF 1: Output negative HREF for data valid Bit[3]: No VSYNC output option 0: Still output VSYNC when frame drop 1: No VSYNC output when frame drop Bit[2]: Analog setting Changing this value is not recommended Bit[1]: VSYNC polarity 0: Positive 1: Negative Bit[0]: Analog setting Changing this value is not recommended
0x29	REG29	0x18	RW	Horizontal tp Counter End Point LSBs
0x2A	REG2A	0x03	RW	Horizontal tp Counter End Point MSBs
0x2B	REG2B	0xF8	RW	Row Counter End Point LSBs
0x2C	REG2C	0x01	RW	Row Counter End Point MSBs
0x2D	REG2D	0x00	RW	Automatically Inserted Dummy Lines in Night Mode LSBs
0x2E	REG2E	0x00	RW	Automatically Inserted Dummy Lines in Night Mode MSBs
0x2F	YAVG	–	R	Luminance Average Value
0x30	REG30	0x00	RW	MSBs of tp Level Exposure Control when exposure is less than one line (LSBs in REG1F (**0x1F**))
0x31	HOUTSIZE	0xA0	RW	DSP H output size 8MSB H output size = {HOUTSIZE[7:0] (**0x31**), REG34[2:1] (**0x34**)}
0x32	VOUTSIZE	0xF0	RW	DSP V output size 8MSB V output size = {VOUTSIZE[7:0] (**0x32**), REG34[0] (**0x34**)}

table 7-1 system control registers (sheet 7 of 25)

address	register name	default value	R/W	description
0x33	HVSIZEOFF	0x00	RW	Bit[7:4]: H size offset Bit[3:0]: V size offset
0x34	REG34	0x00	RW	Bit[7:3]: Not used Bit[2]: DSP H output size 2 LSBs Bit[0]: DSP V output size 1 LSB
0x35~ 0x37	REG35~37	–	RW	Analog Setting Changing these values is not recommended
0x38	REG38	0x10	RW	Bit[7]: Not used Bit[6:4]: Control bits Changing these values is not recommended Bit[3:0]: Monitor[3:0] I2C registers sub-address control bits
0x39~ 0x49	REG39~49	–	RW	Analog Setting Changing these values is not recommended
0x4A	REG4A	0x81	RW	Bit[7:4]: Analog setting Bit[3]: Internal regulator bypass selection 0: Enable 1: Bypass Bit[2:0]: Analog setting
0x4B~ 0x4F	REG39~49	–	RW	Analog Setting Changing these values is not recommended
0x50	REG50	0x2E	RW	LSBs of Banding Starting Step for 50 Hz light source (MSBs in REG52[5:4] (**0x52**))
0x51	REG51	0xFC	RW	LSBs of Banding Starting Step for 60 Hz light source (MSBs in REG52[7:6] (**0x52**))
0x52	REG52	0x10	RW	Bit[7:6]: MSBs of banding starting step for 60 Hz light source (LSBs in REG51 (**0x51**)) Bit[5:4]: MSBs of banding starting step for 50 Hz light source (LSBs in REG50 (**0x50**)) Bit[3:0]: Analog setting Changing these values is not recommended
0x53	REG53	0x00	RW	Analog Setting Changing these values is not recommended

table 7-1 system control registers (sheet 8 of 25)

address	register name	default value	R/W	description
0x54	REG54	0xFC	RW	Bit[7]: Selects DATA[9:2] 0: Input 1: Output Bit[6:5]: Selects DATA[1:0] 0: Input 1: Output Bit[4]: Input/output selection of the HREF pin 0: Input 1: Output Bit[3]: Input/output selection of the VSYNC pin 0: Input 1: Output Bit[2]: Input/output selection of the PCLK pin 0: Input 1: Output Bit[1]: Not used Bit[0]: Group write enable 0: Disable 1: Enable
0x55	REG55	0x40	RW	Bit[7:6]: PLLDiv 00: x1 01: x4 10: x6 11: x8 Bit[5:4]: PreDiv 00: /1 01: /2 10: /3 11: /4 Bit[3:0]: Clock control Changing these values is not recommended
0x56	REG56	0xFF	RW	16-zone Y Average Select In each zone: 00: Not selected 01: Weight x1 10: Weight x2 11: Weight x4 Bit[7:6]: Zone 4 Bit[5:4]: Zone 3 Bit[3:2]: Zone 2 Bit[1:0]: Zone 1

table 7-1 system control registers (sheet 9 of 25)

address	register name	default value	R/W	description
0x57	REG57	0xFF	RW	In each zone: 00: Not selected 01: Weight x1 10: Weight x2 11: Weight x4 Bit[7:6]: Zone 8 Bit[5:4]: Zone 7 Bit[3:2]: Zone 6 Bit[1:0]: Zone 5
0x58	REG58	0xFF	RW	In each zone: 00: Not selected 01: Weight x1 10: Weight x2 11: Weight x4 Bit[7:6]: Zone 12 Bit[5:4]: Zone 11 Bit[3:2]: Zone 10 Bit[1:0]: Zone 9
0x59	REG59	0xFF	RW	In each zone: 00: Not selected 01: Weight x1 10: Weight x2 11: Weight x4 Bit[7:6]: Zone 16 Bit[5:4]: Zone 15 Bit[3:2]: Zone 14 Bit[1:0]: Zone 13
0x5A	UV_K	0x01	RW	k (slope of UV auto adjust curve), y = a - kx (see **figure 4-5**)
0x5B	REG5B	0xFF	RW	Bit[7:6]: gth2 (threshold 2 of UV auto adjust curve), 2 LSBs (MSBs are in **REG5C**[7:5] (0x5C)) By setting gth2 = 0, UV adjust is in manual mode; otherwise, it is in auto mode. Bit[5:0]: a (intercept of UV auto adjust curve), must be set to 0x1F (see **figure 4-5**)

table 7-1 system control registers (sheet 10 of 25)

address	register name	default value	R/W	description
0x5C	REG5C	0x1F	RW	Bit[7:5]: gth2 (threshold 2 of UV auto adjust curve), 3 MSBs (LSBs are in **REG5B**[7:6] (0x5B)) By setting gth2 = 0, UV adjust is in manual mode; otherwise, it is in auto mode. Bit[4:0]: Auto mode - UV offset of UV auto adjust curve Manual mode - UV adjust value (see **figure 4-5**)
0x5D	REG5D	0x00	RW	Bit[7:4]: gth1 (threshold 1 of UV auto adjust curve) (see **figure 4-5**) Bit[3:0]: Control bits Changing these values is not recommended
0x5E~ 0x62	REG5E~62	–	RW	Analog Settings Changing these values is not recommended
0x63	REG63	–	R	Luminance Average Value of one zone. This zone was selected by Monitor[3:0] in REG38[3:0] (**0x38**)
0x64	REG64	0x40	RW	Bit[7:6]: Control bits Changing these values is not recommended Bit[5]: BLC trigger 0: BLC offset will be adjusted when gain changes 1: BLC offset is adjusted every frame Bit[4:0]: Control bits Changing these values is not recommended
0x65	REG65	0x00	RW	Bit[7:4]: Not used Bit[3]: Output data bit swap option 0: Output DATA[9:0] 1: Output DATA[0:9] Bit[2]: Control bit Changing this value is not recommended Bit[1]: GPIO register for pin HREF Bit[0]: GPIO register for pin VSYNC
0x66	REG66	0x00	RW	AWB Bias
0x67	BLC8	0x80	RW	Bit[7:6]: Control bit Changing this value is not recommended Bit[5:0]: BLC target

table 7-1 system control registers (sheet 11 of 25)

address	register name	default value	R/W	description
0x68	BLC9	0x92	RW	BLC Control Register Changing this value is not recommended
0x69	BLCA	0x00	RW	Bit[7:5]: Not used Bit[4]: Control bit Changing this value is not recommended Bit[3]: MBLC When setting this bit to 1, auto BLC will be initiated for 64 frames Bit[2]: Not used Bit[1:0]: Control bits Changing these values is not recommended
0x6A	REG6A	0x00	RW	LSBs of BLC Offsets for Gr Channel
0x6B	REG6B	0x00	RW	LSBs of BLC Offsets for Gb Channel
0x6C	REG6C	0x00	RW	LSBs of BLC Offsets for R Channel
0x6D	REG6D	0x00	RW	LSBs of BLC Offsets for B Channel
0x6E	REG6E	0x00	RW	Bit[7:6]: MSBs of BLC offsets for Gr channel Bit[5:4]: MSBs of BLC offsets for Gb channel Bit[3:2]: MSBs of BLC offsets for R channel Bit[1:0]: MSBs of BLC offsets for B channel
0x6F	REG6F	0x43	RW	Control Register Changing this value is not recommended
0x70~ 0x7E	CONTROL REGISTERS	–	RW	50/60 Hz Auto Detection Control Contact your local OmniVision FAE for settings
0x7F	NOT USED	–	–	Not Used
0x80	ISP CTRL00	0x7F	RW	ISP Control 00 (0: disable; 1: enable) Bit[7]: Not used Bit[6]: Black pixel correction enable Bit[5]: White pixel correction enable Bit[4]: AWB enable Bit[3]: Gamma enable Bit[2]: AWB gain enable Bit[1]: LENC enable Bit[0]: ISP enable

table 7-1 system control registers (sheet 12 of 25)

address	register name	default value	R/W	description
0x81	ISP CTRL01	0x3F	RW	ISP Control 01 (0: disable; 1: enable) Bit[7:6]: Not used Bit[5]: SDE enable Bit[4]: UV adjust enable Bit[3]: YUV422 enable Bit[2]: UV average enable Bit[1]: CMX enable Bit[0]: CIP enable
0x82	ISP CTRL02	0x32	RW	ISP Control 02 (0: disable; 1: enable) Bit[7:6]: Not used Bit[5]: Y average enable Bit[4]: FIFO enable Bit[3]: Vertical scaler enable Bit[2]: Horizontal scaler enable Bit[1]: Window cropping enable Bit[0]: Smooth scale enable
0x83	ISP CTRL03	0x09	RW	Bit[7:6]: Not used Bit[5]: Video OFF 0: Normal outputs 1: No outputs Bit[4]: YAVG YUV mode 0: YAVG inputs are raw data 1: YAVG inputs are y of YUV422 Bit[3]: YAVG after WBC 0: Inputs of YAVG come from awb_gain 1: Inputs of YAVG come from WBC Bit[2]: Raw data output option 0: Output RAW10 data 1: Output RAW8 data Bit[1]: AWB2 after GMA 0: Second inputs of AWB statistic are the inputs of GMA 1: Second inputs of AWB statistic are the outputs of GMA Bit[0]: For testing purposes only
0x84 sub address: 0x38[3:0]=4'h0	BIST CTRL	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Debug mode

table 7-1 system control registers (sheet 13 of 25)

address	register name	default value	R/W	description
0x84 sub address: 0x38[3:0]=4'h1	BIAS CTRL	0xF0	RW	Bit[7]: Color matrix bias enable 0: Color matrix bias is 0 1: Color matrix bias is the color matrix offset Bit[6]: Gamma bias enable 0: Gamma bias is 0 1: Gamma bias is the gamma offset Bit[5]: AWB bias enable 0: AWB bias is 0 1: AWB bias is the AWB offset Bit[4]: Lens correction bias enable 0: LENC bias is 0 1: LENC bias is the LENC offset Bit[3]: Color matrix manual offset enable 0: Color matrix offset is black level 1: Color matrix offset is manual offset Bit[2]: Manual gamma offset enable 0: Gamma offset is the black level 1: Gamma offset is manual offset (refer to **GMA OFF MAN**) Bit[1]: Manual AWB offset enable 0: AWB offset is the black level 1: AWB offset is manual offset (refer to **AWB OFF MAN**) Bit[0]: Manual lens correction offset enable 0: LENC offset is the black level 1: LENC offset is manual offset (refer to **LENC OFF MAN**)
0x84 sub address: 0x38[3:0]=4'h2	LENC OFF MAN	0x00	RW	Bit[7:0]: Manual offset for LENC
0x84 sub address: 0x38[3:0]=4'h3	AWB OFF MAN	0x00	RW	Bit[7:0]: Manual AWB offset
0x84 sub address: 0x38[3:0]=4'h4	GMA OFF MAN	0x00	RW	Bit[7:0]: Manual gamma offset
0x84 sub address: 0x38[3:0]=4'h5	CMX OFF MAN	0x00	RW	Bit[7:0]: Manual color matrix offset

table 7-1 system control registers (sheet 14 of 25)

address	register name	default value	R/W	description
0x84 sub address: 0x38[3:0]=4'h6	ROREG ADDR	–	R	isp_roreg_address Read-only registers' address
0x84 sub address: 0x38[3:0]=4'h7	PRE CTRL00	0x00	RW	Bit[7:5]: Not used Bit[4]: Moving bar enable 0: Color bar is a still image 1: Color bar is a moving image Bit[3]: Not used Bit[2]: For testing Bit[1]: bar enable 0: Output data are normal data 1: Output data are color bar data Bit[0]: For testing
0x84 sub address: 0x38[3:0]=4'h8	PRE CTRL01	0x00	RW	Bit[7:6]: Not used Bit[5:4]: Bar style Output color bar style Bit[3:0]: Bar step Output color bar step
0x85	AGC OFFSET	0x00	RW	Bit[7:0]: Lower limit of denoise threshold in auto mode (offset) (see **figure 5-3**)
0x86	AGC BASE1	0x1E	RW	Bit[7:5]: Not used Bit[4:0]: Sharpness upper limit (base 1) (see **figure 5-2**)
0x87	AGC BASE2	0x02	RW	Bit[7:5]: Not used Bit[4:0]: Sharpness lower limit (base 2) (see **figure 5-2**)

table 7-1 system control registers (sheet 15 of 25)

address	register name	default value	R/W	description
0x88	AGC CTRL	0x00	RW	Bit[7]: Not used Bit[6]: Denoise gain range options (see figure 5-3) 0: Gain range is the maximum gain 1: Gain range is determined by bit[5:4] Bit[5:4]: Denoise gain range (see figure 5-3) 00: Gain range = 8 01: Gain range = 16 10: Gain range = 32 11: Gain range = 64 Bit[3:2]: K (slope of denoise curve) (see figure 5-3) 00: K = 1/8 01: K = 1/4 10: K = 1/2 11: K = 1 Denoise threshold = K × gain + offset Bit[1:0]: Sharpness gain range (see figure 5-2) 00: Gain range = 8 01: Gain range = 16 10: Gain range = 32 11: Gain range = 64
0x89	LENC CTRL	0x30	RW	Bit[7:6]: Not used Bit[5]: Lens correction bias handling 0: LENC bias will be not added back to lenc-corrected data 1: LENC bias will be added back to lenc_corrected data BIt[4]: Rounding enable 0: Disable data rounding 1: Enable data rounding Bit[3:2]: Vertical skip 00: Does not skip a pixel 01: Skips 1 pixel every 2 pixels 10: Skips 3 pixels every 4 pixels 11: Skips 7 pixels every 8 pixels Bit[1:0]: Horizontal skip 00: Does not skip a line 01: Skips 1 line every 2 lines 10: Skips 3 lines every 4 lines 11: Skips 7 lines every 8 lines

table 7-1 system control registers (sheet 16 of 25)

address	register name	default value	R/W	description
0x8A	LENC RED X0	0x40	RW	Bit[7:0]: red_x0[7:0] red_x0 is the horizontal coordinate of the lens center with respect to the left_top corner of the image. Range from 0 to 639. See **LENC RED XY0**[1:0] (**0x8C**)
0x8B	LENC RED Y0	0xF0	RW	Bit[7:0]: red_y0[7:0] red_y0 is the vertical coordinate of the lens center with respect to the left_top corner of the image. Range from 0 to 479. See **LENC RED XY0**[4] (**0x8C**)
0x8C	LENC RED XY0	0x01	RW	Bit[7:5]: Not used Bit[4]: red_y0[8] See **LENC RED Y0**[7:0] (**0x8B**) Bit[3:2]: Not used Bit[1:0]: red_x0[9:8] See **LENC RED X0**[7:0] (**0x8A**)
0x8D	LENC RED A1	0x22	RW	Bit[7]: Not used Bit[6:0]: red_a1 The parameter construct the first group of factors used in LENC correction in red color channels.
0x8E	LENC RED B1	0xC2	RW	Bit[7:0]: red_b1 The parameter construct the second group of factors used in LENC correction in red color channels.
0x8F	LENC RED AB2	0x87	RW	Bit[7:4]: red_b2 The parameter construct the second group of factors used in LENC correction in red color channels. Bit[3:0]: red_a2 The parameter construct the first group of factors used in LENC correction in red color channels.
0x90	LENC GRN X0	0x40	RW	Bit[7:0]: grn_x0[7:0] grn_x0 is the horizontal coordinate of the lens center with respect to the left_top corner of the image. Range from 0 to 639. See **LENC GRN XY0**[1:0] (**0x92**)

table 7-1 system control registers (sheet 17 of 25)

address	register name	default value	R/W	description
0x91	LENC GRN Y0	0xF0	RW	Bit[7:0]: grn_y0[7:0] grn_y0 is the vertical coordinate of the lens center with respect to the left_top corner of the image. Range from 0 to 479. See **LENC GRN XY0**[4] (**0x92**)
0x92	LENC GRN XY0	0x01	RW	Bit[7:5]: Not used Bit[4]: grn_y0[8] See **LENC GRN Y0**[7:0] (**0x91**) Bit[3:2]: Not used Bit[1:0]: grn_x0[9:8] See **LENC GRN X0**[7:0] (**0x90**)
0x93	LENC GRN A1	0x22	RW	Bit[7]: Not used Bit[6:0]: grn_a1 The parameter construct the first group of factors used in LENC correction in green color channels.
0x94	LENC GRN B1	0xC2	RW	Bit[7:0]: grn_b1 The parameter construct the second group of factors used in LENC correction in green color channels.
0x95	LENC GRN AB2	0x87	RW	Bit[7:4]: grn_b2 The parameter construct the second group of factors used in LENC correction in green color channels. Bit[3:0]: grn_a2 The parameter construct the first group of factors used in LENC correction in green color channels.
0x96	LENC BLUE X0	0x40	RW	Bit[7:0]: blu_x0[7:0] blu_x0 is the horizontal coordinate of the lens center with respect to the left_top corner of the image. Range from 0 to 639. See **LENC BLUE XY0**[1:0] (**0x98**)
0x97	LENC BLUE Y0	0xF0	RW	Bit[7:0]: blu_y0[7:0] blu_y0 is the vertical coordinate of the lens center with respect to the left_top corner of the image. Range from 0 to 479. See **LENC BLUE XY0**[4] (**0x98**)

table 7-1 system control registers (sheet 18 of 25)

address	register name	default value	R/W	description
0x98	LENC BLUE XY0	0x01	RW	Bit[7:5]: Not used Bit[4]: blu_y0[8] See **LENC BLUE Y0**[7:0] (**0x97**) Bit[3:2]: Not used Bit[1:0]: blu_x0[9:8] See **LENC BLUE X0**[7:0] (**0x96**)
0x99	LENC BLUE A1	0x22	RW	Bit[7]: Not used Bit[6:0]: blu_a1 The parameter construct the first group of factors used in LENC correction in blue color channels.
0x9A	LENC BLUE B1	0xC2	RW	Bit[7:0]: blu_b1 The parameter construct the second group of factors used in LENC correction in blue color channels.
0x9B	LENC BLUE AB2	0x87	RW	Bit[7:4]: blu_b2 The parameter construct the second group of factors used in LENC correction in blue color channels. Bit[3:0]: blu_a2 The parameter construct the first group of factors used in LENC correction in blue color channels.
0x9C	GMA YST01	0x0E	RW	Bit[7:0]: YST1 Output value at input = 0x04
0x9D	GMA YST02	0x1A	RW	Bit[7:0]: YST2 Output value at input = 0x08
0x9E	GMA YST03	0x31	RW	Bit[7:0]: YST3 Output value at input = 0x10
0x9F	GMA YST04	0x5A	RW	Bit[7:0]: YST4 Output value at input = 0x20
0xA0	GMA YST05	0x69	RW	Bit[7:0]: YST5 Output value at input = 0x28
0xA1	GMA YST06	0x75	RW	Bit[7:0]: YST6 Output value at input = 0x30
0xA2	GMA YST07	0x7E	RW	Bit[7:0]: YST7 Output value at input = 0x38
0xA3	GMA YST08	0x88	RW	Bit[7:0]: YST8 Output value at input = 0x40
0xA4	GMA YST09	0x8F	RW	Bit[7:0]: YST9 Output value at input = 0x48

table 7-1 system control registers (sheet 19 of 25)

address	register name	default value	R/W	description
0xA5	GMA YST10	0x96	RW	Bit[7:0]: YST10 Output value at input = 0x50
0xA6	GMA YST11	0xA3	RW	Bit[7:0]: YST11 Output value at input = 0x60
0xA7	GMA YST12	0xAF	RW	Bit[7:0]: YST12 Output value at input = 0x70
0xA8	GMA YST13	0xC4	RW	Bit[7:0]: YST13 Output value at input = 0x90
0xA9	GMA YST14	0xD7	RW	Bit[7:0]: YST14 Output value at input = 0xB0
0xAA	GMA YST15	0xE8	RW	Bit[7:0]: YST15 Output value at input = 0xD0
0xAB	GMA YSLP	0x20	RW	Bit[7:0]: YSLP15 Slope in the range of (0xD1, 0xFF) Slope = (256 - YST15) x 4/3
0xAC	AWB CTRL0	0x6D	RW	Bit[7]: Advanced AWB setting Bit[6]: Simple AWB mode select 0: Advanced AWB mode 1: Simple AWB mode Bit[5:0]: Advanced AWB setting
0xAD~ 0xC2	AWB CTRL	–	–	Advanced AWB Parameters Contact your local OmniVision FAE for settings
0xC3~ 0xCA	WBC CTRL00~CA	–	RW	WBC Option Changing these values is not recommended
0xCB	CIP DNS THRESH MAN	0x08	RW	Bit[7:0]: Manual setting for denoise threshold
0xCC	CIP CTRL	0x04	RW	Bit[7]: Not used Bit[6]: Manual mode for sharpness 0: Auto mode 1: Manual mode Bit[5]: Manual mode for denoise 0: Auto mode 1: Manual mode Bit[4:0]: Manual setting for sharpness
0xCD	CIP EDGE THRESHOLD	0x06	RW	Bit[7:4]: Not used Bit[3:0]: Sharpness threshold
0xCE	CMX M1	0x41	RW	Bit[7:0]: Color matrix element 1 Coefficient of red to V
0xCF	CMX M2	0x3C	RW	Bit[7:0]: Color matrix element 2 Coefficient of green to V

table 7-1 system control registers (sheet 20 of 25)

address	register name	default value	R/W	description
0xD0	CMX M3	0x06	RW	Bit[7:0]: Color matrix element 3 Coefficient of blue to V
0xD1	CMX M4	0x17	RW	Bit[7:0]: Color matrix element 4 Coefficient of red to U
0xD2	CMX M5	0x3A	RW	Bit[7:0]: Color matrix element 5 Coefficient of green to U
0xD3	CMX M6	0x52	RW	Bit[7:0]: Color matrix element 6 Coefficient of blue to U
0xD4	CMX CTRL	0x5E	RW	Bit[6]: Color matrix doubler 0: Apply color matrix directly 1: Apply double of the color matrix Bit[5]: Sign bit for color matrix element 6 Bit[4]: Sign bit for color matrix element 5 Bit[3]: Sign bit for color matrix element 4 Bit[2]: Sign bit for color matrix element 3 Bit[1]: Sign bit for color matrix element 2 Bit[0]: Sign bit for color matrix element 1 (0: positive; 1: negative)
0xD5	SCALE SMTH CTRL	0x10	RW	Bit[7:6]: Not used Bit[5]: scale_size_restart When it is set, restart the smooth scale procedure if size setting is changed Bit[4]: scale_zoom_mode 0: Zoom in mode 1: Zoom out mode Bit[2:0]: scale_step_num To decide how many steps to do smooth scale. The larger the value is set, the slower the smooth scale moves
0xD6	NOT USED	–	–	Not Used
0xD7	SCALEH XSC MAN	0x00	RW	Bit[7:0]: xsc_man[7:0] Manual value of horizontal scale coefficient (see 0xD8[2:0] for xsc_man[10:8]) Down-scaling ratio = 0x200 / xsc_man[10:0]

table 7-1 system control registers (sheet 21 of 25)

address	register name	default value	R/W	description
0xD8	SCALEH CTRL	0x04	RW	Bit[7]: Horizontal scale option 0: Average mode 1: Skip mode Bit[6]: Horizontal scale mode 0: Auto mode 1: Manual mode Bit[5:4]: h_div_man Manual horizontal divider Down-scaling ratio =1 / 2^h_div_man (used for $1/2^n$ scaling ratio) Bit[3]: Horizontal scaling calculation option 0: Truncate 1: Rounding Bit[2:0]: xsc_man[10:8] Manual value of horizontal scale coefficient (see 0xD7[7:0] for xsc_man[7:0])
0xD9	YUV422 CTRL	0x00	RW	Bit[7:2]: Not used Bit[1]: v_first 0: Output line will be YUYV... 1: Output line will be YVYU... (It will affect definition of U/V in SDE. If it is set, all registers in SDE about U/V must be swapped.) Bit[0]: cnv_opt 0: Average mode 1: Drop mode

table 7-1 system control registers (sheet 22 of 25)

address	register name	default value	R/W	description
0xDA	SDE CTRL	0x00	RW	Bit[7]: Fixed Y enable When it is set, the output Y will be a fixed value. Bit[6]: Negative enable 0: Disable negative color effect 1: Enable negative color effect Bit[5]: Gray enable 0: Disable gray effect 1: Enable gray effect Bit[4]: Fixed V enable When it is set, the output V will be the value set in register sde_vreg(0xE0) Bit[3]: Fixed U enable When it is set, the output U will be the value set in register sde_ureg (0xDF) Bit[2]: Contrast enable 0: Disable contrast/ offset/brightness 1: Enable contrast/ offset/brightness Bit[1]: Saturation enable 0: Disable saturation effect 1: Enable saturation effect Bit[0]: Hue enable 0: Disable hue effect 1: Enable hue effect
0xDB	HUE_COS	0x80	RW	Bit[7:0]: Cosine value for hue effect HUE_COS = |cos value| * 0x80
0xDC	HUE_SIN	0x00	RW	Bit[7:0]: Sine value for hue effect HUE_SIN = |sin value| * 0x80
0xDD	USAT	0x40	RW	Bit[7:0]: U saturation Enhancement for U value in saturation effect $U = U_0$ x USAT / 0x40
0xDE	VSAT	0x40	RW	Bit[7:0]: V saturation Enhancement for V value in saturation effect $V = V_0$ x VSAT / 0x40
0xDF	UREG	0x80	RW	Bit[7:0]: Fixed U value U value for fixed U effect
0xE0	VREG	0x80	RW	Bit[7:0]: Fixed V value V value for fixed V effect
0xE1	YOFFSET	0x00	RW	Bit[7:0]: Y offset for contrast control or Y value for fixed Y effect

table 7-1 system control registers (sheet 23 of 25)

address	register name	default value	R/W	description
0xE2	YGAIN	0x20	RW	Bit[7:0]: Y gain for contrast control Gain = YGAIN / 0x20
0xE3	YBRIGHT	0x00	RW	Bit[7:0]: Brightness
0xE4	SGNSET	0x06	RW	Sign Bit for Hue and Brightness Bit[7:6]: Not used Bit[5]: Sign bit for **HUE_COS** (in V' equation) Bit[4]: Sign bit for **HUE_COS** (in U' equation) Bit[3]: Sign bit for **YBRIGHT** Bit[2]: Sign bit for **YOFFSET** Bit[1]: Sign bit for **HUE_SIN** (in V' equation) Bit[0]: Sign bit for **HUE_SIN** (in U' equation)
0xE5	SCALEV CTRL	0x0C	RW	Bit[7]: Vertical scale mode 0: Auto mode 1: Manual mode Bit[6:4]: Offset for skip mode Bit[3]: Vertical scale option 0: Average mode 1: Skip mode Bit[2]: Manual RAM mode setting Bit[1:0]: v_div Manual vertical divider Down-scaling ratio = 1 / 2^v_div
0xE6	VAP CTRL	0x10	RW	Bit[7:5]: Not used Bit[4]: Average mode 0: Summation 1: Average Bit[3:2]: Not used Bit[1]: Green channel sub-sample mode 0: Summation or average depending on bit[4] 1: Skip Bit[0]: Blue/red channel sub-sample mode 0: Summation or average depending on bit[4] 1: Skip

table 7-1 system control registers (sheet 24 of 25)

address	register name	default value	R/W	description
0xE7	FIFO CTRL	0x00	RW	BIt[7:6]: Not used Bit[5:4]: fifo_speed Speed for FIFO data output Bit[3]: fifo_valid_mode 0: HREF mode 1: Valid mode Bit[2]: fifo_man Manual mode for FIFO setting Bit[1:0]: fifo_opt Offset adjustment for FIFO delay
0xE8	FIFO DELAY	0x00	RW	Bit[7:0]: fifo_delay Manual setting for FIFO delay
0xE9 sub address: 0x38[3:0]=4'h0	YAVG BLK THRE	0x00	RW	Bit[7:0]: blk_thresh Threshold for blackness
0xE9 sub address: 0x38[3:0]=4'h1	YAVG BRT THRE	0x00	RW	Bit[7:0]: brt_thresh Threshold for brightness
0xE9 sub address: 0x38[3:0]=4'h2	YAVG HOFF L	0x00	RW	yavg_winofh Bit[7:0]: Horizontal offset for window cropping in YAVG
0xE9 sub address: 0x38[3:0]=4'h3	YAVG VOFF L	0x00	RW	yavg_winofv Bit[7:0]: Vertical offset for window cropping in YAVG
0xE9 sub address: 0x38[3:0]=4'h4	YAVG CTRL	0x00	RW	BIt[7:6]: Not used Bit[5]: yavg_win_man 0: Window will be the default window 1: Window will be the window set by the registers Bit[4]: yavg_winofv[8] See **YAVG VOFF L** (0xE9, 0x38[3:0] = 4'h2) Bit[3:2]: Not used Bit[1:0]: yavg_winofh[9:8] See **YAVG HOFF L** (0xE9, 0x38[3:0] = 4'h1)
0xE9 sub address: 0x38[3:0]=4'h5	YAVG HSIZE	0x00	RW	Bit[7]: Not used Bit[6:0]: yavg_winh Horizontal size of cropping window. It will be multiplied by 8 to be real size.

table 7-1 system control registers (sheet 25 of 25)

address	register name	default value	R/W	description
0xE9 sub address: 0x38[3:0]=4'h6	YAVG VSIZE	0x00	RW	Bit[7]: Not used Bit[6:0]: yavg_winv Vertical size of cropping window. It will be multiplied by 4 to be real size.
0xEA~ 0xEB	NOT USED	–	–	Not Used
0xEC	REGEC	0x00	RW	Bit[7]: BD50auto 0: Select banding filter for 50/60 Hz manually (**REGEC**[6] (**0xEC**)) 1: Select banding filter for 50/60 Hz by 50/60 auto detection Bit[6]: MBAND50 0: Select banding filter step for 60 Hz 1: Select banding filter step for 50 Hz Bit[5:0]: Control bits Changing these values is not recommended
0xED	NOT USED	–	–	Not Used
0xEE	REGEE	–	RW	Register for Group Latch Function
0xEF	OTP CTRL	–	RW	OTP Control Register 0x55: Read OTP memory 0xAA: Program OTP memory
0xF0~ 0xFF	OTP	–	RW	16 bytes of data to be programmed/read into/from OTP memory

8 electrical specifications

table 8-1 absolute maximum ratings

parameter		absolute maximum rating[a]
operating temperature range[b]		-30°C to +70°C
stable image temperature range[c]		0°C to +50°C
supply voltage (with respect to ground)	V_{DD-A}	4.5V
	V_{DD-IO}	4.5V
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
all input/output voltages (with respect to ground)		-0.3V to V_{DD-IO} + 1V
I/O current on any input or output pin		± 200 mA
peak solder temperature (10 second dwell time)		245°C

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

b. sensor functions but image quality may be noticeably different at temperatures outside of stable image range

c. image quality remains stable throughout this temperature range

table 8-2 DC characteristics (-30°C < T_A < 70°C)

symbol	parameter	min	typ	max	unit
supply					
V_{DD-A}	supply voltage (analog)	3.0	3.3	3.6	V
V_{DD-IO}	supply voltage (digital I/O)	1.7	1.8	3.47	V
I_{DD-A}	active (operating) current[a]		23	35	mA
I_{DD-IO}			25	40	mA
$I_{DDS-SCCB}$[b]	standby current		20	50	µA
$I_{DDS-PWDN}$			20	50	µA
digital inputs (typical conditions: AVDD = 3.3V, DOVDD = 1.8V)					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.26			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs					
V_{IL}[c]	SIOC and SIOD	-0.5	0	0.54	V
V_{IH}[c]	SIOC and SIOD	1.26	1.8	2.3	V

a. test conditions are: tested at room temperature, V_{DD-A} = 3.3V, V_{DD-IO} = 1.8V, use internal DVDD regulator, and output VGA @ 60fps

b. with clock stopped

c. based on DOVDD = 1.8V.

table 8-3 AC characteristics (T_A = 25°C, V_{DD-A} = 3.3V, V_{DD-IO} = 1.8V)

symbol	parameter	min	typ	max	unit
ADC parameters					
B	analog bandwidth		12		MHz
DLE	DC differential linearity error		< 0.5		LSB
ILE	DC integral linearity error		< 0.5		LSB
	settling time for software reset			<1	ms
	settling time for resolution mode change			<1	ms
	settling time for register setting			<300	ms

table 8-4 timing characteristics

symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{OSC}	frequency (XVCLK1)	6	24	27	MHz
t_r, t_f	clock input rise/fall time			5 (10[a])	ns

a. if using the internal PLL

figure 8-1 SCCB interface timing

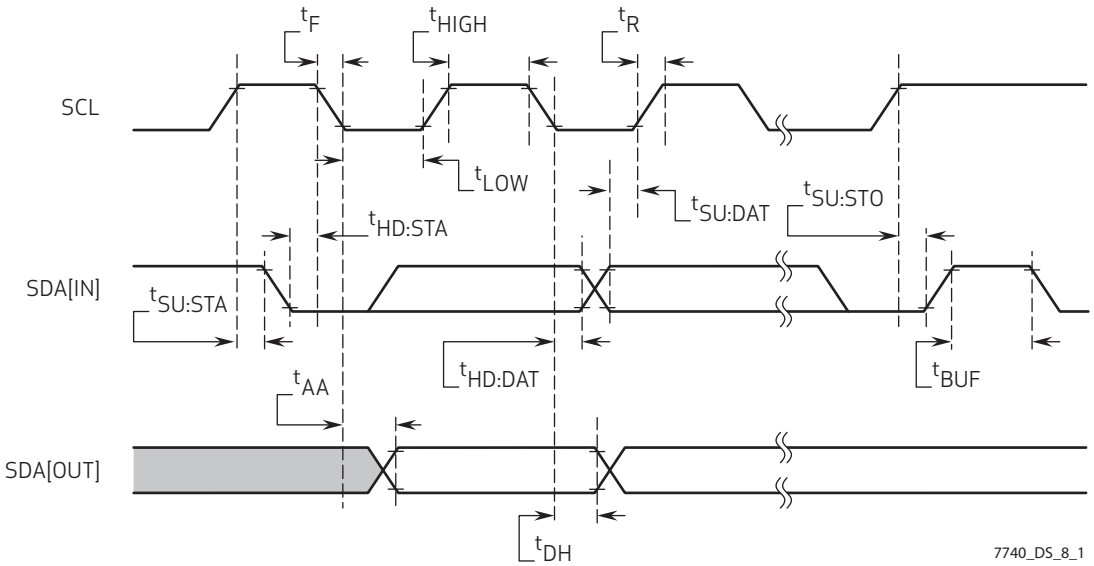


table 8-5 SCCB interface timing specifications[a]

symbol	parameter	min	typ	max	unit
f_{SCL}	clock frequency			400[b]	KHz
t_{LOW}	clock low period	1.3			µs
t_{HIGH}	clock high period	0.6			µs
t_{AA}	SCL low to data out valid	0.1		0.9	µs
t_{BUF}	bus free time before new start	1.3			µs
$t_{HD:STA}$	start condition hold time	0.6			µs
$t_{SU:STA}$	start condition setup time	1.85			µs
$t_{HD:DAT}$	data in hold time	0			µs
$t_{SU:DAT}$	data in setup time	0.1			µs
$t_{SU:STO}$	stop condition setup time	0.6			µs
t_R, t_F	SCCB rise/fall times			0.3	µs
t_{DH}	data out hold time	0.05			µs

a. SCCB timing is based on 400KHz mode

b. SCCB maximum speed is 400KHz when sensor master input clock (XVCLK) is greater than or equal to 13MHz. When XVCLK is less than 13MHz, the maximum SCCB speed is less than 400KHz (approximately XVCLK/32.5)

9 mechanical specifications

9.1 physical specifications

figure 9-1 package specifications

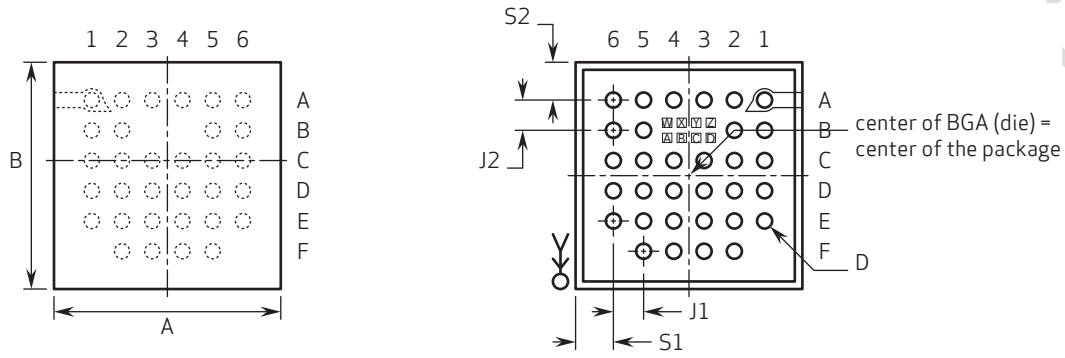


table 9-1 package dimensions (sheet 1 of 2)

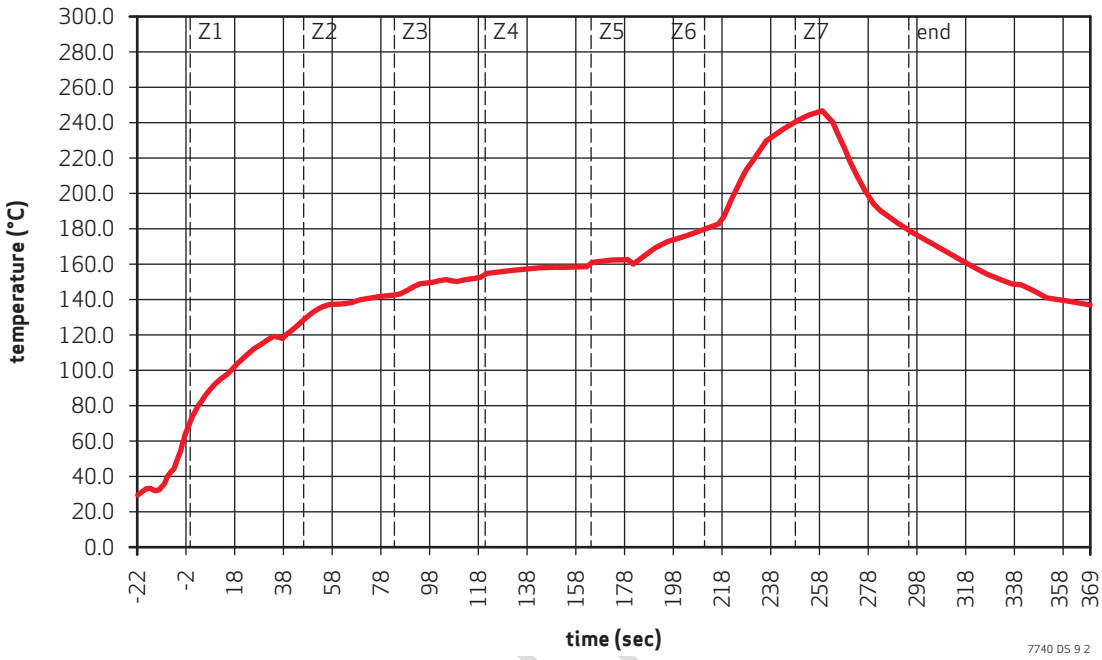
parameter	symbol	min	typ	max	unit
package body dimension x	A	4160	4185	4210	µm
package body dimension y	B	4320	4345	4370	µm
package height	C	720	780	840	µm
ball height	C1	130	160	190	µm
package body thickness	C2	575	620	665	µm
thickness of glass surface to wafer	C3	425	445	465	µm
ball diameter	D	270	300	330	µm
total pin count	N		32		

table 9-1 package dimensions (sheet 2 of 2)

parameter	symbol	min	typ	max	unit
pin count x-axis	N1		6		
pin count y-axis	N2		6		
pins pitch x-axis	J1		610		µm
pins pitch y-axis	J2		630		µm
edge-to-pin center distance analog x	S1	538	568	598	µm
edge-to-pin center distance analog y	S2	568	598	628	µm

9.2 IR reflow specifications

figure 9-2 IR reflow ramp rate requirements



note

The OV7740 uses a lead free package.

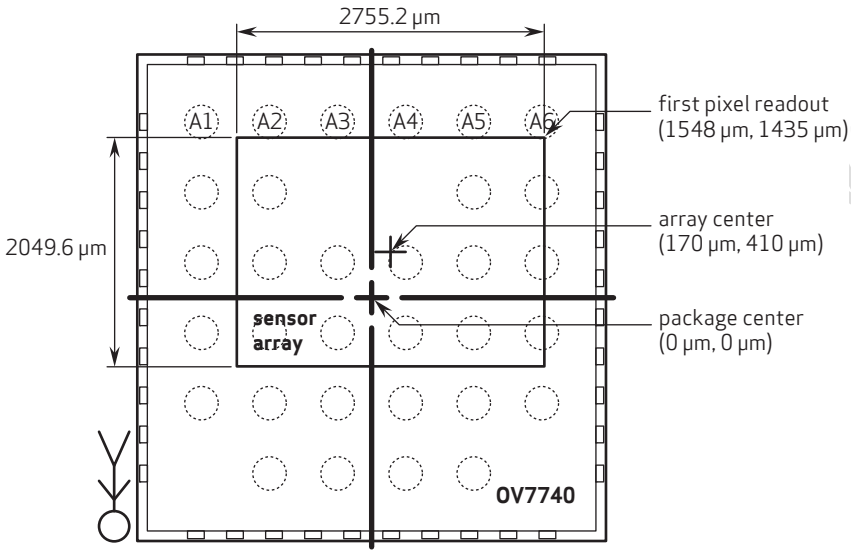
table 9-2 reflow conditions

condition	exposure
average ramp-up rate (30°C to 217°C)	less than 3°C per second
> 100°C	between 330 - 600 seconds
> 150°C	at least 210 seconds
> 217°C	at least 30 seconds (30 ~ 120 seconds)
peak temperature	245°C
cool-down rate (peak to 50°C)	less than 6°C per second
time from 30°C to 245°C	no greater than 390 seconds

10 optical specifications

10.1 sensor array center

figure 10-1 sensor array center



top view

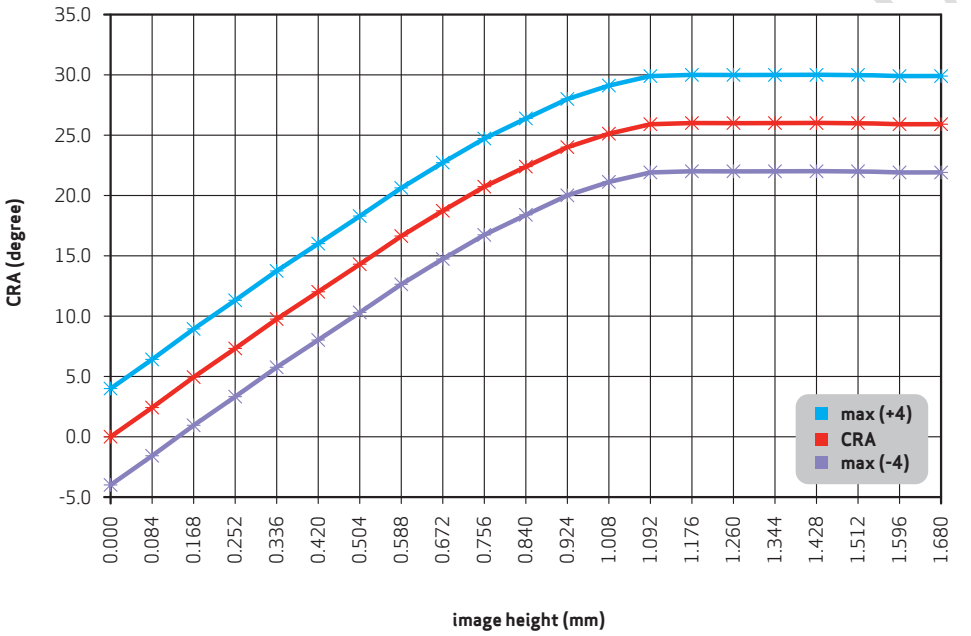
note 1 this drawing is not to scale and is for reference only.

note 2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pins A1 to A6 oriented down on the PCB.

7740_DS_CSP_10_1

10.2 lens chief ray angle (CRA)

figure 10-2 chief ray angle (CRA)



7740_DS_10_2

table 10-1 CRA versus image height plot (sheet 1 of 2)

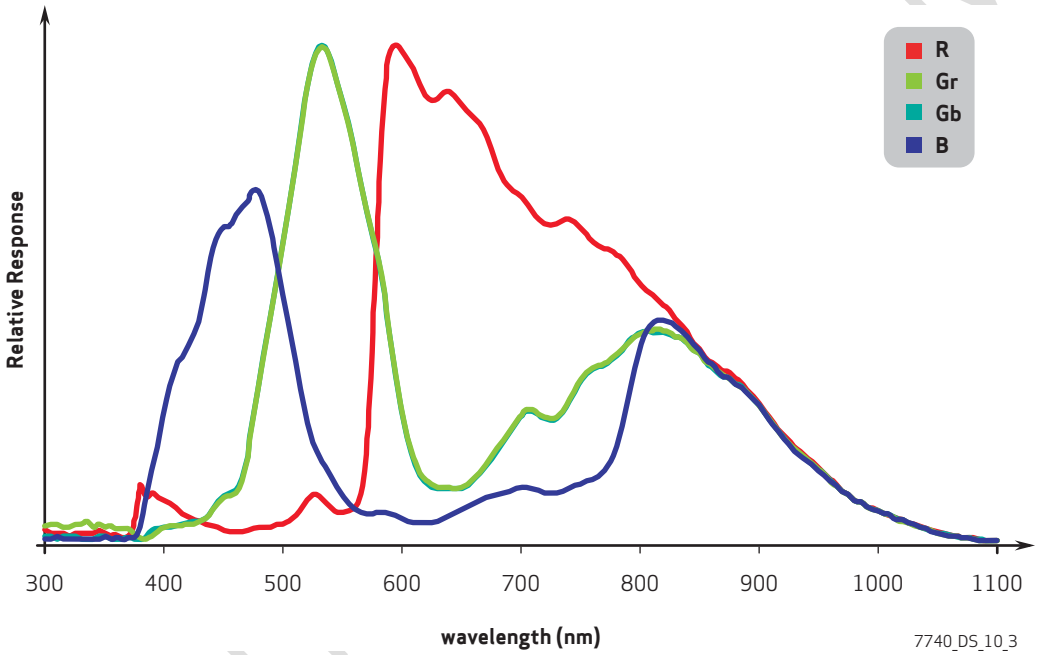
field (%)	image height (mm)	CRA (degrees)
0	0.000	0.0
0.05	0.084	2.4
0.1	0.168	4.9
0.15	0.252	7.3
0.2	0.336	9.7
0.25	0.420	12.0
0.3	0.504	14.3
0.35	0.588	16.6
0.4	0.672	18.7
0.45	0.756	20.7

table 10-1 CRA versus image height plot (sheet 2 of 2)

field (%)	image height (mm)	CRA (degrees)
0.5	0.840	22.4
0.55	0.924	24.0
0.6	1.008	25.1
0.65	1.092	25.9
0.7	1.176	26.0
0.75	1.260	26.0
0.8	1.344	26.0
0.85	1.428	26.0
0.9	1.512	26.0
0.95	1.596	25.9
1	1.680	25.9

10.3 spectrum response

figure 10-3 spectrum response curve



revision history

version 1.0 04.18.2008

- initial release

version 1.1 05.09.2008

- in chapter 4, section 4-2 test pattern updated the description from “For testing purposes, the OV7740 offers one type of test pattern, color bar.” changed to “For testing purposes, the OV7740 offers one type pf test pattern: color bar. There are 4 modes of the color bar (see figure 4-2). The modes of the color bar can be set with the register 0x84[5:4](base address: 0x38[3:0] = 4'h8). In each mode the color bar can be moved from top to bottom if the bar moving function is enabled by setting signal(0x84[4]: base address: 0x38[3:0] = 4'h7) is 1. The moving step can be configured by setting the register 0x84[3:0](base address: 0x38[3:0] = 4'h8) (see table 4-2).”
- in chapter 4, section 4-2 replaced the test pattern figure and updated table 4-2
- in chapter 4, added the following sentence to 4.3.2.3 YAVG “Auto mode only supports non-scaling and non-subsampling image.”
- in chapter 4, modified figure 4-4 “valid pixel size (for VGA, HW = 640, VTS = 480)” changed to “valid pixel size (for VGA, HW = 640, VH = 480)”
- in chapter 4, modified table 4-5 title from “AEC/AGC algorithms” changed to “YAVG window registers”
- in chapter 4, updated section 4.4.1.2 banding mode ON with AEC; from “The band steps for 50Hz and 60Hz light sources can be set in registers 0x49~0x4A.When auto banding is ON, if the next integration time is less than the minimum band step, banding will automatically turn OFF. It will turn ON again when the next integration time becomes larger than the minimum band. If auto banding is disabled, the minimum integration time is one minimal band. Auto banding can be set in register 0x13[5].”
  changed to
  “The band steps for 50Hz and 60Hz light sources can be set in registers 0x50~0x52. When auto banding is ON, if the next integration time is less than the minimum band step, banding will automatically turn OFF. It will turn ON again when the next integration time becomes larger than the minimum band. If auto banding is disabled, the minimum integration time is one minimal band. Auto banding can be set in register 0x13[4].”
- in chapter 4, updated section 4.4.1.4 VAEC from “The OV7740 supports long integration time such as 1 frame, 2 frames, 3 frames and 7 frames. This is achieved by slowing down original frame rate and waiting for exposure. VAEC ceiling can be set in register 0x03[7:5]. VAEC can be disabled by setting register 0x0E[3] to 0.”
  changed to:
  “The OV7740 supports long integration time such as 1 frame, 2 frames, 3 frames and 7 frames. This is achieved by slowing down original frame rate and waiting for exposure. VAEC ceiling can be set in register 0x15[6:4]. VAEC can be disabled by setting register 0x15[7] to 0.”
- in chapter 4, updated table 4-6 title from “AGC registers” changed to “AEC and banding filter register”

- in chapter 4, updated table 4-6 from:

function	register	description
LAEC ON/OFF	0x13[3]	LAEC ON/OFF select 0: OFF 1: ON
banding ON/OFF	0x13[5]	banding ON/OFF 0: OFF 1: ON
VAEC ON/OFF (add frame)	0x15[7]	VAEC ON/OFF select 0: OFF 1: ON
auto banding	0x13[4]	auto banding select 0: OFF 1: ON
VAEC ceiling (max integration time)	0x15[6:4]	VAEC ceiling 001: 1 frame 010: 2 frames 011: 3 frames 1xx: 7 frames
max_band	0x20[5:0]	max band step for in terms of row exposure
banding step	0x50~0x52	0x52[7:6]=BD60st[9:8]; 0x51[7:0] = BD60st[7:0] 0x52[5:4]=BD50st[9:8]; 0x50[7:0] = BD50st[7:0]

changed to:

function	register	description
LAEC ON/OFF	0x13[3]	LAEC ON/OFF select 0: OFF 1: ON
banding ON/OFF	0x13[5]	banding ON/OFF 0: OFF 1: ON
VAEC ON/OFF (add frame)	0x15[7]	VAEC ON/OFF select 0: OFF 1: ON
auto banding	0x13[4]	auto banding select 0: OFF 1: ON
VAEC ceiling (max integration time)	0x15[6:4]	VAEC ceiling 001: 1 frame 010: 2 frames 011: 3 frames 1xx: 7 frames

function	register	description
banding step	0x50~0x52	0x52[7:6]=BD60st[9:8]; 0x51[7:0] = BD60st[7:0] 0x52[5:4]=BD50st[9:8]; 0x50[7:0] = BD50st[7:0]
maximum banding step	0x21	Bit[7:4]: for 50 Hz Bit[3:0]: for 60 Hz

- in chapter 4, updated Table 4-8 digital gain control functions description from:

function	register	description
DGAIN	0x15[1:0]	target 00: Reserved 11: data*4 - target*3

changed to:

function	register	description
DGAIN	0x15[1:0]	00: 1x digital gain 01 or 10: 2x digital gain 11: 4x digital gain

- in chapter 5, updated table 5-1 DSP registers address 0x83 description from

address	register name	default value	R/W	description
0x83	DSP CTRL03	1'b0	RW	Bit[5]: Video 0: disable video off 1: enable video off

changed to:

address	register name	default value	R/W	description
0x83	DSP CTRL03	1'b0	RW	Bit[5]: Video switch 0: video start 1: video stop

- in chapter 5, deleted section 5.3, S2P
- in chapter 5, section 5.7 auto white balance (AWB); removed from the section description “The module judges whether the color temperature is Day, A or CWF. AWB R/G/B Gain are decided by white pixel G/B and G/R value of current color temperature. AWB R/G/B gain also depends previous awb r/g/b gain.”

- in chapter 5, section 5.8 - white black pixel cancellation; removed from the section description “The new WBC algorithm use some modes to select if the vertical line of bad pixels should be removed or enable the module remove the consecutive bad pixels in same or different channel.”
- in chapter 5, section 5.9 - CIP; added to the section description “Setting the register 0xCC Bit[6:5] to 0 will enable auto mode.”
- in chapter 5, section 5.12 - SCALE_H; removed from the section description “whether its enable-register is 1 or not.”
- in chapter 5, deleted section 5.17 - FIFO
- in chapter 6, updated section 6.1.2 - HREF mode from
“HREF mode is the default mode of the DVP (see figure 6-1). Each DVP_VSYNC indicates the starting of a new frame. The OV7740 supports three types of DVP_VSYNC signals (vsync_old, vsync_new, and vsync3) as shown in figure 6-2). DVP_VSYNC, DVP_HREF, and DVP_PCLK can be reversed using the register settings.”

  changed to

  “HREF mode is the default mode of the DVP. Each DVP_VSYNC indicates the starting of a new frame.
- in chapter 6, deleted figure 6-1 DVP timing, figure 6-2 VSYNC timing diagram and section 6.1.3 HSYNC mode

version 1.2 07.18.2008

- on the cover page, changed the lens size from 1/13" changed to 1/5"
- under the ordering information, changed the order number from OV7740-CSP changed to OV07740-A32A
- under key specifications, added package dimensions: 4185µm x 4345µm
- in chapter 4, Table 4-7 BLC control functions; replaced the register values of R offset, B offset, Gr offset and Gb offset from

R offset	0x6A[3:2], 0x6D[7:0]	BLC offset for R channel
B offset	0x6A[1:0], 0x6E[7:0]	BLC offset for B channel
Gr offset	0x6A[7:6], 0x6B[7:0]	BLC offset for Gr channel
Gb offset	0x6A[5:4], 0x6C[7:0]	BLC offset for Gb channel

to

Gr offset	0x6E[7:6], 0x6A[7:0]	BLC offset for Gr channel
Gb offset	0x6E[5:4], 0x6B[7:0]	BLC offset for Gb channel
R offset	0x6E[3:2], 0x6C[7:0]	BLC offset for R channel
B offset	0x6E[1:0], 0x6D[7:0]	BLC offset for B channel

- under chapter 7, changed from register 0x13 Bit[4]: Simple histogram changed to register 0x13 Bit[4]: Enable AEC below banding value

- under chapter 7, changed from register 0x16 Reserved changed to 0x16 Bit[7:6]: Reserved, Bit[5]: Sensor vertical output size 1LSB, Bit[4:3]: Sensor horizontal output size 2LSB, Bit[2]: Sensor vertical output start point 1LSB, Bit[1]: Sensor horizontal output start point 2LSB
- under chapter 7, changed register (17, 18, 19) from

Sensor Horizontal Output Start Point MSBs (LSBs in REG16 Bit[1:0])
Sensor Horizontal Output size MSBs (LSBs in REG16 Bit[4:3])
Sensor Vertical Output Start Point MSBs (LSBs in REG16 Bit[2])

changed to:

Sensor Horizontal Output Start Point 8 MSBs (LSBs in REG16 Bit[1:0])
Sensor Horizontal Output size 8 MSBs (LSBs in REG16 Bit[4:3])
Sensor Vertical Output Start Point 8 MSBs (LSBs in REG16 Bit[2])

- under chapter 7, updated register (0x31, 0x32) from:

0x31	0xA0	RW	DSP Output Total Column Number in One Frame
0x32	0xF0	RW	DSP Output Total Line Number in One Frame

changed to:

0x31	HOUTSIZE	0xA0	RW	DSP H output size 8MSB H output size = {Houtsize [7:0] (0x31), REG 34 [2:1] (0x34)}
0x32	VOUTSIZE	0xF0	RW	DSP V output size 8MSB H output size = {Houtsize [7:0] (0x32), REG 34 [0] (0x34)}

- under chapter 7, added register 0x34

0x34	REG34	0x00	RW	Bit[7:3]: Reserved Bit[2]: DSP H output size 2 LSB Bit[0]: DSP V output size 2 LSB

- under chapter 7, updated the following from:

0x84 sub address: 0x38[3:0]=4'h2	AWB_OFF_MAN	0x00	RW	awb_off_man Manual offset for AWB
0x84 sub address: 0x38[3:0]=4'h3	GMA_OFF_MAN	0x00	RW	gma_off_man Manual offset for LENC
0x84 sub address: 0x38[3:0]=4'h4	CMX_OFF_MAN	0x00	RW	cmx_off_man Manual offset for LENC
0x84 sub address: 0x38[3:0]=4'h5	ISP_ROREG _ADDR	0x00	R	isp_roreg_address Read-only registers' address
0x84 sub address: 0x38[3:0]=4'h6	PRE_CTRL0	0x00	RW	Bit[7:5]: Reserved Bit[4]: bar_move When it is set, the color bar is moving color bar. Bit[3]: Reserved Bit[2]: rblue_inv When it is set, the RBlue signal will be inversed Bit[1]: bar_en 0: DSP PRE output normal data 1: DSP PRE output color bar Bit[0]: sht_neg 0: Latch data at rising clock edge 1: Latch data at falling clock edge
0x84 sub address: 0x38[3:0]=4'h7	PRE_CTRL1	0x00	RW	Bit[7:6]: Reserved Bit[5:4]: bar_style Style of the output color bar Bit[3:0]: bar_step Step of the output color bar

changed to:

0x84 sub address: 0x38[3:0]=4'h3	AWB OFF MAN	0x00	RW	awb_off_man Manual offset for AWB
0x84 sub address: 0x38[3:0]=4'h4	GMA OFF MAN	0x00	RW	gma_off_man Manual offset for GMA
0x84 sub address: 0x38[3:0]=4'h5	CMX OFF MAN	0x00	RW	cmx_off_man Manual offset for CMX
0x84 sub address: 0x38[3:0]=4'h6	ROREG ADDR	0x00	R	isp_roreg_address Read-only registers' address
0x84 sub address: 0x38[3:0]=4'h7	PRE CTRL0	0x00	RW	Bit[7:5]: Reserved Bit[4]: bar_move When it is set, the color bar is moving color bar. Bit[3]: Reserved Bit[2]: rblue_inv When it is set, the RBlue signal will be inversed Bit[1]: bar_en 0: DSP PRE output normal data 1: DSP PRE output color bar Bit[0]: sht_neg 0: Latch data at rising clock edge 1: Latch data at falling clock edge
0x84 sub address: 0x38[3:0]=4'h8	PRE CTRL1	0x00	RW	Bit[7:6]: Reserved Bit[5:4]: bar_style Style of the output color bar Bit[3:0]: bar_step Step of the output color bar

- in chapter 9, updated package dimension for package height and package body thickness from:

package height	C	825	885	945	µm
package body thickness	C2	680	725	770	µm

changed to:

package height	C	720	780	840	µm
package body thickness	C2	575	620	665	µm

- under chapter 8, updated table 8-1 with a new absolute maximum ratings table
- in chapter 10, updated the dimensions on the sensor array center

version 1.21 **07.29.2008**

- updated figure 9-1 with new diagram addressing the cover glass thickness

version 1.3 **03.17.2009**

- in key specifications section on page iii, changed power requirements for active to 120 mW (see table 8-2 for test conditions) and 100 µW (see table 2-2 for test conditions) for standby
- in key specifications section on page iii, changed specification for lens chief ray angle to 25°
- in key specifications section on page iii, changed specification for S/N ratio to 38 dB
- in key specifications section on page iii, changed specification for dynamic range to 71 dB
- in key specifications section on page iii, changed specification for sensitivity to 6.0 V/(Lux · sec)
- in key specifications section on page iii, changed specification for shutter to "rolling shutter"
- in key specifications section on page iii, changed specification for well capacity to 13 Ke^-
- in key specifications section on page iii, changed specification for dark current to 30 mV/sec @ 60°C
- in key specifications section on page iii, changed specification for fixed pattern noise to 1% $V_{PEAK-TO-PEAK}$
- on page 1-2, changed pin type of pin F3 (DGND) from "I/O" to "ground"
- on page 1-2, changed pin type of pin F4 (DVDD) from "I/O" to "power"
- in table 1-1, removed rows for pins B3, B4, F1, and F6
- in table 2-1, changed description of HREF IO control from 0x54[2] to 0x54[4], description of VSYNC IO control from "0x54[1] to 0x54[3], and description of PCLK IO control from 0x54[0] to 0x54[2]
- on page 2-5, added subsection 2.6, group register write and subsection 2.8, reset and moved standby and sleep to subsection 2.9
- on page 3-1, changed figure 3-1 by shifting row 0 so that it displays B Gb B Gb B Gb ... instead of Gr R Gr R Gr R ...

- on page 3-1, changed figure 3-1 by replacing "line zero" with "dummy line"
- on page 4-1, deleted the end of the first paragraph starting from "... the read-out sequence will be adjusted automatically ..." and replaced it with "... the HREF starting point needs to be adjusted, then the ISP block can do color interpolation correctly. In flip mode, the read-out sequence will be adjusted automatically."
- in table 4-1 on page 4-1, added table footnote a, when using the mirror function, the start point of HREF, {AHSTART[7:0], REG16[1:0] (0x16)}, must be adjusted to mirror function in first row
- in table 4-3, added "digital gain" and "analog gain" to description of AGC (gain) function on fourth row
- in table 4-3, added row for manual LAEC enable
- on page 4-3, removed paragraph after table 4-3
- on page 4-4, changed description of step size and t_{STEP} in subsection 4.3.2.1 and subsection 4.3.2.2
- in figure 4-5, corrected figure by changing "ACE" to "AEC" and "AF<2:0>" to "0x15[6:4]"
- added subsection 4.4.1.2, manual LAEC
- in the last sentence of subsection 4.4.1.3, changed from "Auto banding can be set in register 0x13[4]" to "Auto banding can be set in register 0x13[5]"
- in table 4-5, changed register for maximum banding step function from "0x21" to "{0x20, 0x21} and chnaged description to {0x20[7], 0x21[7:4]}: for 50 Hz and {0x20[6], 0x21[3:0]}: for 60 Hz"
- deleted "EVEN ODD" from title of section 4.6
- in table 4-6, changed description of BLC always ON function and MBLC function
- in section 5.1, in the first sentence, replaced "includes:" with "is to integrate all sub-modules. The ISP should always be enabled." and deleted two bullet items that followed
- in table 5-1, removed second and third rows
- in table 5-2, changed title from "DSP top registers" to "DSP pre registers"
- changed title of section 5.3 to gain_adaptive control
- changed title of table 5-4 to gain_adaptive control registers
- in table 5-4, removed first row
- in table 5-4, changed "Range from 0 to 639" to "Range from 0 to 479" in description of registers 0x8B, 0x91, and 0x97
- in table 5-5, removed first row
- in table 5-5, changed description of register 0x84 sub address: 0x38[3:0]=4'h4 from "Manual offset for LENC" to "Manual offset for gamma"
- in table 5-5, added formula to description of register 0xAB
- in table 5-9, changed description of register 0x84 sub address: 0x38[3:0]=4'h5 from "Manual offset for LENC" to "Manual offset for CMX"
- in section 5.10, added register and cross-reference, "0xE5", in image scaler paragraph
- in section 5.10, replaced "1/4" with "1/2" and added " in vertical divider and ISP will automatically set the 1/1.665 ratio" at end of image scaler paragraph.
- removed section 5.12, YUV444TO422
- removed section 5.16, 16-zone luminance average (YAVG)
- in section 6.1.3, replaced section content and removed figure 6-1
- in table 7-1, added gain formula to register 0x00 description
- in table 7-1, changed R/W type for registers 0x05, 0x06 and 0x07 from "RW" to "R"

- in table 7-1, changed description of register bits 0x0E[1:0] from Reserved to Output driving capability
- in table 7-1, changed description of register bits 0x11[5:0] to "Clock divider, sysclk = XVCLK1 * PLLDiv / [(CLK[5:0] +1) * 2 * PreDiv]"
- in table 7-1, changed description of register bit 0x13[3] to "LAEC ON/OFF select"
- in table 7-1, added description of 000, 001, 010, 011, and 1xx to description of register bits 0x15[6:4]
- in table 7-1, changed description of register bits 0x15[3:2] from Reserved to "Night mode triggering point"
- in table 7-1, changed RW type of register 0x2F from "RW" to "R"
- in table 7-1, changed name, default value, RW type, and description of register 0x33 to "HVSIZEOFF", "0x00", "RW", and "Bit[7:4]: H size offset" and "Bit[3:0]: V size offset", respectively
- in table 7-1, added description of registers 0x54 and 0x55 (previously Reserved)
- in table 7-1, added description of registers 0x5A and 0x5B
- in table 7-1, changed RW type of register 0x63 from "RW" to "R"
- in table 7-1, changed "Range from 0 to 639" to "Range from 0 to 479" in description of registers 0x8B, 0x91, and 0x97
- in table 8-1, changed stable image temperature range to "0°C to +50°C"
- in table 8-2, changed typ and max values for active (operating) current (I_{DD-A}) from "25" and "TBD" to "23" and "35," respectively and removed min value
- in table 8-2, changed typ and max values for active (operating) current (I_{DD-IO}) from "25" and "TBD" to "25" and "40," respectively and removed min value
- in table 8-2, changed max value for standby current ($I_{DD-SCCB}$) from "TBD" to "50" and removed min and typ values
- in table 8-2, changed unit for standby current ($I_{DD-SCCB}$) from "mA" to "µA"
- in table 8-2, changed max value for standby current ($I_{DD-PWDN}$) from "TBD" to "50" and removed min and typ values
- in table 8-2, changed row title from "digital inputs (typical conditions: AVDD = 2.8V, DOVDD =1.8V)" to "digital inputs (typical conditions: AVDD = 3.3V, DOVDD =1.8V)"
- in table 8-2, changed max for input voltage LOW (V_{IL}) from TBD to 0.54 and deleted 0.8 from typ column
- in table 8-2, changed min for input voltage HIGH (V_{IH}) from TBD to 1.26 and deleted 1.0 from typ column
- in table 8-2, removed typ values for output voltage HIGH (V_{OH}) and output voltage LOW (V_{OL})
- in table 8-2, added footnote a to active (operating) current, added footnote b to IDDS-SCCB, and changed previous footnote a to footnote c
- on page 8-4, added figure 8-1 and table 8-5
- on page 10-1, changed figure 10-1 by replacing sensor array dimension values from "2050" and "1756" to "2049.6" and "2755.2"
- added section 10.3

version 1.4 04.20.2009

- in key specifications on page iii, changed specifications for analog power supply to 3.3V ± 3%
- removed subsection 4.2, sensor test pattern
- changed title of subsection 5.2 to "test pattern" and modified first sentence of section 5.2
- changed description of register bit 0x0C[0] to "Not used"
- in table 8-2, changed min and max specifications of analog supply voltage (V_{DD-A}) to 3.20 and 3.40, respectively

version 1.5 05.06.2009

- in key specifications on page iii, changed analog power supply specification to 3.0 ~ 3.6V
- in table 4-7, added ", k = {0x5A}/16 to description of slope, k
- in table 7-1, changed description of register bits 0x88[3:2] to:
  00: K = 1/8
  01: K = 1/4
  10: K = 1/2
  11: K = 1
- in table 8-2, changed min and max for supply voltage (analog) to 3.0 and 3.6, respectively

version 1.51 05.19.2009

- in section 10, changed figure 10-3
- in table 7-1, defined address, register name, default value, R/W, and description for 0x4A

the clear advantage™

OmniVision Technologies, Inc.

UNITED STATES

4275 Burton Drive
Santa Clara, CA 95054

tel: + 1 408 567 3000

fax: + 1 408 567 3001

email: salesamerican@ovt.com

UNITED KINGDOM

Hampshire + 44 1256 744 610

FINLAND

Mouhijärvi + 358 3 341 1898

GERMANY

Munich +49 89 63 81 99 88

CHINA

Beijing + 86 10 6580 1690

Shanghai + 86 21 6105 5100

Shenzhen + 86 755 8384 9733

Hong Kong + 852 2403 4011

JAPAN

Tokyo + 81 3 5765 6321

KOREA

Seoul + 82 2 3478 2812

SINGAPORE + 65 6562 8250

TAIWAN

Taipei + 886 2 2657 9800 - ext.#100

website: **www.ovt.com**