

EMBEDDED SYSTEMS

CHAPTER - 8

IC TECHNOLOGY

8. IC Technology [3 Hrs.]

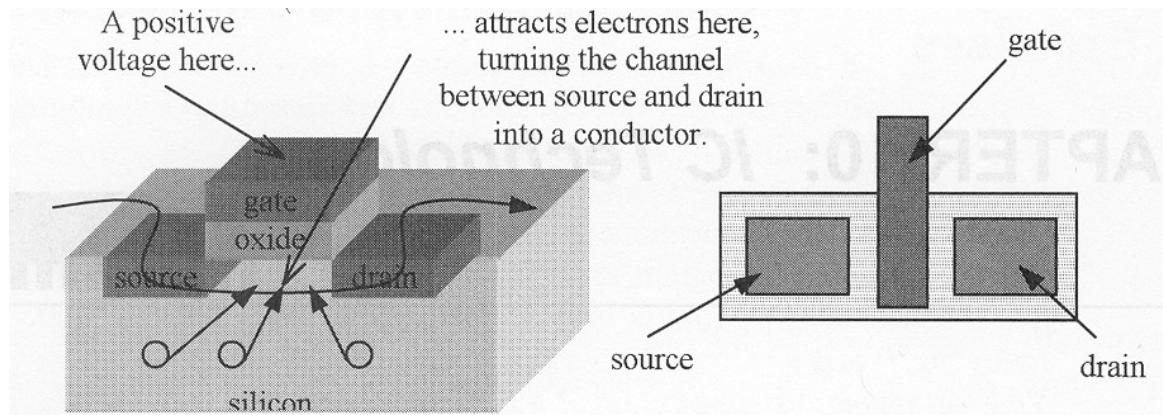
8.1 Full-Custom (VLSI) IC
Technology

8.2 Semi-Custom (ASIC) IC
Technology

8.3 Programming Logic Device
(PLD) IC Technology

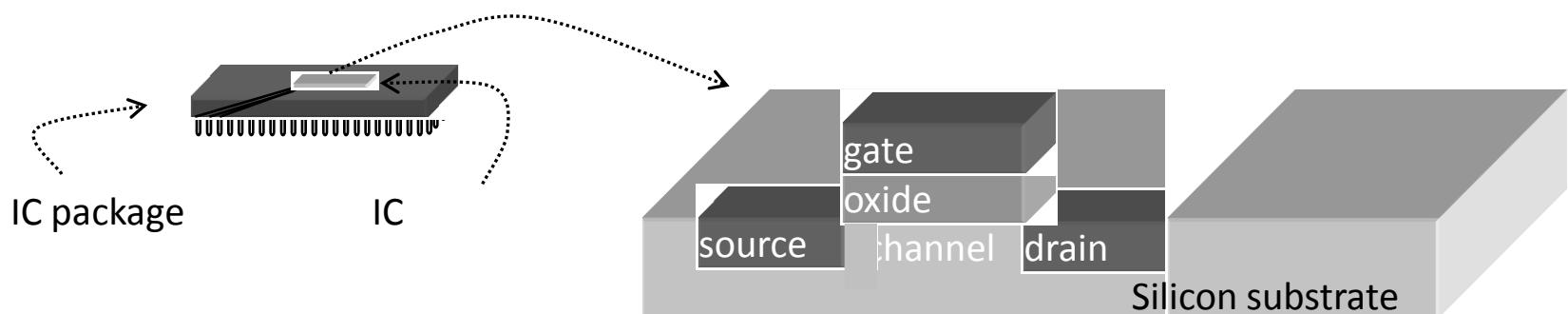
CMOS transistor

- Source, Drain
 - Diffusion area where electrons can flow
 - Can be connected to metal contacts
- Gate
 - Polysilicon area where control voltage is applied
- Oxide
 - Si O₂ Insulator so the gate voltage can't leak



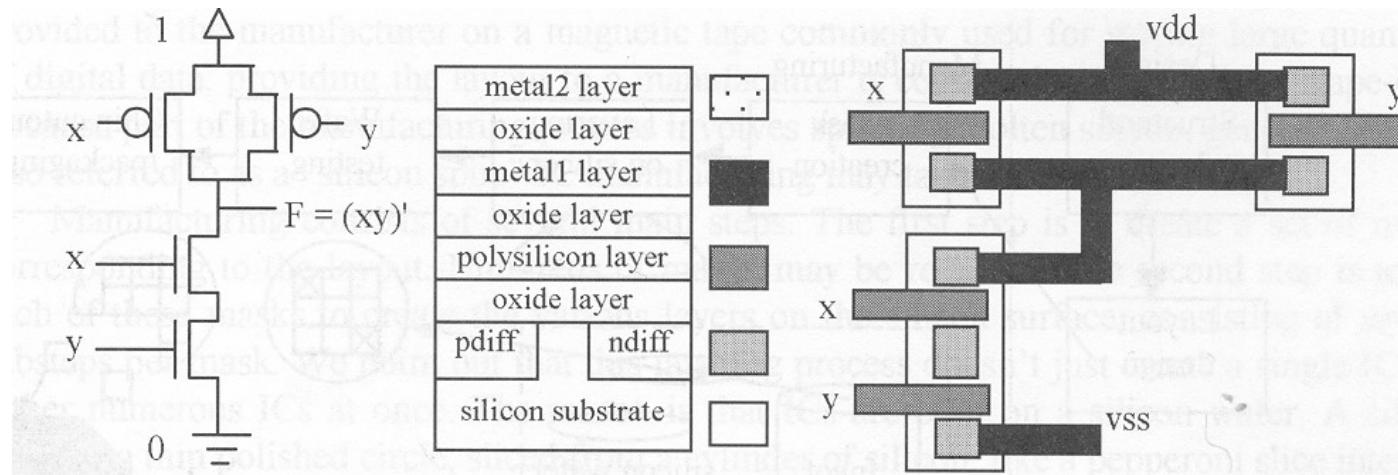
End of the Moore's Law?

- Every dimension of the MOSFET has to scale
 - (PMOS) Gate oxide has to scale down to
 - Increase gate capacitance
 - Reduce leakage current from S to D
 - Pinch off current from source to drain
 - Current gate oxide thickness is about 2.5-3nm
- That's about 25 atoms!!!



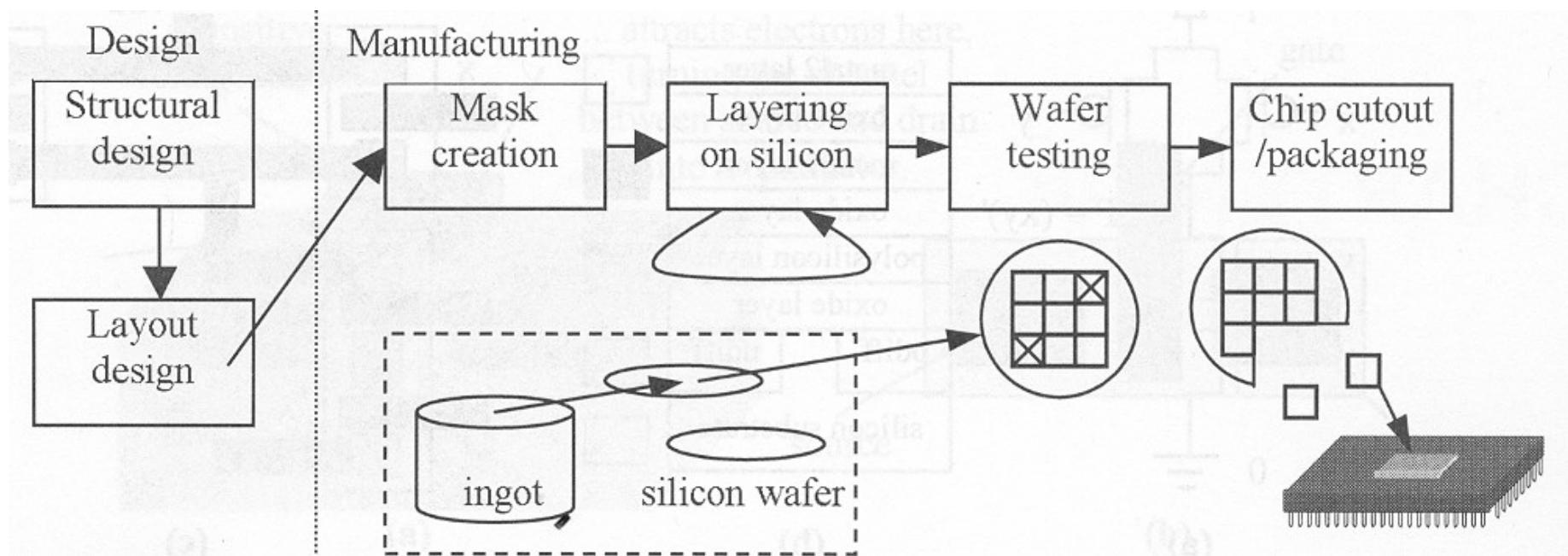
NAND

- Metal layers for routing (~10)
- PMOS don't like 0
- NMOS don't like 1
- A stick diagram form the basis for mask sets



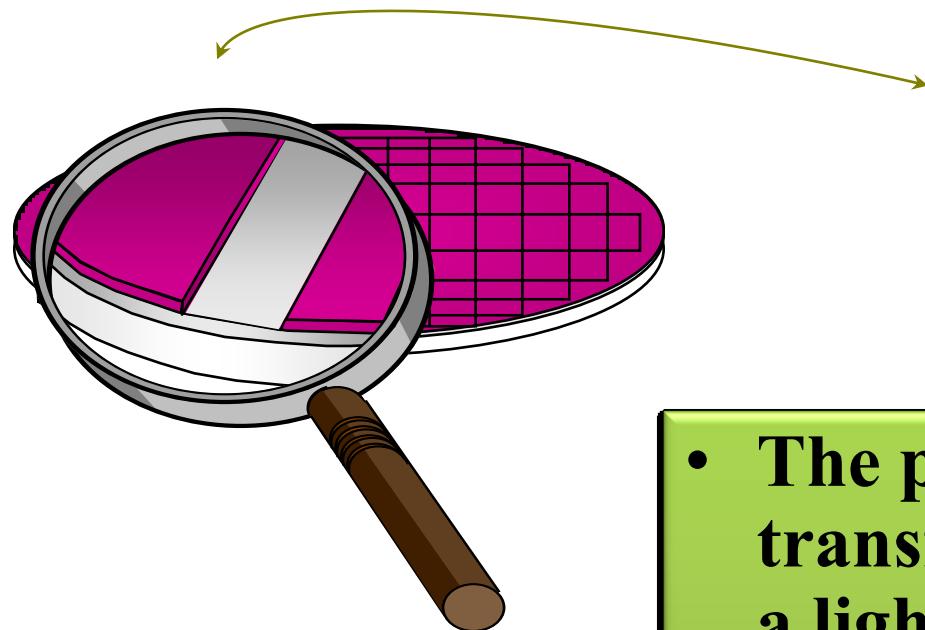
Silicon manufacturing steps

- Tape out
 - Send design to manufacturing
- Spin
 - One time through the manufacturing process
- Photolithography
 - Drawing patterns by using photoresist to form barriers for deposition

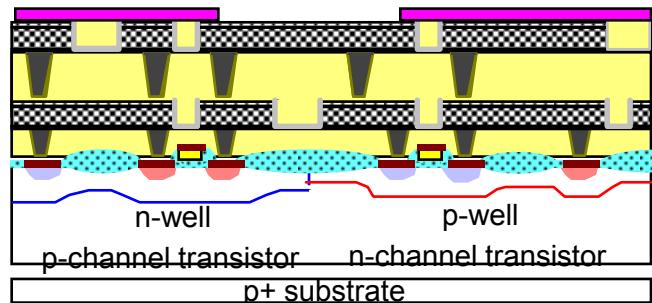


Introduction to Photolithography

Introduction to Photolithography



Transistor Layers



- The patterns are first transferred from the mask to a light sensitive materials (e.g. Si wafer, glass)
- Function of a barrier in the following process (oxidation, etch, ion implantation, etc.)

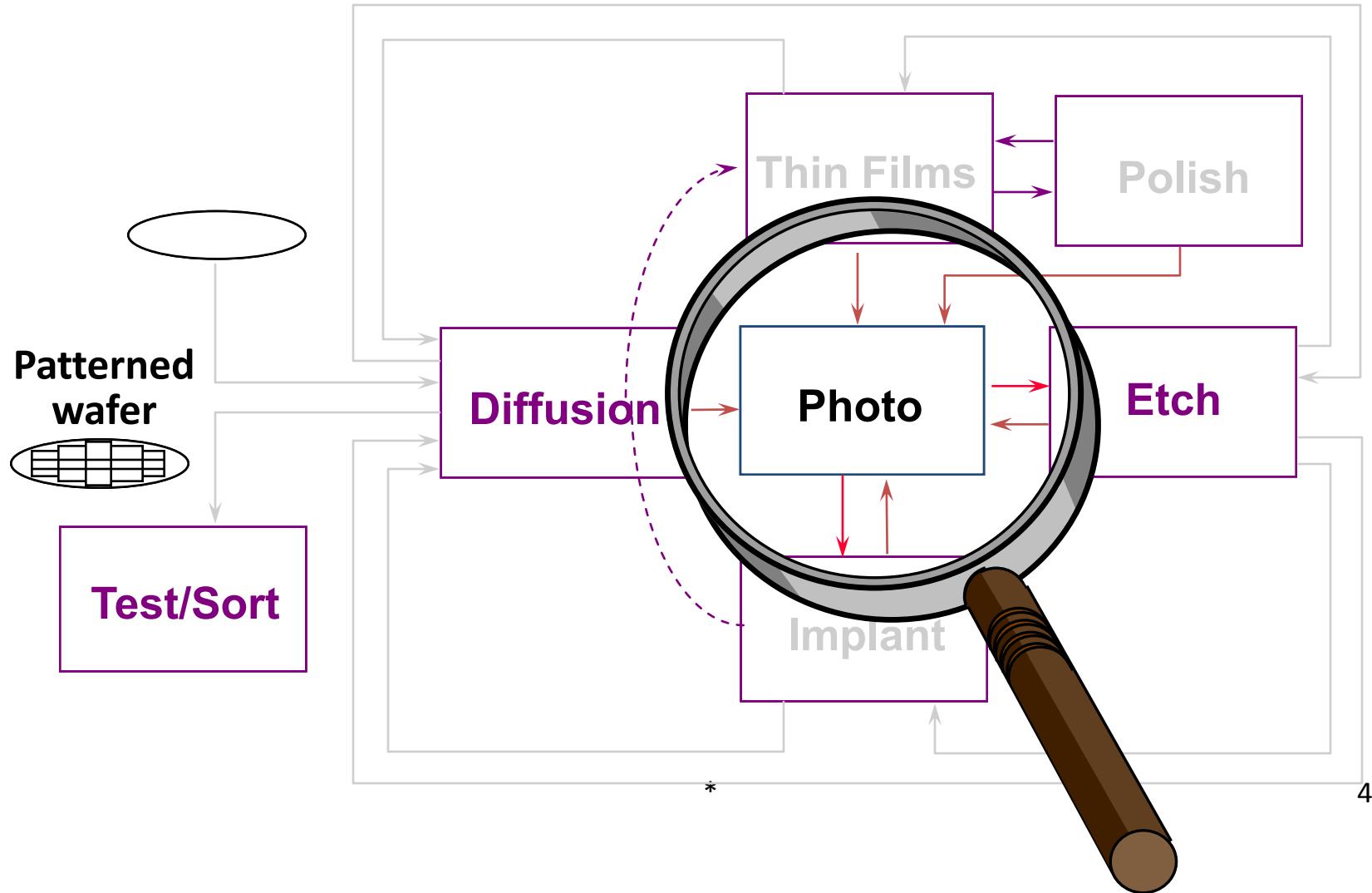
Photolithography -- Definitions

- *Photolithography* is used to produce 3-D images using light sensitive photoresist and controlled exposure to light.

- ◆ *Microlithography* is the technique used to print ultra-miniature patterns
 - used primarily in the semiconductor industry.



Photolithography is at the Center of the Wafer Fabrication Process



What else is Photolithography?

- 3-dimensional circuit patterning
- Most critical step in IC process
 - Determines feature *resolution*
 - Determines *overlay accuracy*
- Bottleneck in the fab process
- The leading technology



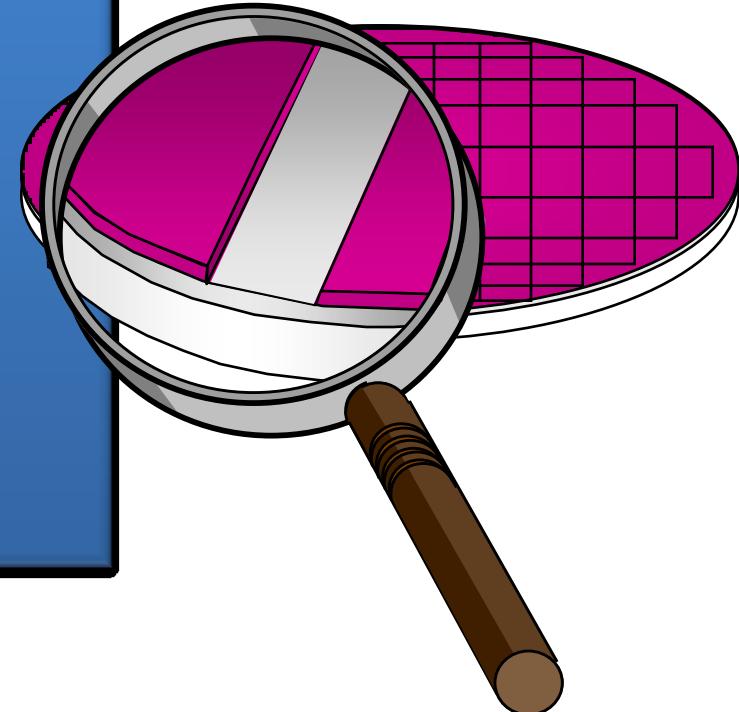
Wafer Conditions Prior to Patterning

- Surface conditions include:
 - film composition, e.g.: silicon, nitride, polysilicon, metal, etc.
 - bare surface vs. patterned surface
 - surface reflectivity
- Surface conditions may affect
 - photoresist-to-wafer adhesion
 - alignment accuracy
 - linewidth resolution
 - exposure settings
 - bake time



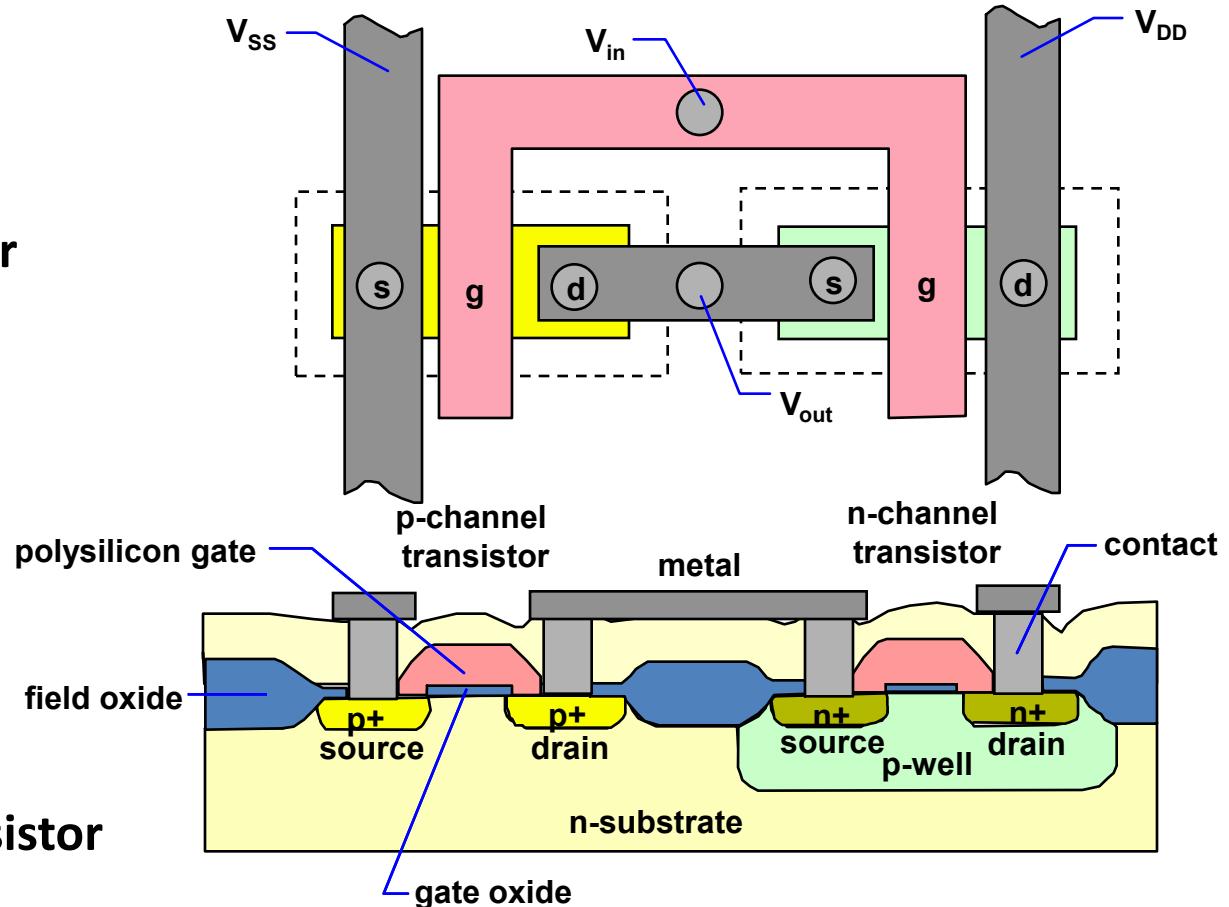
Wafer Conditions after Photolithography

- resist coated wafer
- patterned resist layer
- withstands etching process
- withstands ion implanting
- quality measures
 - linewidth resolution
 - overlay accuracy
 - particles & defects



Importance of Resolution and Overlay Registration

Top view of Transistor



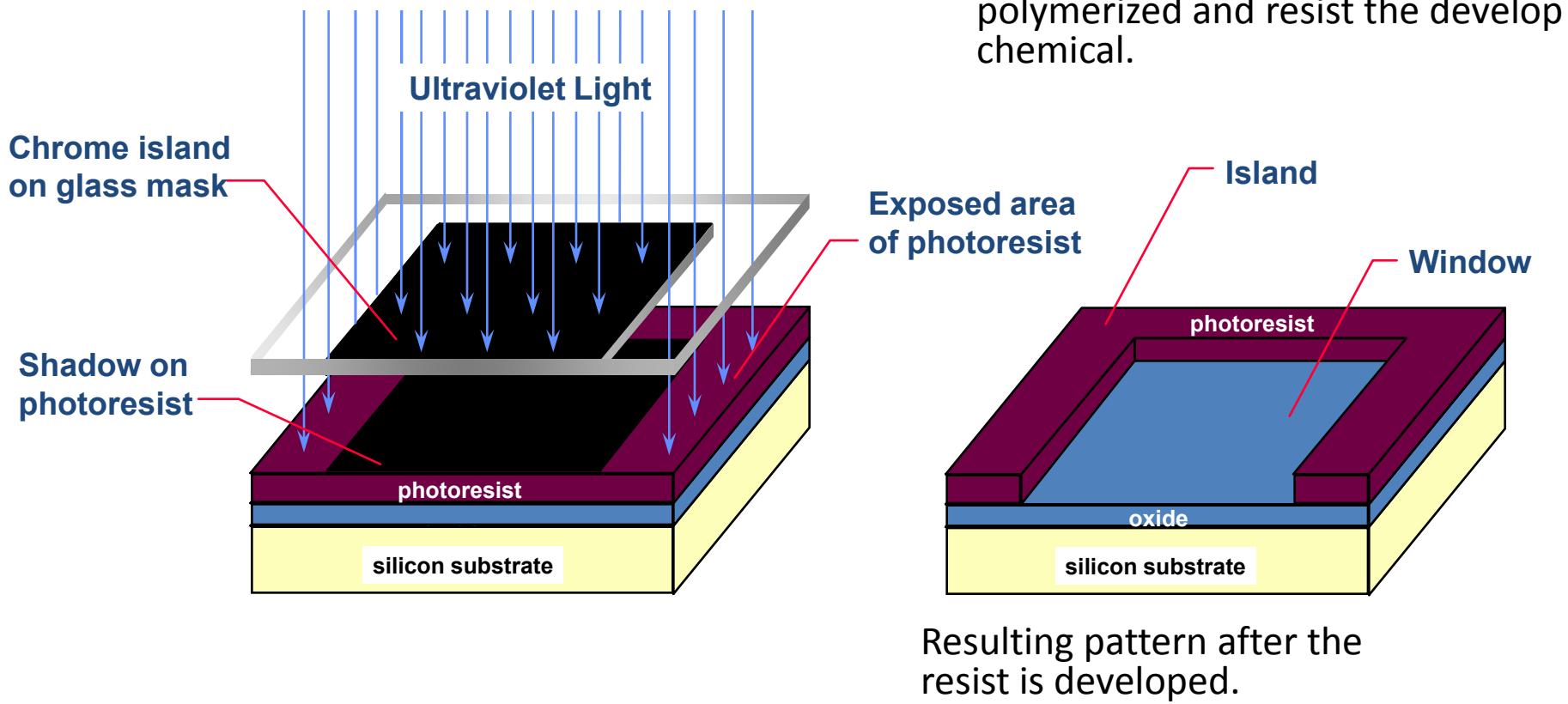
Cross-section of Transistor

Types of Photolithography Processes

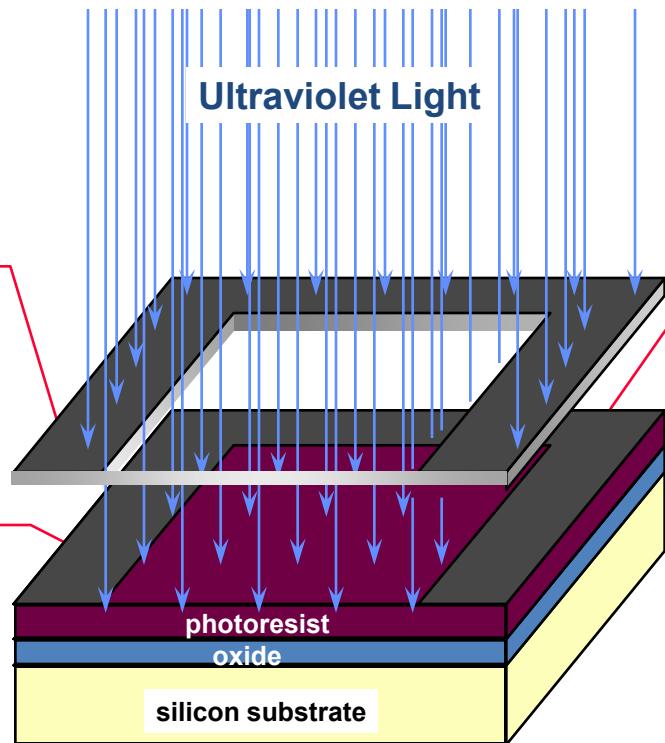
Negative: Prints a pattern that is opposite of the pattern that is on the mask.

Positive: Prints a pattern that is the same as the pattern on the mask.

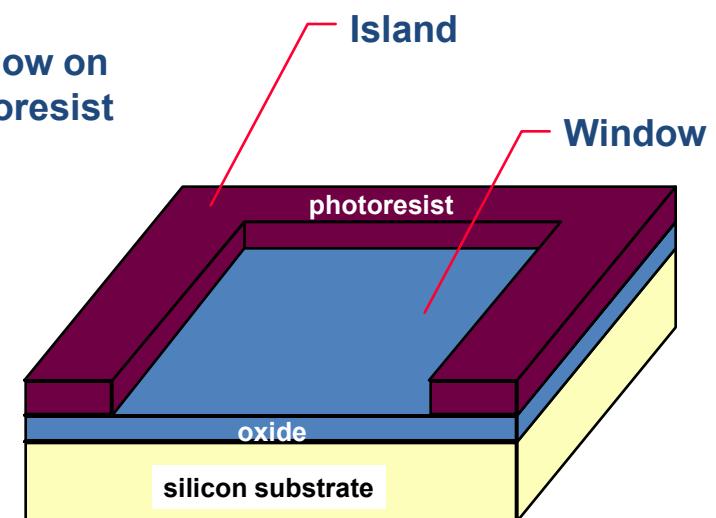
Negative Lithography



Positive Lithography



Areas exposed to light become photosoluble.



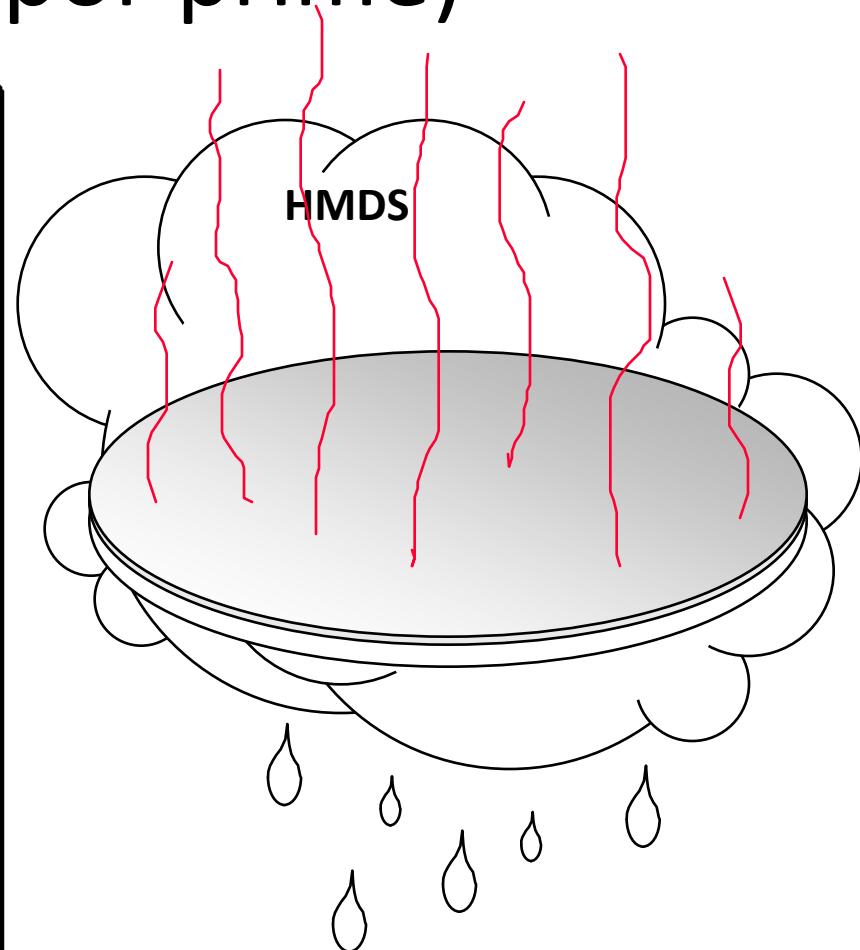
Resulting pattern after the resist is developed.

Ten Basic Steps of Photolithography

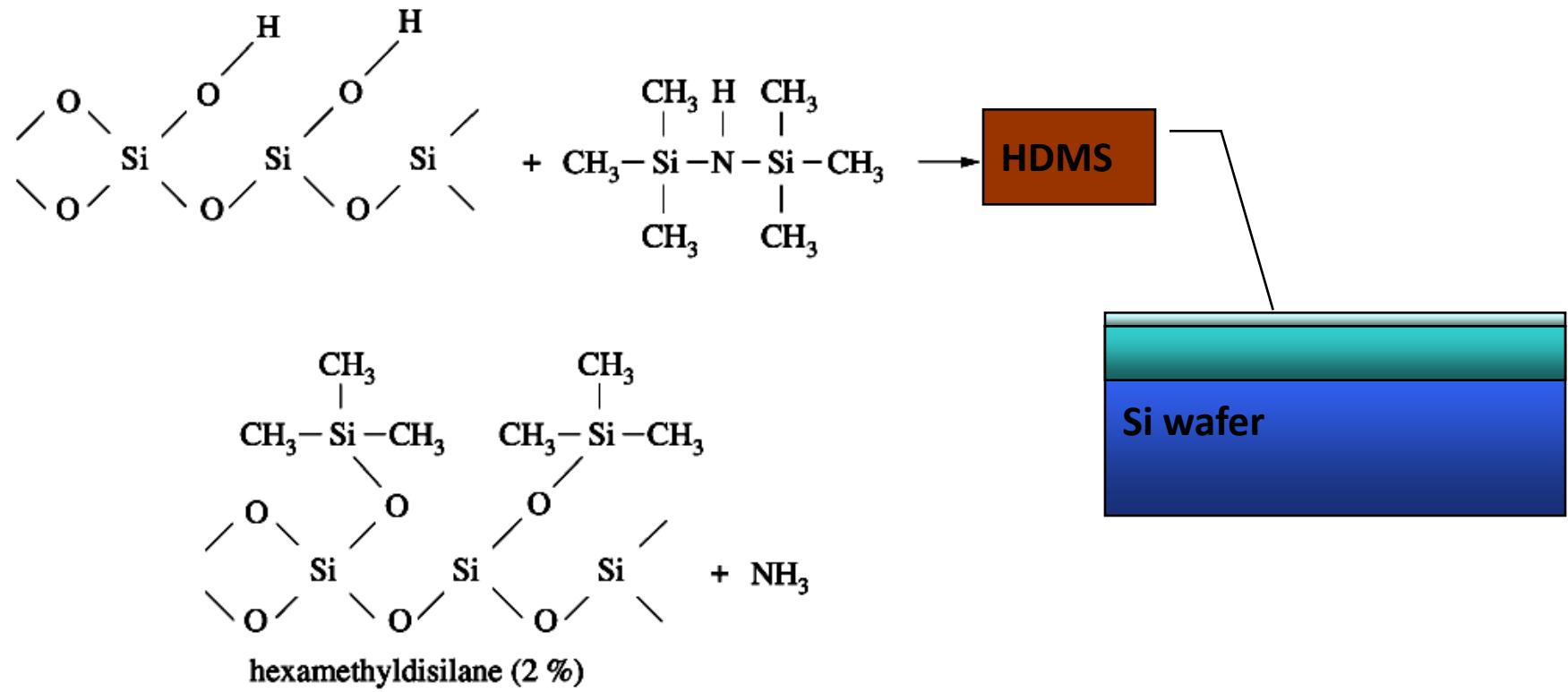
1. Surface Preparation
2. Photoresist Application
3. Soft Bake
4. Align & Expose
5. Develop
6. Hard Bake
7. Develop Inspection
8. Etch
9. Resist Strip
10. Final Inspection

1. Surface Preparation (HMDS vapor prime)

- Dehydration bake in enclosed chamber with exhaust
- Clean and dry wafer surface (hydrophobic)
- Hexamethyldisilazane (HMDS)
- Temp ~ 200 - 250°C
- Time ~ 60 sec.

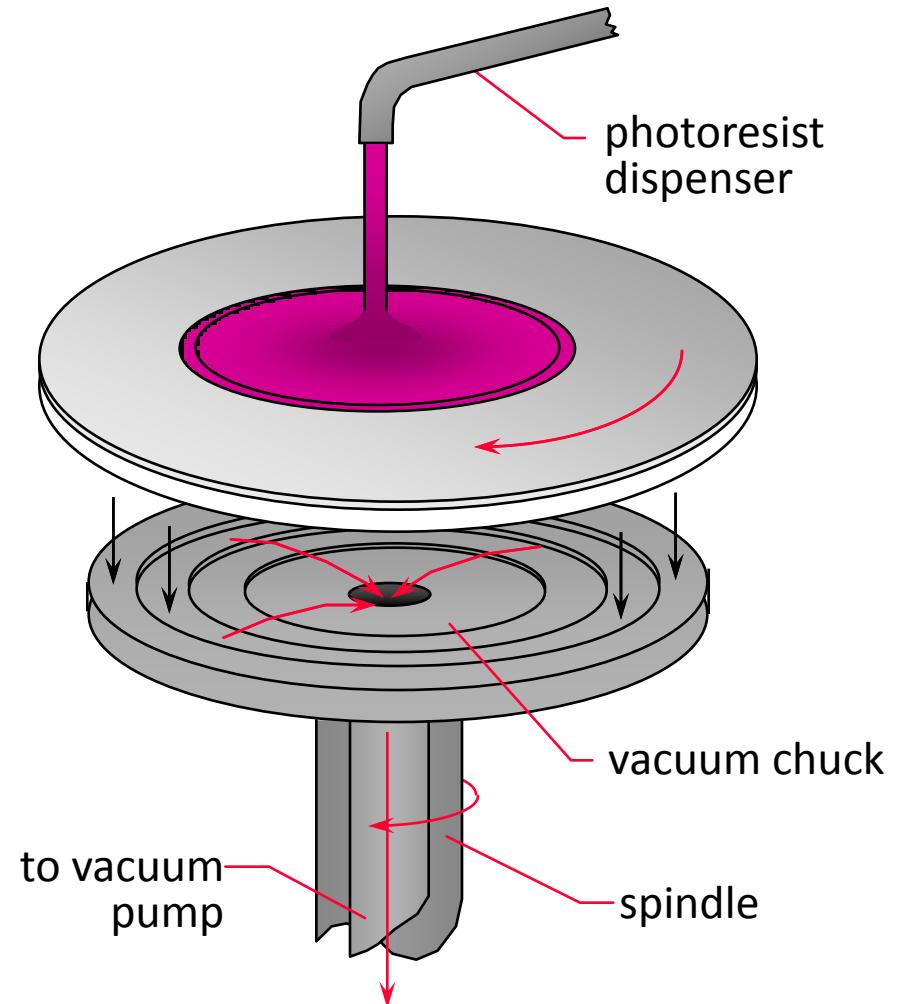


- Spin coater used 2500rpm~3000 rpm for 15 seconds
- Si wafer surface treatment → adhesion develop

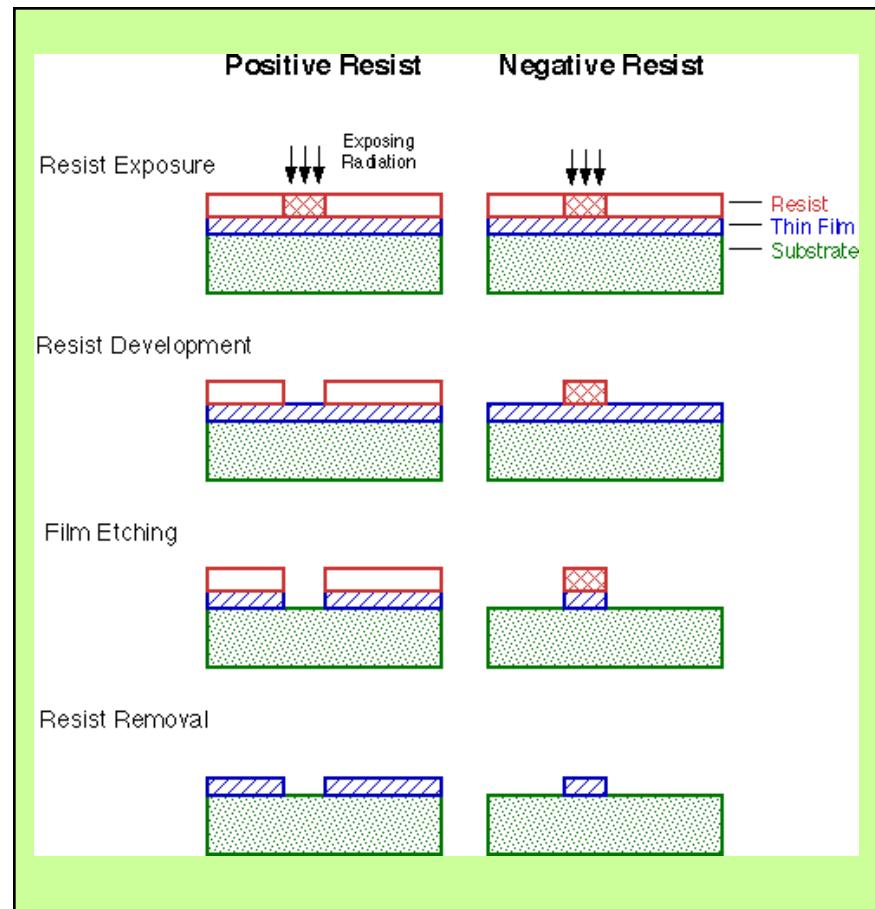


2. Photoresist Application

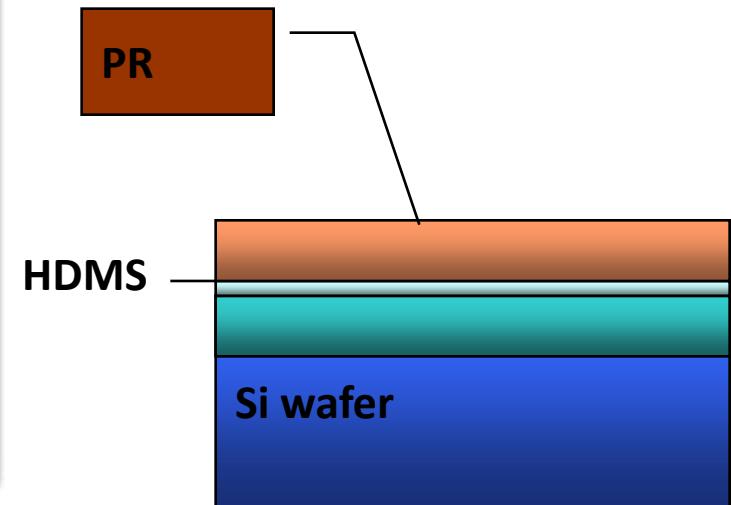
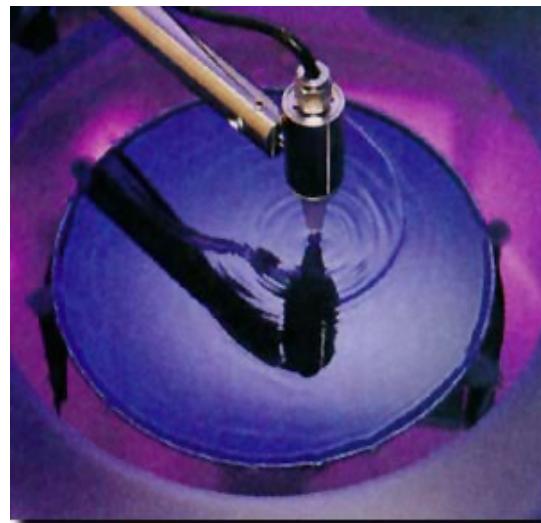
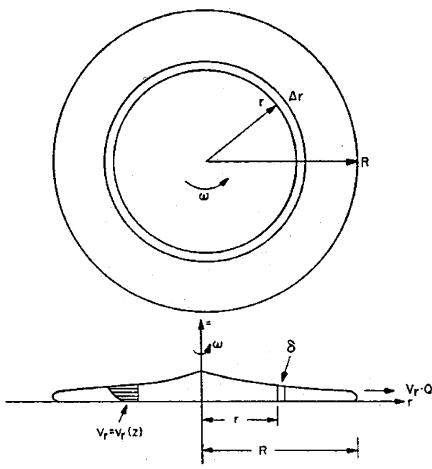
- Wafer held onto vacuum chuck
- Dispense ~5ml of photoresist
- Slow spin ~ 500 rpm
- Ramp up to ~ 3000 - 5000 rpm
- Quality measures:
 - time
 - speed
 - thickness
 - uniformity
 - particles & defects



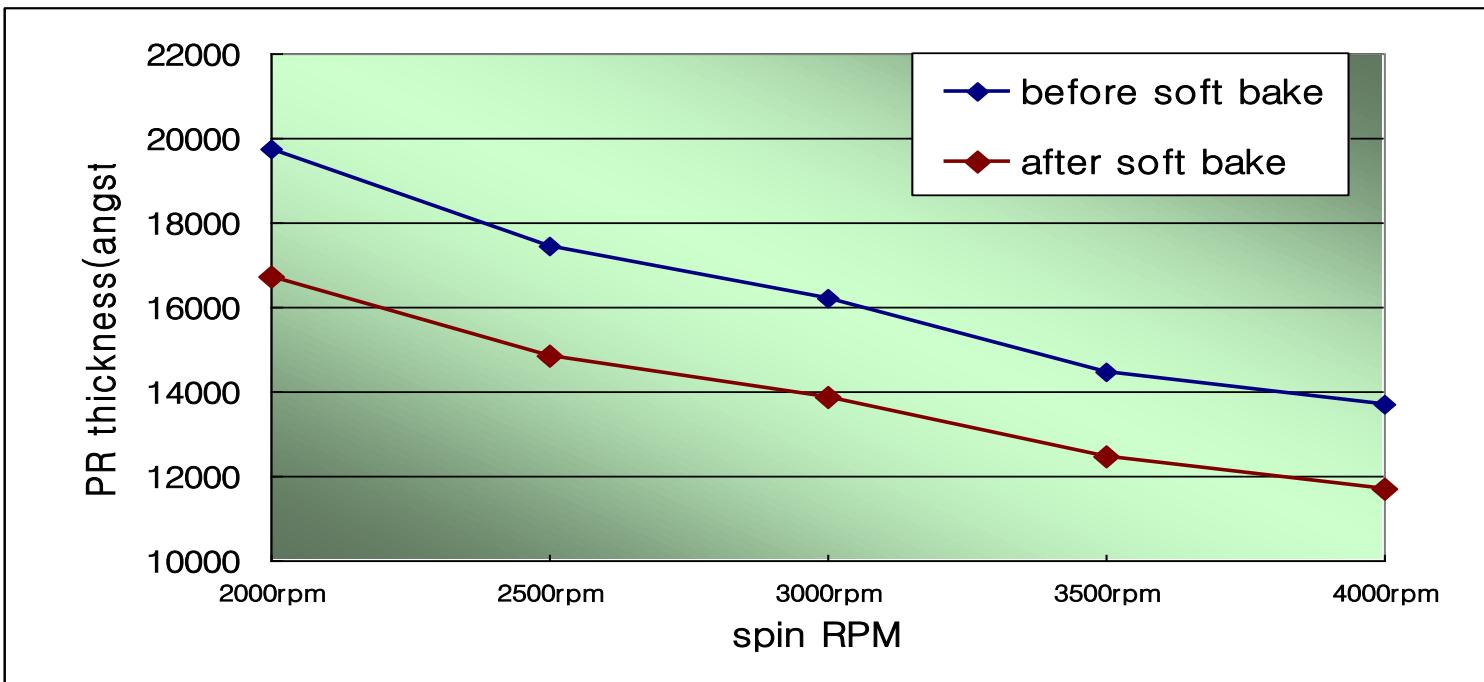
- **PR = Sensitizer (PAC) + resin + solvent**
- **Pattern polarity**
 - **Positive type** : AZ PR series (Shipley)
 - **Negative type** : HR PR series (Hunt Chemical)



- using spin motor create uniform coating PR thickness on the wafer
- important element for thickness and uniform : resin %, cohesion, spin speed, accelerator, time



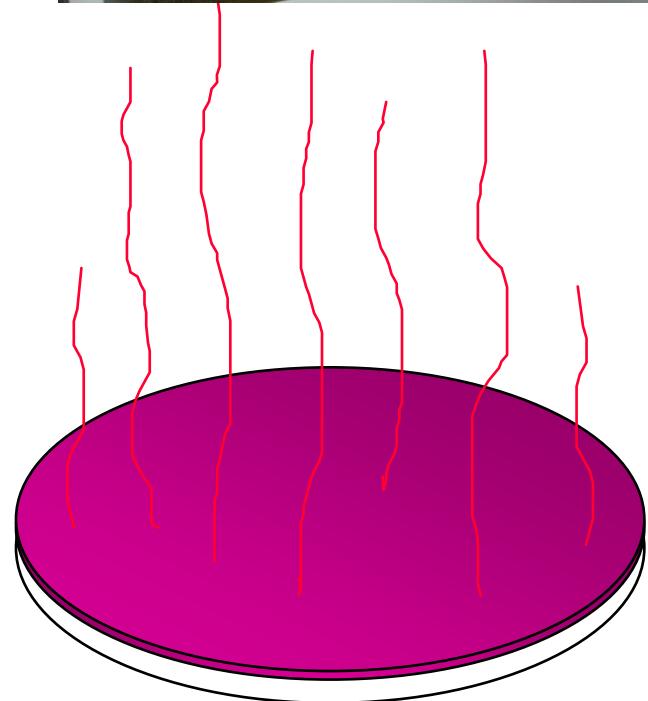
Result: Variation of PR thickness



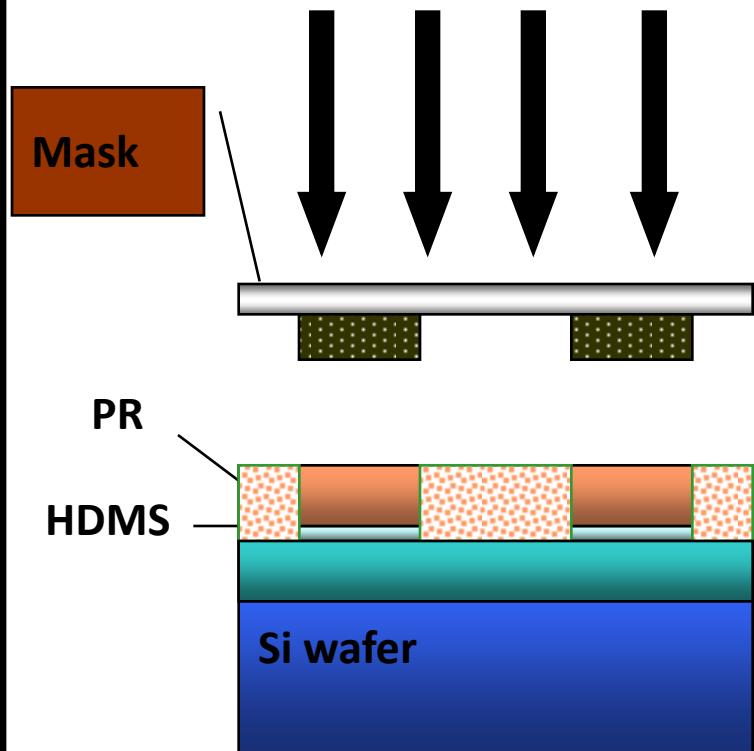
- Spin speed (rpm) ↑ → PR thickness ↓
- Condensation after soft bake → Solvent evaporation

3. Soft Bake

- Partial evaporation of photo-resist solvents
- Improves adhesion
- Improves uniformity
- Improves etch resistance
- Improves linewidth control
- Optimizes light absorbance characteristics of photoresist

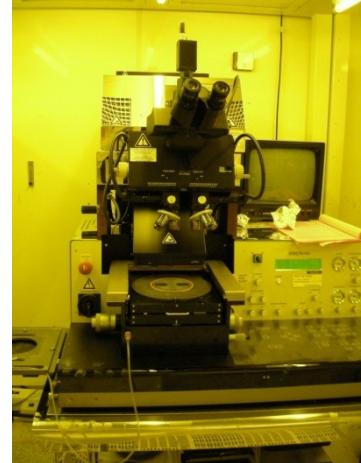
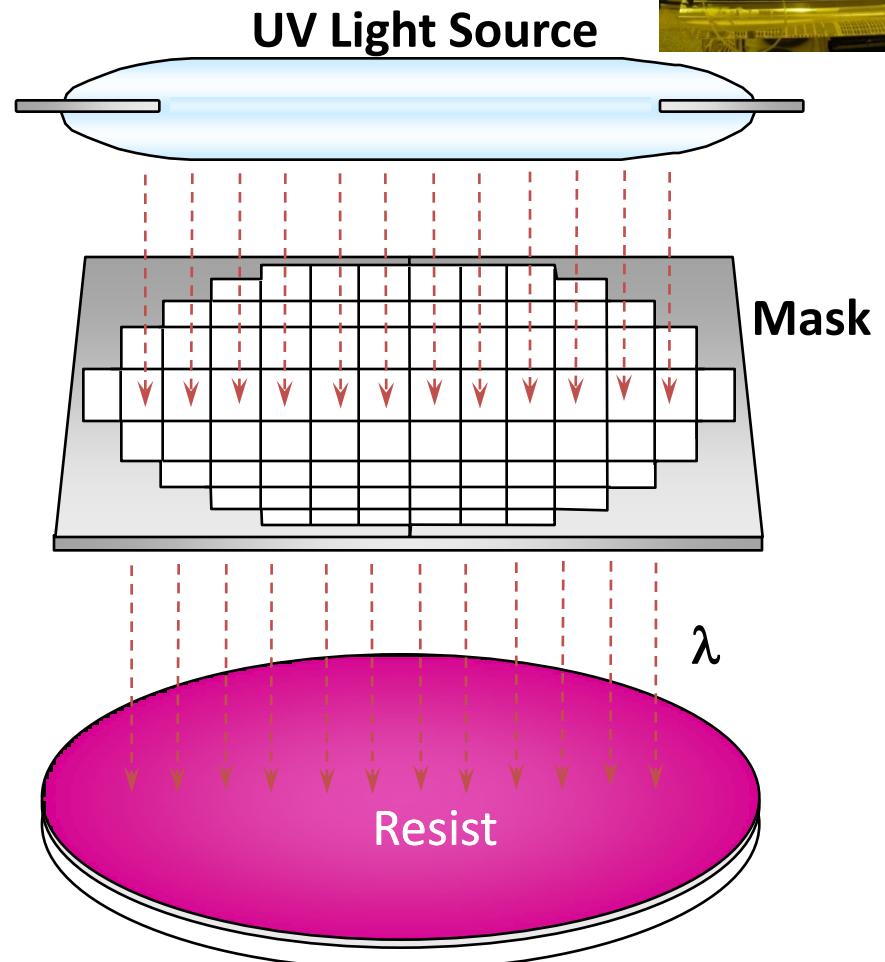


- Soft bake(95°C, 30min in oven)
: improve adhesion and remove solvent from the PR
- Alignment
: a photo mask, a square glass plate with patterned emulsion or metal film on one side is placed over the wafer
- Exposure(UV light : 12mW)
: leaving bare SiO₂ in the exposed area. A negative resist remain on the surface wherever it is exposed.



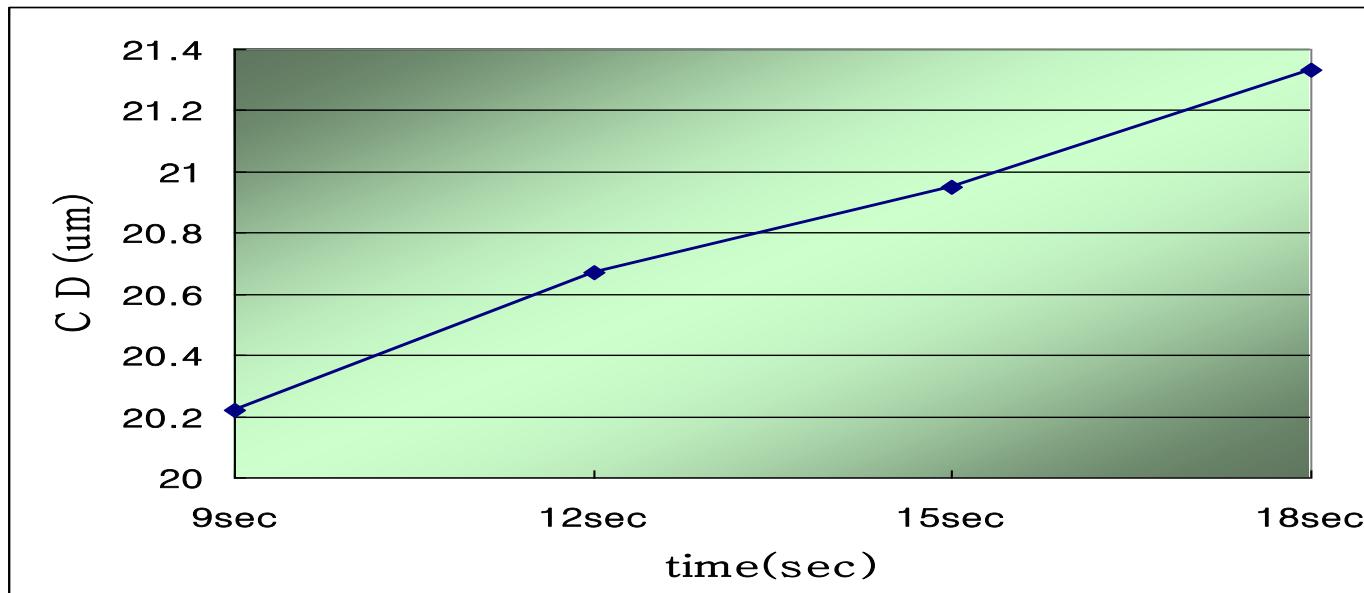
4. Alignment and Exposure

- Transfers the mask image to the resist-coated wafer
- Activates photo-sensitive components of photoresist
- Quality measures:
 - linewidth resolution
 - overlay accuracy
 - particles & defects



- Photoresist thickness is related to Coating Spin
 - *spin speed increase* → *thickness decrease*
 - *After soft bake* → *thickness decrease*
- Critical Dimension is related to Exposure time
 - *expose time increase* → *CD increase*
 - *proper expose time need for exact process*

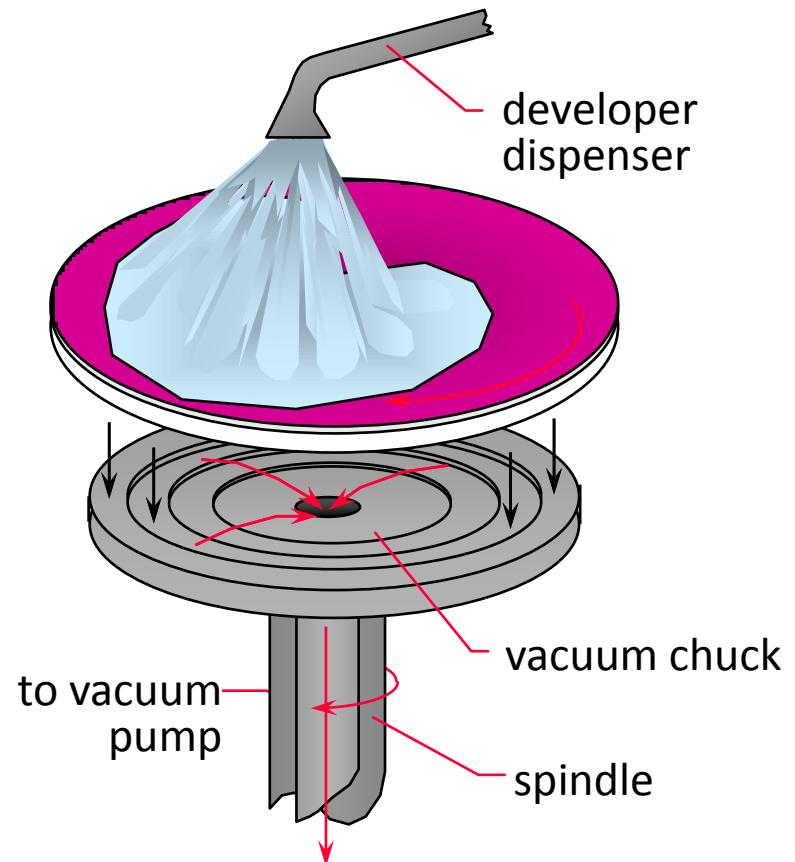
Variation of Critical Dimension (CD)



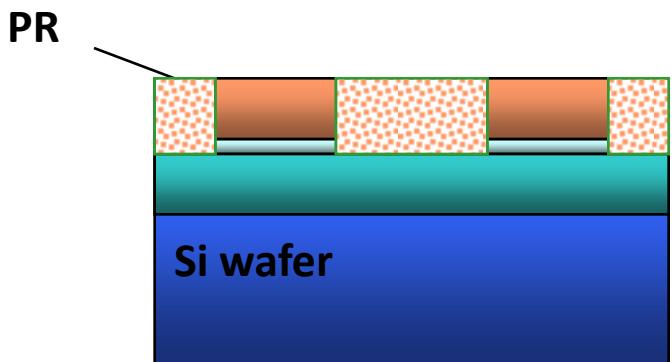
- Exposing time ↑ → CD ↑

5. Develop

- Soluble areas of photoresist are dissolved by developer chemical
- Visible patterns appear on wafer
 - windows
 - islands
- Quality measures:
 - line resolution
 - uniformity
 - particles & defects



- Post exposure bake
- Develop
:6AZMIF 300:1H₂O
(70 sec., room temp.)

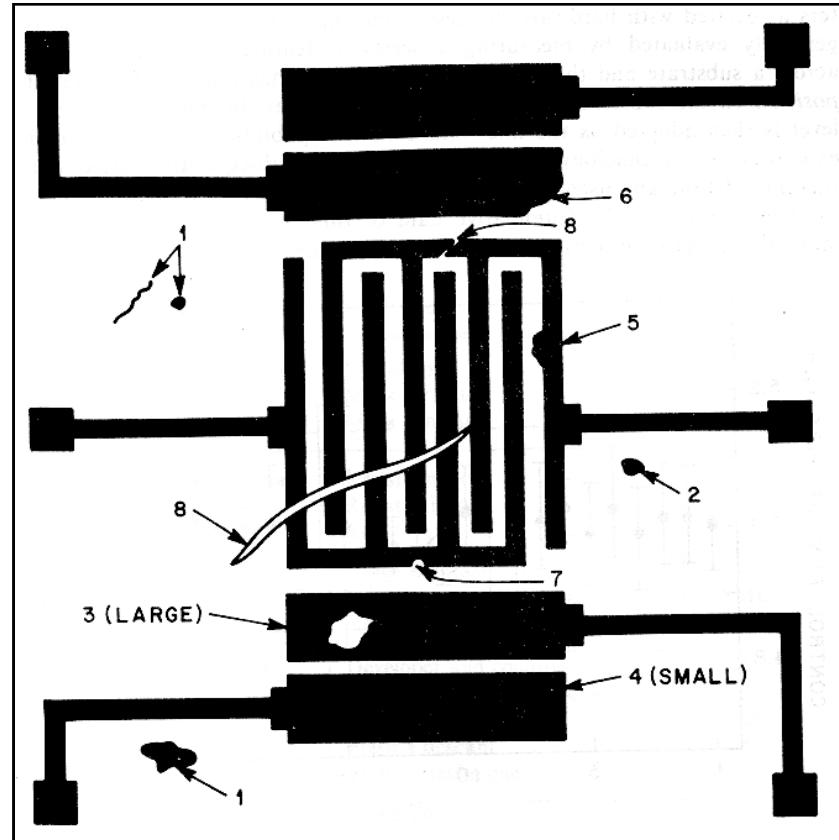


- **Inspection**

1. Contamination
2. Opaque spot
3. Large hole
4. Pin hole
5. Excess material
6. Lack of adhesion
7. Intrusion
8. Scratch

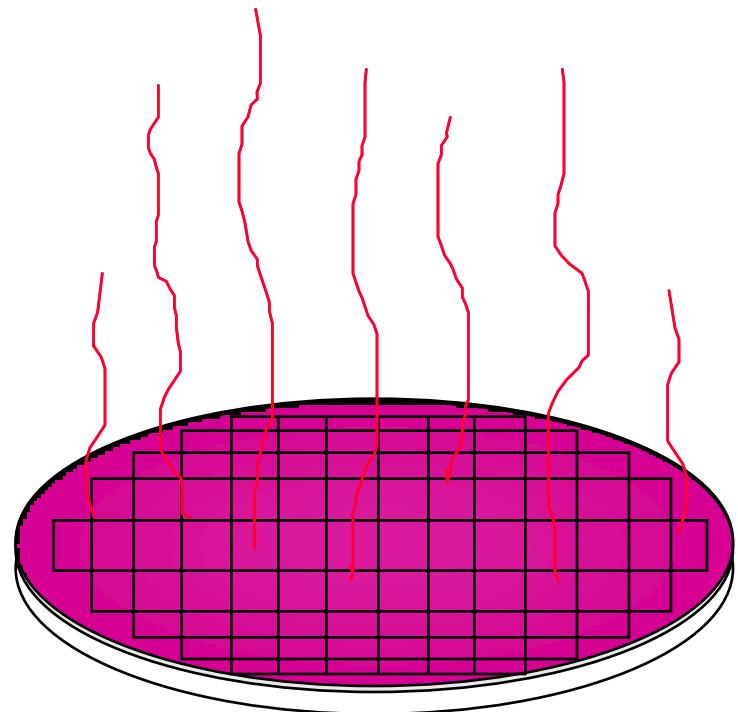
Rework

- **Hard bake (110°C, 30 min.)**
: to harden the photoresist and improve adhesion to the substrate.



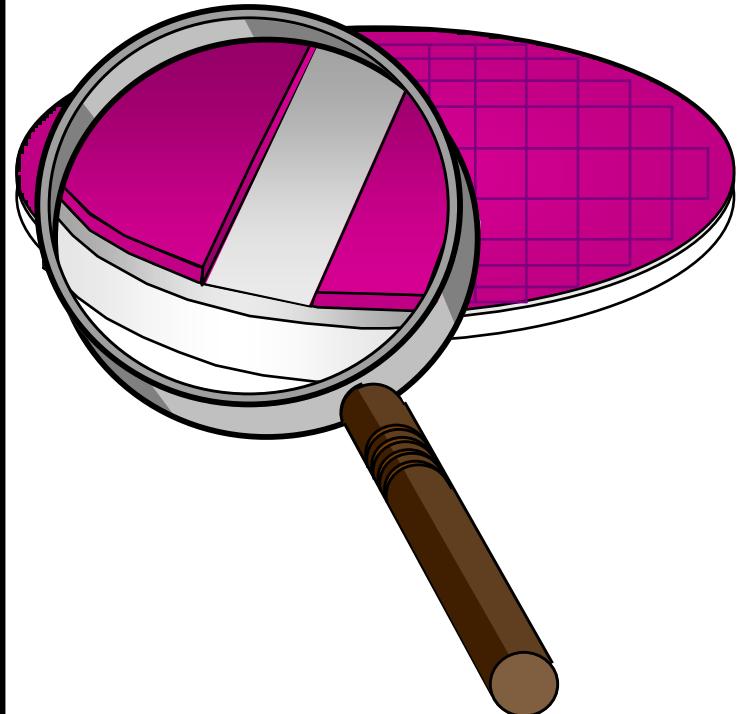
6. Hard Bake

- ◆ Evaporate remaining photoresist
- ◆ Improve adhesion
- ◆ Higher temperature than soft bake



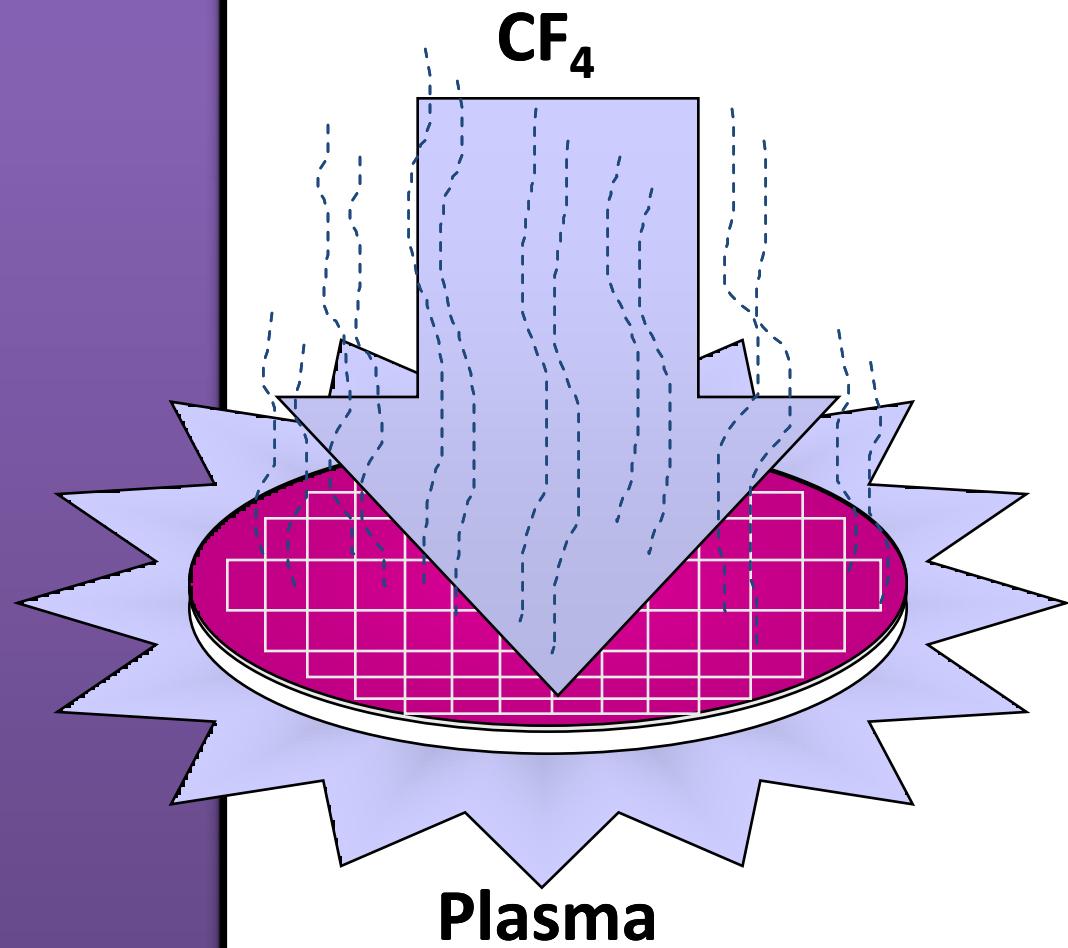
7. Develop Inspect

- Optical or SEM metrology
- Quality issues:
 - particles
 - defects
 - critical dimensions
 - linewidth resolution
 - overlay accuracy



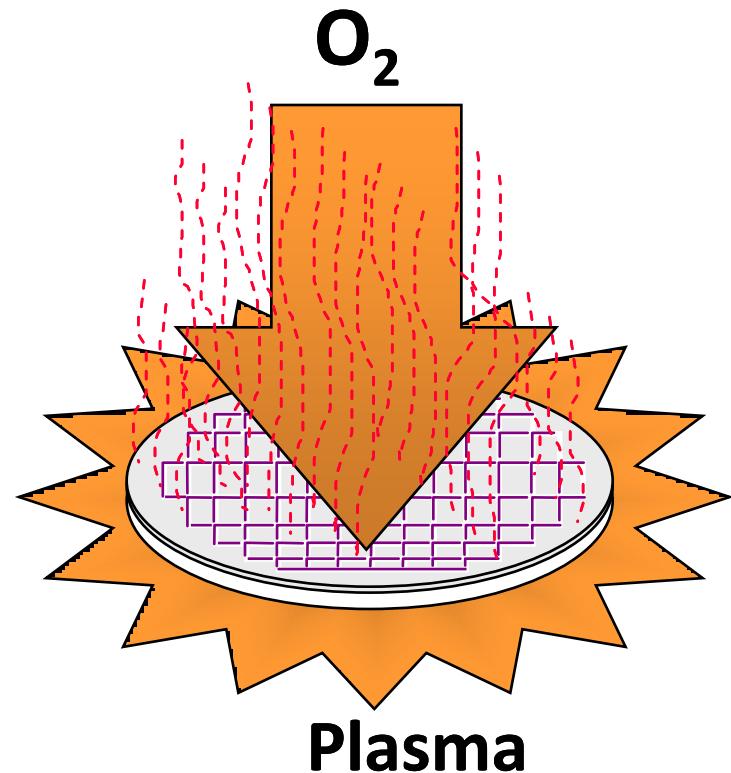
8. Etch

- Selective removal of upper layer of wafer through windows in photoresist
- Two basic methods:
 - wet acid etch
 - dry plasma etch
- Quality measures:
 - defects and particles
 - step height
 - selectivity
 - critical dimensions



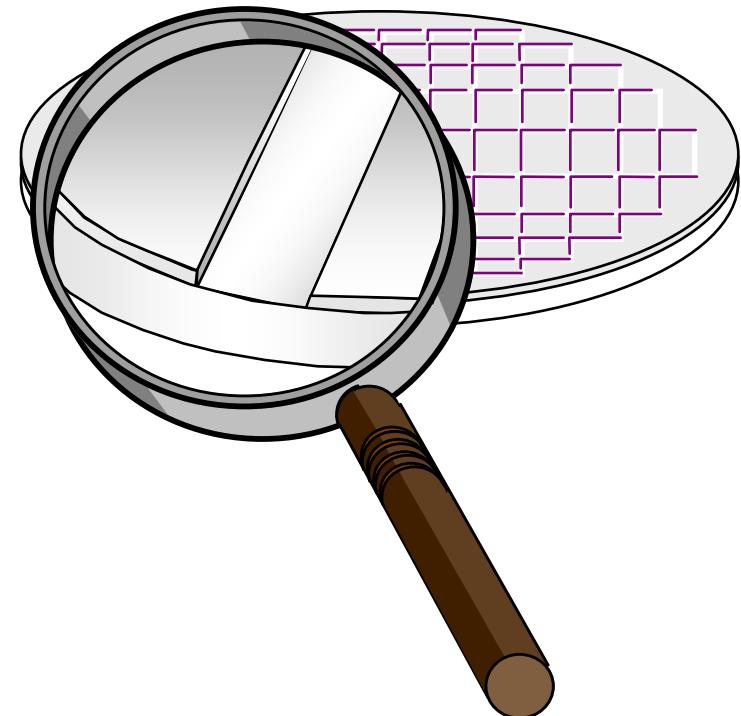
9. Photoresist Removal (strip)

- No need for photoresist following etch process
- Two common methods:
 - wet acid strip
 - dry plasma strip
- Followed by wet clean to remove remaining resist and strip byproducts



10. Final Inspection

- Photoresist has been completely removed
- Pattern on wafer matches mask pattern (positive resist)
- Quality issues:
 - defects
 - particles
 - step height
 - critical dimensions





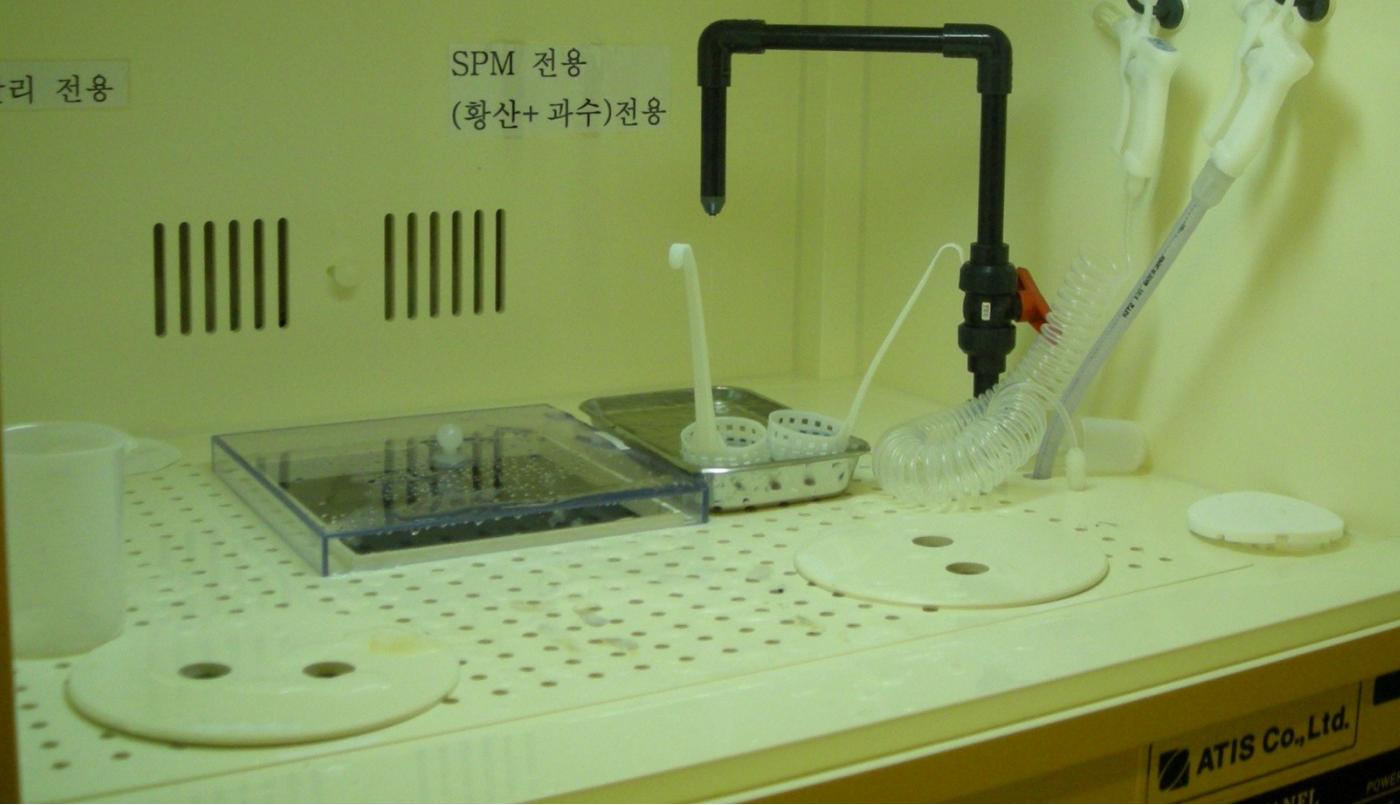
알칼리 전용

SPM 전용
(황산+과수)전용

00

글리 전용

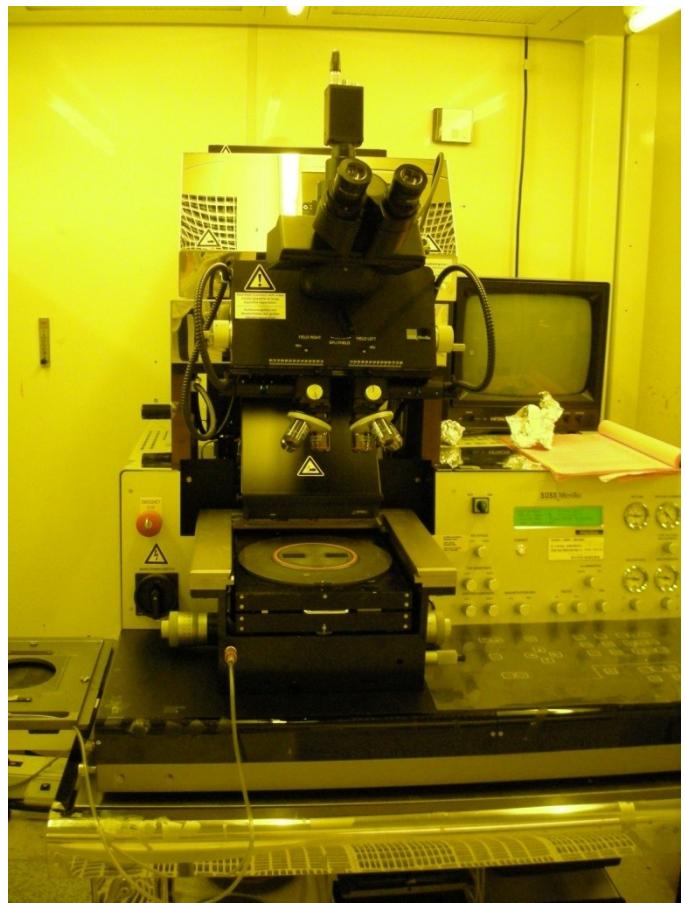
SPM 전용
(황산+과수)전용



ATIS Co.,Ltd.
NFT POWER



















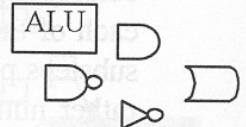


Full Custom

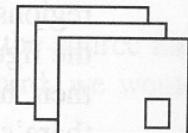
- Very Large Scale Integration (VLSI)
- Placement
 - Place and orient transistors
- Routing
 - Connect transistors
- Sizing
 - Make fat, fast wires or thin, slow wires
 - May also need to size buffer
- Design Rules
 - “simple” rules for correct circuit function
 - Metal/metal spacing, min poly width...

START

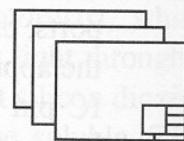
Designers create layouts for basic components.



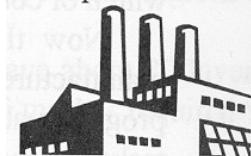
Designers place the components, resulting in masks.



Designers provide the connections among components, which are translated to masks.



The masks are sent to the fabrication plant to produce ICs.

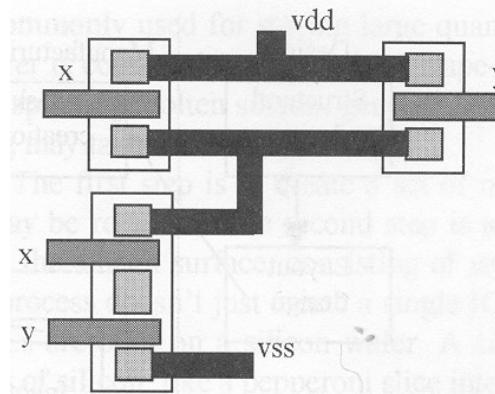
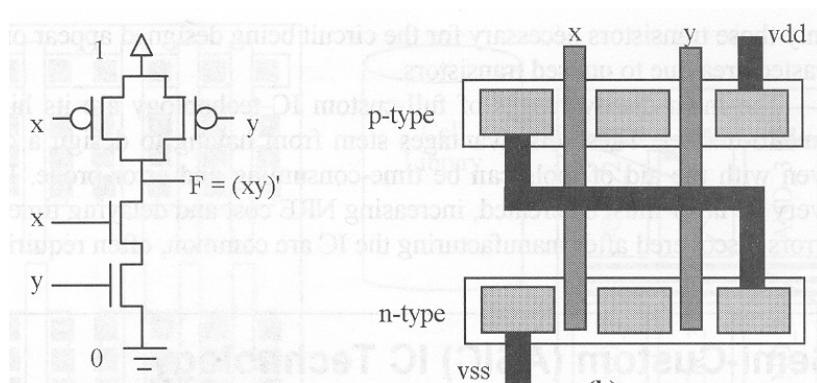
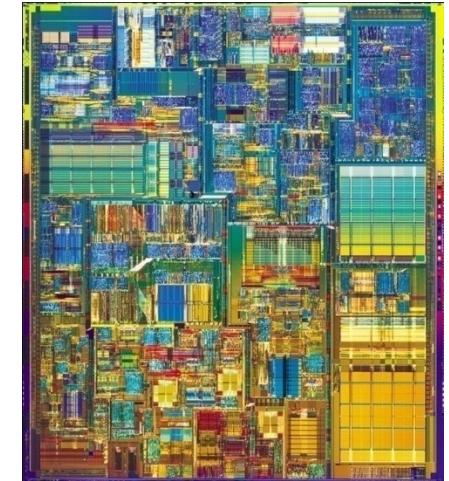


ICs are now ready to be tested/used.



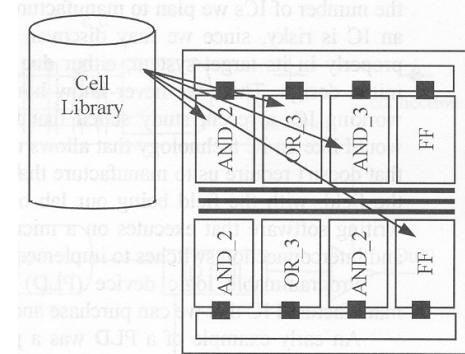
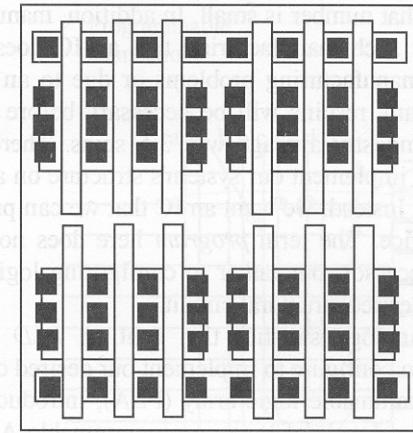
Full Custom

- Best size, power, performance
- Hand design
 - Horrible time-to-market/flexibility/NRE cost...
 - Reserve for the most important units in a processor
 - ALU, Instruction fetch...
- Physical design tools
 - Less optimal, but faster...



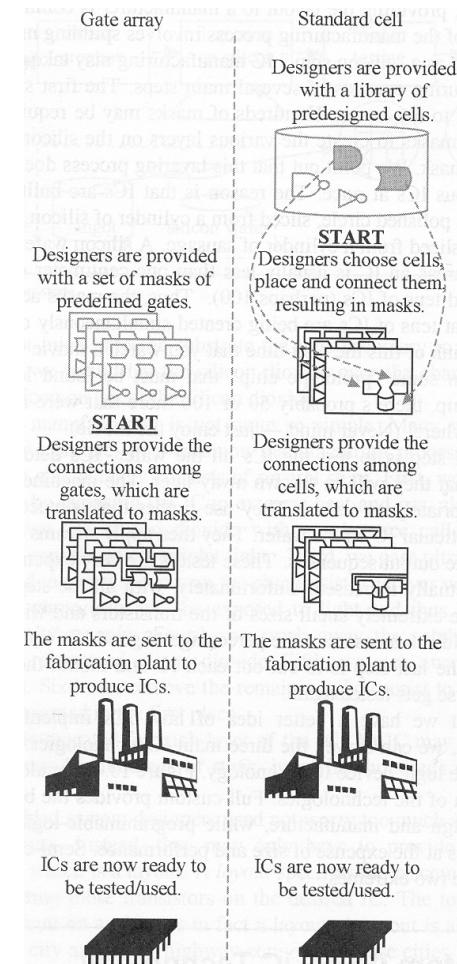
Semi-Custom

- Gate Array
 - Array of prefabricated gates
 - “place” and route
 - Higher density, faster time-to-market
 - Does not integrate as well with full-custom
- Standard Cell
 - A library of pre-designed cell
 - Place and route
 - Lower density, higher complexity
 - Integrate great with full-custom

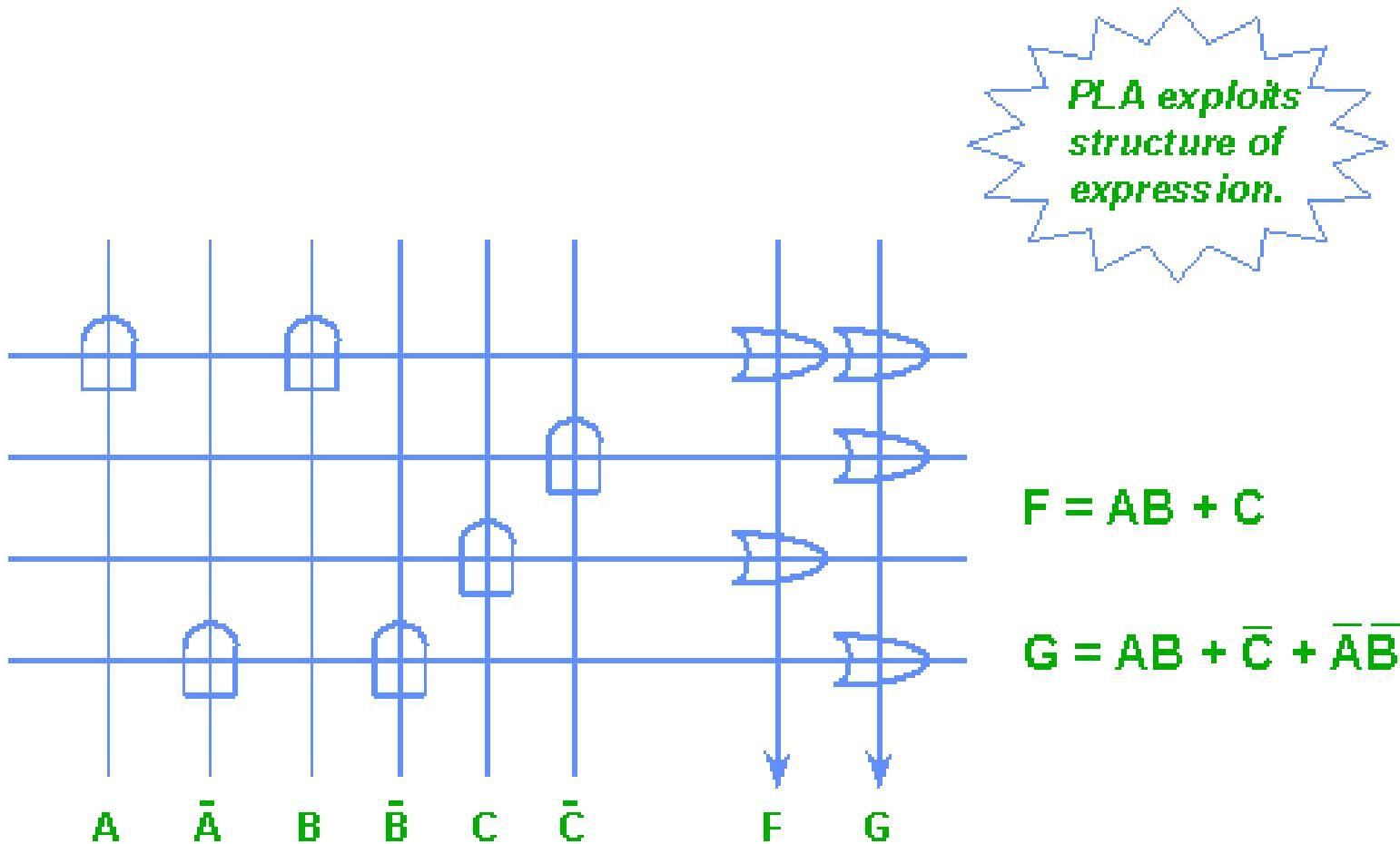


Semi-Custom

- Most popular design style
- Jack of all trade
 - Good
 - Power, time-to-market, performance, NRE cost, per-unit cost, area...
- Master of none
 - Integrate with full custom for critical regions of design



Programmable Logic Array (PLA)



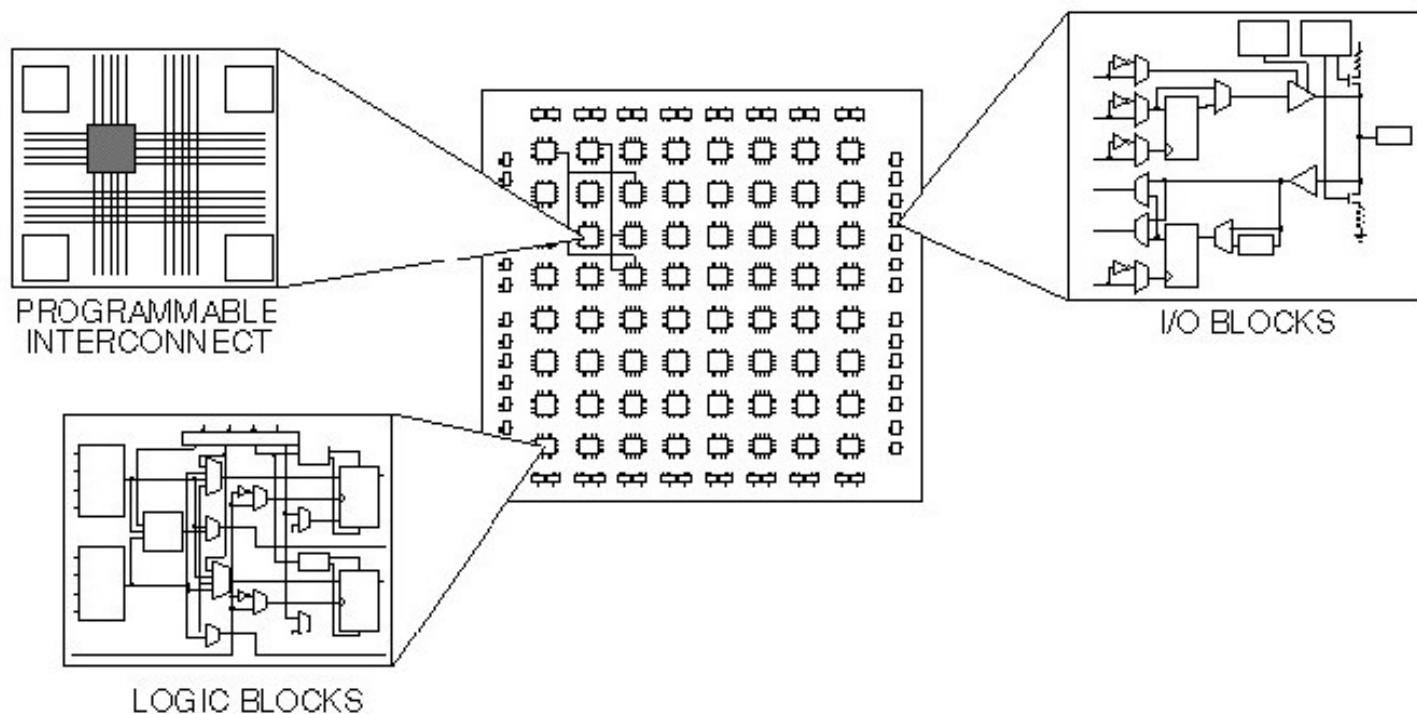
Programmable Logic Device

- Programmable Logic Device
 - Programmable Logic Array, Programmable Array Logic, Field Programmable Gate Array
- All layers already exist
 - Designers can purchase an IC
 - To implement desired functionality
 - Connections on the IC are either created or destroyed to implement
- Benefits
 - Very low NRE costs
 - Great time to market
- Drawback
 - High unit cost, bad for large volume
 - Power
 - Except special PLA
 - slower



1600 usable gate, 7.5 ns
\$7 list price

Xilinx FPGA



Configurable Logic Block (CLB)

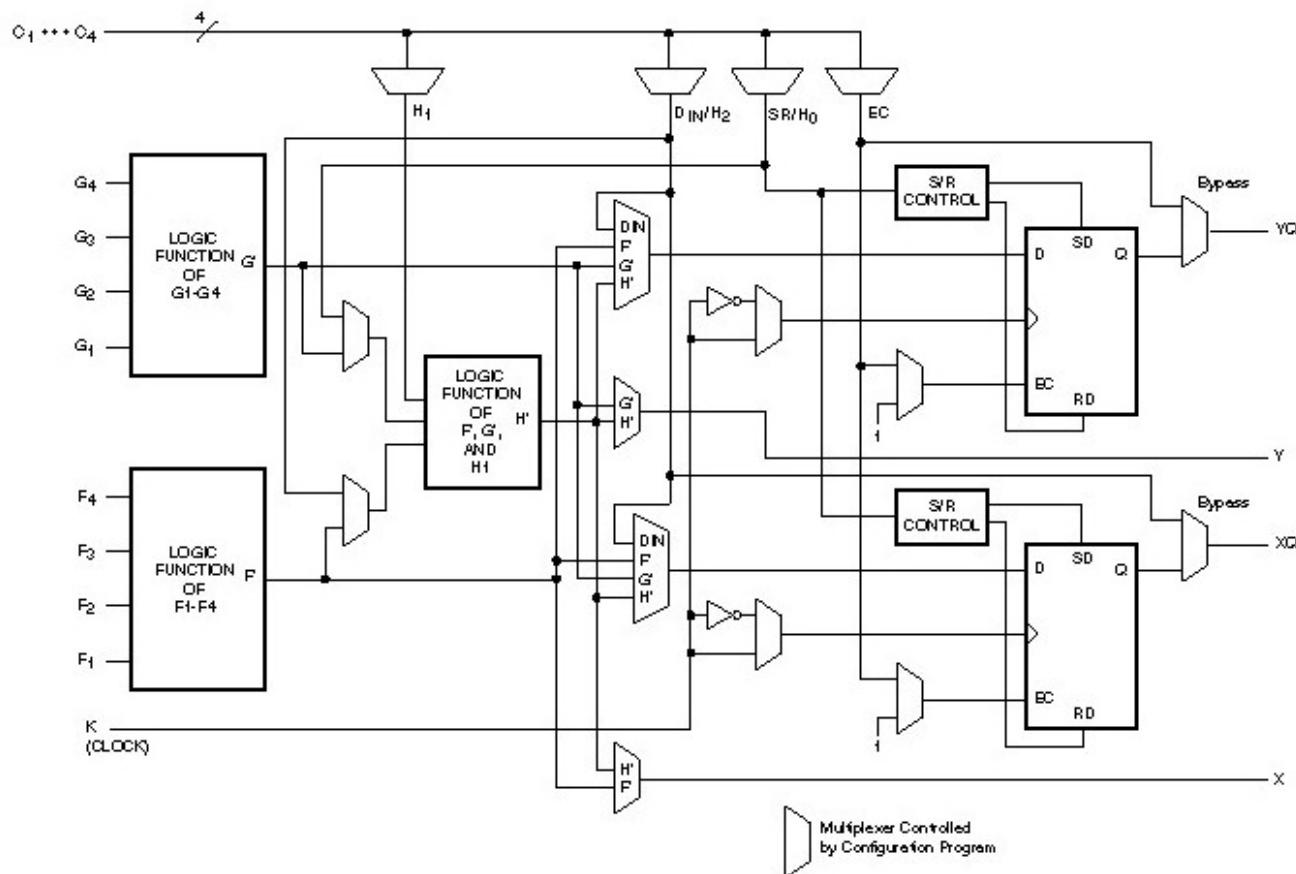
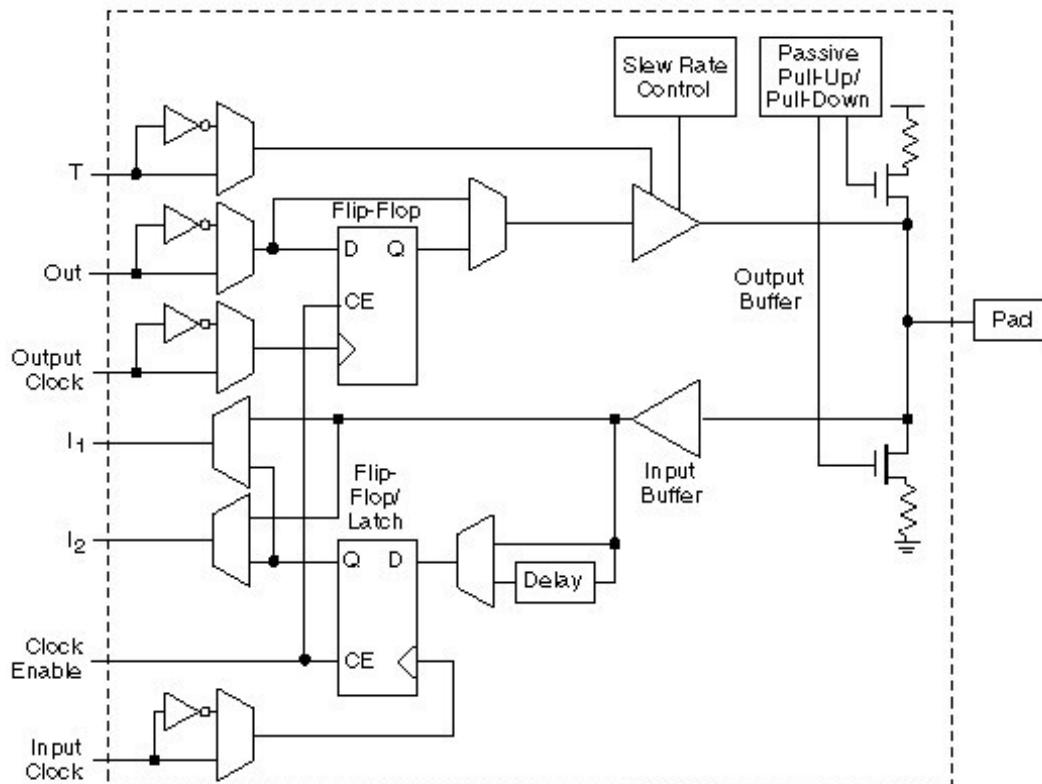
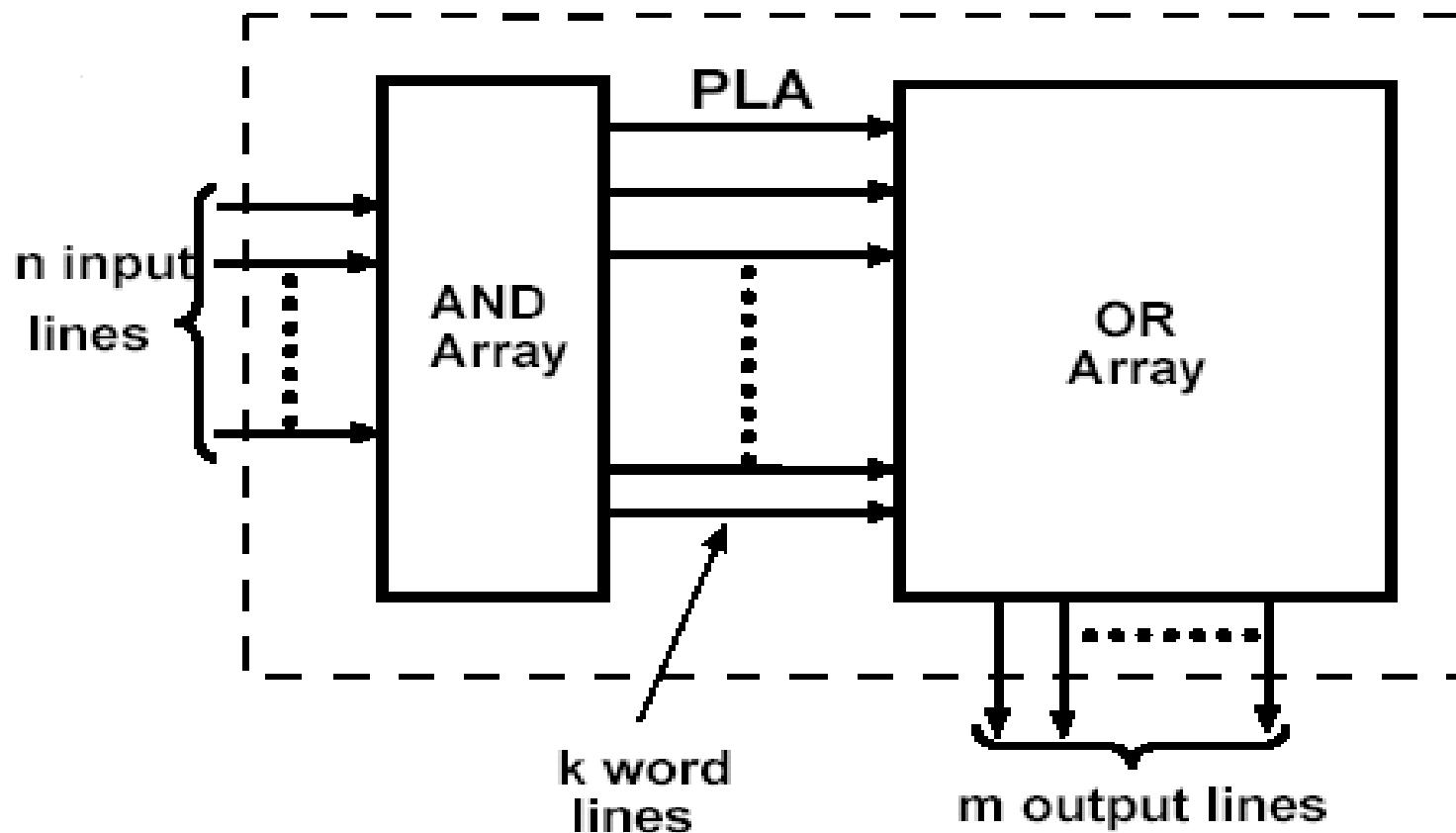


Figure 1: Simplified Block Diagram of XC4000-Series CLB (RAM and Carry Logic functions not shown)

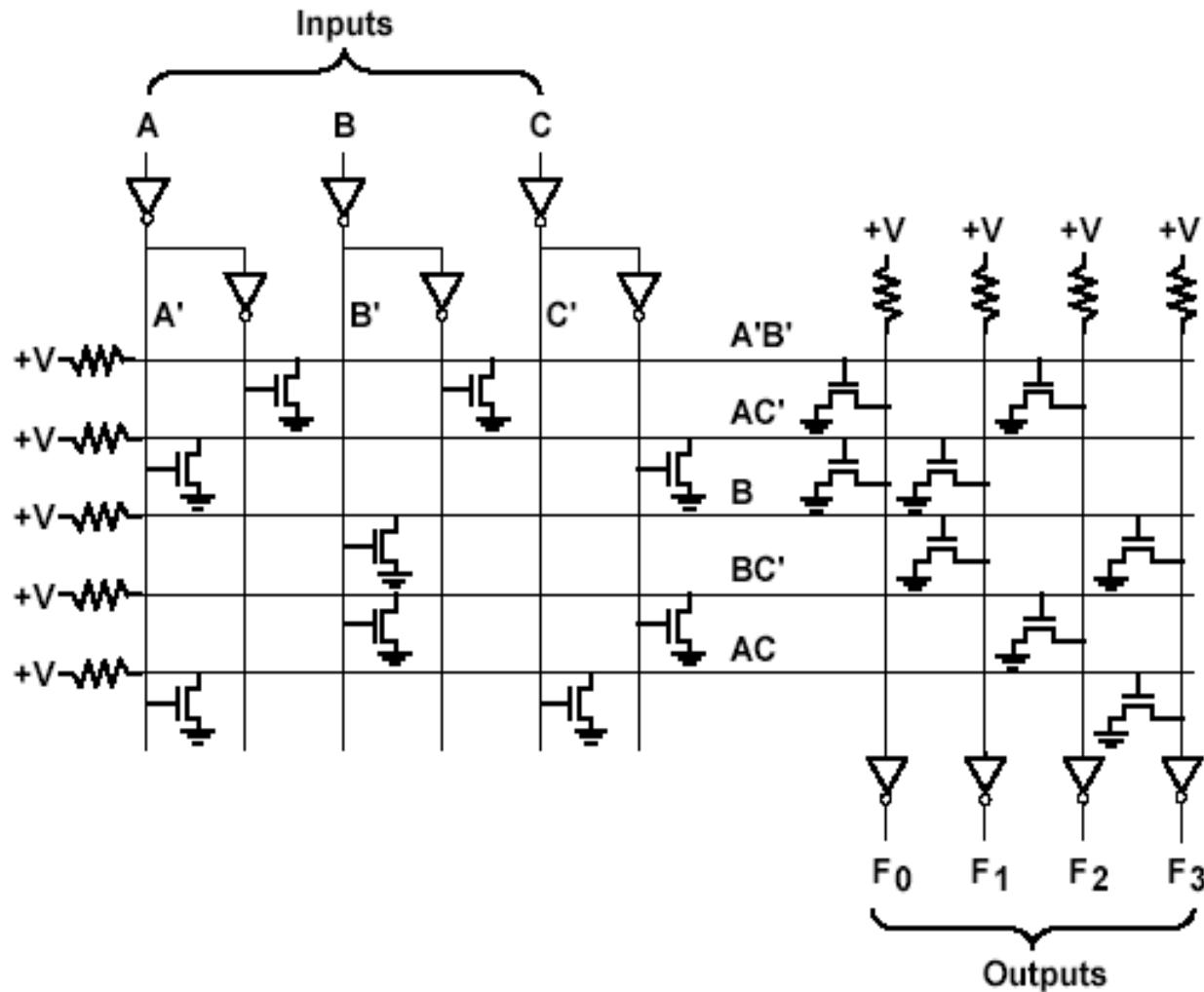
I/O Block



PROGRAMMABLE LOGIC ARRAYS (PLAs)



N-MOS PLA WITH 3 INPUT, 5 PRODUCT TERMS, AND 4 OUTPUTS



$$F_0 = \Sigma m(0, 1, 4, 6)$$

$$= A'B' + AC'$$

$$F_1 = \Sigma m(2, 3, 4, 6, 7)$$

$$= B + AC'$$

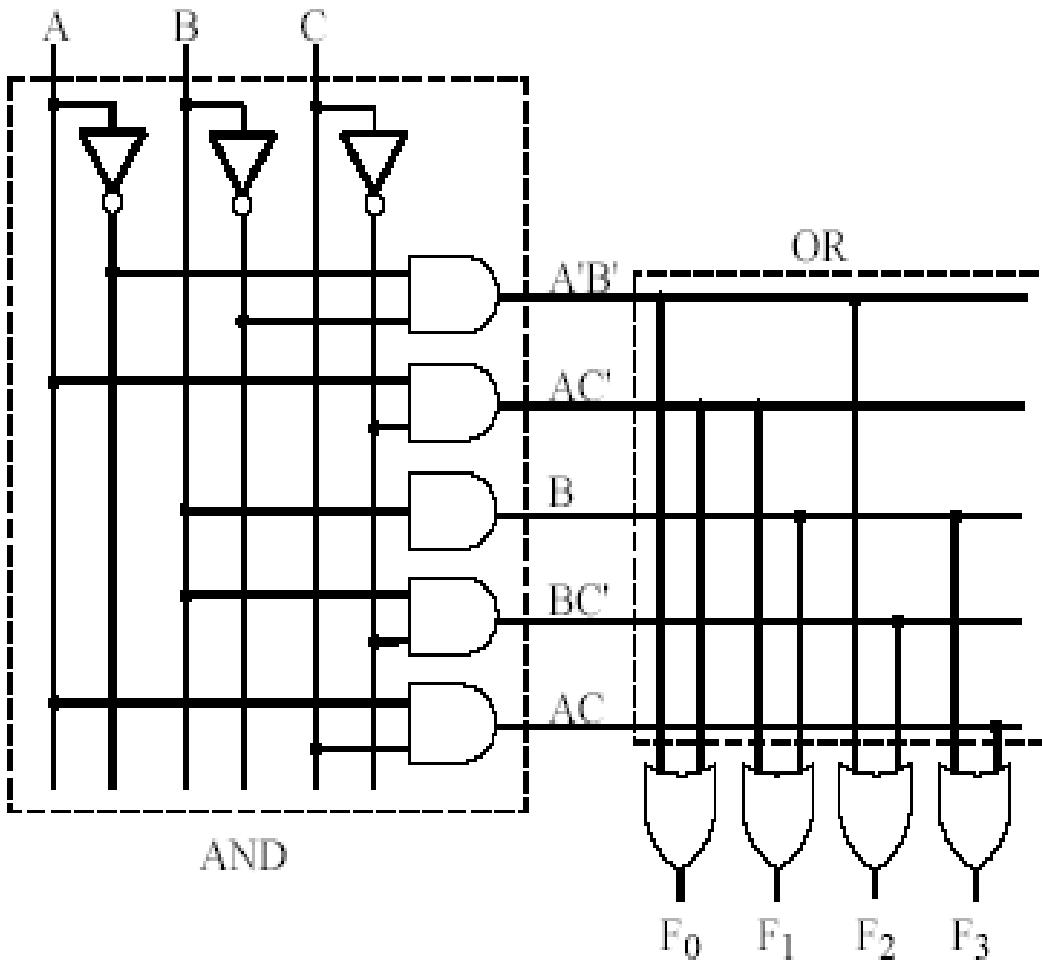
$$F_2 = \Sigma m(0, 1, 2, 6)$$

$$= A'B' + BC'$$

$$F_3 = \Sigma m(2, 3, 5, 6, 7)$$

$$= AC + B$$

AND-OR ARRAY EQUIVALENT OF NMOS 3 INPUT 5 PRODUCT TERMS AND 4 OUTPUTS



Product	Inputs			Outputs			
	A	B	C	F_0	F_1	F_2	F_3
$A'B'$	0	0	-	1	0	1	0
AC'	1	-	0	1	1	0	0
B	-	1	-	0	1	0	1
BC'	-	1	0	0	0	1	0
AC	1	-	1	0	0	0	1

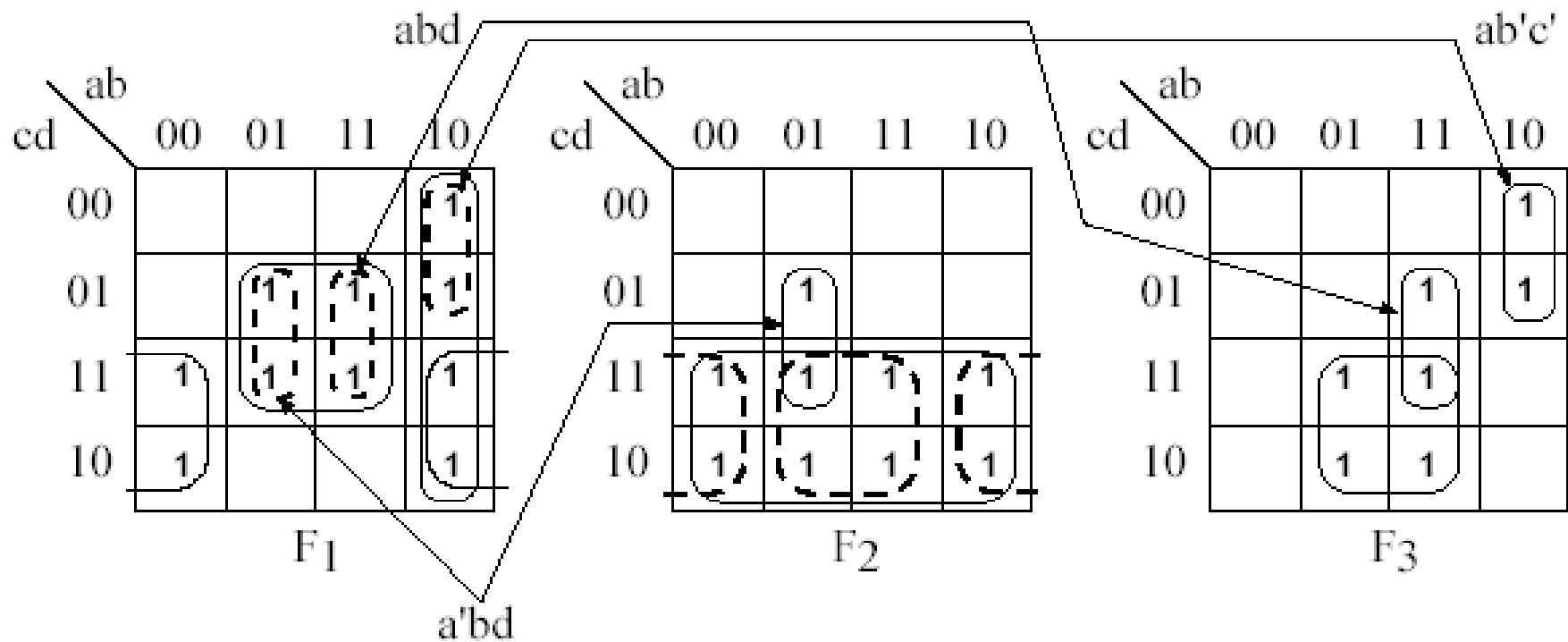
PLA table

REALIZATION OF PLA FOR A GIVEN EQUATION

$$F_1 = \Sigma m(2,3,5,7,8,9,10,11,13,15) = BD + B'C + AB'$$

$$F_2 = \Sigma m(2,3,5,6,7,10,11,14,15) = C + A'BD$$

$$F_3 = \Sigma m(6,7,8,9,13,14,15) = BC + AB'C' + ABD$$



REALIZATION OF PLA FOR A GIVEN EQUATION

a	b	c	d	F1	F2	F3
0	1	-	1	1	1	0
1	1	-	1	1	0	1
1	0	0	-	1	0	1
-	0	1	-	1	1	0
-	1	1	-	0	1	1

$$\begin{aligned}F1 &= bd(a+a') + b'c + ab'(c+c') \\&= abd + a'bd + b'c + ab'c' + ab'c\end{aligned}$$

$$\begin{aligned}F2 &= c(b+b') + a'bd \\&= bc + b'c + a'bd\end{aligned}$$

$$F3 = bc + ab'c' + abd$$

$$F1 = a'bd + abd + ab'c' + b'c$$

$$F2 = a'bd + b'c + bc$$

$$F3 = abd + ab'c' + bc$$

Reduced PLA table

REALIZATION OF PLA FOR A GIVEN EQUATION

PLA Realization of Equations

