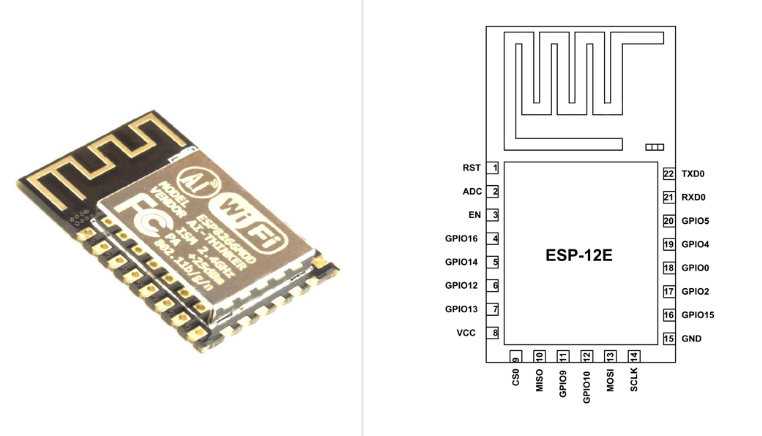
**1. ESP8266-12E WI-FI Module**

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* It’s a WI FI module used for wireless connection.
* consists of 22 pins and they are

|  |  |  |
| --- | --- | --- |
| **Pin** | **Name** | **Description** |
| 1 | RST | Reset Pin of the module |
| 2 | ADC | A/D Conversion. Input voltage range 0-1v,scope:0-1024 samples |
| 3 | EN | Enable Pin (Active HIGH) |
| 4 | GPIO16 | GPIO16: can be used to wake up the chipset from deep sleep mode. |
| 5 | GPIO14 | GPIO14/HSPI\_CLK |
| 6 | GPIO12 | GPIO12/HSPI\_MISO |
| 7 | GPIO13 | GPIO13/HSPI\_MOSI/ UART0\_CTS |
| 8 | VDD | +3.3V Power supply |
| 9 | CS0 | Chip selection Pin of SPI interface |
| 10 | MISO | MISO Pin of SPI interface |
| 11 | GPIO9 | GPIO9 |
| 12 | GPIO10 | GPIO10 |
| 13 | MOSI | MOSI Pin of SPI interface |
| 14 | SCLK | Clock Pin of SPI interface |
| 15 | GND | Ground Pin |
| 16 | GPIO15 | GPIO15/HSPICS/UART0\_RTS |
| 17 | GPIO2 | GPIO2/UART1\_TXD |
| 18 | GPIO0 | GPIO0 |
| 19 | GPIO4 | GPIO4 |
| 20 | GPIO5 | GPIO5 |
| 21 | RXD0 | UART0 RXD /GPIO3 |
| 22 | TXD0 | UART0 TXD /GPIO1 |

**Features**

* Supports 802.11 b/g/n
* Low power 32-bit MCU
* It has 10-bit ADC.
* 512kB Flash Memory.
* Supports TCP/IP protocol stack.
* Integrated power amplifier and matching network.
* Integrated PLL, regulators, and power management units.
* Supports antenna diversity.
* Support STA/AP/STA+AP operation modes.
* Support Smart Link Function for both Android and iOS devices.
* Support, (H) SPI, UART, I2C, I2S, PWM, GPIO.
* STBC, 1x1 MIMO, 2x1 MIMO.
* A-MPDU & A-MSDU aggregation and 0.4s guard interval.
* Deep sleep power < 5uA.
* Wake up and transmit packets in < 2ms.
* Standby power consumption of < 1.0mW.
* Operating temperature range -40C ~ 125C.

**Parameters**

* Operating voltage is 3.0~3.6V
* Frequency range is 2.4GHz
* Operating current is 80mA
* Wi-Fi 2.4 GHz, support WPA/WPA2 security
* Supports encryption of WEP/AES
* Wi-Fi mode will be station/softAP/softAP+station
* Network protocols used are TCP/IP v4/UDP/FTP/HTTP

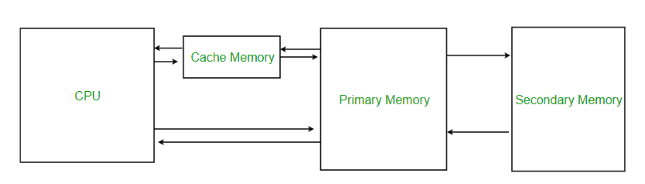
**Important Terminologies**

**1. Non volatile memory (NVM)**

* It is used to store the data and retain the data without electrical power i.e. no data is lost when the computer or device is power off.

**2. Cache Memory**.

* It is used to speed up and synchronizing with high-speed CPU.
* Cache memory is an extremely fast memory type that acts as a buffer between RAM and the CPU.
* It holds frequently requested data and instructions so that they are immediately available to the CPU when needed.
* Cache memory is used to reduce the average time to access data from the Main memory.
* Cache memory is costlier than main memory
* The cache is a smaller and faster memory which stores copies of the data from frequently used main memory locations.



**3**. **Digital buffer**

* It’s an electronic circuit used to isolate the input from the output, providing either no voltage or input voltage. It draws very little current and will not disturb the original circuit.

**4. Buffer cache**

* Reading the information from disk only once it will take more time for the first time and then keeping it in memory until it is needed is called disk buffering, and the memory used for the purpose is called the buffer cache

**5. Buffer vs. Cache**

* Buffer's policy is FIFO.
* Cache's policy is Recently Used.

***6.* Static random-access memory (SRAM)**

* SRAM is [volatile memory](https://en.wikipedia.org/wiki/Volatile_memory).
* Data is lost when power is turned off.
* Uses flip-flop to store each bit.
* SRAM is faster and more expensive.
* SRAM space that is available to users is assigned as below RAM size < 36kB
* There is no programmable ROM in the SOC; therefore, user program must be stored in an external SPI flash.

**7. Flash memory**

* [Non volatile](https://en.wikipedia.org/wiki/Non-volatile_memory) [computer memory](https://en.wikipedia.org/wiki/Computer_memory) [storage medium](https://en.wikipedia.org/wiki/Computer_data_storage) that can be electrically erased and reprogrammed.
* The two main types of flash memory are [NAND](https://en.wikipedia.org/wiki/NAND_gate) and [NOR](https://en.wikipedia.org/wiki/NOR_gate) [logic gates](https://en.wikipedia.org/wiki/Logic_gate).

**8. 32-bit Microcontroller (MCU)**

* It has 32-bit arithmetic logic units, registers, and bus width.
* It means processor/controller can process on 32 bit data.
* Extra low power consumption and 16-bit RSIC
* The CPU clock speed is 80MHz. It can also reach a maximum value of 160MHz.

**9. Analog to digital converter (ADC)**

* Accepts an analog input a voltage or a current and converts it to a digital value that can be read by a microprocessor/controller.
* The resolution of the ADC is the number of bits it uses to digitize the input samples.
* For an n bit ADC the number of discrete digital levels that can be produced is 2^n. Thus, a 12 bit digitizer can resolve 4096 levels.
* A 10-bit ADC has 2^10 or 1,024 possible output codes. So the resolution is 5V/1,024, or 4.88mV

**10. Phase locked loop or phase lock loop (PLL)**

* It is a [control system](https://en.wikipedia.org/wiki/Control_system) that generates an output [signal](https://en.wikipedia.org/wiki/Signal_(electrical_engineering)) whose [phase](https://en.wikipedia.org/wiki/Phase_(waves)) is related to the phase of an input signal.
* It’s a feedback circuit consists of voltage driven oscillator to monitor and constantly adjust in order to match the frequency of an input signal.
* A phase-locked loop can track an input frequency, or it can generate a frequency that is a multiple of the input frequency.
* These properties are used for computer clock synchronization, [demodulation](https://en.wikipedia.org/wiki/Demodulation), and [frequency synthesis](https://en.wikipedia.org/wiki/Frequency_synthesis).
* It is widely used in communication system.

11. **Antenna diversity**/**space diversity**/**spatial diversity**

* Uses two or more antennas to improve the quality and reliability of a wireless link.
* There is no clear [line-of-sight](https://en.wikipedia.org/wiki/Line-of-sight_propagation) (LOS) between transmitter and receiver.
* Instead the signal is reflected along multiple paths before finally being received.
* Each of these bounces can introduce phase shifts, time delays, attenuations, and distortions that can destructively interfere with one another at the aperture of the receiving antenna.

**12. Secure Digital Input Output (SDIO)**

* Type of Secure Digital card interface.
* It can be used as an interface for input or output devices.

**13. Space time block coding (STBC)**

* It is a technique used in [wireless communications](https://en.wikipedia.org/wiki/Wireless) to transmit multiple copies of a data stream across a number of [antennas](https://en.wikipedia.org/wiki/Antenna_(radio)) and to exploit the various received versions of the data to improve the reliability of data transfer.

**14. Soft AP**

* A common method of configuring Wi-Fi products without a display or input device, such as a Wi-Fi enabled appliance, home security camera, smart home product or any other [IOT](https://en.wikipedia.org/wiki/Internet_of_things) device.

**15. Wi-Fi Protected Access (WPA)**

* Security and security certification programs developed by the Wi-Fi Alliance to secure wireless computer networks.

**16. Wired Equivalent Privacy (WEP)**

* It is a security algorithm for IEEE 802.11 wireless networks. Introduced as part of the original 802.11 standard approved in 1997, its intention was to provide data confidentiality comparable to that of a traditional wired network.

**17. Advanced Encryption Standard (AES)**

The [encryption](https://en.wikipedia.org/wiki/Encryption) of electronic data established by the U.S. [National Institute of Standards and Technology](https://en.wikipedia.org/wiki/National_Institute_of_Standards_and_Technology) (NIST) in 2001.

**18. External SPI Flash**

* 4 MB external SPI flash to store user programs.
* Up to 16 MB memory capacity can be supported.
* OTA is disabled: the minimum flash memory that can be supported is 512 kB.
* OTA is enabled: the minimum flash memory that can be supported is 1 MB.
* Several SPI modes can be supported, including Standard SPI, Dual SPI, and Quad SPI.

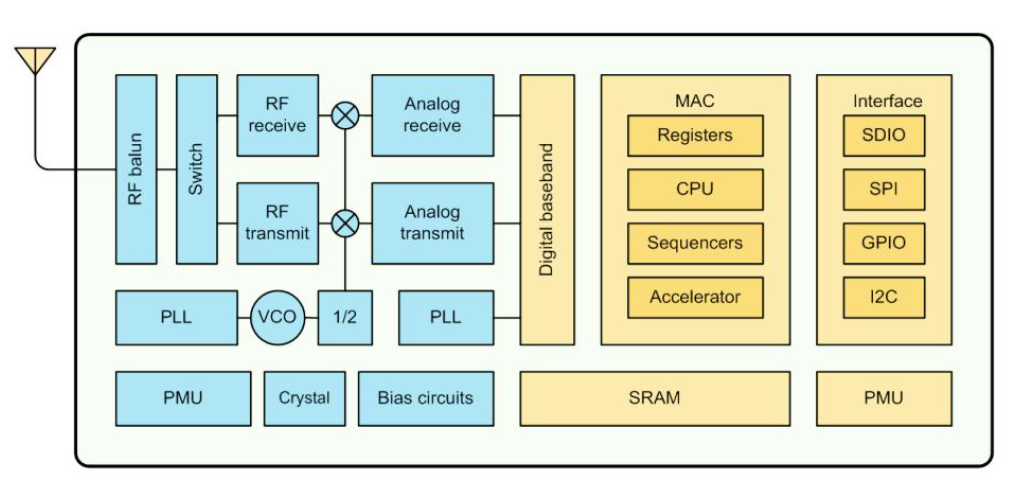
**19. Crystal frequency**

* Frequency of crystal oscillators supported includes 40MHz, 26MHz and 24MHz.
* In circuit design, capacitors C1 and C2, which are connected to the earth, are added to the input and output terminals of the crystal oscillator respectively.
* The values of the two capacitors can be flexible, ranging from 6pF to 22pF
* Normally, the capacitive values of C1 and C2 are within 10pF if the crystal oscillator frequency is 26MHz, while the values of C1 and C2 are 10pF.

**20. Power Consumption**

* Modem-Sleep requires the CPU to be working, as in PWM or I2S applications. According to 802.11 standards, it saves power to shut down the Wi-Fi Modem circuit while maintaining a Wi-Fi connection with no data transmission. E.g. in DTIM3, to maintain a sleep 300ms wake 3ms cycle to receive AP’s Beacon packages, the current is about 15mA.
* During Light-Sleep, the CPU may be suspended in applications like Wi-Fi switch. Without data transmission, the Wi-Fi Modem circuit can be turned off and CPU suspended to save power according to the 802.11 standard. E.g. in DTIM3, to maintain a sleep 300ms wake 3ms cycle to receive AP’s Beacon packages, the current is about 0.9mA.
* Deep Sleep does not require Wi-Fi connection to be maintained. For application with long time lags between data transmission, e.g. a temperature sensor that checks the temperature every 100s, sleep 300s and waking up to connect to the AP (taking about 0.3~1s), the overall average current is less than 1mA.

**Block Diagram of ESP8266EX**

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**RF Balun**

* Blaun is electronic device that converts between balanced signal and unbalanced signal.
* In order to connect different lines of impedance RF balun is used eg: transformation of 450 ohm balanced signal to 75 ohm unbalanced signal.
* It is used as a common mode choke which rejects high frequency signal and passes low frequency signal.
* To broadcast a signal RF balun is used
* Improved noise immunity and better RF performance.
* Balun acts a RF transmission line
* Switch is used whether to transmit or receive the signals.

**RF receiver and transmitter**

* A receiver receives the modulated RF and demodulates signal.
* Transmitter is capable of transmitting a radio wave and modulating that wave to carry data.

**PLL**

* It is a [control system](https://en.wikipedia.org/wiki/Control_system) that generates an output [signal](https://en.wikipedia.org/wiki/Signal_(electrical_engineering)) whose [phase](https://en.wikipedia.org/wiki/Phase_(waves)) is related to the phase of an input signal.
* It’s a feedback circuit consists of voltage driven oscillator to monitor and constantly adjust in order to match the frequency of an input signal.
* A phase-locked loop can track an input frequency, or it can generate a frequency that is a multiple of the input frequency.
* These properties are used for computer clock synchronization, [demodulation](https://en.wikipedia.org/wiki/Demodulation), and [frequency synthesis](https://en.wikipedia.org/wiki/Frequency_synthesis).
* Divider circuit is used to divide the frequency by 2.

**VCO**

* Oscillation frequency is controlled by an input voltage.
* Input voltage determines the oscillation frequency.
* Used for frequency modulation or phase modulation by applying a modulating signal to the input.
* Integral part of the PLL.

**Analog Receive and transmit**

* Receiver converts analog signal and converts to digital bit stream.
* Transmitter converts digital bit stream to analog signal.

**Digital baseband**

* It acts as both Transmitter as well as receiver.
* Also known as line coding (representation in digital bits).
* Transfer or receive a digital bit stream over a channel typically a wire.

**Power management Unit (PMU)**

* It’s a microcontroller, manages power functions of digital platforms.

Function:

* Monitors power conversion.
* Charging batteries.
* Controlling power to other integrated circuits.
* Shutting down unnecessary components which are using power.
* Controlling sleep and power functions.
* Regulating the RTC.

**Crystal frequency**

* Microcontroller and processor CPU uses crystal frequency.
* Provide an efficient frequency oscillation.
* Produces a stable output for long time.

**Biasing Circuit**

* Used to establish a fixed level of voltage or current.
* Setting an initial operating condition.
* Operating point is known as bias point.
* Circuits include transistor logic.

**SRAM**

* SRAM is [volatile memory](https://en.wikipedia.org/wiki/Volatile_memory).
* Data is lost when power is removed.
* Uses flip-flop to store each bit.
* SRAM is faster and more expensive.
* SRAM space that is available to users is assigned as below RAM size < 36kB.
* There is no programmable ROM in the SOC; therefore, user program must be stored in an external SPI flash.

**MAC**

* Includes registers which are costly and fast accessible storage. It will be having some specific functions i.e. read or write.
* Includes sequencers that provide a sequence numbers for the data in order to store the data in sequence order.
* Includes Accelerator used to increase the CPU performance
* It has CPU in it manages all the data, communication and other control signals.

**Interface**

* GPIO: It is an uncommitted digital signal pin on an [integrated circuit](https://en.wikipedia.org/wiki/Integrated_circuit) or electronic circuit board whose behavior including whether it acts as input or output is controllable by the user at [run time](https://en.wikipedia.org/wiki/Run_time_(program_lifecycle_phase)).
* I2C:  It is widely used for attaching lower speed peripheral [ICs](https://en.wikipedia.org/wiki/Integrated_circuit) to processors and [microcontrollers](https://en.wikipedia.org/wiki/Microcontroller) in short distance, intra-board communication.
* SPI: It is a [synchronous](https://en.wikipedia.org/wiki/Synchronous_circuit) [serial communication](https://en.wikipedia.org/wiki/Serial_communication) interface specification used for short distance communication
* SDIO: Type of Secure Digital card interface. It can be used as an interface for input or output devices.

**Flash Memory**

* Electronic non volatile storage medium.
* It can be electrically erased and reprogrammed.
* There are 2 types NAND and NOR.
* NAND flash memory may be erased, written, and read in blocks.
* NOR flash memory allows single word or byte to be written to an erased location and to read.
* Flash memory stores information in an array of memory cells made from floating gate transistor.
* In single level cell device each cell stores only one bit information.
* In multi level cell device can store multiple bits.
* It can be read or programmed a byte or word at a time.
* It can be erased only a block at a time.
* NOR flash allows random access reading.
* NAND flash allows only page access.
* Flash memory devices are typically fast at reading than writing.
* Performance depends upon the quality of storage controllers.
* Serial flash is a low power flash memory that provides only serial access to the data rather than addressing.
* In order to increase a speed code is copied from flash into ram before execution.

**Static Random Access Memory (SRAM)**

* Retains the data bits till power is ON.
* Use flip flops to store the each bit.
* Volatile memory i.e. data is lost when power is removed.
* Faster and more expensive.
* Power consumption depends on how frequently it is accessed.
* Faster access of data.
* SRAM is used for computer cache memory.
* With asynchronous interface access up to 16MB in general purpose products.
* With synchronous interface access up to 18MB in general purpose products.
* In microcontrollers uses around 32bytes to 128Kbps.
* In microprocessor uses around 8kbps to many Mbps.
* ESRAM i.e. some amount is also embedded in some products to implement user interface.
* DRAM is used for main memory which has refresh cycles.
* SRAM operates in 3 states i.e. standby, read, write

**Types of SRAM**

**Non volatile SRAM (NVSRAM)**

* It has a standard SRAM function.
* NVSRAM stores the important and critical data when power is lost.
* Used in wide range i.e. networking, aerospace, medical etc.

**Pseudo SRAM**

* It has DRAM storage core with self refresh circuit.
* Slower than SRAM
* Cost advantage over SRAM.

**By Transistor type**

* BJT (used in TTL and ECL) - very fast but consumes a lot of power.
* MOSFET(used in CMOS)-low power and very commonly used

**By function**

* Asynchronous- independent of clock frequency
* Synchronous- depends on clock edge.

### By feature

* [Zero bus turnaround](https://en.wikipedia.org/w/index.php?title=Zero_bus_turnaround&action=edit&redlink=1) (ZBT) – the turnaround is the number of clock cycles it takes to change access to the SRAM from write to read and vice versa.
* [sync Burst](https://en.wikipedia.org/w/index.php?title=SyncBurst&action=edit&redlink=1) (sync Burst SRAM or synchronous burst SRAM) – write access to the SRAM to increase write operation to the SRAM
* [DDR SRAM](https://en.wikipedia.org/w/index.php?title=DDR_SRAM&action=edit&redlink=1) – Synchronous, single read/write port, double data rate I/O
* [Quad Data Rate SRAM](https://en.wikipedia.org/wiki/Quad_Data_Rate_SRAM) – Synchronous, separate read and write ports, quadruple data rate I/O.

### By flip-flop type

* Binary SRAM.
* [Ternary](https://en.wikipedia.org/wiki/Ternary_computer) SRAM.

**General purpose input and output (GPIO)**

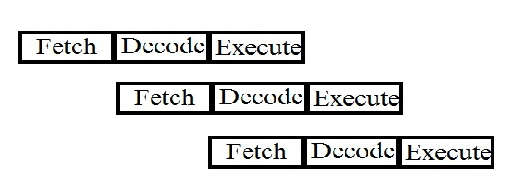
* It’s a digital Signal pin on the IC.
* It acts as input or output controlled by the user.
* In IC’s provide GPIO as a primary function.
* Microcontroller will have GPIO’s depending upon the application interface with the external circuits.
* In microcontroller GPIO pin will have alternate function.
* These pins are programmable controlled.
* In some of the electronic boards will expose GPIO through connectors for external device.
* All the GPIO pins are configurable.
* It may be damaged by greater voltage.
* It is used to control devices such as lights, solenoids, motors etc.
* Many GPIO lines can be used as parallel interface for communication i.e. I2C.
* GPIO pins can be configured to be input or output.
* GPIO pins can be enabled or disabled.
* Input values are readable.
* Output values are readable and writable
* Input values can be used as interrupt.

**RISC**

* Reduced Instruction Set Computing.
* In order to produce more CPU power, instruction set is less.
* Pipelining is introduced in order to execute more efficiently.
* Instruction uses only few addressing modes.
* Instructions are fixed length and uniform format.
* Large number of registers is available to prevent interaction with the memory.
* Register to Register operation.
* Take 1 clock cycle per instruction to execute except LOAD and STORE instruction it will take 2 clock cycles per instruction to execute.
* LOAD and STORE are the only instructions will access memory.
* By using RISC reduces the execution time.
* Used in portable devices.

**Pipelining**

The process of fetching the next instruction when the present instruction is being executed is called pipelining.



### Advantages of Pipelining

* Instruction throughput increases.
* Increase in the number of pipeline stages increases the number of instructions executed simultaneously.
* Faster ALU can be designed when pipelining is used.
* Pipelined CPU’s works at higher clock frequencies than the RAM.
* Pipelining increases the overall performance of the CPU.

**Difference between RISC and CISC**

|  |  |  |
| --- | --- | --- |
| Function | CISC | RISC |
| * Instruction Size * Instruction Length * Number of Instruction * Execution Speed * Registers Used * Hardware * Memory access * Pipelined | * Varies * 1,2,3 or 4 bytes * More * Slow * Less * complex * Frequently * not pipelined | * Fixed * 4 bytes * Less * More compared to CISC * More * simple * Rarely * Highly Pipelined |