Roll No. 6211[redacted]

Total No. of Questions : 9] [Total No. of Printed Pages : 7

(2042)

B.C.A. (CBCS) RUSA IInd Semester Examination

3745

DIGITAL ELECTRONICS

Paper : BCA-0203

Time : 3 Hours] **[Maximum Marks : 70**

Note :– (i) Question No. **1** (Part–A) is compulsory. Attempt *four* questions choosing *one* question each from Part–B, C, D and E.

(ii) Figures at the right indicate marks.

Part–A

(Compulsory Question)

1. (A) Select the correct alternative for MCQs.

(i) With forward bias to a *pn* junction, the width of depletion layer :

(a) Increases

(b) Decreases

(c) Remains the same

(d) None of these

(ii) A digital circuit that can store only one bit is a :

(a) Register

(b) NOR gate

(c) Flip-flop

(d) XOR gate

(iii) The logical sum of two or more than two logical products is termed as :

(a) OR operation

(b) POS

(c) SOP

(d) NAND operation

(iv) Which of the given logic family provide minimum power dissipation ?

(a) JFET

(b) CMOS

(c) ECL

(d) TTL

(v) The number of inputs in a half adder is :

(a) 8

(b) 2

(c) 11

(d) 32

(vi) What is the value to be considered for a 'don't care condition' ?

(a) 0

(b) 1

(c) Either 0 or 1

(d) Any number except 0 and 1

(vii) Which device has one input and many outputs ?

(a) Multiplexer

(b) Demultiplexer

(c) Counter

(d) Flip-flop

(viii) A K-map of n-variables contains ..... cells.

(ix) The condition S = R = 1 is called as ..... condition.

(x) CMOS stands for ..... 1×10=10

(B) Answer the following in **25** to **50** words :

(i) Describe combinational circuit.

(ii) Distinguish between TTL and CMOS families.

(iii) Draw symbol and truth table of OR, NOT and NAND gate.

(iv) Explain the function of J-K Flip-flop.

(v) Draw the circuit diagram of an 8-input multiplexer. 4×5=20

Part–B

(Unit–I) 10 each

2. Discuss in detail Bipolar Junction Transistor and draw its circuit symbol.

3. Explain the non-saturated bipolar logic family, ECL in detail.

Part–C

(Unit–II)

4. Explain the various laws of Boolean algebra. Also state De-Morgan's theorem with example. 10

5. (a) Discuss 'NAND gates are Universal Gate'.

   (b) Draw the circuit diagram of NOR gate and also give its truth table. 6,4

Part–D

(Unit–III) 10 each

6. Simplify the following Boolean function using K-map and draw the circuit for simplified expression :

   $F(W, X, Y, Z) = \Sigma(0, 2, 4, 5, 9, 11, 14, 15)$

7. Explain the SOP form and POS form of simplifying Boolean expression using K-maps.

Part–E

(Unit–IV) 10 each

8. What is a Flip-flop ? Compare the operations of D and T Flip-flops with the help of their truth-table.

9. Draw and explain the working of Full Adder Circuit with Truth-table

Pihu Kashyap

Total No. of Questions : 9] [Total No. of Printed Pages : 4

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BCA (CBCS) IInd Semester Examination

7074

DIGITAL ELECTRONICS

BCA-203

Time : 3 Hours] [Maximum Marks : 70

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/ continuation sheet will be issued.

Note :- Attempt any *five* questions in all. Select *one* question each from Units I, II, III and IV. Unit V (Q. No. 9) is compulsory.

Unit–I

1. (a) Discuss the characteristics of transistor-transistor logic and emitter-coupled logic digital families. 9

   (b) Write short notes on Integrated circuits. 5

2. (a) Explain the forward and reverse biasing of p-n junction. 10

   (b) Explain valence and conduction bonds in solids. 4

Unit–II

3. (a) Prove the following expressions using Boolean algebra :

(i) $(A + B) \cdot (\bar{A} + C) = AC + \bar{A}B$

(ii) $A + \bar{A}B + A\bar{B} = A + B$ 7

(b) Give the logic symbol and truth tables for the following combinational gates :

(i) Exclusive OR gate

(ii) Exclusive NOR gate 7

4. (a) Explain basic Boolean Law's with suitable examples. 5

(b) Apply Demorgan's theorem to the following expressions :

(i) $\overline{(W + X)Y}$

(ii) $\overline{(A + \bar{B} + C + \bar{D})}$

(iii) $\overline{\bar{X} + \bar{Y} + \bar{Z}}$ 9

Unit–III

5. (a) Simplify the following Boolean function by using K-map and implement it using NoR gates.

$f(ABCD) = \Sigma m(2, 3, 4, 5, 6, 7, 11, 14, 15)$ 10

(b) Give the sum of Product expression of AND-OR realization. 4

6. (a) Explain the minimization technique for 4-variables by giving minterms and maxterms. 7

(b) Distinguish between algebraic method and Karnaugh method for minimisation of Boolean expressions. 7

Unit–IV

7. (a) Give the logic diagram and truth table for a Half-Adder. 8

(b) What is an encoder ? Give the truth table for octal to binary encoder 6

8. (a) What is a sequential circuit ? Explain its types. 6

(b) Give the construction of Master-Slave JK flip-flop. 8

Unit–V (Compulsory Question)

9. Attempt all parts :

(i) Define K-Map.

(ii) .....is a universal gate.

(iii) Differentiate between intrinsic and extrinsic semiconductors.

(iv) Explain race around conditions in flip-flops.

(v) Give the truth table for NAND gate.

(vi) Write the Boolean expression for a 2-input NOR gate.

(vii) Simplify $Y = \bar{A}Q + AQ$ 2×7=14

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Total No. of Questions : 9] [Total No. of Printed Pages : 7

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B.C.A. (CBCS) RUSA IInd Semester Examination

4387

DIGITAL ELECTRONICS

Paper : BCA-0203

Time : 3 Hours] **[Maximum Marks : 70**

Note :– Attempt *five* questions in all, selecting one question each from Unit–I to Unit–IV. Part–A (Q. No. 1) is compulsory.

Part–A

(Compulsory Question)

1. (A) Attempt all parts. Select the correct option for MCQ's.

(i) The output of an AND gate with 3-inputs A, B and C is HIGH when :

(a) A = 1, B = 1, C = 0

(b) A = 0, B = 0, C = 0

(c) A = 1, B = 0, C = 0

(d) A = 1, B = 1, C = 1 8.

(ii) When used with an IC, what does the term 'QUAD' indicate ?

(a) 2 circuits

(b) 4 circuits

(c) 8 circuits

(d) 6 circuits 9

(iii) The format used to present the logic output for the various combinations of logic inputs to a gate is called a (an) :

(a) Boolean Constant

(b) Boolean Variable

(c) Truth Table

(d) Input Logic Function

(viii) On the Master-Slave flip-flop, when it is master enabled ?

(a) When the gate is HIGH

(b) When the gate is LOW

(c) Both of these

(d) None of these

(ix) Under normal conditions a diode conducts current when it is :

(a) Reverse biased

(b) Forward biased

(c) Saturated

(d) Avalanched

(x) An *n*-type semiconductor material :

(a) is intrinsic

(b) has trivalent impurity atoms added

(c) has pentavalent impurity atoms added

(d) requires no doping 1×10=10

(iv) Which of the following expressions is in the sum-of-products (SOP) form ?

(a) (A + B) (C + D)

(b) (A) B (CD)

(c) AB + CD

(d) AB (CD)

(v) The commutative law of Boolean addition states that A + B = A × B. (True/False)

(vi) The Boolean expression C + CD is equal to ..... .

(vii) When transistors are used in digital circuits they usually operate in the :

(a) active region

(b) breakdown region

(c) saturation and cutoff regions

(d) linear region

(b) Give the circuit diagram of XOR gate. Also give its truth table. 4,6

5. (a) How can you connect NAND gates to get an OR gate ?

(b) What are the two basic rules used to draw equivalent gates ? 6,4

Part–D

(Unit–III)

6. (a) Simplify the following function in sum-of-product SOP form using four variable Karnaugh's map :

$F(A, B, C, D) = \Sigma m\ (0, 1, 2, 3, 4, 5, 7, 11, 15)$

(b) What are redundant groups in K-map ? 8,2

7. (a) Explain how basic gates can be realized using NAND gates. Also give the diagram.

(b) What do you mean by Combinational Circuit ? 6,4

(B) Answer the following in **25** to **50** words :

(i) State the associative property of Boolean Algebra.

(ii) What is meant by Karnaugh map method ?

(iii) State advantages and disadvantages of TTL.

(iv) What is a Decoder ?

(v) Define Minterm and Maxterm. 4×5=20

Part–B

(Unit–I)

2. (a) Discuss the working of *p-n* junction diode.

(b) Explain energy bands in solids. 5,5

3. (a) Discuss Saturated and Non-saturated Logic.

(b) Which is faster ECL or TTL ? Explain. 5,5

Part–C

(Unit–II)

4. (a) Simplify the expressions using Boolean Algebra :

(i) $A\bar{B}C + ABC$

(ii) $(\bar{A} + B + C)(A + B + \bar{C})$

Part–E

(Unit–IV)

8. (a) What is a Multiplexer ? Explain difference between MUX and DEMUX.

(b) What do you mean by Shift-Registers ? Discuss. 5,5

9. (a) Explain the working and circuit of a Half-Adder.

(b) Give the design of 3 × 8 decoder. 6,4

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Total No. of Questions : 9] [Total No. of Printed Pages : 3

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B.C.A. (CBCS) RUSA IInd Semester Examination

4029

DIGITAL ELECTRONICS

Paper : BCA-0203

Time : 3 Hours] **[Maximum Marks : 70**

Note :– Attempt *five* questions in all. Select *one* question from each Unit–I, II, III and IV. Question No. **9** (Unit–V) is compulsory.

Unit–I

1. (a) Explain Band theory in solids.

   (b) Discuss forward and reverse biasing of a *p-n* junction. 7,7

2. (a) Explain the characteristics of TTL, CMOS and ECL logic families.

   (b) Explain the working of Bipolar Junction Transistor. 8,6

7.0

Unit–II

3. (a) Explain basic logic gates and also give their truth tables. 8,6

(b) State and explain deMorgan's theorem.

4. (a) Simplify the following using Boolean Algebra :

(i) $\bar{A}B + AC + \bar{A}\bar{B}C$

(ii) $A + \bar{A}B + A\bar{B}$

(iii) $(A + B)\cdot(\bar{A} + C)$

(b) What are universal gates ? Show that NAND is a universal gate. 6,8

Unit–III

5. (a) Using four variable map, find the minimal SOP expression for the Boolean function :

$f(w, x, y, z) = \Sigma m(2, 5, 7, 9, 10, 11, 13, 15)$

(b) What is *k*-map ? What is the significance of pairs, quads and octets in a *k*-map ? 10,4

6. (a) Discuss the minimization technique for 4-variables by giving minterms and maxterms.

(b) Discuss Venn diagram by giving a suitable example. 8,6

Unit–IV

7. (a) Explain the working and logic diagram of a full adder with three inputs.

   (b) Design a decimal to BCD encoder circuit. 8,6

8. (a) What is a flip-flop ? Draw the circuit diagram of JK-flip-flop using NAND gate.

   (b) What is a multiplexer ? Give the logic diagram of 4 × 1 multiplexer. 7,7

Unit–V

(Compulsory Question)

9. Attempt all parts.

   (a) What is breakdown voltage ?

   (b) ..... and ..... are universal gates.

   (c) Give the Boolean expression for 2-input NOR gate.

   (d) What is a decoder ?

   (e) What is race-around condition in flip-flops ?

   (f) What do you mean by product of sum (POS) ?

   (g) What is CE configuration of a transistor ? 7×2=14

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Total No. of Questions : 9] [Total No. of Printed Pages : 3

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BCA (CBCS) RUSA IInd Semester Examination

3759

DIGITAL ELECTRONICS

Paper : BCA-203

Time : 3 Hours] [Maximum Marks : 70

Note :- Attempt *five* questions in all. Select *one* question from each Units I, II, III and IV. Question No. 9 (Unit–V) is compulsory.

Unit–I

1. (a) Differentiate between conductor, insulator and semiconductor on the basis of energy gap. 7

   (b) Explain depletion region. How is it formed in forward and reverse biasing ? 7

2. (a) Discuss the working of diode as switch. 7

   (b) Explain different types of transistor configurations. 7

Unit–II

3. (a) Prove the following using Boolean Algebra : 8

(i) $A + \bar{A}B + A\bar{B} = A + B$

(ii) $\bar{X}\bar{Y}\bar{Z} + \bar{X}Y\bar{Z} + X\bar{Y}\bar{Z} + XY\bar{Z} = \bar{Z}$

(b) Give the logic symbol and truth tables for NAND and NOR gates. 6

4. (a) Explain the basic laws of Boolean Algebra with suitable examples. 8

(b) Apply Demorgan's theorem to the following expressions : 6

(i) $\overline{(A+\bar{B})(\bar{C}+D)}$

(ii) $\overline{(A+B)C}$

(iii) $\overline{(\bar{A}+\bar{B}+\bar{C})}$

Unit–III

5. (a) Obtain the minimal POS expression for $f(ABCD) = \pi M (0, 1, 2, 4, 5, 6, 9, 11, 12, 13, 14, 15)$ and implement it using NOR gates. 9

(b) Give the Venn diagram for $\bar{B}+A$. 5

6. (a) Explain Don't-Care conditions in K-map using suitable example. 7

(b) Explain SOP and POS expressions with suitable examples. 7

Unit–IV

7. (a) Give the logic diagram and truth table for a full Adder. 8

(b) What is race-around condition in JK flip flops ? How it can be avoided ? 6

8. (a) Design a 16 × 1 MUX using four 4 × 1 multiplexers. 8

(b) What is a shift register ? Explain their types. 6

Unit–V

(Compulsory Question)

9. Explain the following :

(a) Bipolar Junction transistor

(b) Integrated circuits

(c) NAND gate as universal gate

(d) Karnaugh map

(e) Encoder

(f) Master-Slave flip flop

(g) BCD adder 7×2=14