PIHU Kashyap

Total No. of Questions: 9]

[Total No. of Printed Pages: 4

(1056)

BCA (CBCS) IInd Semester Examination 7074

DIGITAL ELECTRONICS BCA-203

Time: 3 Hours]

[Maximum Marks: 70

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/ continuation sheet will be issued.

Note :- Attempt any five questions in all. Select one question each from Units I, II, III and IV. Unit V (Q. No. 9) is compulsory.

Unit-I

l.	(B)	Discuss the characteristics of transistor-transistor logic and emitter-coupled logic digital families.	9
	(B)	Write short notes on Integrated circuits.	5
2	100	Explain the forward and reverse biasing of p-n	
		junction.	10
		Explain valence and conduction bonds in solids.	4
H	-69	T	Over

Unit-II

- (a) Prove the following expressions using Boolean algebra:
 - (i) $(A + B) \cdot (\overline{A} + C) = AC + \overline{A}B$

(ii) $A + \overline{A}B + A\overline{B} = A + B$

- (b) Give the logic symbol and truth tables for the following combinational gates:
 - (i) Exclusive OR gate
 - (ii) Exclusive NOR gate

4. (a) Explain basic Boolean Law's with suitable

examples.

- (b) Apply Demorgan's theorem to the following expressions:
 - (i) $\overline{(W+X)Y}$
 - (ii) $(A + \overline{B} + C + \overline{D})$
 - (iii) $\overline{\overline{X} + \overline{Y} + \overline{Z}}$

9

7

5

Unit-III

Simplify the following Boolean function by using K-map and implement it using NoR gates.

 $f(ABCD) = \Sigma m(2, 3, 4, 5, 6, 7, 11, 14, 15)$ 10

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(2)

 (b) Give the sum of Product expression of AND- OR realization. 4 OR realization. 5. (a) Explain the minimization technique for 4-variables by giving minterms and maxterms. 7 by giving minterms and maxterms. 7 Characteristic method and Karnaugh method for minimisation of Boolean expressions. 7
. Unit-IV
7. (a) Give the logic diagram and truth table for a Half-Adder. (b) What is an encoder? Give the truth table for octal to binary encoder 8. (a) What is a sequential circuit? Explain its types: (b) Give the construction of Master-Slave JK flipflop. Unit-V (Compulsory Question)
9. Attempt all parts :
(ii) Define K-Map. (iii)is a universal gate. (iii) Differentiate between intrinsic and extrinsic semiconductors.
H-69 (3) Turn Over

- (iv) Explain race around conditions in flip-flops.
- (v) Give the truth table for NAND gate.
- (vi) Write the Boolean expression for a 2-input NOR gate.
- (vii) Simplify $Y = \overline{A}Q + AQ$

2×7=14