Roll No. .....

Total No. of Questions : 9] [Total No. of Printed Pages : 7

(2043)

B.C.A. (CBCS) RUSA IInd Semester Examination

4207

DIGITAL ELECTRONICS

Paper : BCA-0203

Time : 3 Hours] **[Maximum Marks : 70**

Note :- (i) Question No. **1** (Part-A) is compulsory. Attempt *four* questions chosing *one* question each from Parts-B, C, D and E.

(ii) Figures at the right indicate marks.

Part–A

(Compulsory Question)

1. (A) Select the correct alternative for MCQs.

(i) Under normal conditions a diode conducts current when it is ..... .

(a) reverse biased

(b) forward biased

(c) avalanched

(d) saturated

(ii) In the toggle mode, a J-K flip-flop has :

(a) J = 0, K = 1

(b) J = 1, K = 1

(c) J = 0, K = 0

(d) J = 1, K = 0

(iii) De Morgan's law states that :

(a) (A + B)′ = A′ * B

(b) (AB)′ = A′ + B′

(c) (AB)′ = A′ + B

(d) (AB)′ = A + B

(iv) A K-map is an abstract form of which diagram organized as a square matrix :

(a) Block diagram

(b) Cycle diagram

(c) Square diagram

(d) Venn diagram

(v) TTL is a class of digital circuits built from :

(a) Resistors only

(b) JEFT only

(c) BJT only

(d) Both (a) and (c)

(vi) The basic storage element in a digital system is ..... .

(a) flip-flop

(b) counter

(c) multiplexer

(d) encoder

(vii) What will be the output from a D flip-flop if the clock is low and D = 0 ?

(a) 0

(b) 1

(c) No change

(d) Toggle between 0 and 1

(viii) Which of these sets of logic gates are known as universal gates ?

(a) XOR, NAND, OR

(b) OR, NOT, XOR

(c) NOR, NAND, XNOR

(d) NOR, NAND

(ix) A combinational circuit does not have ..... .

(x) Number of inputs for a full adder is ..... . 1×10=10

(B) Answer the following in **25** to **50** words :

(i) Distinguish between De-multiplexer and decoder.

(ii) Write a short note on don't care condition.

(iii) Give the applications and advantages of CMOS.

(iv) Explain BCD adder.

(v) Explain energy bands in solids. 4×5=20

Part–B

(Unit–I) 10 each

2. Discuss in detail the forward and reverse bias in *p-n* junction diode with suitable diagram.

3. What are digital logic families ? Compare all logic families and their characteristics.

Part–C

(Unit–II) 10 each

4. Simplify the following expressions using Boolean algebra :

(i) $Y = (A + B)\ (A + B')\ (A' + B')$

(ii) $Y = (C + D)' + A'CD' + (ABC)'$

$+ ABCD' + ACD'$

5. Discuss NOR, NAND and XOR gates in detail with truth table and symbols.

Part–D

(Unit–III) 10 each

6. Given :

$$F(A, B, C, D) = \Sigma(0, 2, 3, 6, 7, 12, 13, 14) + d(1, 4, 11, 15)$$

where d denotes the don't care condition.

Find simplified expression :

(i) In SOP form

(ii) In POS form, also realize the simplified expression using gates.

7. Define Combinational circuits. Discusss in detail the Karnaugh-map technique with suitable example.

Part–E

(Unit–IV) 10 each

8. Draw and write the truth table of J-K flip-flop. What is race around condition in J-K flip-flop ? How can it be avoided ?

9. Describe the need of a multiplexer in a system. Draw the logic diagram of 8 × 1 multiplexer and 2 × 4 decoder.