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B. E. (Third Semester) Examination, Nov.-Dec. 2016

(New Scheme)

(IT Branch)

DIGITAL ELECTRONICS and LOGIC DESIGN

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

Note : Attempt all questions. Part (a) from each question is compulsory. Attempt any two parts from (b), (c) and (d) of each question.

Unit-I

1. (a) Define K-map. 2

(b) Simplify the Boolean expression by using K-map

$$F(W, X, Y, Z) = \sum m(2, 3, 8, 10, 11, 12, 14, 15)$$

with logic diagram also. 7

(c) Simplify by the Tabular method. 7

$$F = \sum m(0, 1, 2, 5, 6, 7, 8, 9, 10, 14)$$

(d) Write short notes on : (any **two**) 7

(i) Demorgan's Theorem

(ii) Self complementing code & ASCII code

(iii) Universal Gate

Unit-II

2. (a) What is Logic Family? 2

(b) Explain Totem pole and open collector condition in TTL with circuit diagram. 7

(c) Define different parameters of Logic Family. 7

(d) Explain the working of CMOS inverter giving its circuit diagram & explain CMOS NOR gate function. 7

Unit-III

3. (a) Difference between Combinational Circuit & Sequential Circuit. 2

(b) Explain serial adder with require diagram. 7

(c) Explain full subtractor. 7

(d) Define Multiplexer and solve the boolean expression using 8 : 1 MUX. 7

$$F(A, B, C, D) = \sum m(0, 1, 2, 4, 5, 7, 9, 11, 13, 15)$$

Unit-IV

4. (a) Define Latchs. 2

(b) What is Shift Register? Give its types. 7

(c) Design a T-type counter that goes through states 0, 3, 5, 6, 0..... Is the counter self-starting. 7

(d) Design a BCD counter with JK flip flop. 7

Unit-V

5. (a) What are the different application of ROM? 2

(b) Difference among PROM, PLA and PAL. 7

(c) A combinational circuit is defined by the function

$$F_1(A, B, C) = \sum(3, 5, 6, 7)$$

$$F_2(A, B, C) = \sum(0, 2, 4, 7)$$

Implement the circuit with the PLA having 3 inputs, 4 product terms & two outputs. 7

(d) Difference between Meelay machine and Moore machine with example. 7