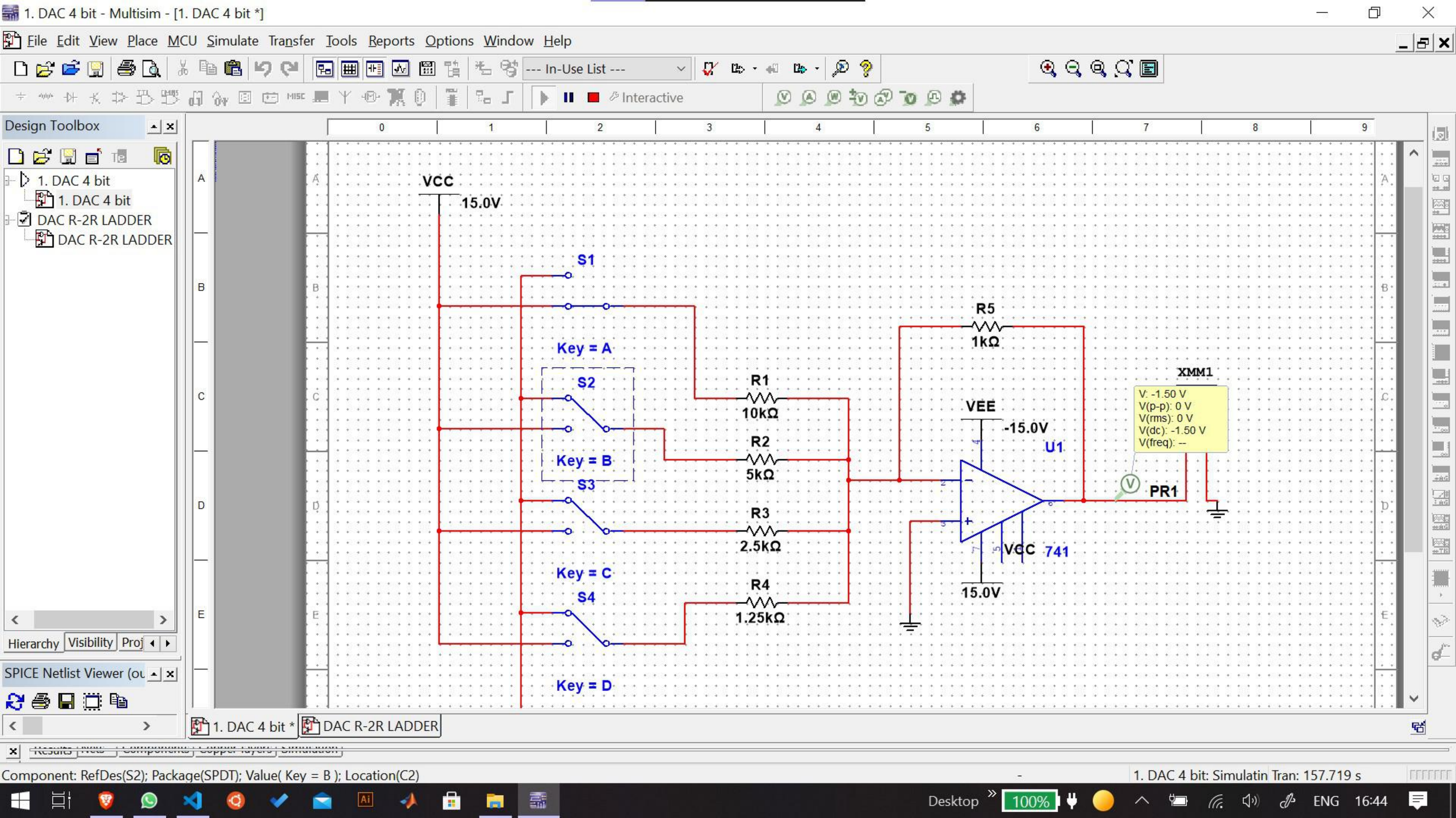

1. DAC 4 bit - Multisim - [1. DAC 4 bit *]
File Edit View Place MCU Simulate Transfer Tools Reports Options Window Help
--- In-Use List ---
Interactive
Design Toolbox
1. DAC 4 bit
1. DAC 4 bit
DAC R-2R LADDER
DAC R-2R LADDER
Hierarchy Visibility Proj
SPICE Netlist Viewer (ou
VCC
15.0V
S1
Key = A
S2
R1
10kΩ
R2
5kΩ
Key = B
S3
R3
2.5kΩ
Key = C
S4
R4
1.25kΩ
Key = D
R5
1kΩ
VEE
-15.0V
U1
XMM1
V: -1.50 V
V(p-p): 0 V
V(rms): 0 V
V(dc): -1.50 V
V(freq): --
PR1
VCC
741
15.0V
1. DAC 4 bit *
DAC R-2R LADDER
Component: RefDes(S2); Package(SPDT); Value(Key = B); Location(C2)
1. DAC 4 bit: Simulatin Tran: 157.719 s
Desktop
100%
ENG
16:44

DESIGN CALCULATION:

Pre Emphasis, $F_c = \frac{1}{2\pi(\frac{L}{R})}$ $R = 10k\Omega$, $f_c = 2.1kHz$

$$2.1\times10^3 = \frac{10\times10^3}{2\pi\times L}$$

$$L = \frac{10\times10^3}{2\times2.1\times\pi\times10^3}$$

$$\boxed{L = 0.75\,H}$$

De Emphasis: $R = 75k\Omega$, $f_c = 2.1kHz$

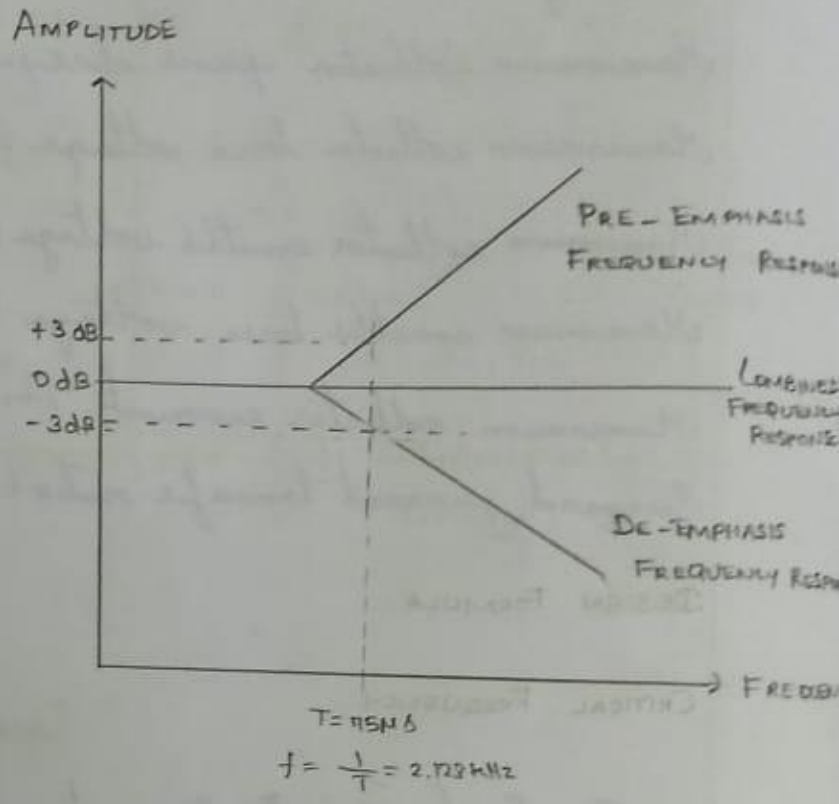
$$F_c = \frac{1}{2\pi RC}$$

$$C = \frac{1}{2\pi R f_c}$$

$$= \frac{1}{2\times\pi\times2.1\times75\times10^6}$$

$$\boxed{C = 1nF}$$

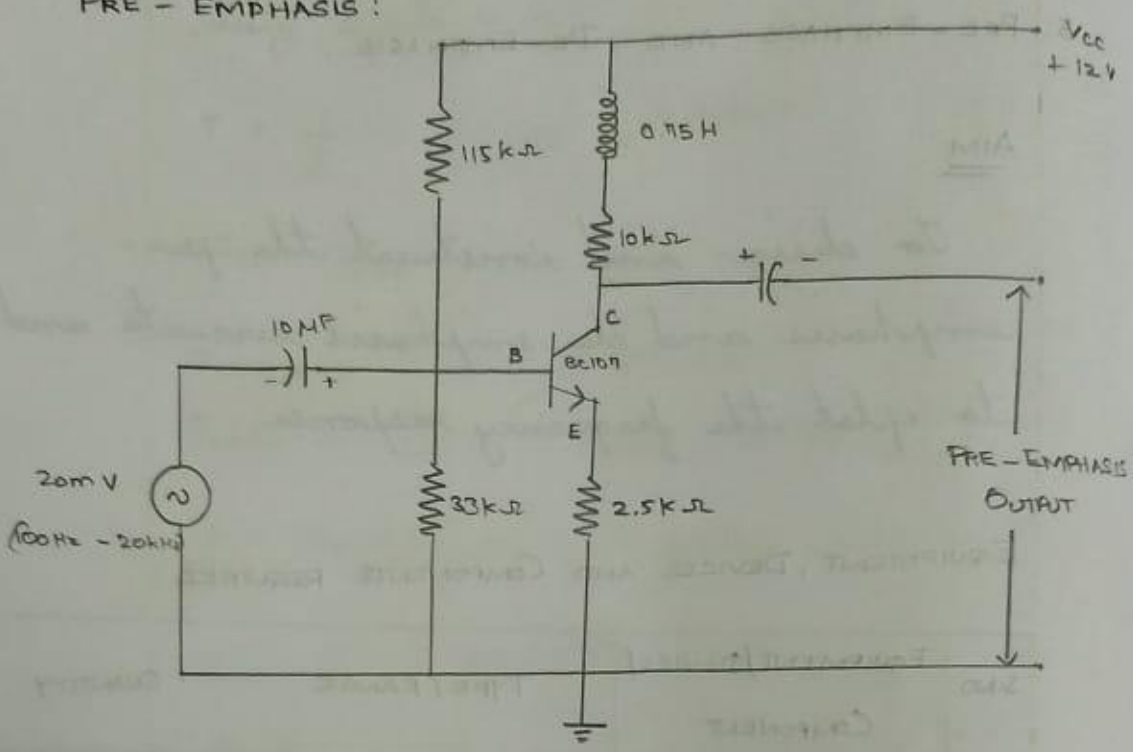
MODEL GRAPH :



COMBINED FREQUENCY RESPONSE :

CIRCUIT DIAGRAM:

PRE - EMPHASIS:



DE - EMPHASIS: