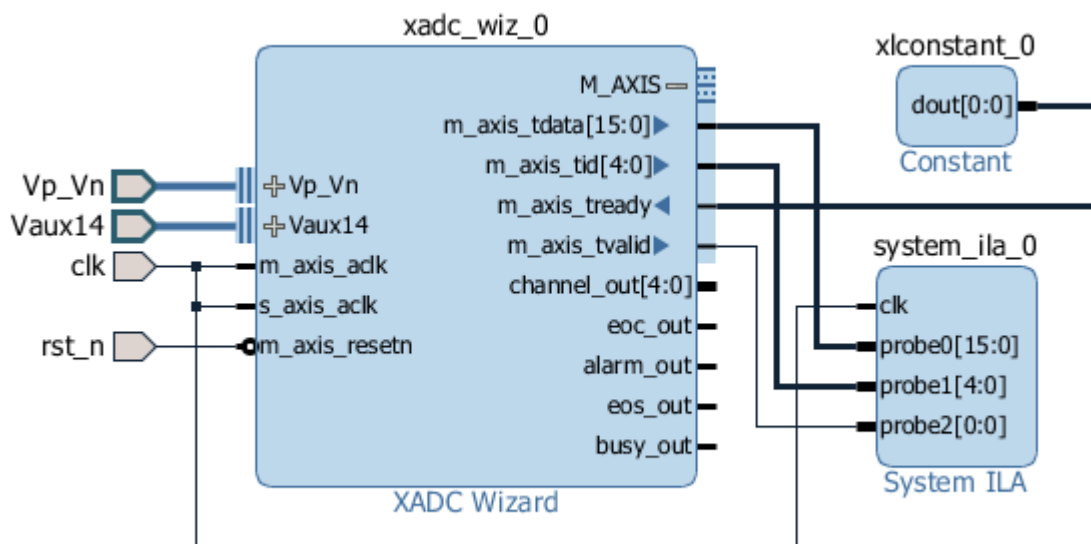


1. Block Design

Terdiri dari IP XADC dan system ILA untuk debugging melihat nilai output ADC.



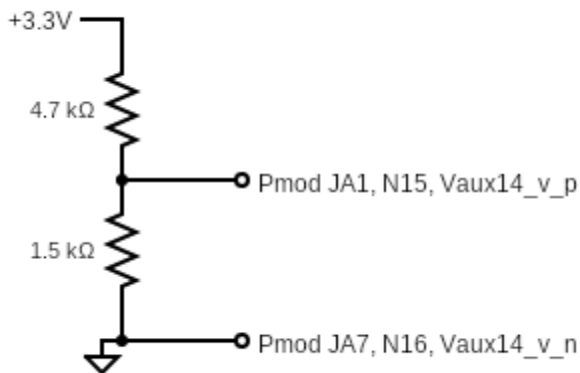
2. Constraint

Menggunakan pin clk dan SW0 untuk reset.

```
7 ##Clock signal
8 set_property -dict { PACKAGE_PIN L16   IOSTANDARD LVCMOS33 } [get_ports { clk }]; #IO_L11P_T1_SRCC_35 Sch=sysclk
9 create_clock -add -name sys_clk_pin -period 10.00 -waveform { 0 5 } [get_ports { clk }]; #set
10
11 ##Switches
12 set_property -dict { PACKAGE_PIN G15   IOSTANDARD LVCMOS33 } [get_ports { rst_n }]; #IO_L19N_T3_VREF_35 Sch=SW0
13
14 ##Pmod Header JA (XADC)
15 set_property -dict { PACKAGE_PIN N15   IOSTANDARD LVCMOS33 } [get_ports { Vaux14_v_p }]; #IO_L21P_T3_DQS_AD14P_35 Sch=JA1_R_p
16 #set_property -dict { PACKAGE_PIN L14   IOSTANDARD LVCMOS33 } [get_ports { Vaux7_v_p }]; #IO_L22P_T3_AD7P_35 Sch=JA2_R_P
17 #set_property -dict { PACKAGE_PIN K16   IOSTANDARD LVCMOS33 } [get_ports { Vaux15_v_p }]; #IO_L24P_T3_AD15P_35 Sch=JA3_R_P
18 #set_property -dict { PACKAGE_PIN K14   IOSTANDARD LVCMOS33 } [get_ports { Vaux6_v_p }]; #IO_L20P_T3_AD6P_35 Sch=JA4_R_P
19 set_property -dict { PACKAGE_PIN N16   IOSTANDARD LVCMOS33 } [get_ports { Vaux14_v_n }]; #IO_L21N_T3_DQS_AD14N_35 Sch=JA1_R_N
20 #set_property -dict { PACKAGE_PIN L15   IOSTANDARD LVCMOS33 } [get_ports { Vaux7_v_n }]; #IO_L22N_T3_AD7N_35 Sch=JA2_R_N
21 #set_property -dict { PACKAGE_PIN J16   IOSTANDARD LVCMOS33 } [get_ports { Vaux15_v_n }]; #IO_L24N_T3_AD15N_35 Sch=JA3_R_N
22 #set_property -dict { PACKAGE_PIN J14   IOSTANDARD LVCMOS33 } [get_ports { Vaux6_v_n }]; #IO_L20N_T3_AD6N_35 Sch=JA4_R_N
```

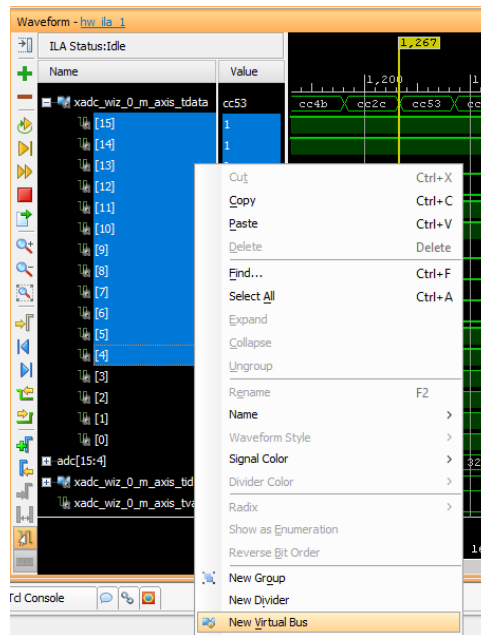
3. Rangkaian Input untuk Test ADC

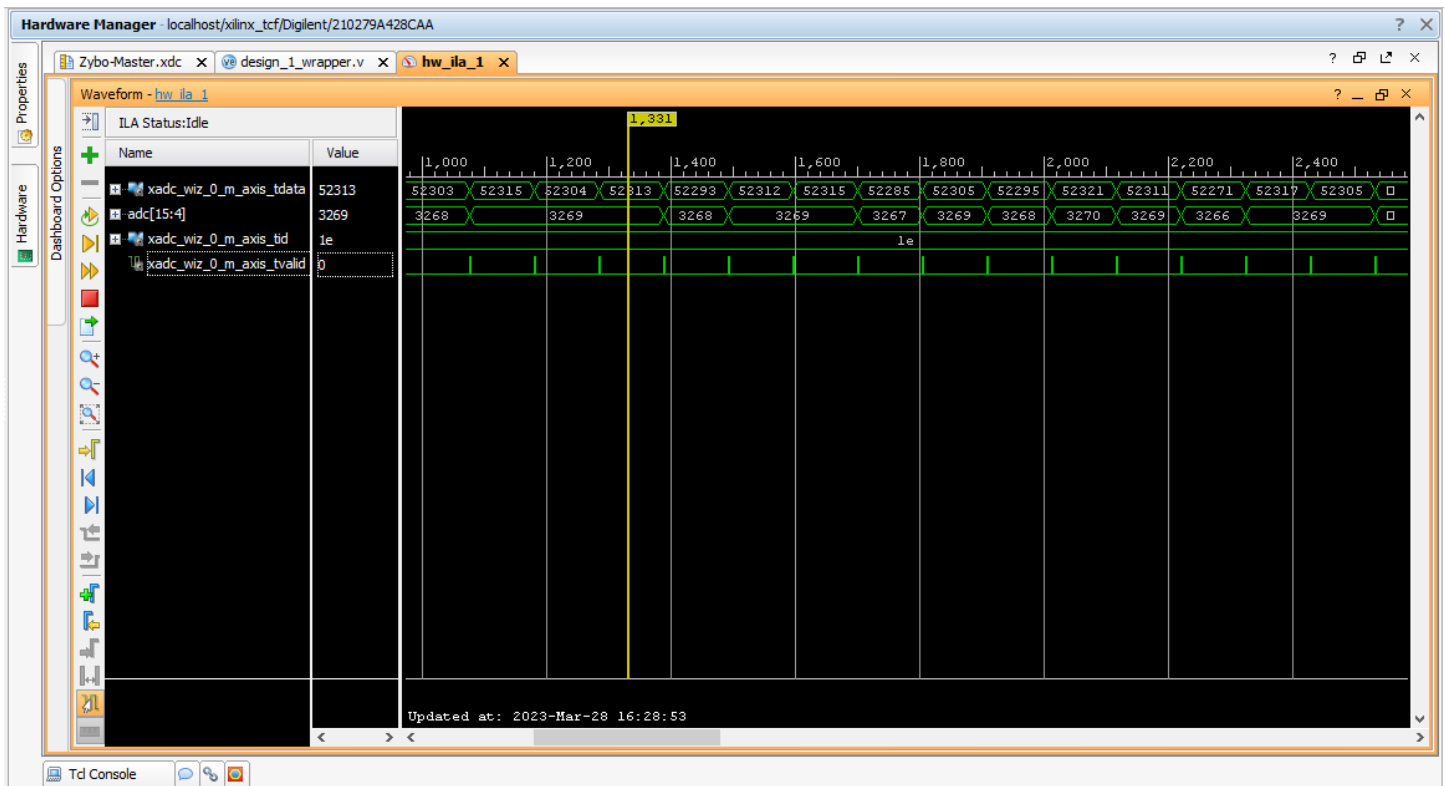
Maximum tegangan input XADC adalah **0V – 1V**. Jadi kita harus membuat pembagi tegangan untuk diinputkan sebagai sinyal input ke ADC. Pembagi berikut ini menghasilkan output 0.798V yang akan diinputkan ke ADC.



4. Debugging dengan ILA

Program Zybo dengan Hardware Manager di Vivado, kemudian tampilan ILA akan keluar. Buat sinyal virtual yang berisi data dari `xadc_wiz_0_m_axis_tdata` mulai dari bit **15 sampai 4** menjadi `adc[15:4]`. Karena ADC memiliki spesifikasi 12-bit.





Sinyal output pada `adc[15:4]` adalah sekitar **3266-3270**. Data ADC valid ketika `xadc_wiz_0_m_axis_tvalid` bernilai **1**. Nilai perhitungan $ADC = 0.798V * 2^{12} = 3268.608$, sehingga hasil pembacaan ADC sudah benar.

5. Konfigurasi IP XADC

Re-customize IP

XADC Wizard (3.3)

Documentation IP Location

☐ Show disabled ports

Component Name: design_1_xadc_wiz_0_0

Basic | ADC Setup | Alarms | Single Channel | Summary

Interface Options

☐ AXI4Lite ☐ DRP ☒ None

Startup Channel Selection

☐ Simultaneous Selection
☐ Independent ADC
☒ Single Channel
☐ Channel Sequencer

AXI4STREAM Options

☒ Enable AXI4Stream
FIFO Depth: 7 [7 - 1020]

Control/Status Ports

☐ reset_in ☐ Temp Bus ☐ JTAG Arbiter
Event Mode Trigger: ☒ convst in ☐ convstclk in

Timing Mode

☒ Continuous Mode ☐ Event Mode

DRP Timing Options

☒ Enable DCLK
DCLK Frequency(MHz): 100
ADC Conversion Rate(KSPS): 1000
Acquisition Time (CLK): 4
Clock divider value = 4
ADC Clock Frequency(MHz) = 25.00
Actual Conversion Rate(KSPS) = 961.54

Analog Sim File Options

Sim File Selection: Default
Analog Stimulus File: design
Sim File Location: ./

OK Cancel

Re-customize IP

XADC Wizard (3.3)

Documentation IP Location

☐ Show disabled ports

Component Name: design_1_xadc_wiz_0_0

Basic | **ADC Setup** | Alarms | Single Channel | Summary

Sequencer Mode: Off

Channel Averaging: None

ADC Calibration

☐ ADC Offset Calibration
☒ ADC Offset and Gain Calibration

Supply Sensor Calibration

☐ Sensor Offset Calibration
☒ Sensor Offset and Gain Calibration

☒ Enable CALIBRATION Averaging

External Multiplexer Setup

☐ External Multiplexer
Channel for MUX: VP_VN
☐ Enable muxaddr_out port

Power Down Options

☐ ADCB
☐ ADCA

OK Cancel

Re-customize IP

XADC Wizard (3.3)

Documentation
IP Location

☐ Show disabled ports

Vp_Vn
Vaux14
m_axis_ack
s_axis_ack
m_axis_resetrn

M_AXIS
channel_out[4:0]
eoc_out
alarm_out
eos_out
busy_out

Component Name
design_1_xadc_wiz_0_0

Basic
ADC Setup
Alarms
Single Channel
Summary

☐ Over Temperature Alarm (°C)

Trigger
125.0
[-40.0 - 125.0]
Reset
70.0
[-40.0 - 125.0]

☐ User Temperature Alarm (°C)

Trigger
85.0
[-40.0 - 125.0]
Reset
60.0
[-40.0 - 125.0]

☐ VCCINT Alarm (Volts)

Lower
0.97
[0.0 - 1.05]
Upper
1.03
[0.0 - 1.05]

☐ VCCAUX Alarm (Volts)

Lower
1.75
[0.0 - 1.89]
Upper
1.89
[0.0 - 1.89]

☐ VCCBRAM Alarm (Volts)

Lower
0.95
[0.0 - 1.05]
Upper
1.05
[0.0 - 1.05]

☐ VCCPint Alarm (Volts)

Lower
0.95
[0.0 - 1.05]
Upper
1.00
[0.0 - 1.05]

☐ VCCPaux Alarm (Volts)

Lower
1.71
[0.0 - 1.89]
Upper
1.8
[0.0 - 1.89]

☐ VCCDDro Alarm(Volts)

VCCDDRO Voltage

☒ 1.2
☐ 1.35
☐ 1.5
☐ 1.8

OK
Cancel

Re-customize IP

XADC Wizard (3.3)

Documentation
IP Location

☐ Show disabled ports

Vp_Vn
Vaux14
m_axis_ack
s_axis_ack
m_axis_resetrn

M_AXIS
channel_out[4:0]
eoc_out
alarm_out
eos_out
busy_out

Component Name
design_1_xadc_wiz_0_0

Basic
ADC Setup
Alarms
Single Channel
Summary

Select Channel	Channel Enable	Average Enable	Bipolar	Acquisition Time
VAUXP14 VAUXN14	<input checked="" type="checkbox"/>		<input type="checkbox"/>	<input type="checkbox"/>

OK
Cancel

6. Konfigurasi System ILA

Re-customize IP

System ILA (1.0)

Documentation IP Location

IP Symbol Resources

BRAM

Resource Estimat

Percent (%)

100.0
90.0
80.0
70.0
60.0
50.0
40.0
30.0
20.0
10.0
0.0

0.0 1.0

Component Name design_1_system_ila_0_0

To configure more than 64 probe ports use Vivado Tcl Console

General Options Probe_Ports(0..7)

Monitor Type

Monitor Type NATIVE

Number of Probes 3 Native Probe width propagation AUTO

Sample Data Depth 8192

☒ Same Number of Comparators for All Probe Ports

Number of Comparators 1

☐ Trigger Out Port

☐ Trigger In Port

Input Pipe Stages 0

Trigger And Storage Settings

☐ Capture Control

☐ Advanced Trigger

Background task running on the design. Customization changes are not allowed

OK Cancel

Re-customize IP

System ILA (1.0)

Documentation IP Location

IP Symbol Resources

BRAM

Resource Estimat

Percent (%)

100.0
90.0
80.0
70.0
60.0
50.0
40.0
30.0
20.0
10.0
0.0

0.0 1.0

Component Name design_1_system_ila_0_0

To configure more than 64 probe ports use Vivado Tcl Console

General Options **Probe_Ports(0..7)**

Probe Port	Probe Width [1..4096]	Number of Comparators	Data and/or Trigger
PROBE0	1	1	DATA AND TRIGGER
PROBE1	1	1	DATA AND TRIGGER
PROBE2	1	1	DATA AND TRIGGER

The width of the probes are set based on AUTO propagation in IP Integrator design.
Update the Native probe width propagation to MANUAL in general settings page to enable setting the individual probe width parameters manually.

Background task running on the design. Customization changes are not allowed

OK Cancel

