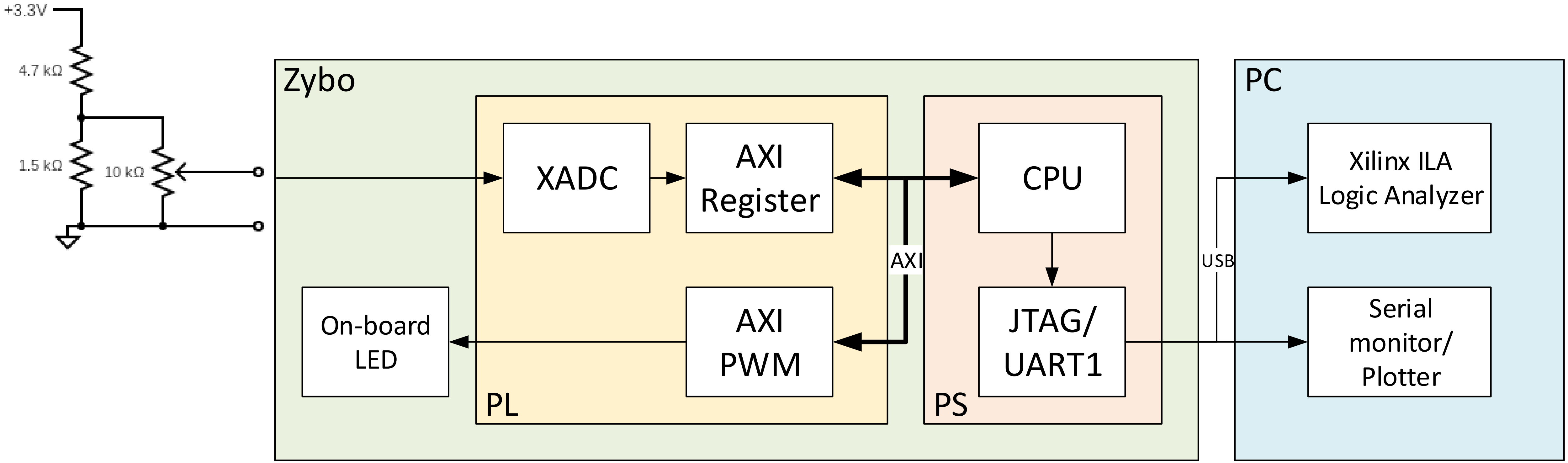
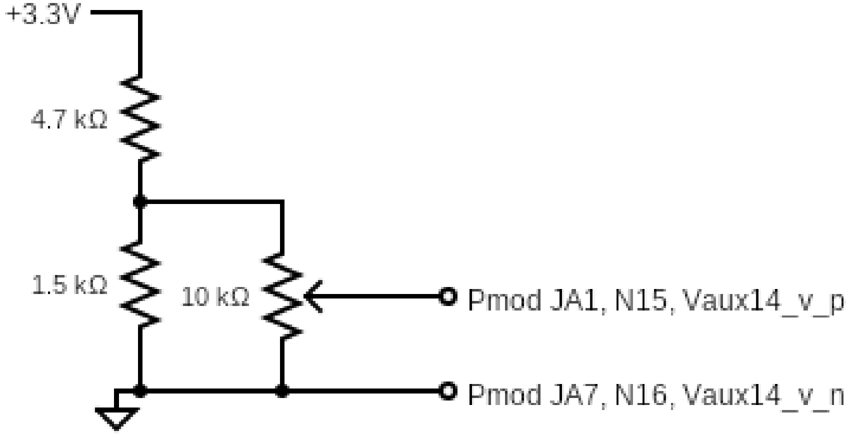
Project ADC, PS, dan PWM

Erwin Setiawan

Block Diagram



Rangkaian Input



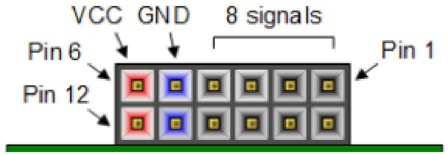
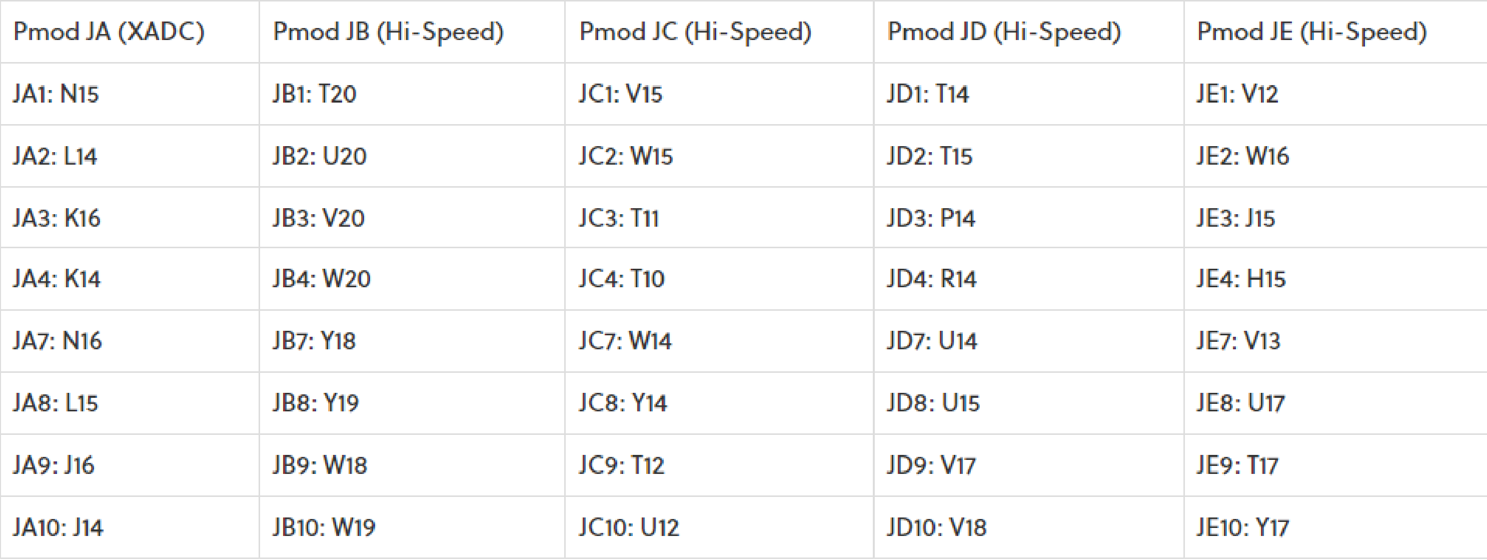
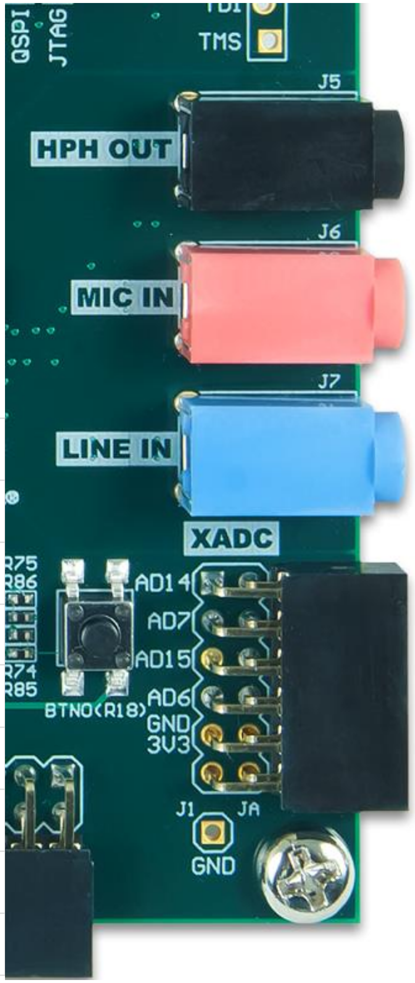
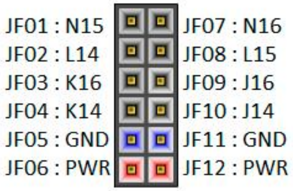


Figure 16. Pmod diagram.



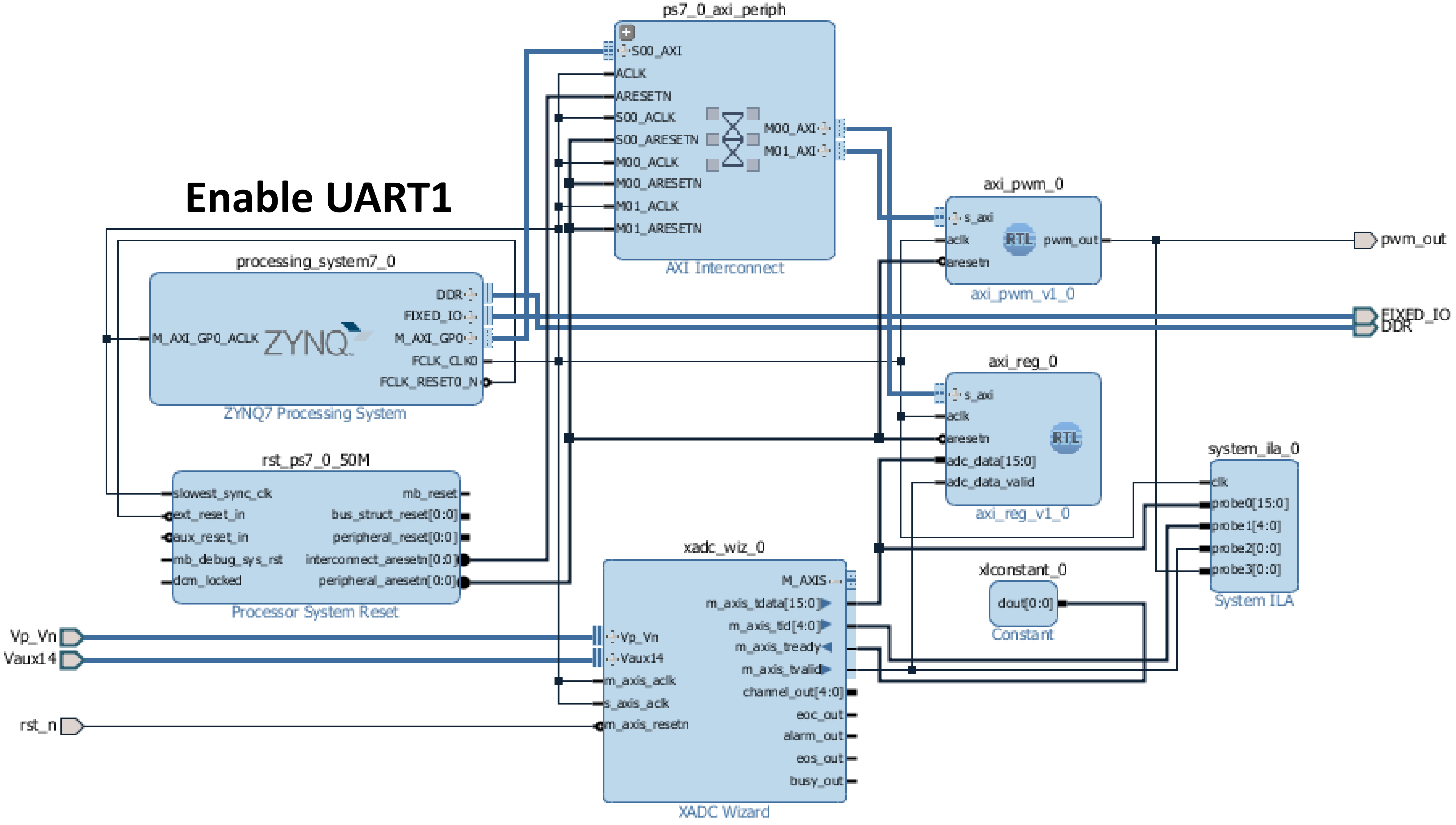
Pmod JA (XADC)	Pmod JB (Hi-Speed)	Pmod JC (Hi-Speed)	Pmod JD (Hi-Speed)	Pmod JE (Hi-Speed)
JA1: N15	JB1: T20	JC1: V15	JD1: T14	JE1: V12
JA2: L14	JB2: U20	JC2: W15	JD2: T15	JE2: W16
JA3: K16	JB3: V20	JC3: T11	JD3: P14	JE3: J15
JA4: K14	JB4: W20	JC4: T10	JD4: R14	JE4: H15
JA7: N16	JB7: Y18	JC7: W14	JD7: U14	JE7: V13
JA8: L15	JB8: Y19	JC8: Y14	JD8: U15	JE8: U17
JA9: J16	JB9: W18	JC9: T12	JD9: V17	JE9: T17
JA10: J14	JB10: W19	JC10: U12	JD10: V18	JE10: Y17



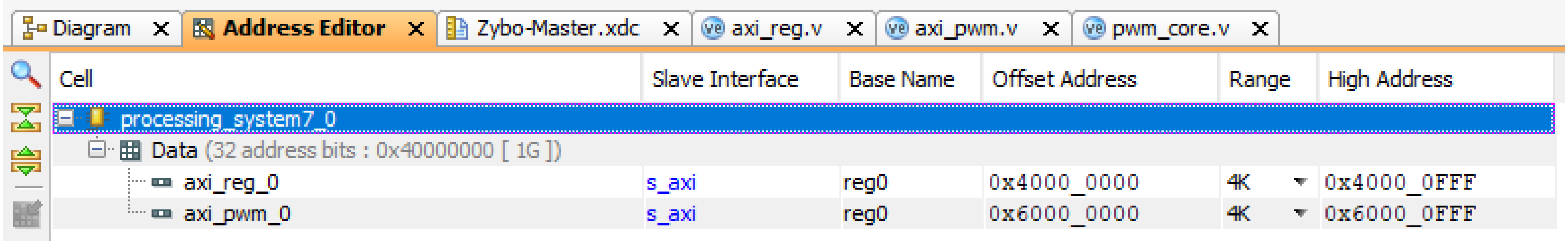


JF01 : N15	JF07 : N16
JF02 : L14	JF08 : L15
JF03 : K16	JF09 : J16
JF04 : K14	JF10 : J14
JF05 : GND	JF11 : GND
JF06 : PWR	JF12 : PWR

Enable UART1

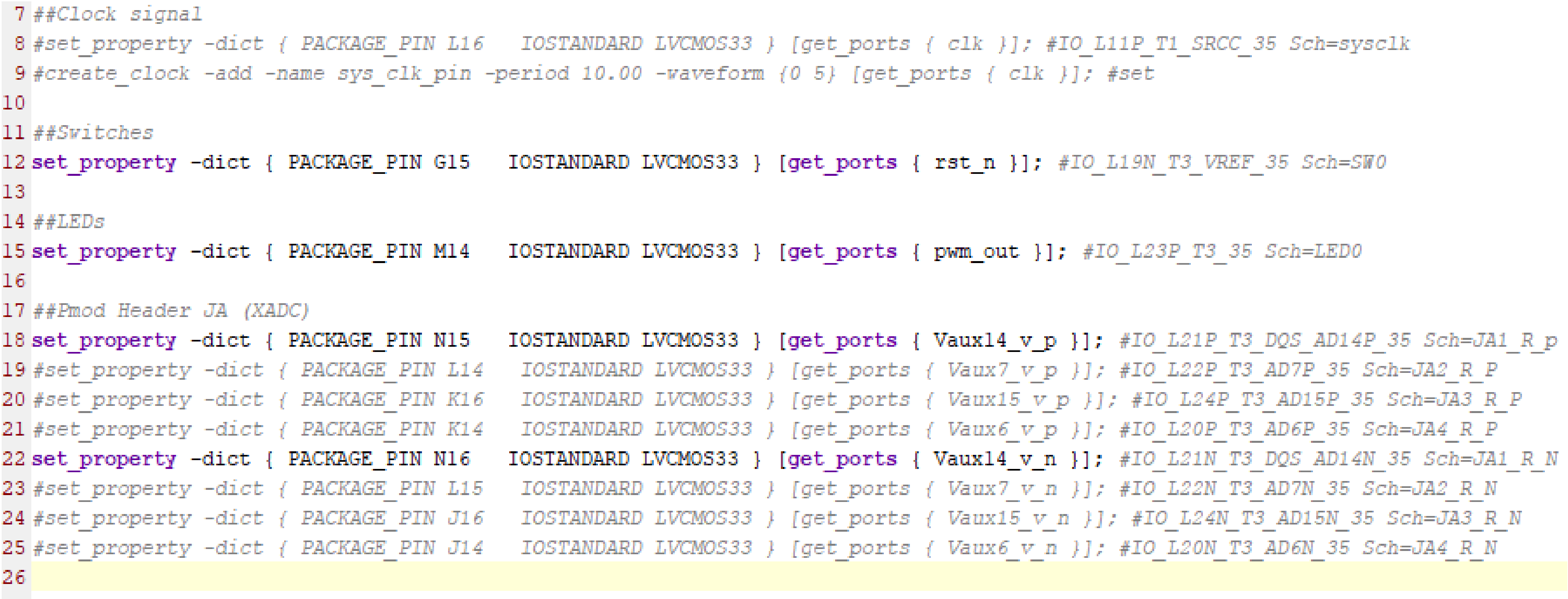


Address Map



Cell	Slave Interface	Base Name	Offset Address	Range	High Address
processing_system7_0					
Data (32 address bits : 0x40000000 [1G])					
axi_reg_0	s_axi	reg0	0x4000_0000	4K	0x4000_0FFF
axi_pwm_0	s_axi	reg0	0x6000_0000	4K	0x6000_0FFF

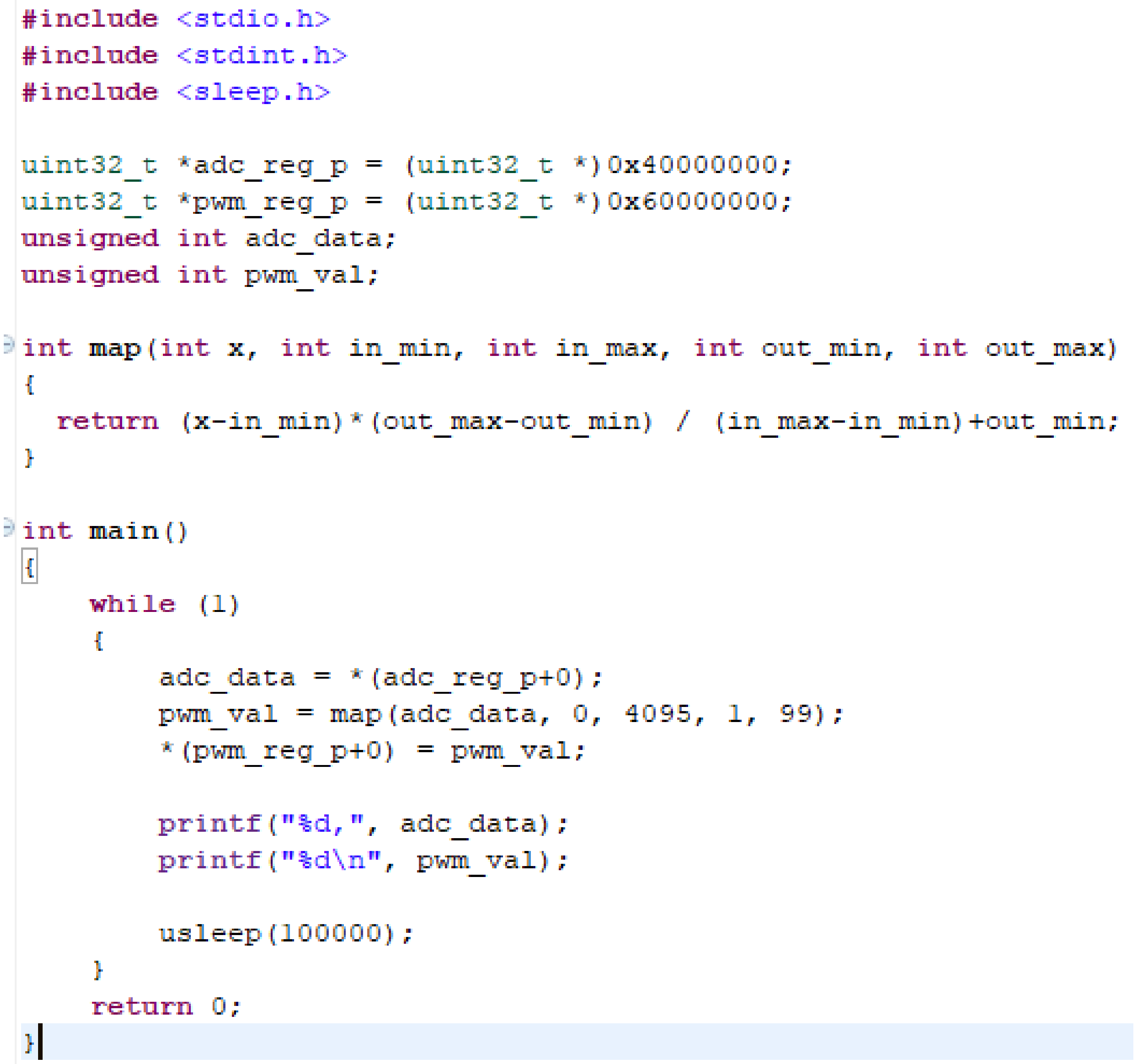
Constraint



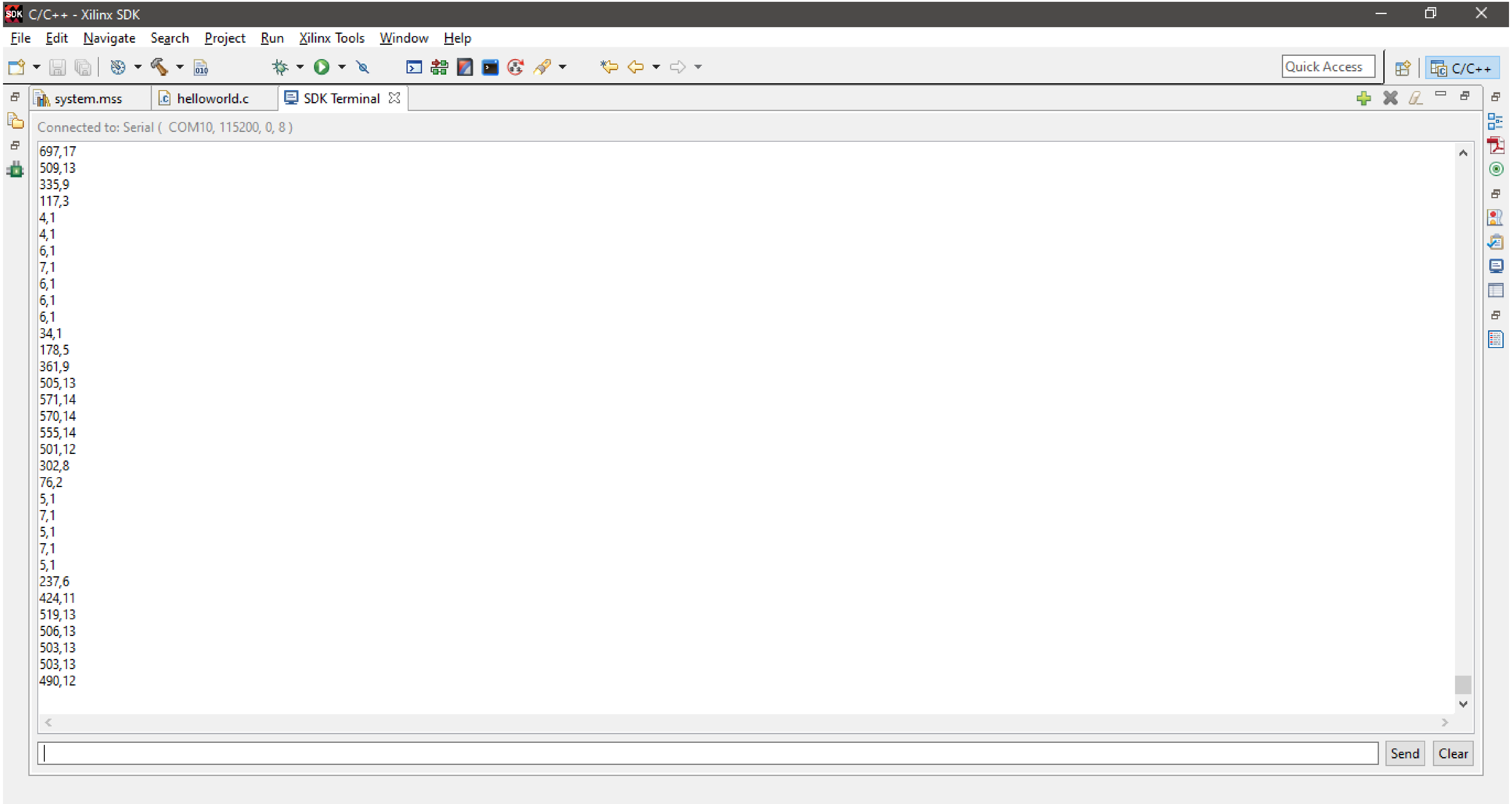
```
##Clock signal
#set_property -dict { PACKAGE_PIN L16   IOSTANDARD LVCMOS33 } [get_ports { clk }]; #IO_L11P_T1_SRCC_35 Sch=sysclk
#create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports { clk }]; #set

##Switches
set_property -dict { PACKAGE_PIN G15   IOSTANDARD LVCMOS33 } [get_ports { rst_n }]; #IO_L19N_T3_VREF_35 Sch=SW0

##LEDs
set_property -dict { PACKAGE_PIN M14   IOSTANDARD LVCMOS33 } [get_ports { pwm_out }]; #IO_L23P_T3_35 Sch=LED0

##Pmod Header JA (XADC)
set_property -dict { PACKAGE_PIN N15   IOSTANDARD LVCMOS33 } [get_ports { Vaux14_v_p }]; #IO_L21P_T3_DQS_AD14P_35 Sch=JA1_R_p
#set_property -dict { PACKAGE_PIN L14   IOSTANDARD LVCMOS33 } [get_ports { Vaux7_v_p }]; #IO_L22P_T3_AD7P_35 Sch=JA2_R_P
#set_property -dict { PACKAGE_PIN K16   IOSTANDARD LVCMOS33 } [get_ports { Vaux15_v_p }]; #IO_L24P_T3_AD15P_35 Sch=JA3_R_P
#set_property -dict { PACKAGE_PIN K14   IOSTANDARD LVCMOS33 } [get_ports { Vaux6_v_p }]; #IO_L20P_T3_AD6P_35 Sch=JA4_R_P
set_property -dict { PACKAGE_PIN N16   IOSTANDARD LVCMOS33 } [get_ports { Vaux14_v_n }]; #IO_L21N_T3_DQS_AD14N_35 Sch=JA1_R_N
#set_property -dict { PACKAGE_PIN L15   IOSTANDARD LVCMOS33 } [get_ports { Vaux7_v_n }]; #IO_L22N_T3_AD7N_35 Sch=JA2_R_N
#set_property -dict { PACKAGE_PIN J16   IOSTANDARD LVCMOS33 } [get_ports { Vaux15_v_n }]; #IO_L24N_T3_AD15N_35 Sch=JA3_R_N
#set_property -dict { PACKAGE_PIN J14   IOSTANDARD LVCMOS33 } [get_ports { Vaux6_v_n }]; #IO_L20N_T3_AD6N_35 Sch=JA4_R_N

```

Source Code

- https://github.com/yohanes-erwin/pemrograman_zynq/tree/main/ADC_PS_PWM



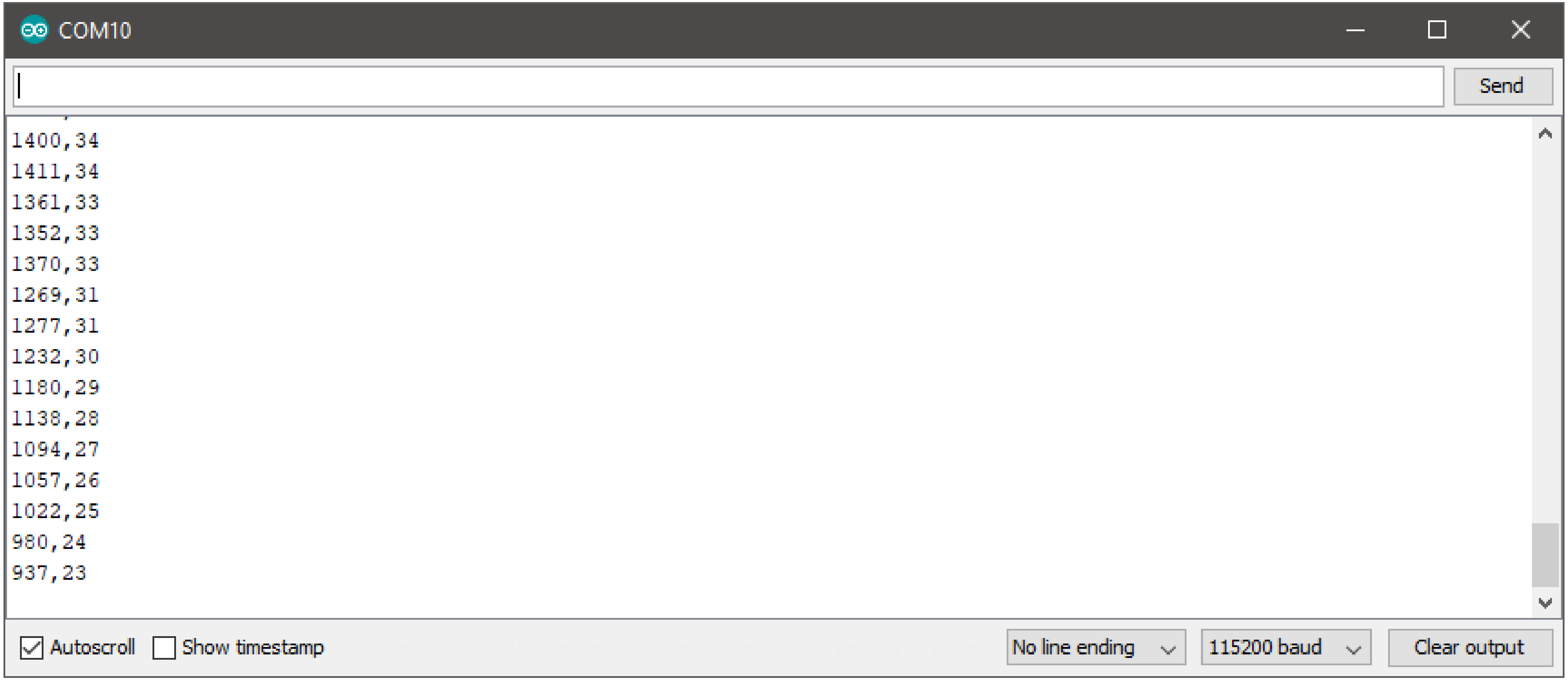
```
#include <stdio.h>
#include <stdint.h>
#include <sleep.h>

uint32_t *adc_reg_p = (uint32_t *)0x40000000;
uint32_t *pwm_reg_p = (uint32_t *)0x60000000;
unsigned int adc_data;
unsigned int pwm_val;

int map(int x, int in_min, int in_max, int out_min, int out_max)
{
  return (x-in_min)*(out_max-out_min) / (in_max-in_min)+out_min;
}

int main()
{
    while (1)
    {
        adc_data = *(adc_reg_p+0);
        pwm_val = map(adc_data, 0, 4095, 1, 99);
        *(pwm_reg_p+0) = pwm_val;

        printf("%d,", adc_data);
        printf("%d\n", pwm_val);

        usleep(100000);
    }
    return 0;
}
```



Connected to: Serial (COM10, 115200, 0, 8)

```
697,17
509,13
335,9
117,3
4,1
4,1
6,1
7,1
6,1
6,1
6,1
34,1
178,5
361,9
505,13
571,14
570,14
555,14
501,12
302,8
76,2
5,1
7,1
5,1
7,1
5,1
237,6
424,11
519,13
506,13
503,13
503,13
490,12
```

Arduino Serial Terminal



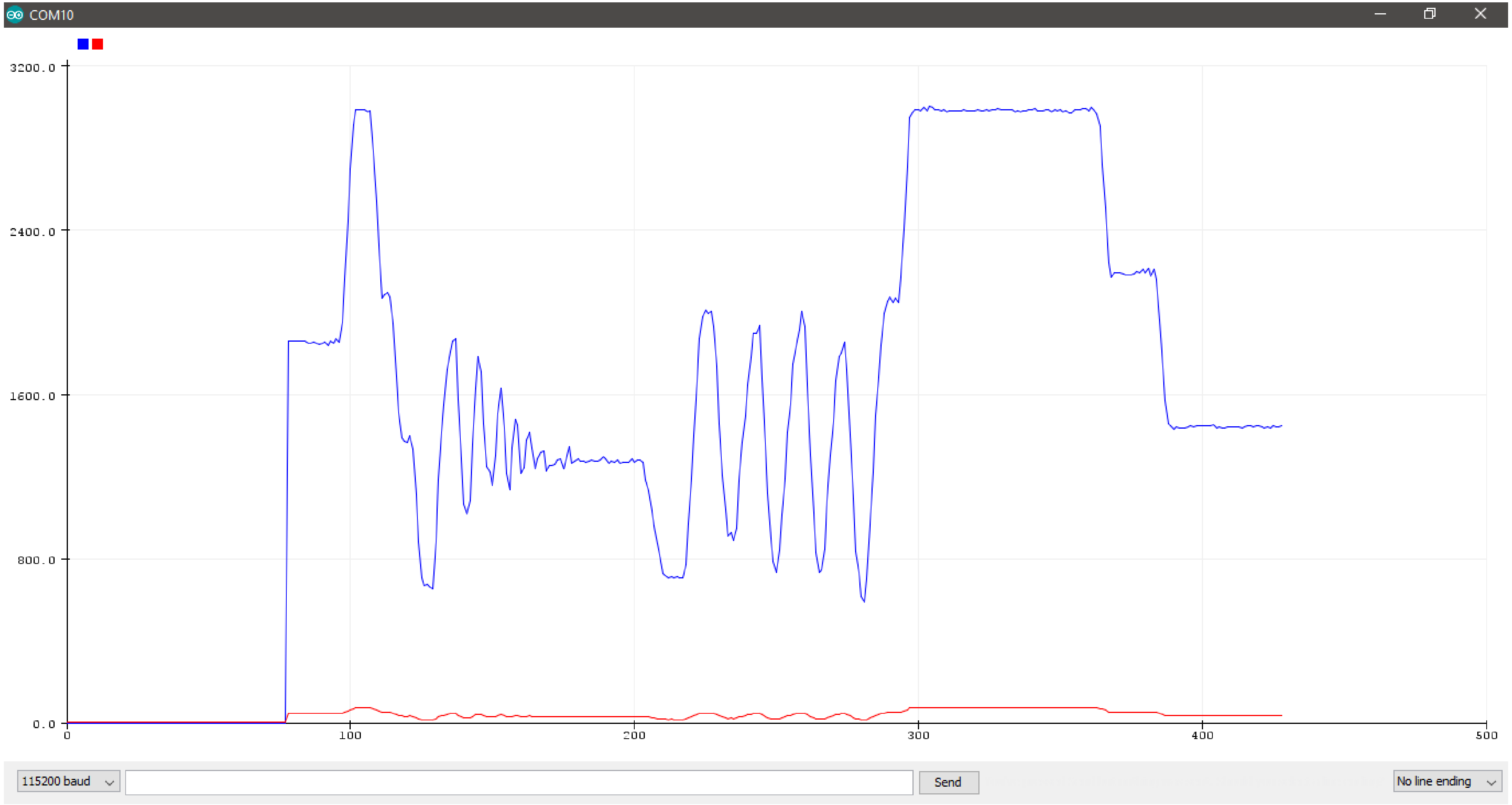
```
1400,34
1411,34
1361,33
1352,33
1370,33
1269,31
1277,31
1232,30
1180,29
1138,28
1094,27
1057,26
1022,25
980,24
937,23
```

☑ Autoscroll □ Show timestamp

No line ending

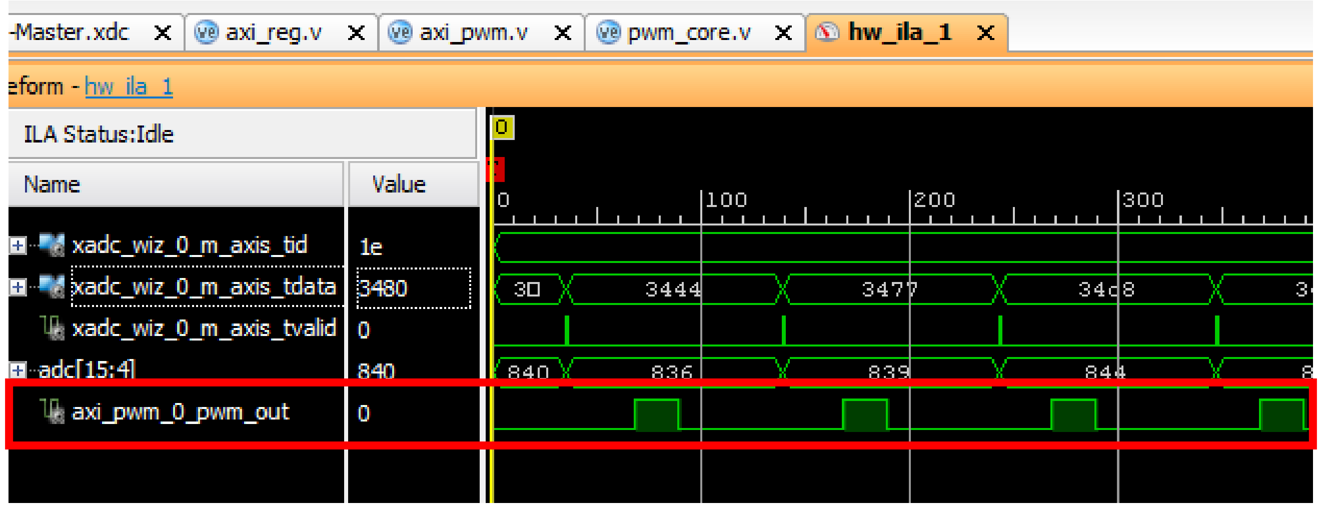
115200 baud

Arduino Plotter ADC dan PWM Duty Cycle



PWM Output pada ILA dan LED

Duty Cycle 20%

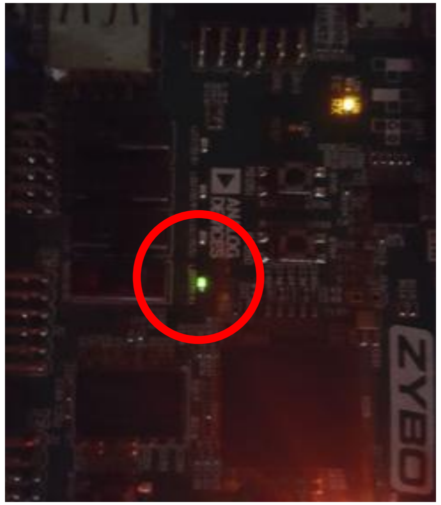


-Master.xdc ✕ | axi_reg.v ✕ | axi_pwm.v ✕ | pwm_core.v ✕ | hw_ila_1 ✕

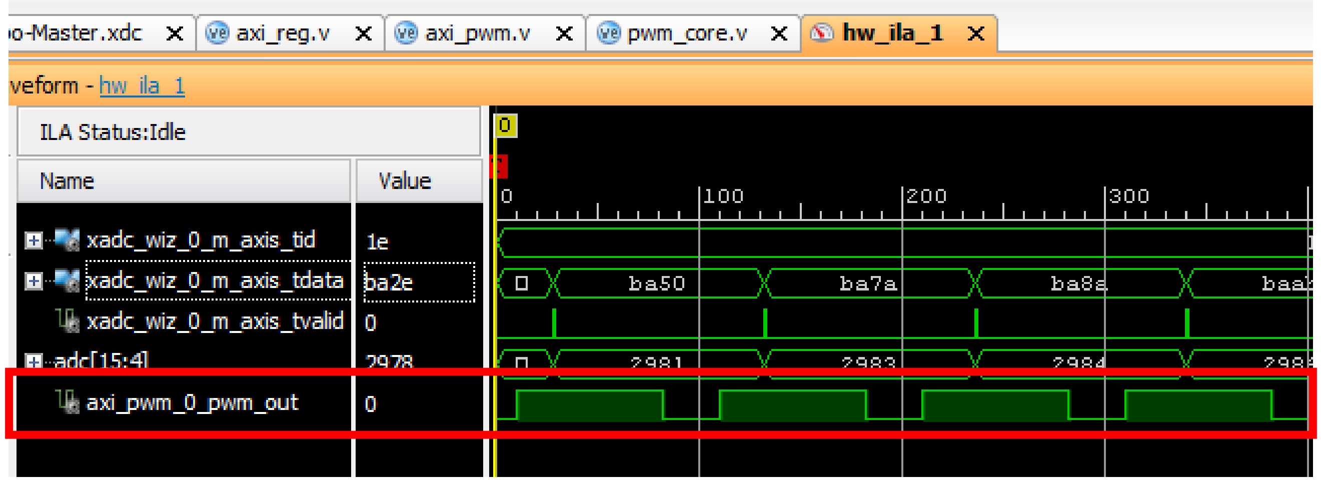
eform - hw_ila_1

ILA Status:Idle

Name	Value
xadc_wiz_0_m_axis_tid	1e
xadc_wiz_0_m_axis_tdata	3480
xadc_wiz_0_m_axis_tvalid	0
adc[15:4]	840
axi_pwm_0_pwm_out	0



Duty Cycle 80%



o-Master.xdc ✕ | axi_reg.v ✕ | axi_pwm.v ✕ | pwm_core.v ✕ | hw_ila_1 ✕

veform - hw_ila_1

ILA Status:Idle

Name	Value
xadc_wiz_0_m_axis_tid	1e
xadc_wiz_0_m_axis_tdata	ba2e
xadc_wiz_0_m_axis_tvalid	0
adc[15:4]	2978
axi_pwm_0_pwm_out	0