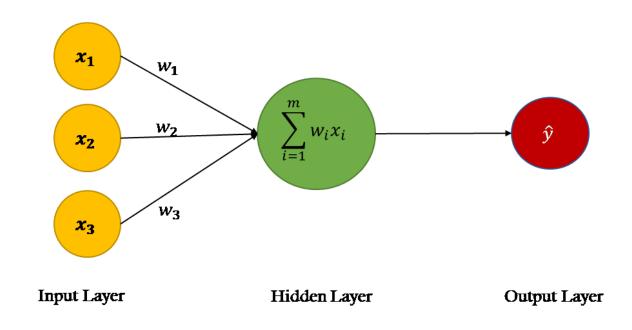
Aplikasi ANN

Erwin Setiawan

Artificial Neural Network (ANN)

Artificial Neural Network (ANN) Sederhana

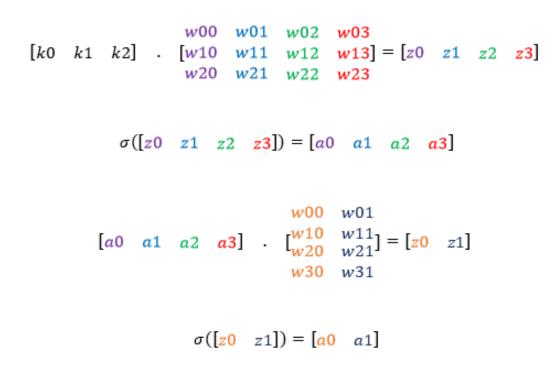
Contoh ANN sederhana dengan 3 input, 1 hidden node, dan 1 output.

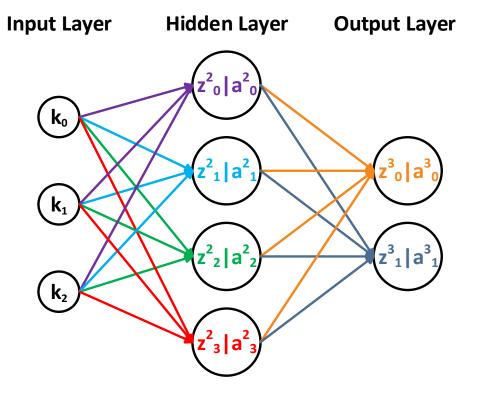


$$y = w1*x1 + w2*x2 + w3*x3$$

ANN dengan Perkalian Matrix

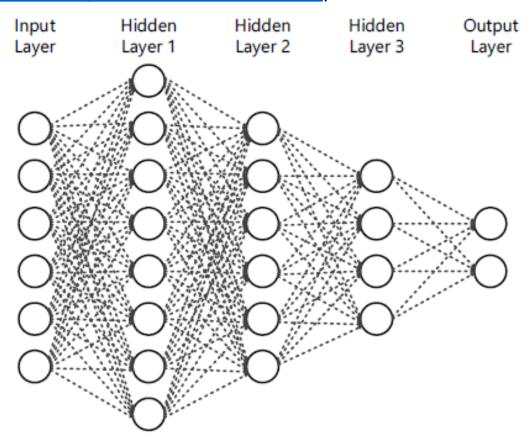
• Menghitung ANN dengan perkalian matrix. Di sini terdapat juga fungsi aktivasi sigmoid (σ).





Deep Neural Network

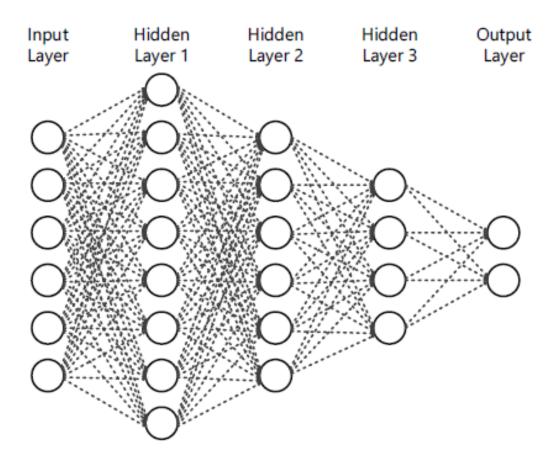
• ANN yang memiliki hidden layer lebih dari 2 disebut Deep Neural Network (DNN). Contoh model dari paper: Implementation of Systolic Co-processor for Deep Neural Network Inference based on SoC (https://ieeexplore.ieee.org/document/8649920).



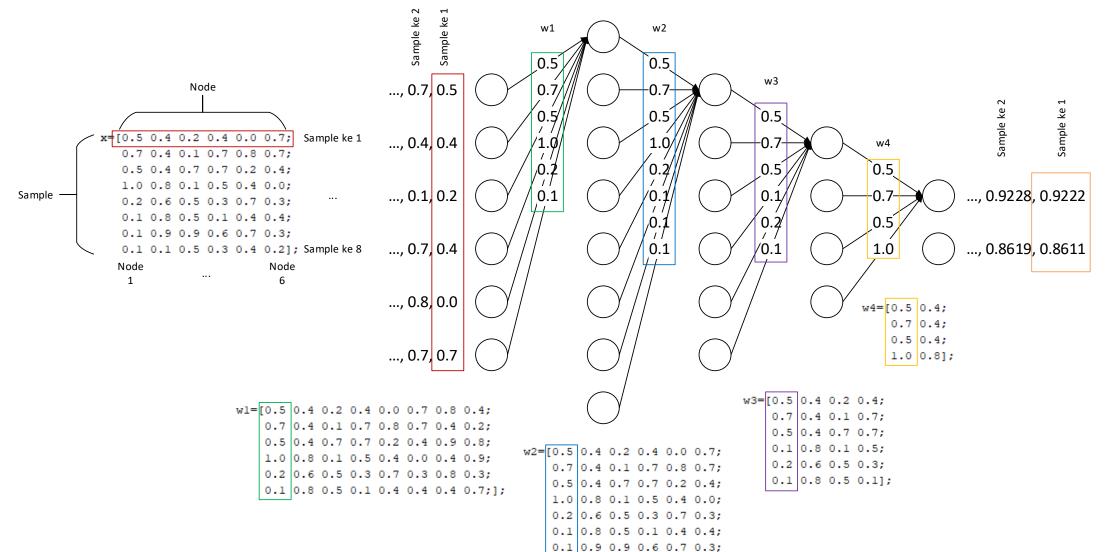
Model ANN

Model MATLAB Deep Neural Network

File model matlab: https://github.com/yohanes-
 erwin/pemrograman zynq/blob/main/Aplikasi ANN/model/model ann.m



Ilustrasi Matrix pada Model



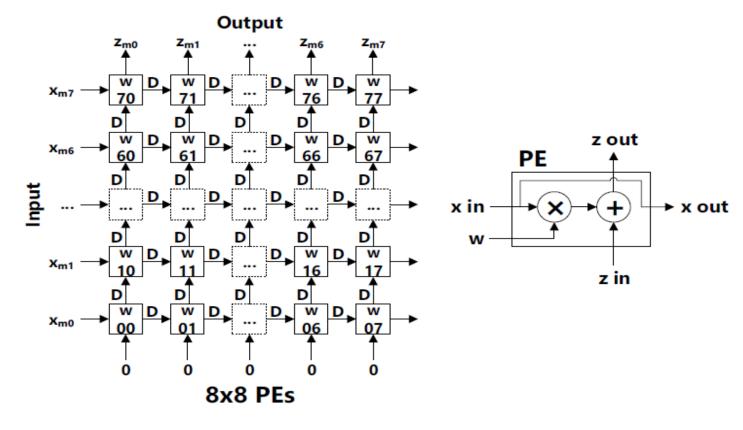
0.1 0.1 0.5 0.3 0.4 0.2];

	1	2			
1	0.9222	0.8611			
2	0.9228	0.8619			
3	0.9227	0.8618			
4	0.9226	0.8616			
5	0.9226	0.8616			
6	0.9224	0.8614			
7	0.9230	0.8621			
8	0.9218	0.8607			

Design Accelerator ANN

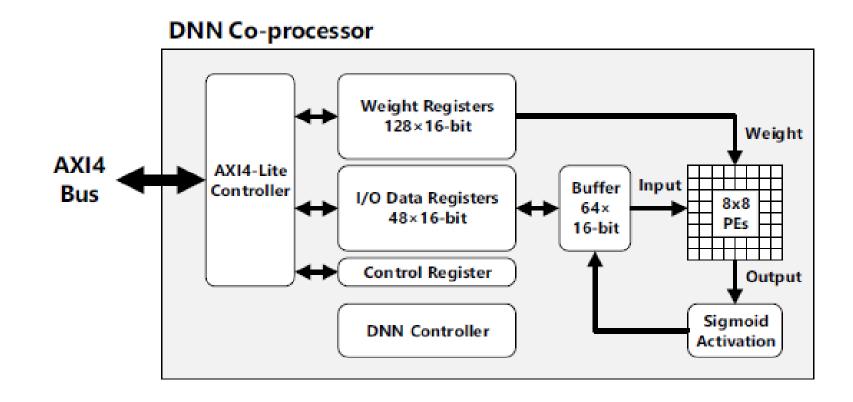
Perkalian Matrix

• Datapath systolic perkalian matrix untuk ukuran maximal perkalian 8x8.



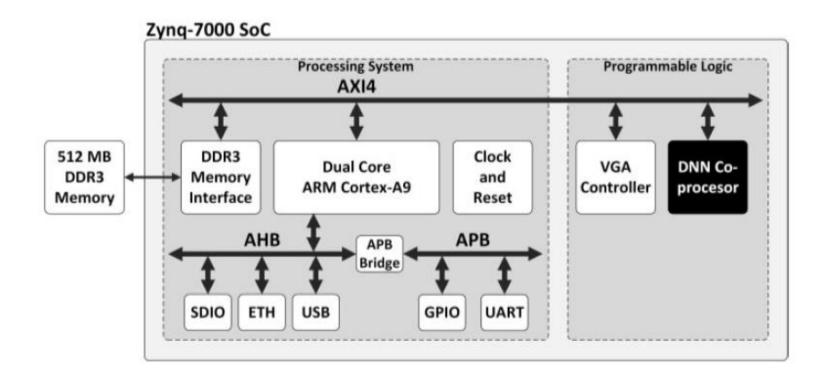
Design Accelerator DNN

• Design accelerator (co-processor) DNN dengan datapath systolic matrix 8x8, register untuk data, weight, dan interface AXI4-lite.



Design SoC DNN

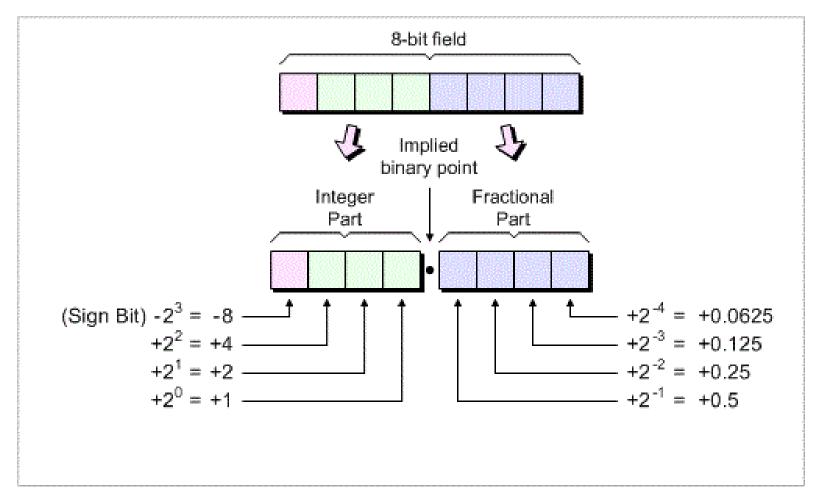
 Design SoC secara keseluruhan terdiri dari DNN co-processor dan processing system tempat program C dijalankan untuk mengakses DNN co-processor tersebut.



Kode Verilog Co-processor DNN

- File module RTL: https://github.com/yohanes-erwin/pemrograman zyng/tree/main/Aplikasi ANN/module
- File **testbench**: https://github.com/yohanes-erwin/pemrograman.zynq/tree/main/Aplikasi_ANN/testbench
- File **program C**: https://github.com/yohanes-erwin/pemrograman.zynq/tree/main/Aplikasi.ann/program

Bilangan Fixed Point



https://www.allaboutcircuits.com/technical-articles/fixed-point-representation-the-q-format-and-addition-examples/

Sebit field

Implied binary point

Integer Part

Fractional Part $+2^{-4} = +0.0625$ $+2^2 = +4$ $+2^1 = +2$ $+2^0 = +1$ Sebit field $+2^4 = +0.0625$ $+2^4 = +0.0625$ $+2^2 = +0.125$ $+2^1 = +0.5$

- 01010110 = 86 (integer)
- 01010110 = 5.375 (fixed-point 1 sign 3 integer 4 fraction)

$$0 \times 2^{3} + 1 \times 2^{2} + 0 \times 2^{1} + 1 \times 2^{0} + 0 \times 2^{-1} + 1 \times 2^{-2} + 1 \times 2^{-3} + 0 \times 2^{-4} = 5.375$$

- Fixed-Point yang digunakan di perkalian marix dan ANN adalah 16-bit dengan
 - 1 sign bit (0: positif, 1: negative)
 - 5 integer bit
 - 10 fraction bit

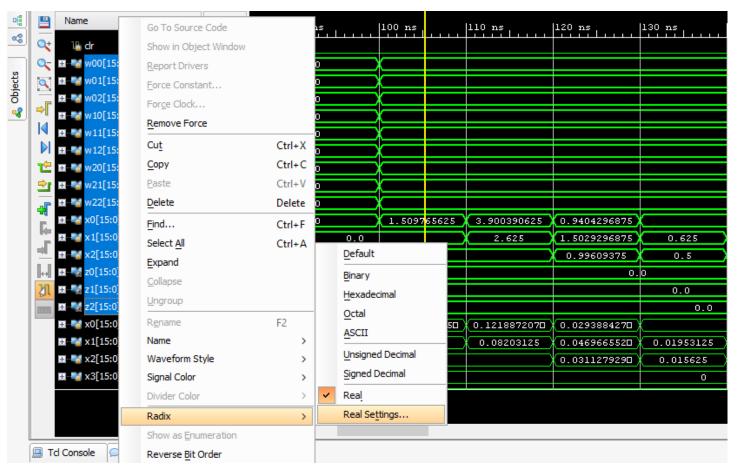
```
w00 = 16'b00 0010 0001 1001 10; w00 = 16'b0000100001100110;
```

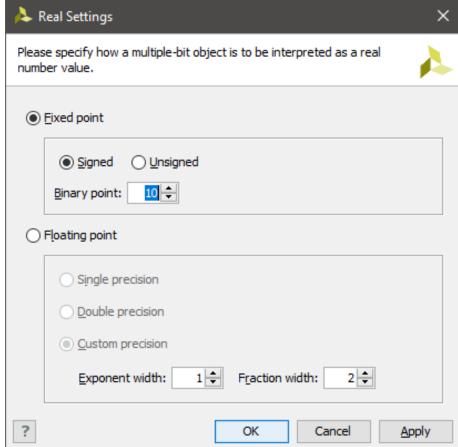
Tanda _ (underscore) hanya untuk memudahkan pembacaan bit tidak ada pengaruhnya dengan nilainya. Kedua variable tersebut akan bernilai sama. Compiler akan mengabaikan tanda _.

```
>> q2dec('0000100001100110', 5, 10, 'bin')
ans =
    2.0996
>> dec2q(2.0996, 5, 10, 'bin')
ans =
    '0000100001100101'
```

https://www.mathworks.com/matlabcentral/fileexchange/61670-fixed-point-q-format-to-decimal-converter https://www.mathworks.com/matlabcentral/fileexchange/61669-decimal-to-fixed-point-q-format-converter

Cara Mengganti Tampilan ke Fixed Point



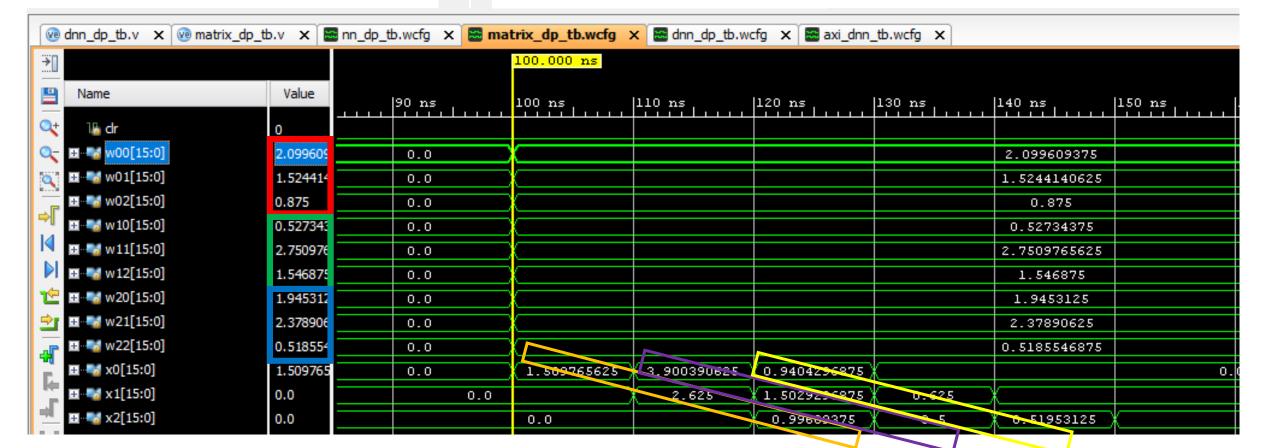


Simulasi Perkalian Matrix

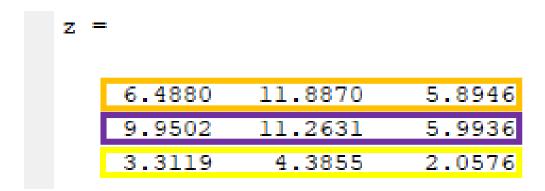
Perkalian Matrix

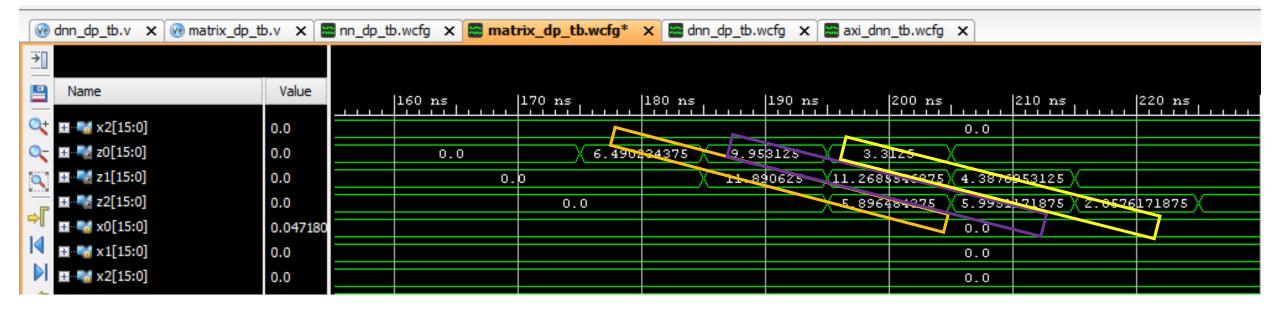
```
clear;
     clc;
      x=[1.509 2.625 0.996;
         3.900 1.502 0.500
5
                                    6.4880
                                            11.8870
                                                       5.8946
         0.940 0.625 0.519];
                                                       5.9936
                                    9.9502 11.2631
     w=[2.099 1.524 0.875;
                                    3.3119 4.3855
                                                       2.0576
         0.527 2.750 1.546;
         1.945 2.378 0.518];
      z=x*w:
```

Input



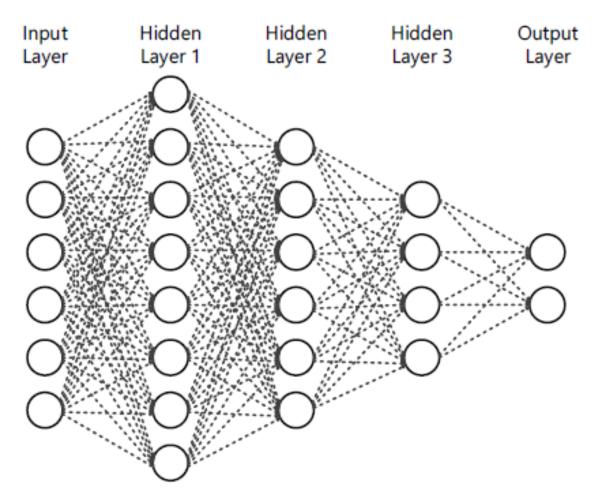
Output





Simulasi Proses 1 Layer ANN

Model ANN



Implementation of Systolic Co-processor for Deep Neural Network Inference based on SoC

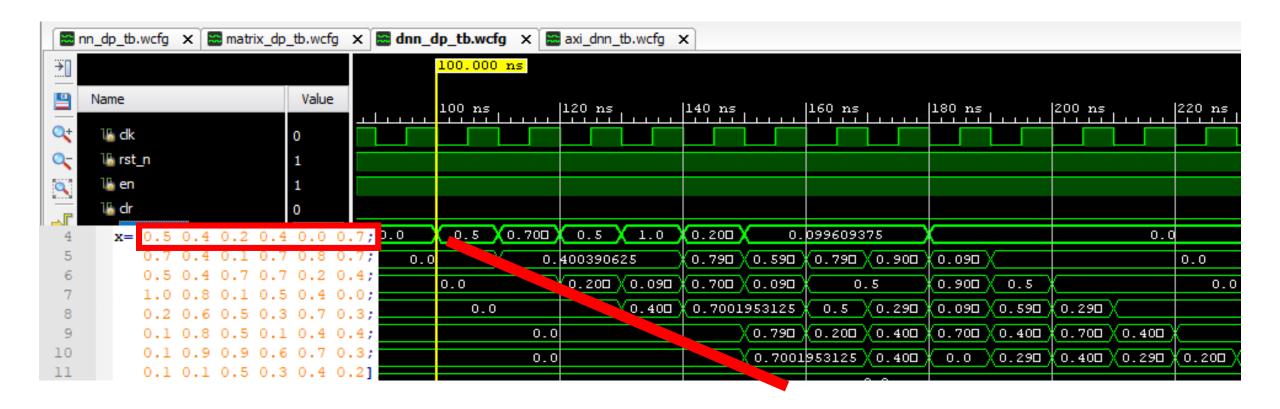
Model ANN di Matlab

```
clear:
      clc;
      % Input
      x=[0.5 0.4 0.2 0.4 0.0 0.7;
 5
         0.7 0.4 0.1 0.7 0.8 0.7;
 6
         0.5 0.4 0.7 0.7 0.2 0.4;
         1.0 0.8 0.1 0.5 0.4 0.0;
         0.2 0.6 0.5 0.3 0.7 0.3;
 8
         0.1 0.8 0.5 0.1 0.4 0.4;
10
         0.1 0.9 0.9 0.6 0.7 0.3;
11
         0.1 0.1 0.5 0.3 0.4 0.2];
12
      % Weight input to hidden 1
13
      w ihl=[0.5 0.4 0.2 0.4 0.0 0.7 0.8 0.4;
14
             0.7 0.4 0.1 0.7 0.8 0.7 0.4 0.2;
15
             0.5 0.4 0.7 0.7 0.2 0.4 0.9 0.8;
16
             1.0 0.8 0.1 0.5 0.4 0.0 0.4 0.9;
17
             0.2 0.6 0.5 0.3 0.7 0.3 0.8 0.3;
18
             0.1 0.8 0.5 0.1 0.4 0.4 0.4 0.7;1;
19
      % Weight hidden 1 to hidden 2
20
      w hlh2=[0.5 0.4 0.2 0.4 0.0 0.7;
21
             0.7 0.4 0.1 0.7 0.8 0.7;
22
             0.5 0.4 0.7 0.7 0.2 0.4;
23
             1.0 0.8 0.1 0.5 0.4 0.0;
24
             0.2 0.6 0.5 0.3 0.7 0.3;
25
             0.1 0.8 0.5 0.1 0.4 0.4;
             0.1 0.9 0.9 0.6 0.7 0.3;
26
27
             0.1 0.1 0.5 0.3 0.4 0.2];
```

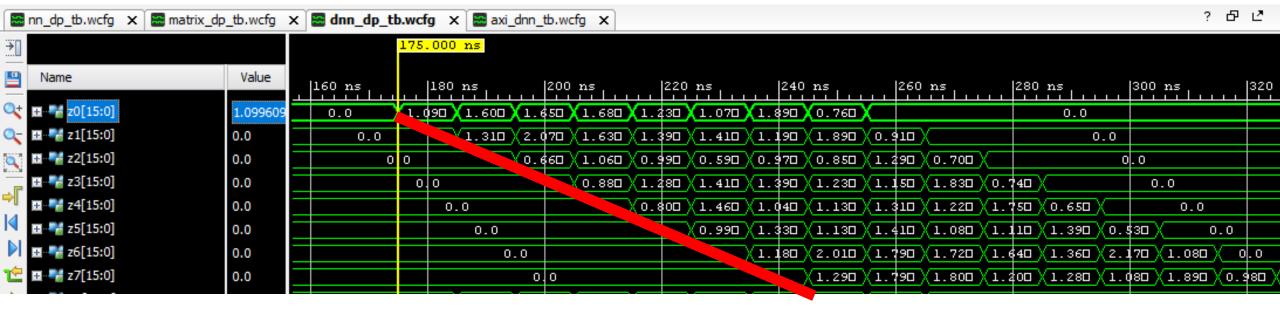
```
% Weight hidden 2 to hidden 3
29
      w h2h3=[0.5 0.4 0.2 0.4;
30
             0.7 0.4 0.1 0.7;
31
             0.5 0.4 0.7 0.7;
32
             1.0 0.8 0.1 0.5;
33
             0.2 0.6 0.5 0.3;
34
             0.1 0.8 0.5 0.11;
35
      % Weight hidden 3 to output
36
      w h3o=[0.5 0.4;
37
             0.7 0.4;
38
             0.5 0.4;
39
             1.0 0.81;
40
      % Output
      zl=x*w ihl;
41
42
      al=1./(1+exp(-z1));
43
      z2=a1*w h1h2;
      a2=1./(1+exp(-z2));
      z3=a2*w h2h3;
      a3=1./(1+exp(-z3));
46
      z4=a3*w h3o;
47
48
      a4=1./(1+exp(-z4));
```

Simulasi 1 Layer

dnn_dp_tb.v mensimulasikan satu layer pertama



Z	1 =							
	1.1000	1.3200	0.6700	0.8900	0.8000	0.9900	1.1800	1.2900
	1.6100	2.0800	1.0700	1.2900	1.4600	1.3300	2.0100	1.8000
	1.6600	1.6400	1.0000	1.4200	1.0400	1.1300	1.7900	1.8100
	1.6900	1.4000	0.6000	1.4000	1.1400	1.4200	1.7300	1.2100
	1.2400	1.4200	0.9800	1.2400	1.3100	1.0900	1.6500	1.2900
	1.0800	1.2000	0.8600	1.1600	1.2200	1.1100	1.3700	1.0900
	1.9000	1.9000	1.3000	1.8400	1.7500	1.3900	2.1700	1.9000
fx	0.7700	0.9200	0.7100	0.7500	0.6600	0.5400	1.0900	0.9900

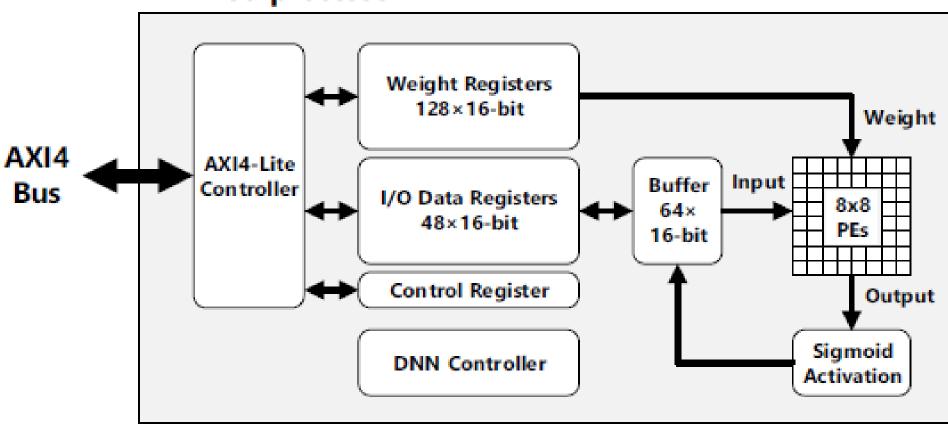


al	=								
	0.7503	0.7892	0.6615	0.7089	0.6900	0.7291	0.7649	0.7841	
	0.8334	0.8889	0.7446	0.7841	0.8115	0.7908	0.8818	0.8581	
	0.8402	0.8375	0.7311	0.8053	0.7389	0.7558	0.8569	0.8594	
	0.8442	0.8022	0.6457	0.8022	0.7577	0.8053	0.8494	0.7703	
	0.7756	0.8053	0.7271	0.7756	0.7875	0.7484	0.8389	0.7841	
	0.7465	0.7685	0.7027	0.7613	0.7721	0.7521	0.7974	0.7484	
	0.8699	0.8699	0.7858	0.8629	0.8520	0.8006	0.8975	0.8699	
	0.6835	0.7150	0.6704	0.6792	0.6593	0.6318	0.7484	0.7291	
fx									2 47 48
nn_dp_tb,wcfg ×	matrix_dp_tb.wcfg >			tb.wcfg X					? 라션
<u>*1</u>		185.000 ns	5						
Name	Value	180 ns	200 ns	220 ns	40 ns 26	0 ns 280	ns 300 :	ns 320 ns	s 34
→ z6[15:0]	0.0		0.0		30 2.010 1.790				0.0
Q-	0.0		0.0		X1.290 X1.790	1 × 1.800 × 1.200	X1.280 X1.080 X	1.890 (0.980)	0.0
a0[15:0]				و مسائد مساؤمی	<u>10 X 0.860 X 0.670</u>	_	0.		
a1[15:0]	0.5				25 (0.760 (0.860		,	0.5	
a2[15:0]	0.5	0.5			30 (0.710 (0.690			0.5	
a3[15:0]	0.5	0.5			978515625 💢 0.760			0.5	
a4[15:0]	0.5		0.5		00 × 0.730 × 0.750			0.5	
⇒r ± • a6[15:0]	0.5		0.5	\ 0. ()	LO X 0.780 X 0.750		X 0.830 X 0.780 X		0.5
a7[15:0]	0.5		0.5		X0.750 X0.870		ب ب	0.740 \ 0.860 \ 0.	

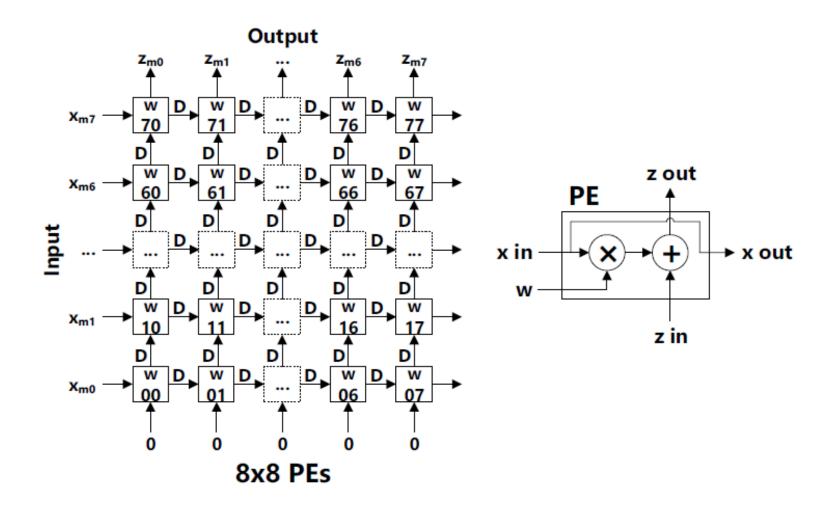
Simulasi Proses Lebih dari 1 Layer

Block Diagram

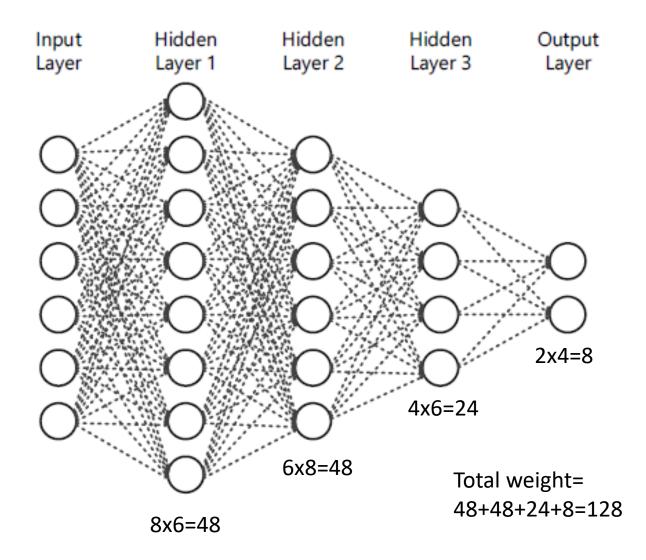
DNN Co-processor



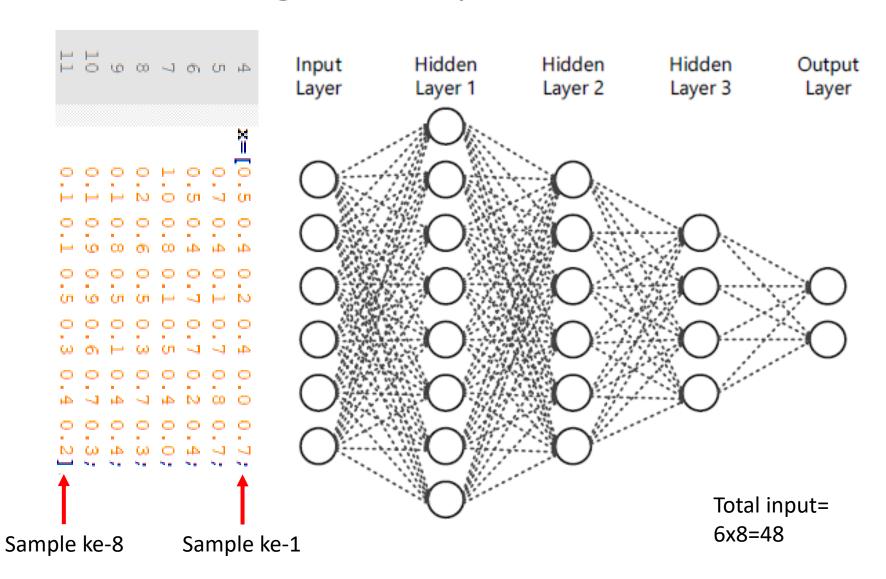
Processor Perkalian Matrix



Jumlah Register Weight



Jumlah Register Input

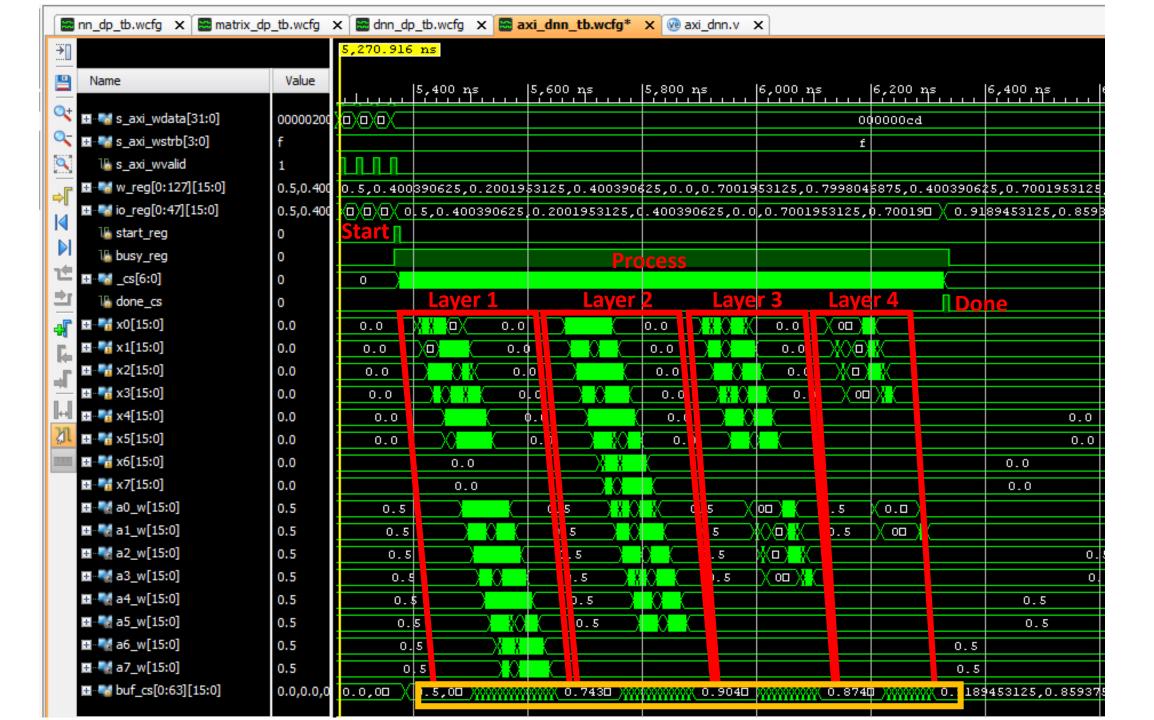


Jumlah Register Buffer

- Jumlah register buffer berfungsi untuk menyimpan hasil perklaian matrix yang ukurannya menyesuaikan ukuran perkalian matrix.
- Karena ukuran perkalian matrix maximal 8x8, maka jumlah element matrix-nya adalah 8x8=64.
- Sehingga perlu 64 register untuk menyimpan output perkalian matrix.

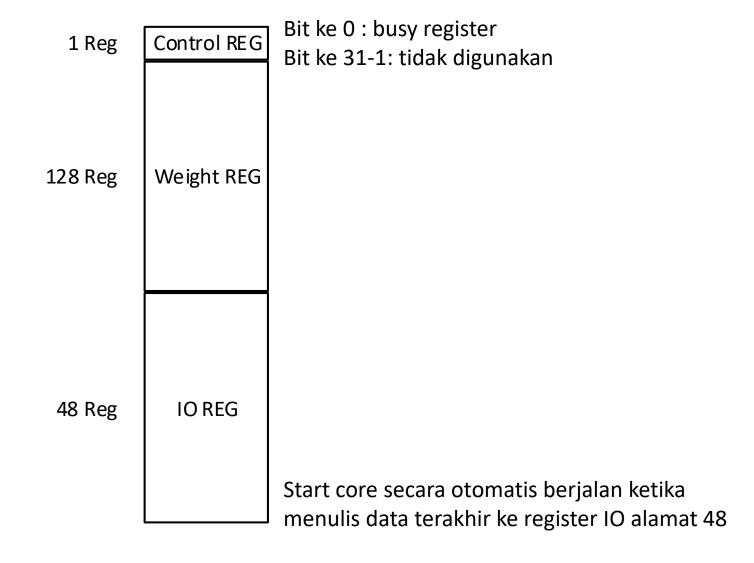
State Machine untuk Controller

- 1. Menunggu sinyal START
- 2. Load input X dari IO reg ke buf reg
- 3. Load weight untuk layer n ke weight reg (register systolic)
- 4. Process perkalian input X dan weight layer n
- 5. Membaca output perkalian systolic yang sudah dilakukan fungsi sigmoid dan disimpan di buf reg
- 6. Ulangi ke step 3 sampai jumlah layer 4 terpenuhi
- 7. Menulis output dari buf reg ke IO reg
- 8. Generate sinyal DONE

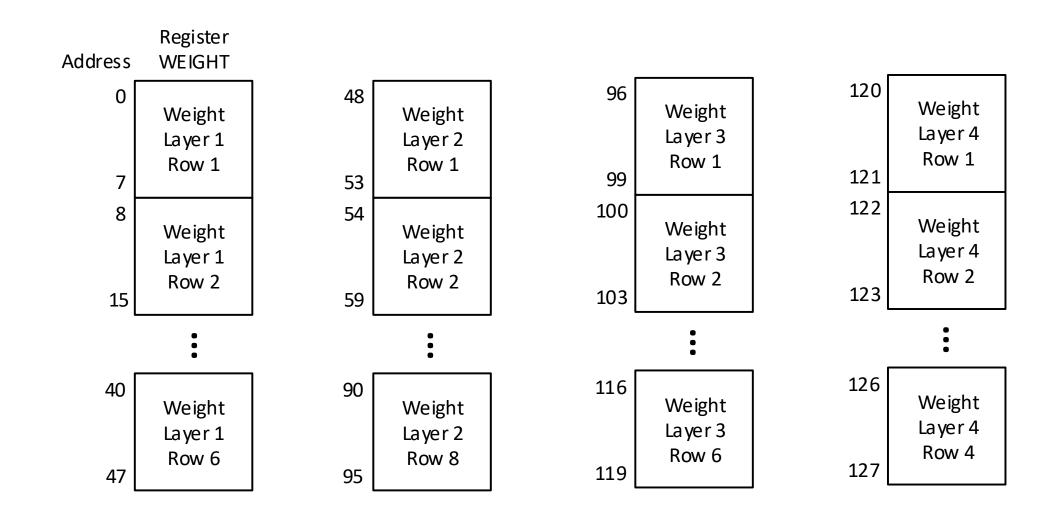


Address Register Map

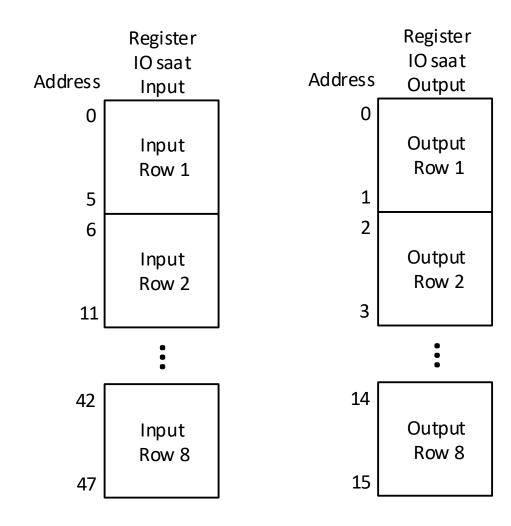
Address Map



Address Register Weight



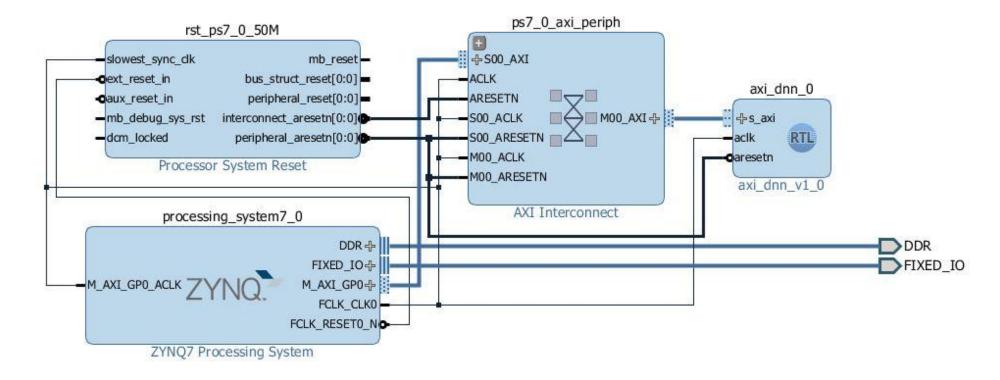
Address Register IO



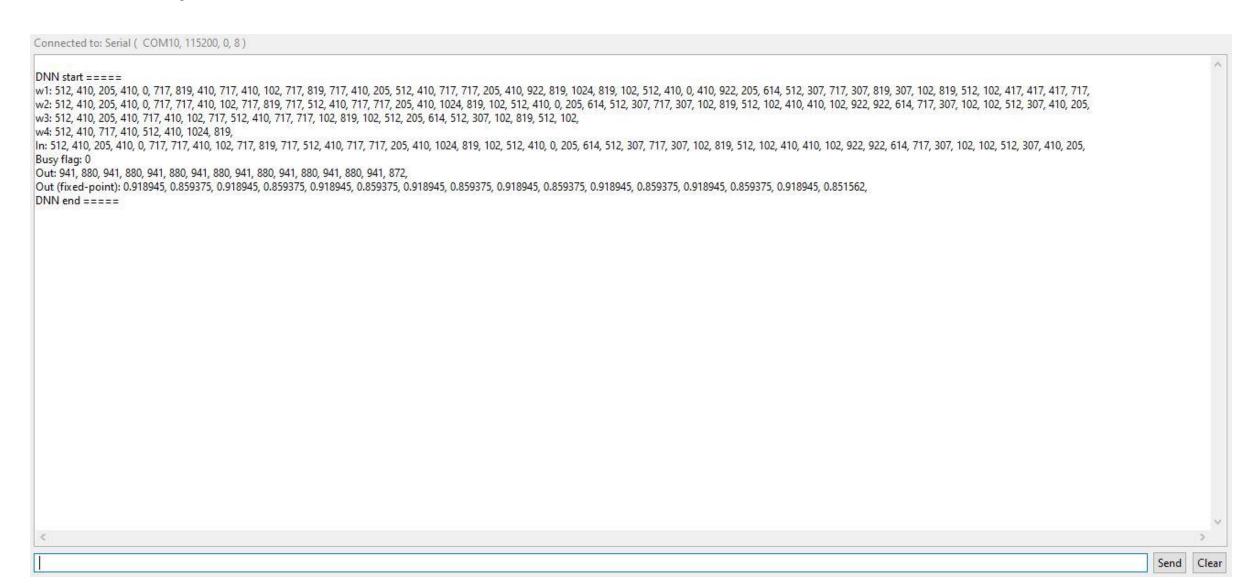
Implementasi di Board ZYBO

Block Design

- Tambahkan ZYNQ PS dan aktifkan UART 1
- Tambahkan module axi_dnn



Output SDK Terminal



Thank You