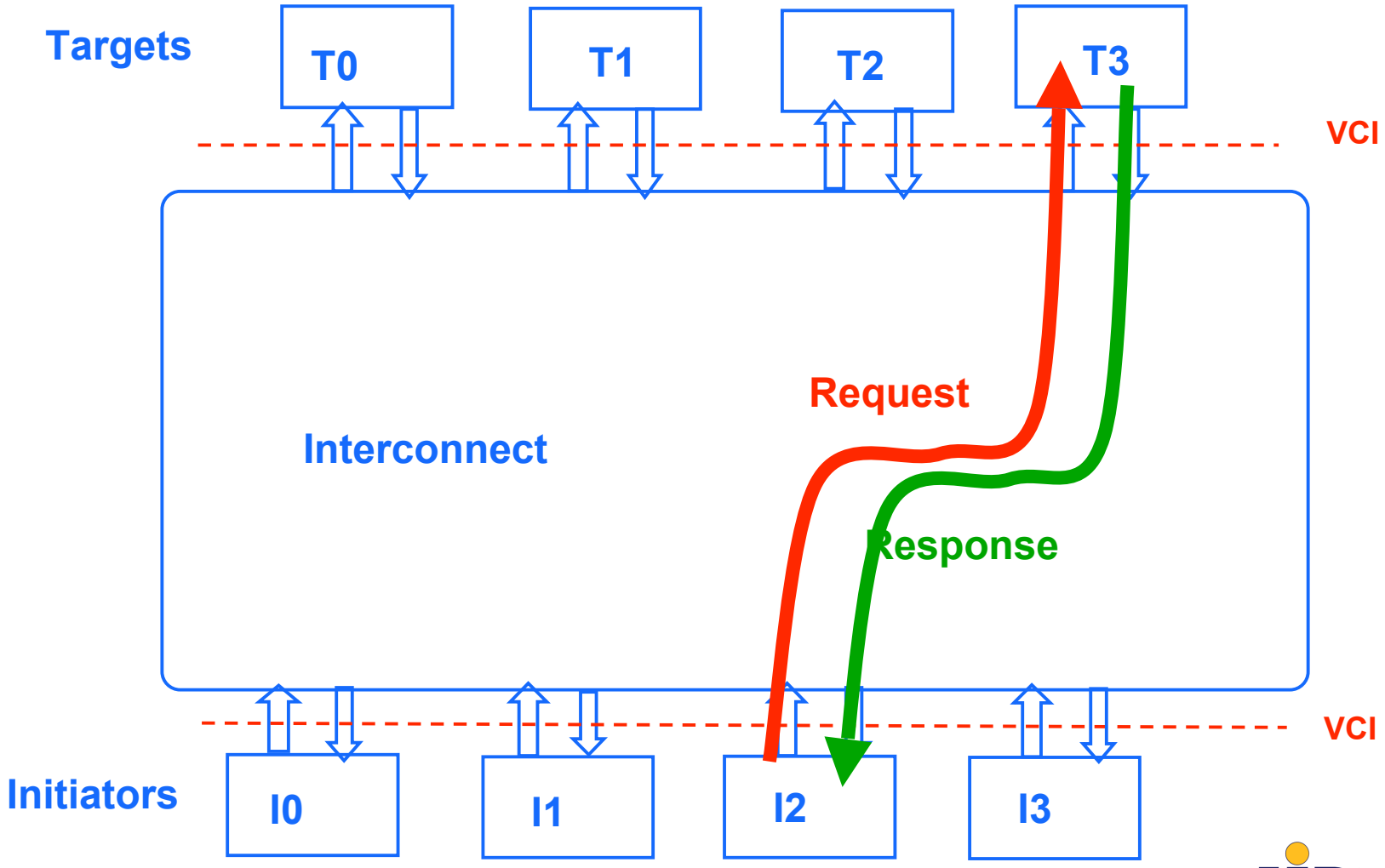
The SPIN & DSPIN networks on chip

Alain Greiner

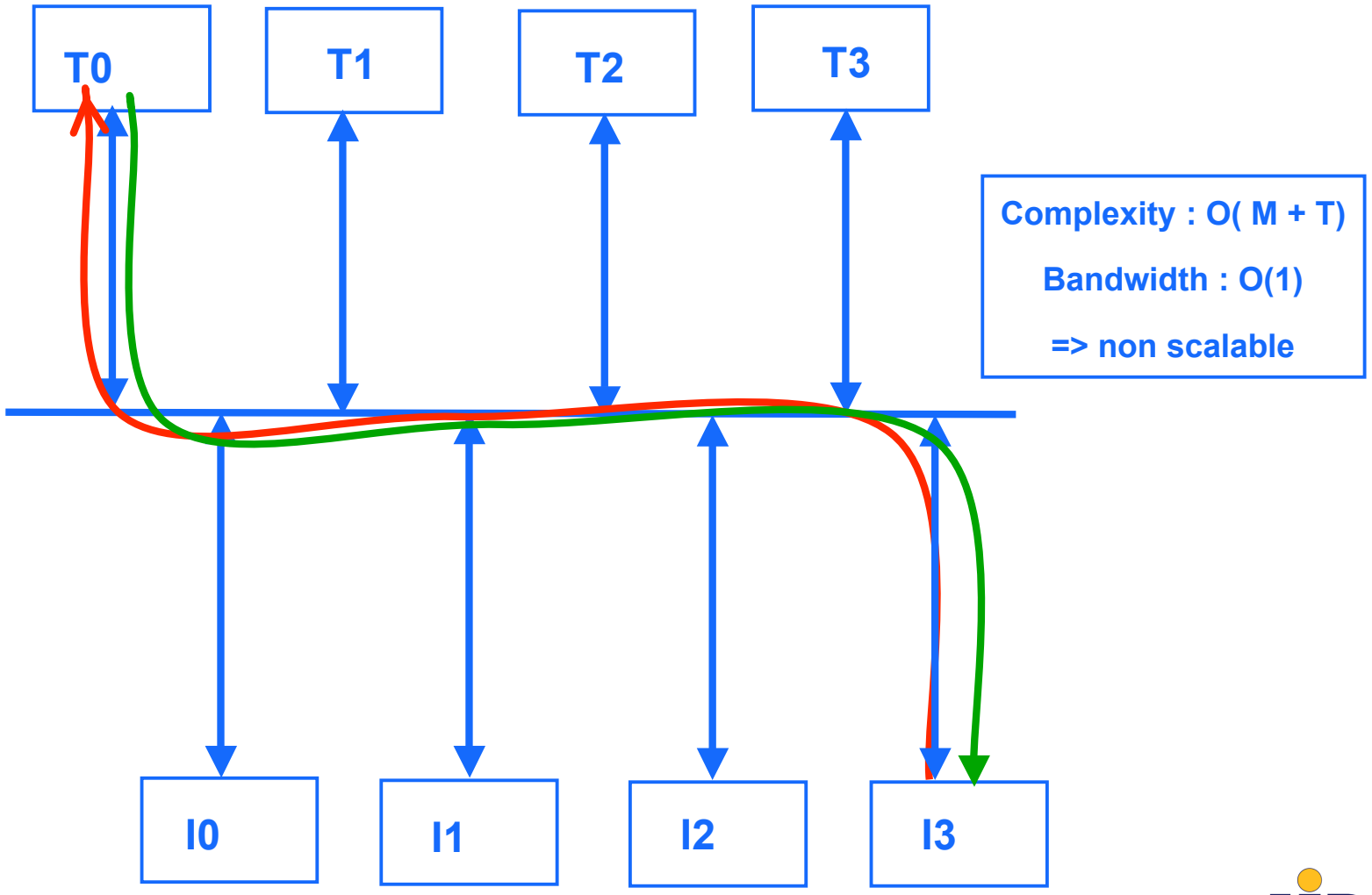
Outline

- Introduction
- The SPIN micro-network architecture
- The SPIN32 evaluation chip
- The DSPIN micro-network architecture
- DSPIN performances
- Conclusion

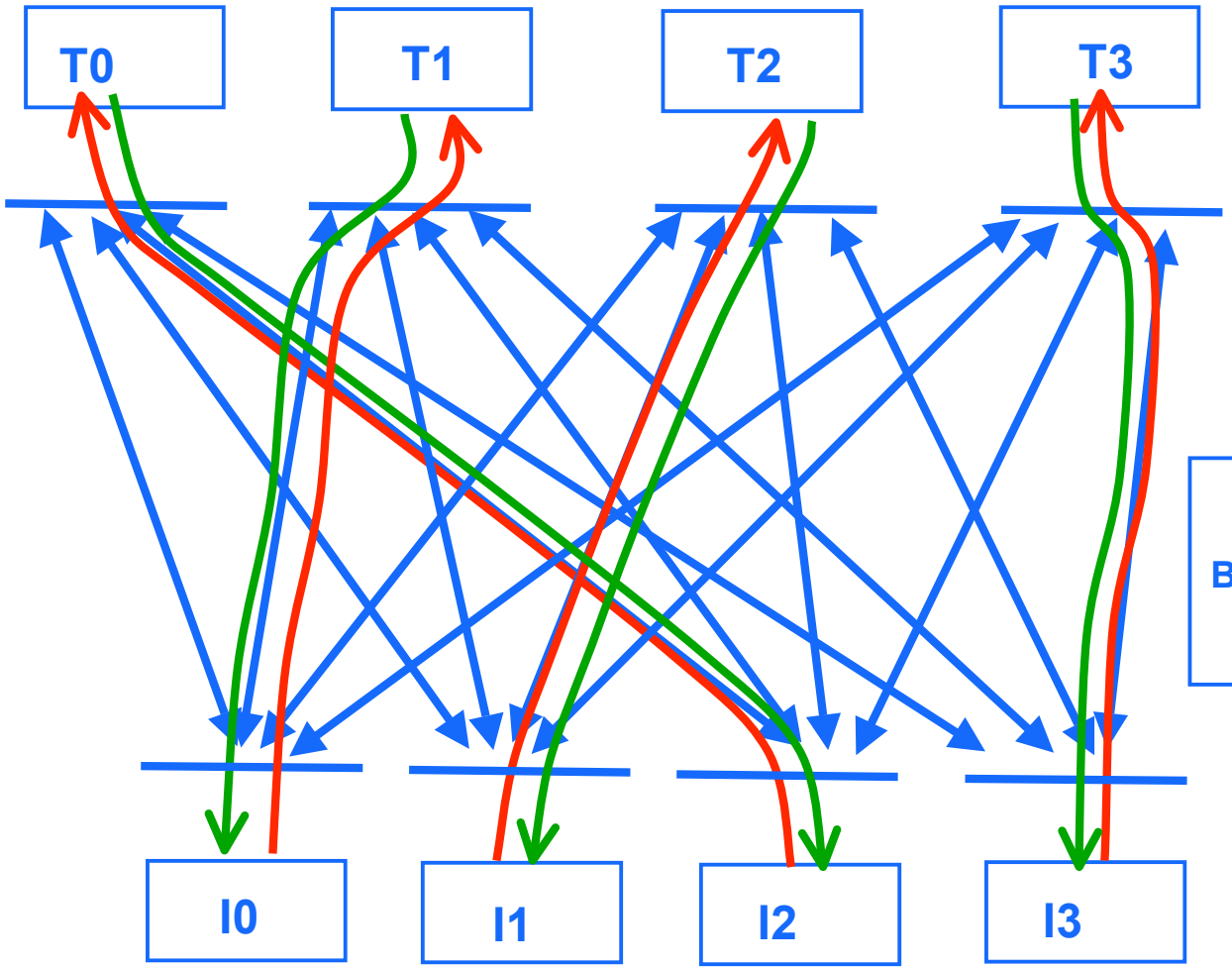
Multiprocessors architectures



Shared bus


T0
T1
T2
T3
I0
I1
I2
I3
Complexity : O(M + T)
Bandwidth : O(1)
=> non scalable

Cross-bar

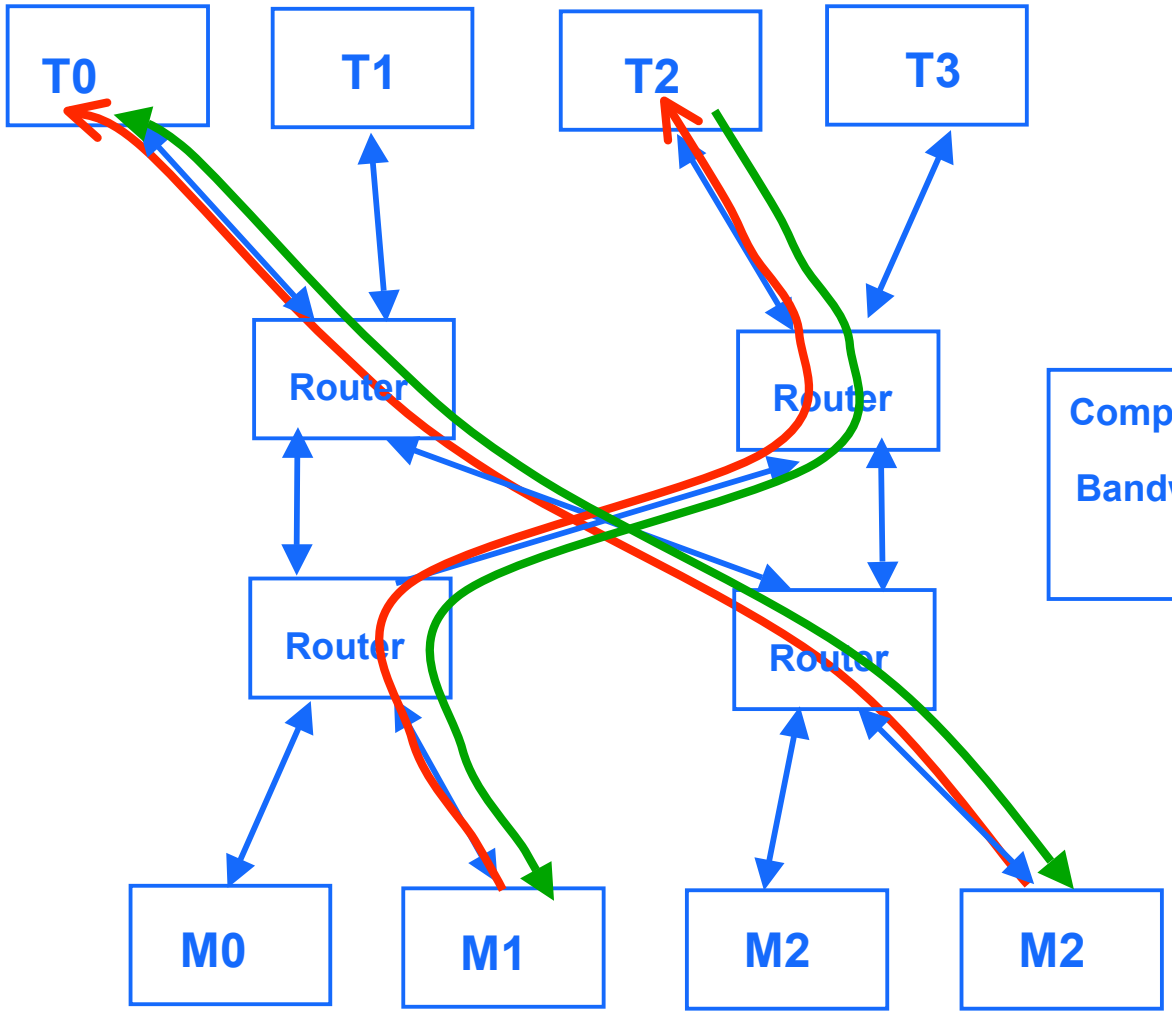


Complexity : O(M * T)

Bandwidth : O(max (M,T))

=> non scalable

Multi-stage network



Complexity : O(log(M + T))

Bandwidth : O(max (M,T))

=> scalable

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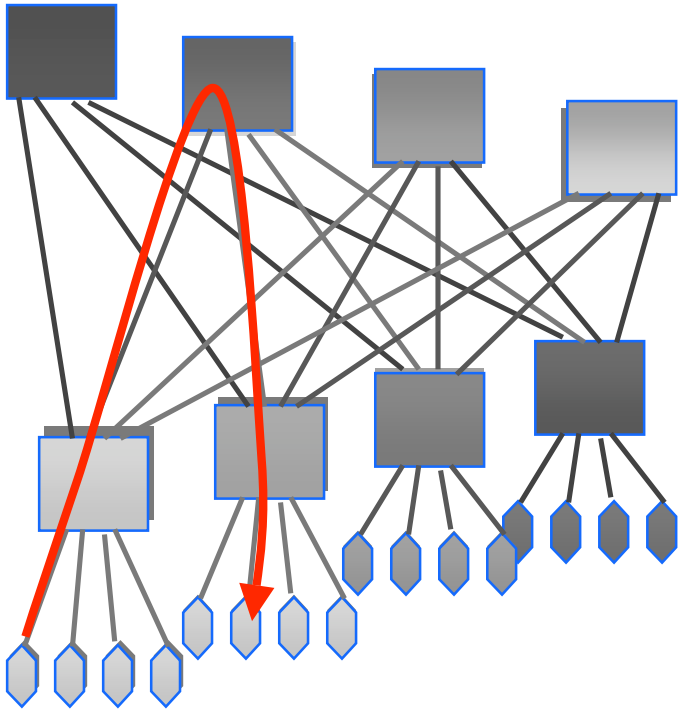
SPIN micro-network architecture

- multi-level Fat-Tree topology
- packet switching network
- wormhole routing
- point to point bidirectional links
- credit-based flow control
- adaptative routing

SPIN network



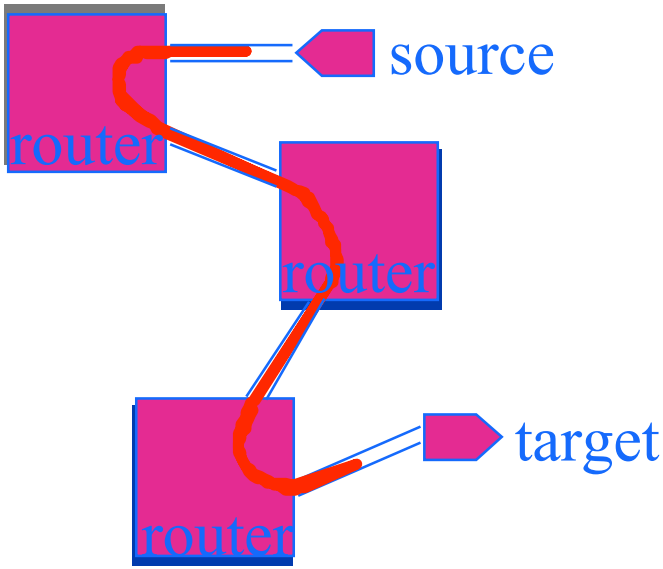
Multistage Packet Switched Networks

Packet Switching :

- **No circuit reservation**
- **Atomic transaction = *packet***

Wormhole routing:

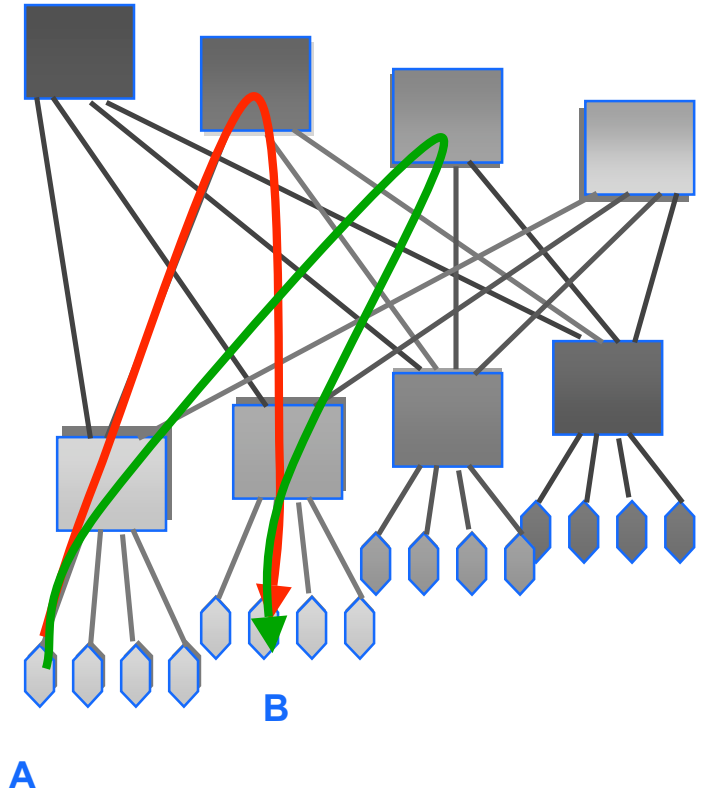
- **routers forward packets ASAP**
- **packets span several routers**



Adaptive routing

- Upward routing is adaptive
- Downward routing is deterministic

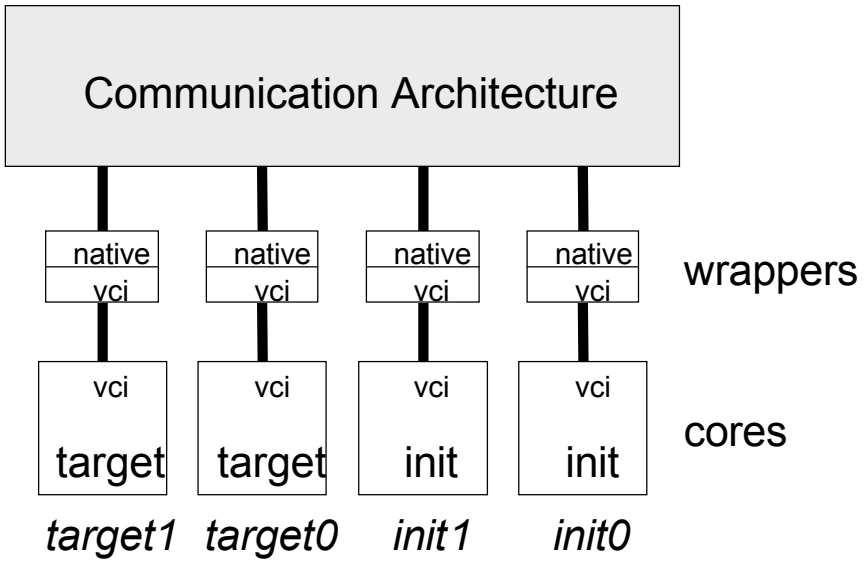
SPIN network



Performance evaluation

© Simulation of multi-master / multi-target architectures running a synthetic workload.

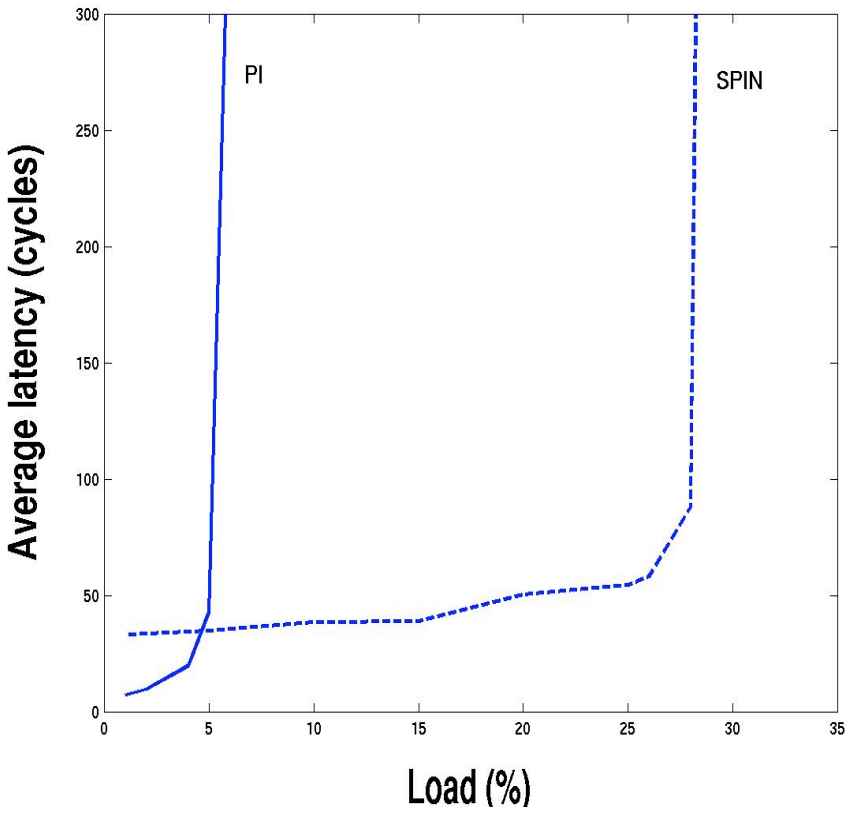
© All components are described in the SoCLib environment as cycle-true bit-true models for SystemC,.



Latency / Load

- The variable parameter is the offered load
- 32 cores : 16 initiators and 16 targets.
- Random traffic : The 16 initiators send randomly read request (8 words = a cache line) to the 16 targets (for both architectures).
- Measure the average latency for a transaction.

SPIN / PI-BUS comparison



- saturation threshold = 30%

-Minimal latency = 30 cycles

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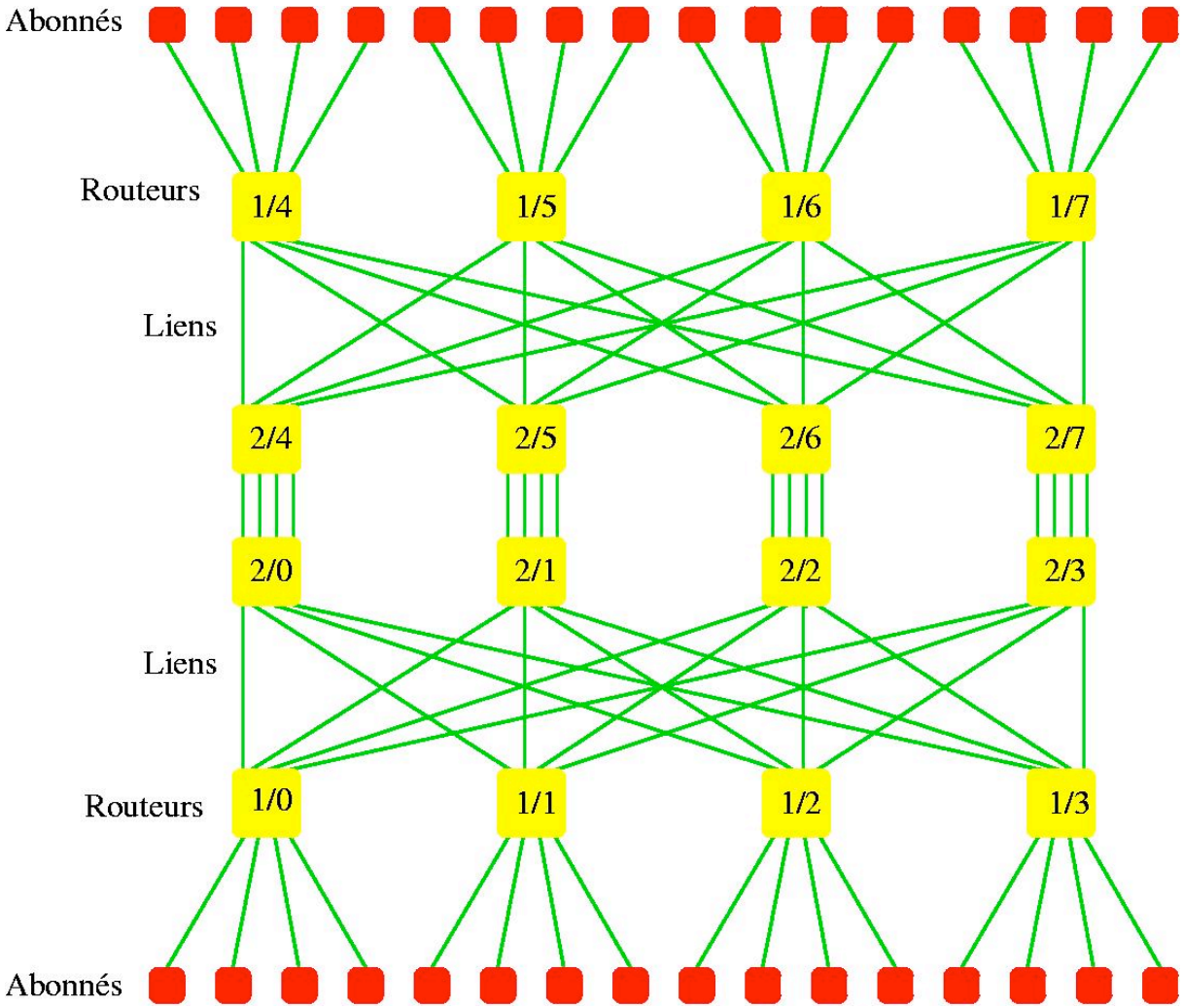
Evaluation chip : SPIN32

main goals :

- Provide a silicon proof of the *SPIN* concept in 0.13µ CMOS
- Confirm the simulation results : latency & throughput
- Measure the maximum clock frequency
- Measure the reliability under several stress environments
- Measure the power consumption

A 32 ports SPIN network

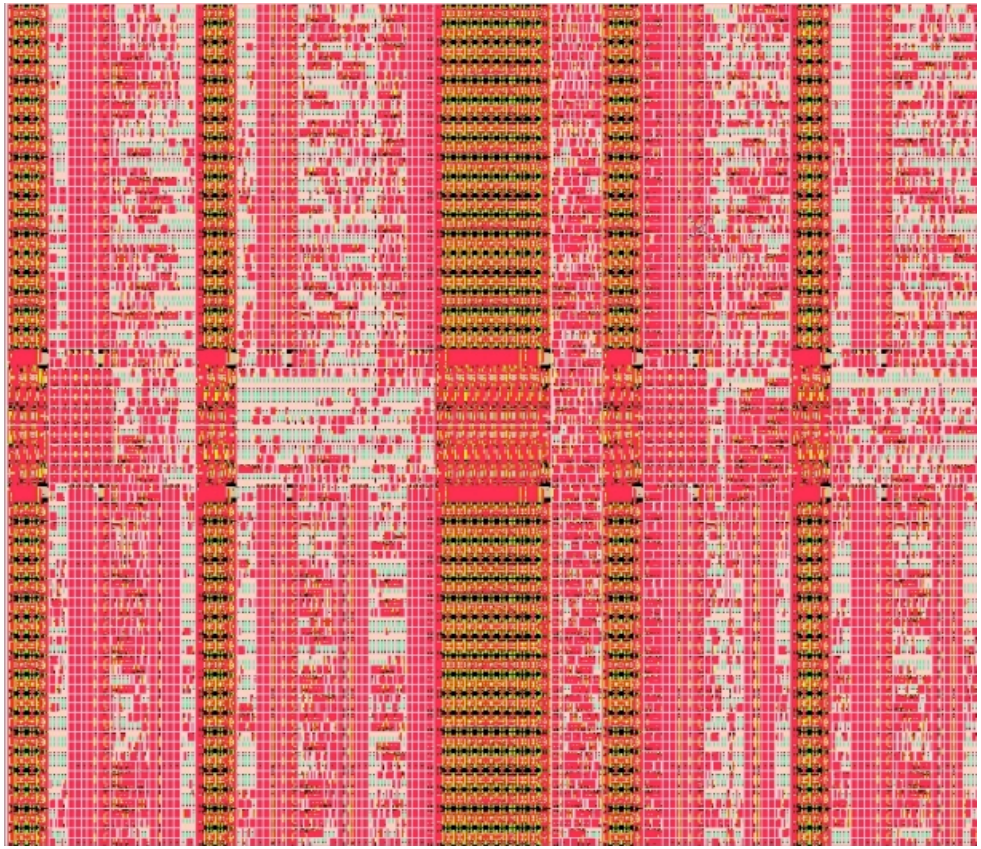


Evaluation chip architecture

The 32 ports SPIN micro-network (*spin32* macrocell) is surrounded by a dedicated instrumentation logic.

This evaluation chip has been fabricated by *ST Microelectronics* in *0.13 micron* CMOS process.

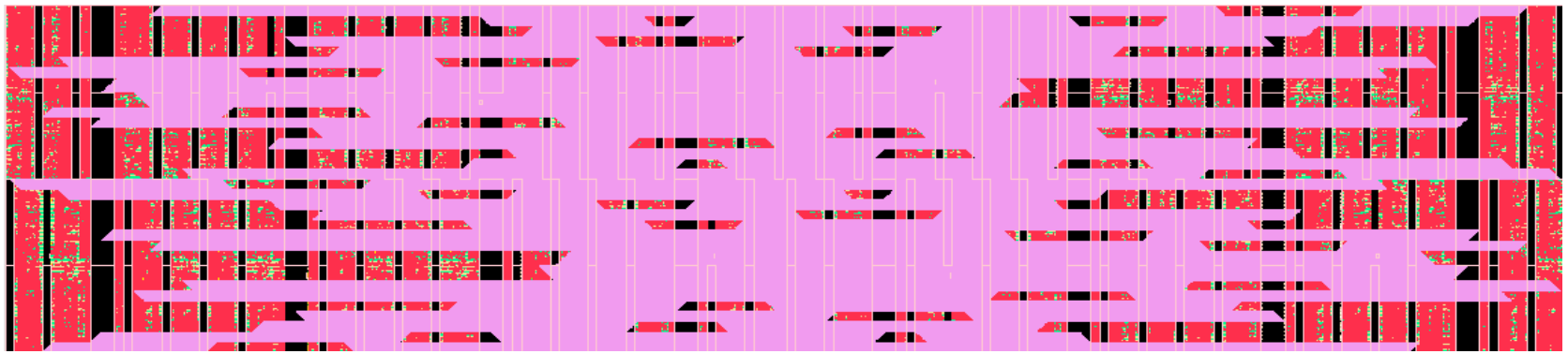
RSPIN router layout



- © Symbolic layout for process portability
- © Area is 0.24 mm² in *CMOS 0.13µ*

SPIN32 macrocell layout

- © Symbolic layout for process portability
- © Inter-routers wires are routed over cells in metal 4, 5 and 6
- © 1 390 464 transistors
- © 4.6 mm^2 in *STMicroelectronics 0.13* μ with 6 metal layers



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SPIN strengths

© For shared memory architectures, the SPIN micro-network with VCI / SPIN wrappers provides the same service as a classical “system bus” (making possible IP reuse).

© SPIN demonstrated a truly scalable bandwidth.

© A 32 ports SPIN can be physically implemented in 4.6 mm^2 for a 0.13 μ CMOS process, with all wires routed on top of the routers.

SPIN weaknesses

- Adaptive routing improve the saturation theshold…,

  but destroys the « in order delivery » property.
- The fat-tree topology has a minimal diameter…,

  but is not very flexible.
- The SPIN32 « hard macrocell » is highly opimized…,

  but it is not synthesisable.
- The centralized approach for the SPIN network is

  not compatible with the GALS (Globally Asynchronous, Locally synchronous) approach.

DSPIN / SPIN

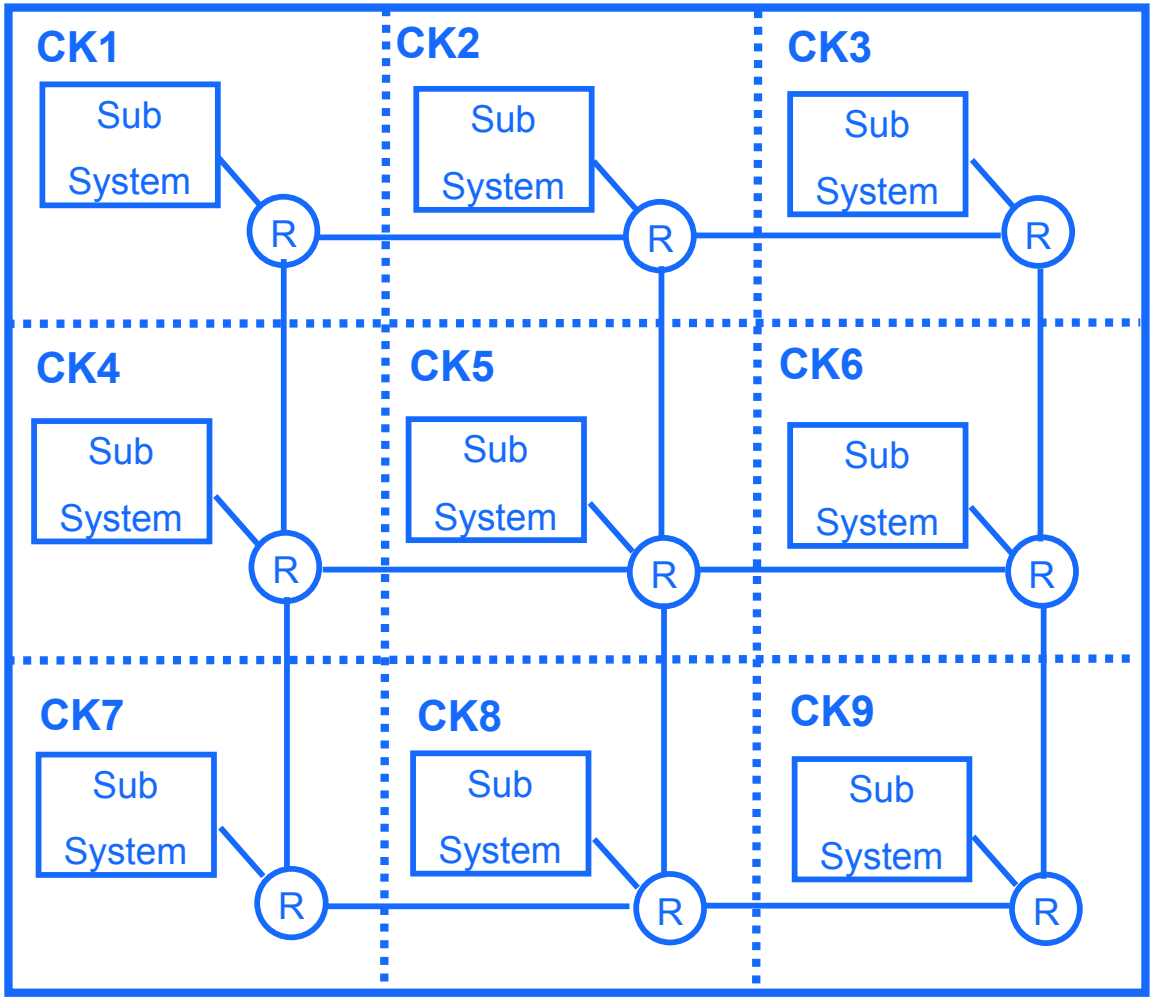
What is conserved

- © Packet switching
- © Wormhole routing
- © Full duplex physical links
- © VCI interface
- © Shared address space

What is different

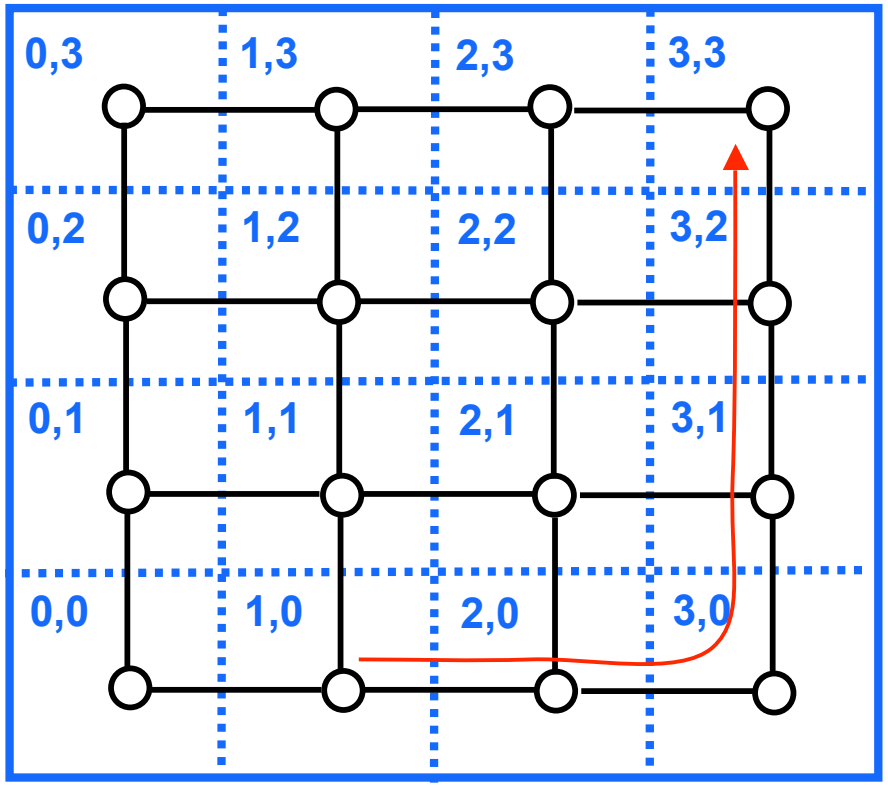
- © Mesh topology
- © Distributed
- © Asynchronous
- © Deterministic routing
- © Synthesisable
- © Clustering

DSPIN : Mesh Topology



Deterministic Routing

DSPIN uses the X-first routing algorithm, that gives the micro-network the « in-order delivery » property.



if X > Xloc -> EAST

If X < Xloc -> WEST

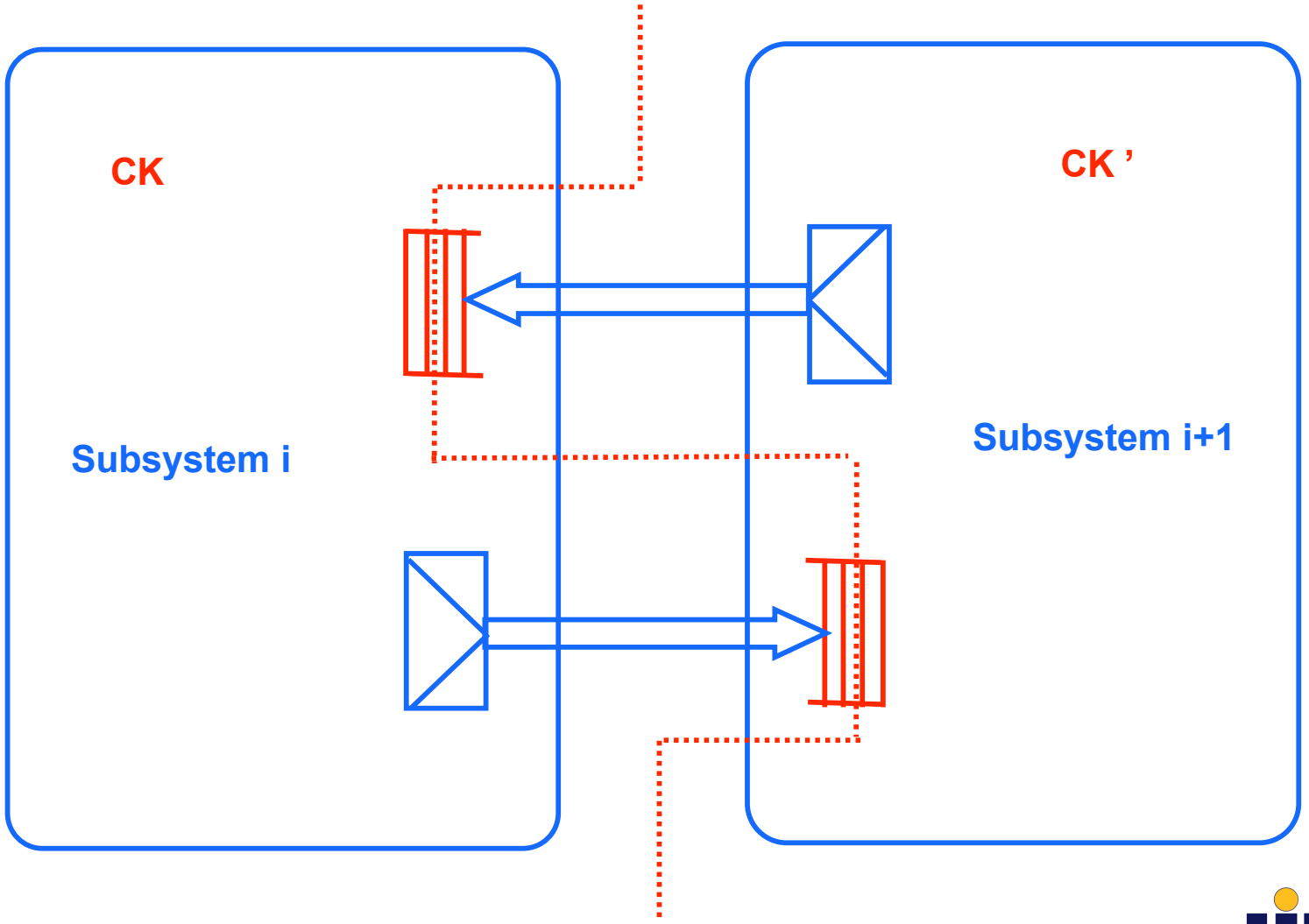
If X = Xloc

if Y > Yloc -> NORTH

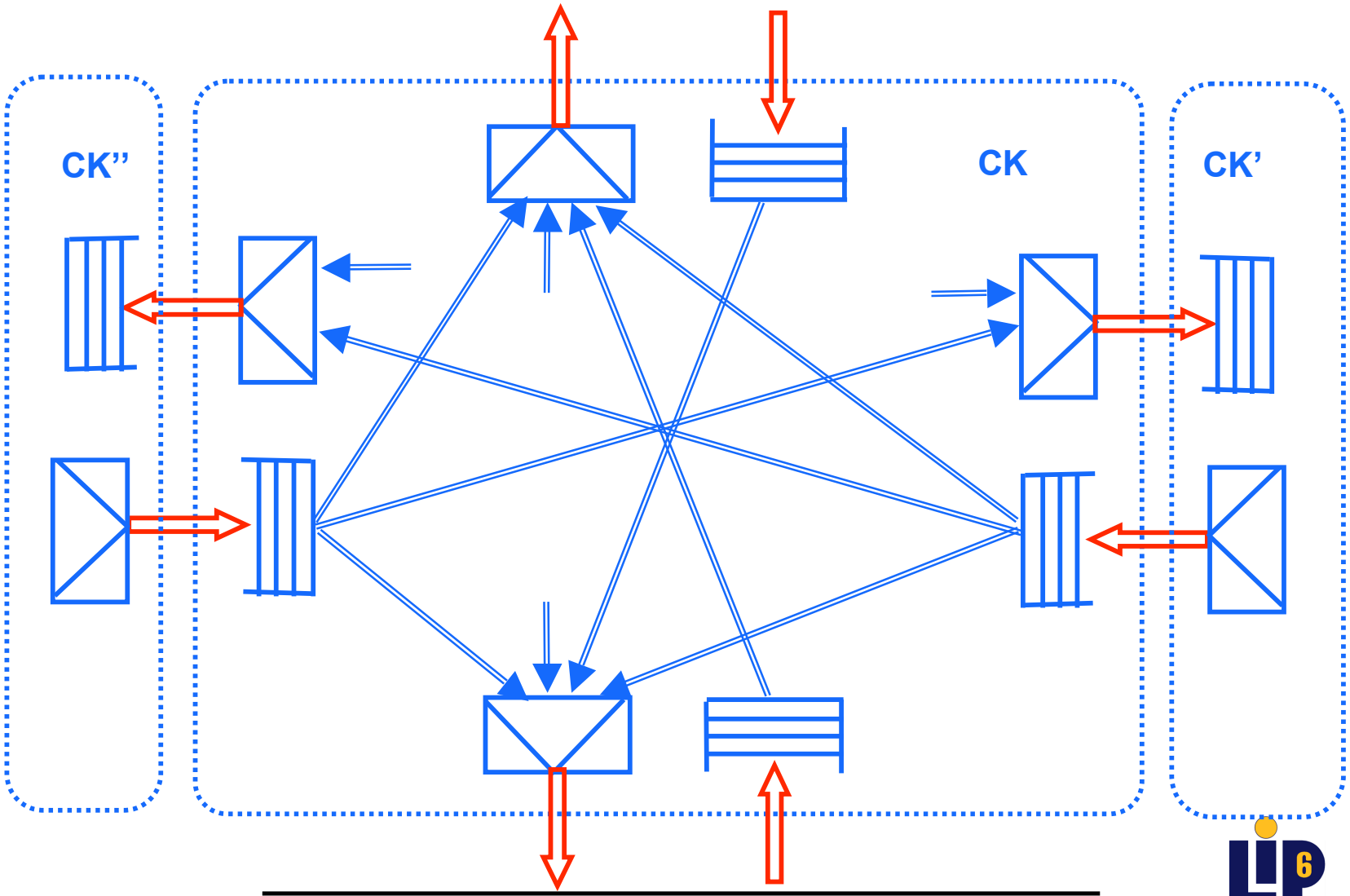
if Y < Yloc -> SOUTH

if Y = Yloc -> LOCAL

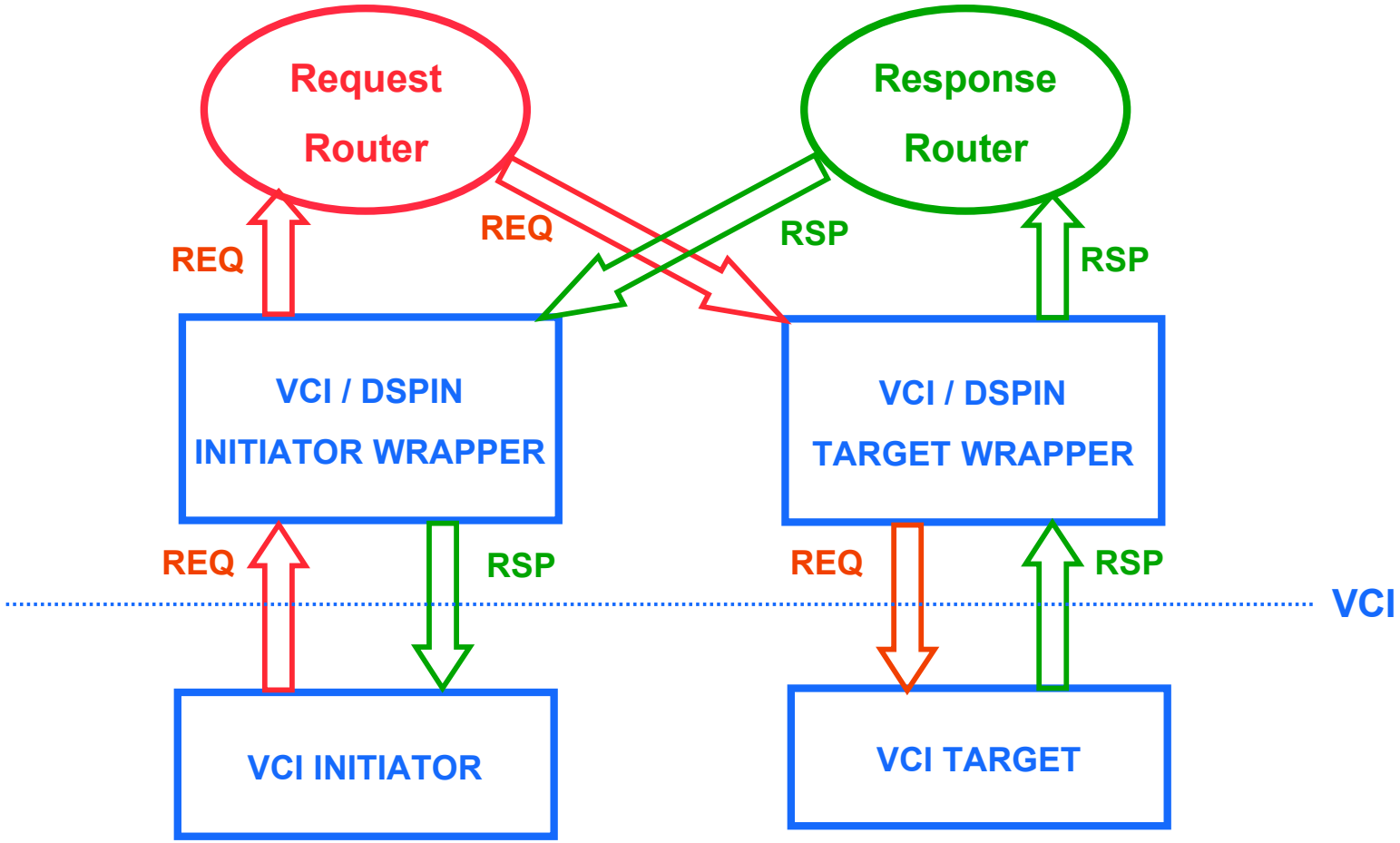
DSPIN : Clock Boundaries



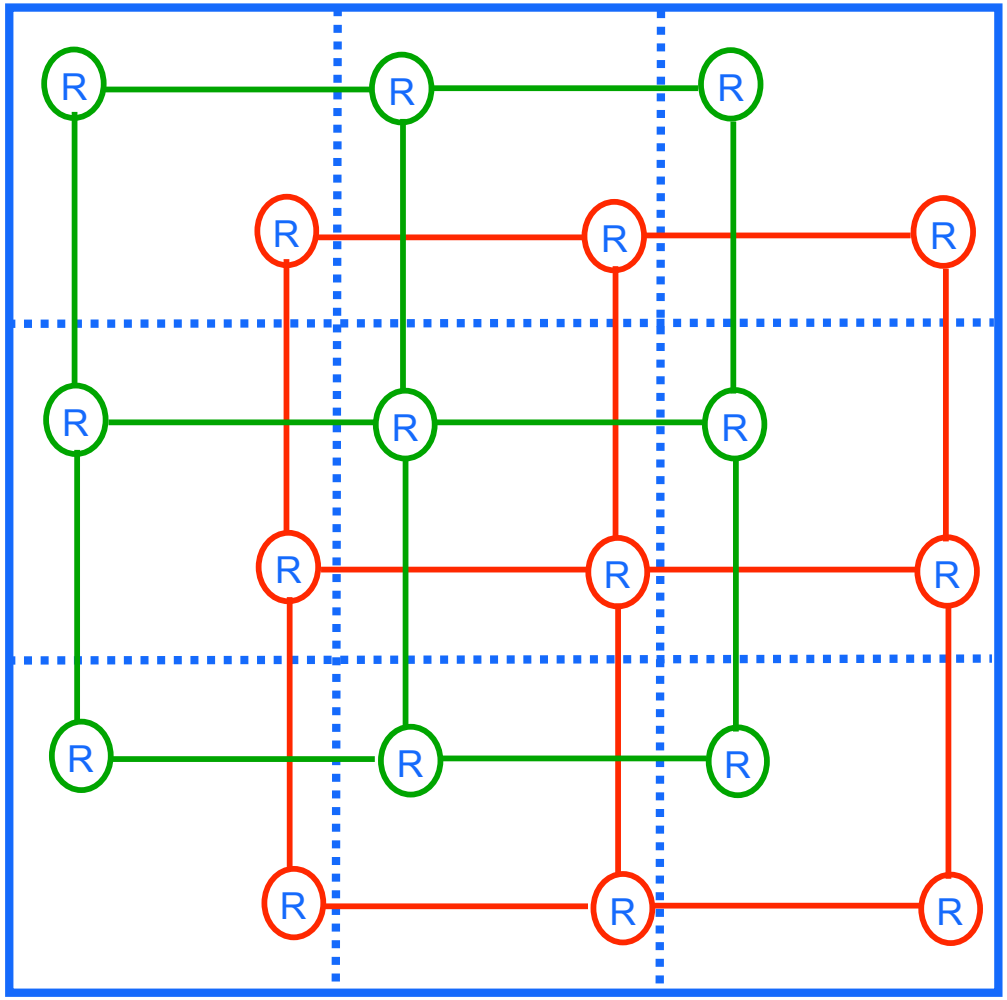
Distributed DSPIN Router



Separated Requests & Responses

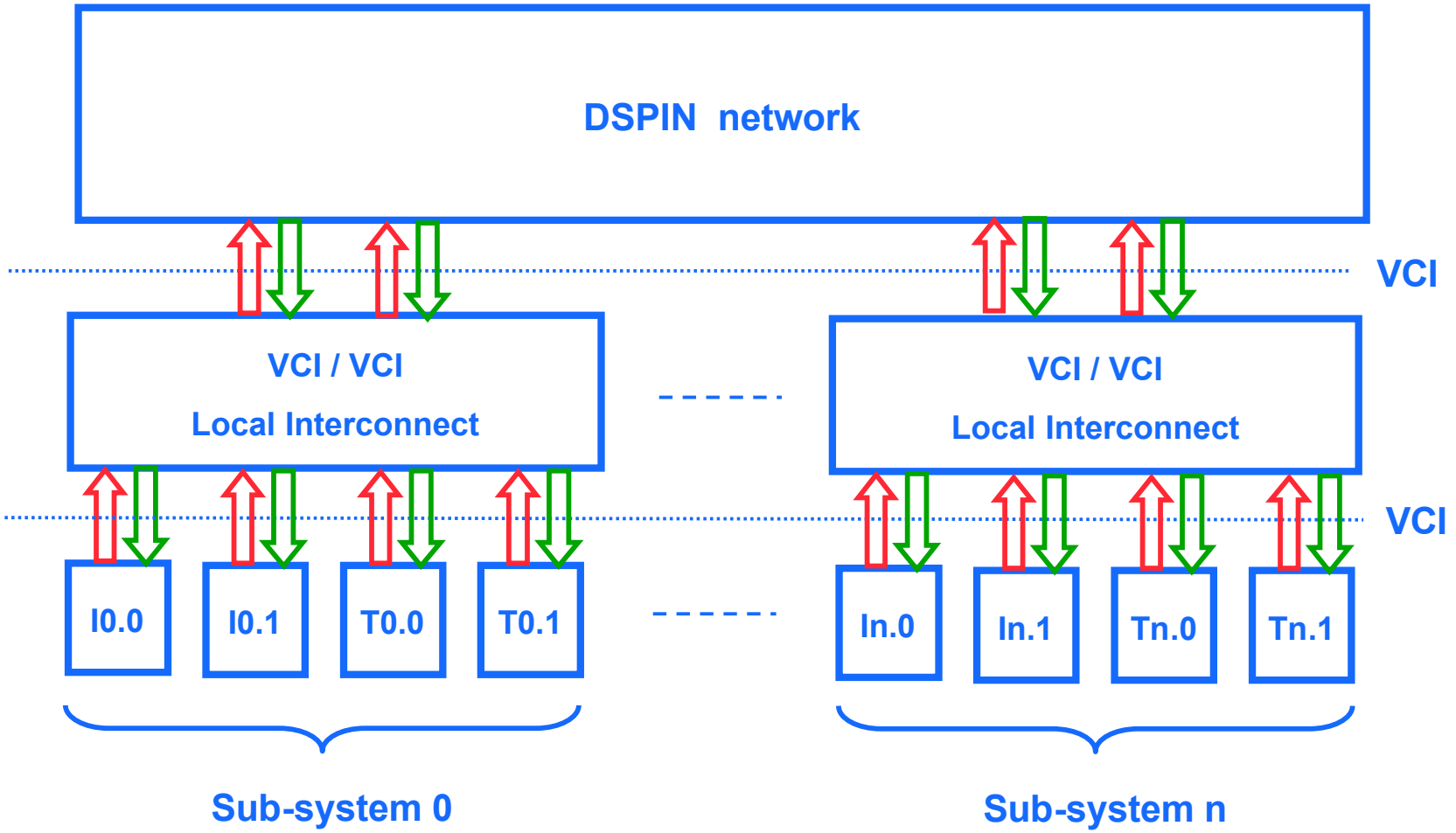


Interleaved Request & Response networks



In order to prevent dead-locks, DSPIN uses two fully independant networks for requests and responses

Two level hierarchical routing



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DSPIN status

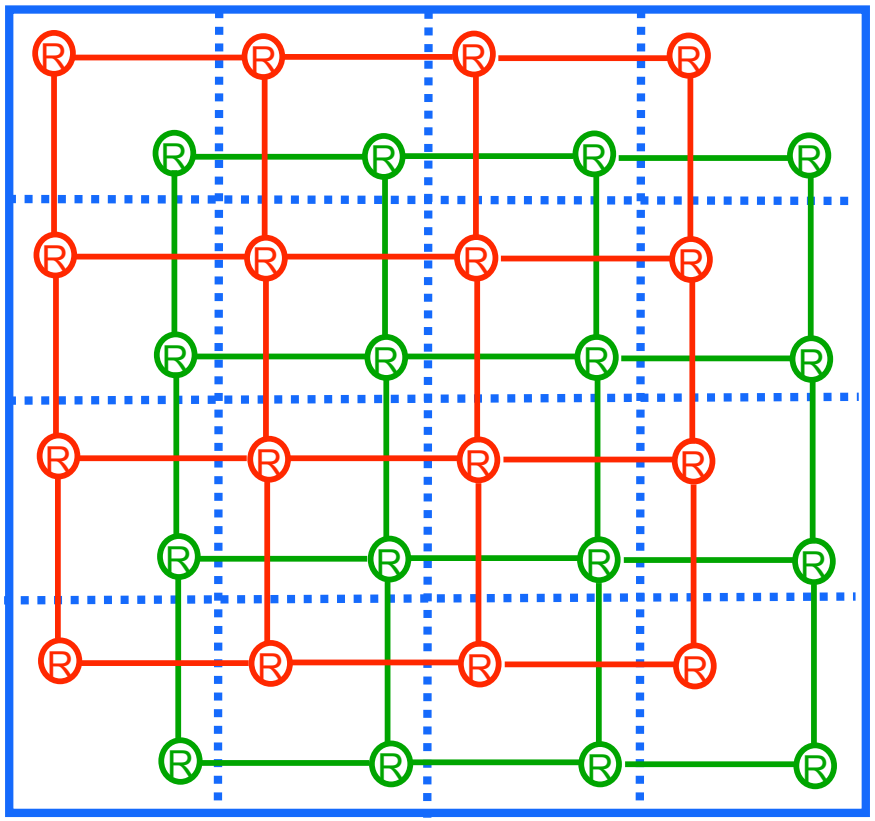
© SystemC Cycle-Accurate and Bit-Accurate simulation models have been written for the 3 DSPIN components :

- DSPIN router
- DSPIN/VCI initiator wrapper
- DSPIN/VCI target wrapper

Those SystemC models have been validated in a 16 processors integrated network.

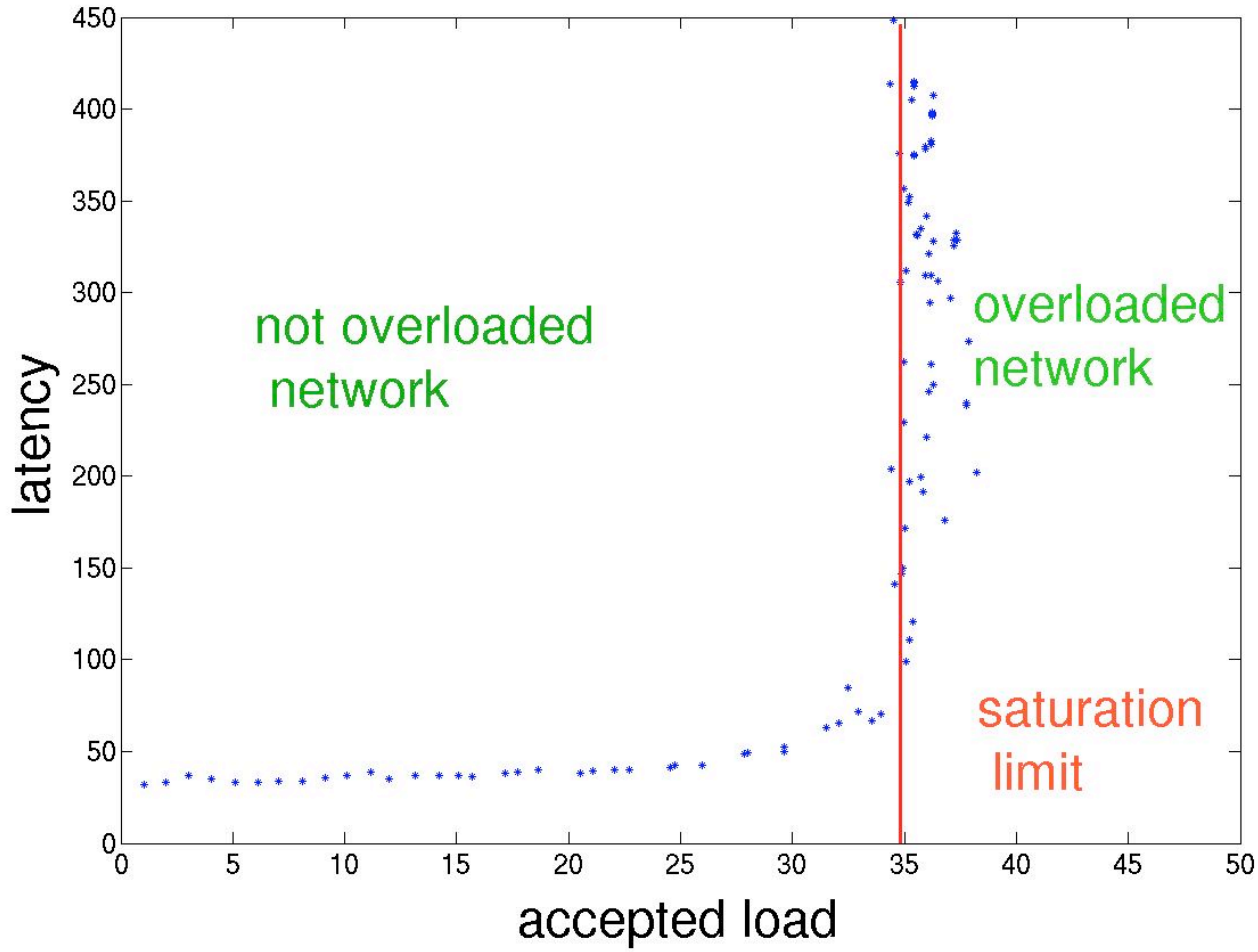
© VHDL synthesizable models have been designed and synthesized, using SYNOPSYS and the Alliance standard cells library. The footprint of the DSPIN router is two times smaller than the footprint of the SPIN router.

The simulation plat-form



- 16 nodes architecture
- Each node contains
  1 processor and 1 RAM
- Each processor sends
  randomly distributed
  read request to all RAMS
- Each request is 8 words
  (a cache line)

Saturation threshold & minimal latency



Conclusions

© The DSPIN architecture, as the SPIN architecture, provides the system designer a truly scalable bandwidth.

© The DSPIN architecture is suited to the GALS (Globally Synchronous / Locally Synchronous) approach.

© The DSPIN architecture solves the problem of timing closure due to long wires, that is critical in DSM processes.

© The DSPIN performances (bandwidth and latency) are equivalent to the SPIN performances, with a smaller footprint.

© The DSPIN components (routers and wrappers) are synthesizable, which is mandatory for an industrial product.

© All SystemC SPIN &DSPIN simulation models will be integrated in the SOCLIB modeling and simulation platform.

© A physical implementation of the DSPIN architecture is planned in 2005 at CROLLES (90 nanometer process), in cooperation with the group of J.P Schoelkopf.