On-chip Detection Methodology for Break-Even Time of Power Gated Function Units

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Abstract— **In a fine-grain leakage saving technique to power gate function units, the efficiency is sensitive to overhead energy dissipating at turning on/off power switches. To get gain in energy savings, the powered-off period has to be longer than the minimum required time i.e. the break-even time (BET). While effectiveness of BET-aware power-gating control has been described in literatures, how to actually detect BET that fluctuates with the temperature and process variation has not been reported so far. This paper proposes an on-chip detection methodology for BET using pMOS/nMOS leakage monitors with MTCMOS circuit structure. We applied this methodology to the leakage monitors and a CPU including a power-gated multiplier implemented in 65nm CMOS technology. Results showed that our methodology detects BET at 5%-17% difference from that of the conventional simulation-based off-line technique.**

Primary Classification -
B. Hardware B.7 INTEGRATED CIRCUITS B.7.0 General
General Terms - Design
Keywords - leakage monitor; power gating; break-even time

I. INTRODUCTION

Power gating (PG) is one of the key techniques to reduce leakage power in scaled devices. In multi-core processors [1], unused processor cores are powered off by turning off on-chip power switches (PS) for the cores. In this "core-level" PG, power-off is possible only when the entire core becomes unused. This constraint reduces the opportunity to save the leakage. To increase this opportunity, PG in finer granularity has been proposed [2] [3]. In [2], the authors presented a technique to power gate execution units such as a fixed-point unit and a floating-point unit in a microprocessor. In [3], an approach has been proposed to power gate function units such as an ALU, a shifter, a multiplier or a divider in a CPU core by pre-decoding instructions. In these fine-grain power-gating (FGPG) approaches, energy saving efficiency becomes more sensitive to energy overhead caused by powering off/on the circuits, as compared to the coarse-grain techniques. To gain in energy savings, the powered-off period has to be long enough to compensate the energy overhead. The minimum powered-off time to gain in energy savings is referred to as the break-even time (BET) [2]. BET is the time at which leakage energy saved by powering off becomes equal to the energy overhead. In [4], the authors reported that BET reduces exponentially as the temperature goes up. They also reported simulation results for a MIPS CPU core running a DCT program showing that powering off function units at every idle event does not reduce the total energy but instead increase energy by 1.5x at the room temperature. This is because idle events with over-BET idleness share only 1% in the total idle events for a multiplier, shifter and ALU. In contrast, at higher temperature, BET gets shorter and hence the share of over-BET idle events increases. To reduce energy dissipation effectively, a control scheme to switch enabling and disabling PG depending on BET is required. In [2], the authors proposed a Time-Based (TB) sleep control scheme to count idle cycles from the beginning of idleness and to enable PG if the counted value reaches BET. In [4], the authors demonstrated that the TB sleep control utilizing temperature-dependent BET gives further 7% and 20% energy-savings at 65□C and 100□C, respectively, as compared to the TB control utilizing a fixed BET in a multiplier.

Thus, importance of BET in FGPG has been pointed out in many literatures. However, methodology on how to actually detect temperature-dependent BET on chip during the operation has not been studied so far. In this paper, we describe an on-line BET detection methodology to use a leakage monitor capturing temperature and process-variation sensitive leakage current. Contributions of this paper are three fold:

(1) We built analytical models for the response of a leakage monitor and investigated the relationship to BET.

(2) We proposed a novel on-chip detection methodology for BET of power-gated function units by using a leakage monitor.

(3) By applying to a power-gated multiplier in an actually implemented RISC CPU core, we demonstrated that the proposed methodology detects BET in good accuracy.

The rest of the paper is organized as follows: Section 2 describes related work. Section 3 presents analytical models for the leakage monitor and Section 4 describes the detection methodology that we propose. Section 5 describes the experimental setup for evaluation and Section 6 presents the results.

II. RELATED WORK

Techniques to know BET have been reported in several literatures. In [3], the authors presented a simulation-based approach to estimate BET. By using a circuit simulator, they analyzed the total energy of a function unit both at the PG-

enabled and the PG-disabled modes while changing the sleep cycles. BET is obtained by finding the sleep cycles where the energy values for the PG-enabled and the PG-disabled cases become equal. However, this approach is essentially an off-line technique. It is not possible to detect BET that dynamically changes with the temperature at a real chip in this approach.

A technique to measure BET with a real chip is reported in [5]. When measuring BET of a power-gated multiplier, a test program with a simple loop consisting of a multiplication and several interval cycles is provided to a CPU core. Current dissipations are measured for PG-enabled and PG-disabled cases. BET can be obtained by finding the interval cycles where current dissipations for the PG-enabled and PG-disabled cases become equal. However, this technique requires current measurements using an external ampere meter. Also, the measurements need to be conducted for the PG-enabled and PG-disabled cases while changing the interval cycles at the specified temperature. It is not possible to use this technique to dynamically monitor BET during the operation and to use the result for adaptive PG control.

A key component to meet this requirement is an on-chip leakage monitor. Kuroda et al [6] proposed a circuit to monitor the fluctuation of leakage current caused by process variations. Kim [7] reported an improved circuit with higher sensing gain. However, since these circuits are less sensitive to the temperature variation, detecting temperature-dependent BET with them is difficult. Instead of using a leakage monitor, employing a temperature sensor is another option. On-chip thermal sensor circuits have been reported in [8] and [9]. However, it is reported that since the thermal-sensor response is affected by process variation, calibration using a process monitor is required. This means that if we use a thermal sensor to detect BET, we need a process monitor circuit as well and need a complicated calibration. Since our goal is not to know the temperature itself but to know BET, this approach makes a design more complex.

A leakage monitor that we proposed in [10] is a potential circuit that allows us to sense leakage change for both temperature fluctuation and process variation at a single circuit. In the paper, a basic idea to sense the temperature dependent leakage is described and simulation results are presented. However, how to use this circuit to detect BET is not described. Furthermore, investigations on the relationship between the leakage-monitor response and BET are not described, either.

To the best our knowledge, this is the first work to demonstrate the methodology to detect BET of power-gated function units by using a leakage monitor that senses both temperature fluctuation and process variation.

III. MTCMOS LEAKAGE MONITOR

A. Analytical Model

In our detection methodology, we employ a leakage monitor presented in [10]. The structure is depicted in Fig. 1. The main part is composed of two components: a model circuit and a voltage comparator. In the model circuit, Low-Vt transistors of P1 and N1 are connected to a High-Vt power-switch transistor N2 in series and the gate voltage of P1 and N1 is set to V_{DD}. Initially the enable signal EN_{MODEL} is set to „1'. When EN_{MODEL} is set to „0', the power-switch N2 is turned off and the parasitic capacitance of the virtual-ground (VGND) line is gradually charged up by the leakage current flowing through P1. This results in increase of the VGND voltage. When the leakage in P1 becomes large, the VGND voltage rises faster. This means that leakage current can be monitored by detecting the rise-time of the VGND voltage. In the entire leakage monitor circuit, the VGND voltage is compared with the pre-determined reference voltage (V_{REF}) at the voltage comparator circuit. The time is measured by a counter after turning off N2 until the VGND voltage reaches V_{REF}.

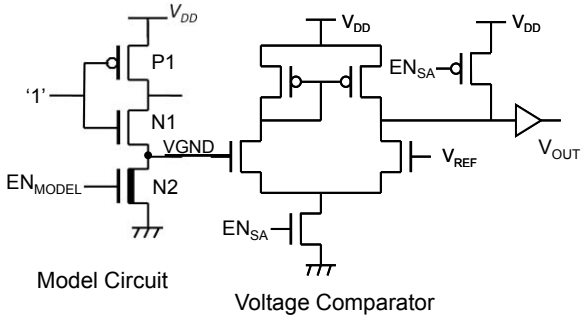

Figure 1. MTCMOS leakage monitor circuit (pMOS monitor)

In order to see how the rise-time of the VGND voltage changes with temperature-dependent leakage, we built an analytical model in the following way. First, we derived an equation expressing how the VGND voltage V rises with the time. Assuming that after turning off N2 the VGND voltage rises by □V within the time □t, the electric charge Q stored into the capacitance C_{VGND} within □t can be expressed as

$$Q = C_{VGND} \cdot \Delta V = I(V) \cdot \Delta t \quad (1)$$

where I(V) is the leakage current of P1. Sub-threshold leakage I(V) can be expressed as

$$I(V) = I_0 \exp(-V_T(V_{DS})/mU_t) \quad (2)$$

where I_0 is the coefficient which is independent of V_T or the voltage; $V_T(V_{DS})$ is the threshold voltage dependent on the drain-source voltage; m is the body-effect coefficient; and Ut is the thermal voltage. The threshold voltage $V_T(V_{DS})$ can be expressed as

$$V_T(V_{DS}) = V_T - \eta \cdot |V_{DS}| = V_T - \eta \cdot (V_{DD} - V) \quad (3)$$

where V_T is the threshold voltage when V_{DS} is zero; and □ is the DIBL factor. From (1), (2) and (3), the following differential equation is derived:

$$\frac{dV}{dt} = \frac{I_0}{C_{VGND}} \exp\left(\frac{\eta V_{DD} - V_T}{mU_t}\right) \exp\left(-\frac{\eta}{mU_t} V\right). \quad (4)$$

We define the detection time t_d as the time at which V reaches V_{REF}. Solving (4), considering the boundary conditions at t=0 and $t=t_d$, and replacing U_t with kT/q give

$$t_d = \frac{m}{\eta} \cdot \frac{kT}{q} \cdot \frac{C_{VGND}}{I_o} \exp\left(\frac{V_T - \eta V_{DD}}{m} \cdot \frac{q}{kT}\right) \left\{\exp\left(\frac{\eta V_{REF}}{m} \cdot \frac{q}{kT}\right) - 1\right\}. \quad (5)$$

We further define the Detection Time Ratio (*DTR*) as the ratio of t_d at the absolute temperature T over t_d at the room temperature T_{RT}. Then, *DTR* can be expressed as

$$DTR(T) = A(T) \cdot T \cdot \exp(K_2/T) \quad (6)$$

where

$$A(T) = \frac{1}{T_{RT}} \exp\left(-\frac{K_2}{T_{RT}}\right) \exp\left\{\frac{\eta V_{DD} q}{mk}\left(\frac{1}{T_{RT}} - \frac{1}{T}\right)\right\} \cdot \frac{\exp\left(\frac{\eta V_{REF}}{m} \cdot \frac{q}{kT}\right) - 1}{\exp\left(\frac{\eta V_{REF}}{m} \cdot \frac{q}{kT_{RT}}\right) - 1} \quad (7)$$

and $K_2=qV_T/mk$. Notice that *DTR* is determined only by T, V_{DD} and V_{REF} and is independent of I_0 and C_{VGND}. For V_{DD}=1.2V, V_{REF}=0.6V, T_{RT}=298K (i.e. 25□C), V_T=0.4V and m=1.38, we plotted *DTR* against T based on (6). The result is shown in Fig. 2. As depicted, *DTR* reduces as the temperature increases.

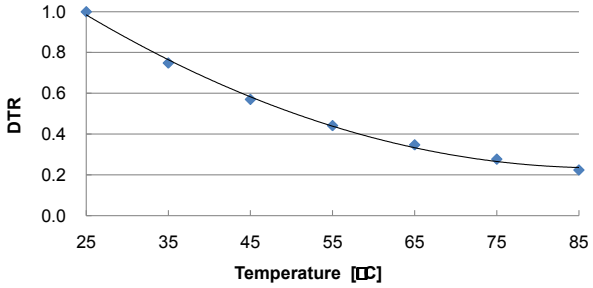

Figure 2. *DTR* as the function of temperature

Temperature dependence of BET was reported in [4]. The authors defined the break-even time ratio *BETR* as the ratio of BET at T over BET at T_{RT}. *BETR* at the temperature T can be expressed as

$$BETR(T) = T_{RT}^{\frac{3}{2}} \exp(-K_2/T_{RT}) T^{-\frac{3}{2}} \exp(K_2/T) \quad (8)$$

where $K_2=qV_T/mk$ as above. *BETR* reduces with the temperature as well as *DTR*. It should be noted that *DTR* and *BETR* both include the same factor "$\exp(K_2/T)$". In order to see the relationship between *BETR* and *DTR*, we computed both values for various temperatures and plotted *BETR* against *DTR*. The result is shown in Fig. 3. It should be noted that *BETR* increases almost linearly with *DTR* for the temperature range of 25□C to 85□C. The R^2 value at the linear approximation is 0.994. This means that *BETR* at T can be detected by the leakage-monitor responses at T and T_{RT}. Further, if BET at the room temperature is known in advance, BET at the operating temperature can be computed by multiplying BET at T_{RT} and *BETR*.

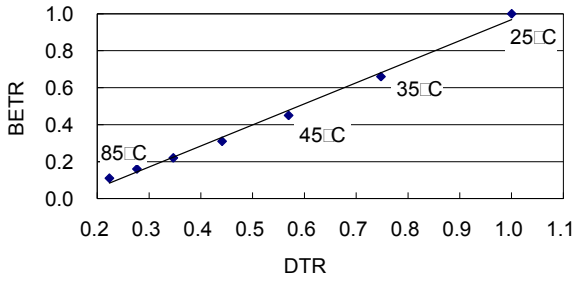

Figure 3. Relationship between BETR and DTR in analytical model

B. nMOS Leakage Monitor

The leakage monitor depicted in Fig. 1 senses only pMOS leakage. To detect BET of a function unit accurately, a monitor circuit to sense nMOS leakage is required as well. This is because sub-threshold leakage current in a function unit flows through not only pMOS transistors but also nMOS transistors. The circuit depicted in Fig. 4 is an MTCMOS leakage monitor that we propose for nMOS leakage monitoring. In this circuit, the speed of voltage-lowering at the virtual VDD (VVDD) is monitored. The VVDD voltage reduces faster as nMOS leakage increases. Analytical model for the nMOS leakage monitor is identical to the model for the pMOS leakage monitor.

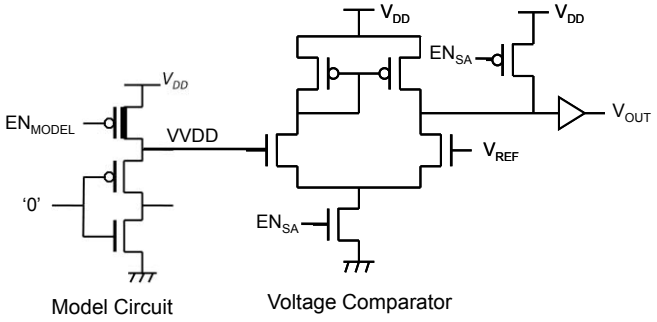

Figure 4. nMOS leakage monitor circuit

C. Weighted Response of pMOS and nMOS Leakage Monitors

The next challenge is how to extract information from the responses of pMOS and nMOS monitors such that it can reflect the entire leakage of function units. Since the shares of pMOS leakage and nMOS leakage depend on function units, we propose to use the share as a weight factor. The shares of pMOS and nMOS leakage can be estimated by simulations for two process corners (FS and TT), where FS stands for fast nMOS slow pMOS; TT stands for typical nMOS typical pMOS. Further we define the fast and slow corners as the corners where V_T is 10% lower and higher than the typical, respectively. Since the sub-threshold leakage current changes in proportional to $1/\exp(V_T/mU_t)$, the leakage increases to 3.1x when □V_T□becomes 10% smaller and reduces to 1/3.1 when □V_T□_ gets 10% larger at the room temperature at V_T=0.4V. For the TT corner, the total sub-threshold leakage $I_{L,TT}$ can be expressed as $I_{L,TT} = r_p$□$I_{L,TT} + r_p$□$I_{L,TT}$, where r_p and r_n are the shares of nMOS and pMOS leakage in the total leakage, respectively. Then, leakage current for the FS corner can be expressed as

$$I_{L,FS} = 3.1 \cdot r_n I_{L,TT} + (1/3.1) \cdot r_p I_{L,TT} \quad (9)$$

$$r_n + r_p = 1. \quad (10)$$

Solving these simultaneous equations gives us the following expressions for r_p and r_n:

$$r_p = 1.12 - 0.36 \cdot I_{L,FS}/I_{L,TT} \quad (11)$$

$$r_n = 0.36 \cdot I_{L,FS}/I_{L,TT} - 0.12. \quad (12)$$

Analyzing $I_{L,FS}$ and $I_{L,TT}$ by simulation allows us to obtain r_p and r_n.

Further we propose to use the weighted responses of pMOS and nMOS leakage monitors as a parameter to reflect the entire leakage of a function unit. When the power-switch in the leakage monitor is ON, leakage current flowing through turned-off pMOS (or turned-off nMOS) at the room temperature can be expressed as

$$I_{L,RT} = I_0 \exp\left(\frac{\eta V_{DD} q}{mkT_{RT}}\right) \exp\left(-\frac{V_T q}{mkT_{RT}}\right). \quad (13)$$

From the expressions (5) and (13), the detection time of a leakage monitor at the room temperature can be expressed as

$$t_{d,RT} = K_d / I_{L,RT} \quad (14)$$

where $K_d = \frac{m}{\eta} \cdot \frac{kT_{RT}}{q} \cdot \frac{C_{VGND}}{I_0} \left\{\exp\left(\frac{\eta V_{REF}}{m} \cdot \frac{q}{kT_{RT}}\right) - 1\right\}$. Notice that K_d independent of V_T. This means that when V_T changes, $t_{d,RT}$ changes in inversely proportion to $I_{L,RT}$. The response of a leakage monitor at the room temperature can be expressed as

$$M_{RT} = t_{d,RT} / T_{cyc,M} \quad (15)$$

where $T_{cyc,M}$ is the cycle time of a counter provided in the leakage monitor to measure $t_{d,RT}$ in a digital number. In order to investigate the impact of V_T variation on the response of a leakage monitor, we look at the ratio of the response at a given process condition against the response at the typical condition. We define this ratio as the normalized response. For pMOS, the normalized response can be expressed as

$$M_{RT,p\ norm} = M_{RT,p} / M_{RT,p,typ} = t_{d,RT,p} / t_{d,RT,p,typ} = \left(I_{L,p} / I_{L,p,typ}\right)^{-1} \quad (16)$$

where $M_{RT,p}$, $t_{d,RT,p}$ and $I_{L,p}$ are the monitor response, the detection time and leakage current for pMOS at the given process condition; $M_{RT,p,typ}$, $t_{d,RT,p,typ}$ and $I_{L,p,typ}$ are those at the typical condition. From (16), we obtain

$$I_{L,p} = I_{L,p,typ} / M_{RT,p\_norm}. \quad (17)$$

Likewise, for nMOS, the normalized response is defined as

$$M_{RT,n\_norm} = M_{RT,n} / M_{RT,n,typ} \quad (18)$$

and we obtain

$$I_{L,n} = I_{L,n,typ} / M_{RT,n\_norm} \quad (19)$$

where $I_{L,n}$ and $I_{L,n,typ}$ are the leakage currents at the given process condition and the typical condition, respectively. Meanwhile, as reported in [4], BET at the room temperature can be expressed as

$$BET_{RT} = K_b / I_{L,RT} \quad (20)$$

where $K_b = K_1 T_{RT}^{-3/2} \exp\left(\frac{\eta V_{DD} q}{mkT_{RT}}\right)$. K_1 is a factor which is independent of V_T. Notice that BET_{RT} changes in inversely proportion to $I_{L,RT}$ when V_T changes. To look at the impact of V_T variation on BET, we focus on the ratio of BET at a given process condition against the response at the typical condition at the room temperature. The ratio is defined as the normalized BET and can be expressed as

$$BET_{norm} = BET_{RT} / BET_{RT,TT} = I_{L,TT} / I_L = I_{L,TT} / \left(I_{L,p} + I_{L,n}\right). \quad (21)$$

By substituting (17) and (19) into (21), and using the definition for r_p and r_n, we finally obtain

$$BET_{norm} = \frac{1}{\frac{r_p}{M_{RT,p\_norm}} + \frac{r_n}{M_{RT,n\_norm}}} \quad (22)$$

Thus, BET_{norm} can be computed from the weighed response $r_p / M_{RT,p\_norm}$ and $r_n / M_{RT,n\_norm}$.

IV. Proposed Methodology for BET Detection

Based on the observation described in the previous section, we propose a methodology to detect BET using pMOS and nMOS leakage monitors. The procedure is depicted in Fig. 5. At Step1, we get the pMOS leakage monitor to operate at the room temperature and obtain the response, $M_{RT,p}$. At Step2, we get M_{RT,p_norm} by dividing $M_{RT,p}$ by $M_{RT,p,typ}$. At Step3 we obtain the nMOS monitor's response $M_{RT,n}$, and at Step4 we compute M_{RT,n_norm} from $M_{RT,n}$, and $M_{RT,n,typ}$. At Step5, from the data for M_{RT,p_norm} and M_{RT,n_norm}, we compute BET_{norm} by using the equation (22). Values of r_p and r_n should be calculated in advance using the equations (11) and (12). Leakage currents $I_{L,SF}$, $I_{L,TT}$ and $I_{L,FS}$ for a function unit are obtained by simulation or measurement. At Step6, we obtain BET_{RT} by multiplying BET_{norm} by BET_{TT}. This is made possible because of the definition of BET_{norm} shown in the equation (21). The values of $M_{RT,p,typ}$, M_{RT,p_norm}, $M_{RT,n,typ}$ and BET_{TT} need to be pre-characterized using simulation or measurement. Notice that all steps so far are performed only once when the chip is fabricated. This is because the main purpose of them is to detect process variation of the chip. When they are done within the chip test, BET_{RT} obtained is registered in on-die non-volatile memory or a fused ROM. The subsequent steps aim to detect temperature fluctuation at the operating environment. At Step7, we make the pMOS monitor operate and get the response $M_{op,p}$ at the operating temperature. You could use an nMOS monitor instead because the objective is to sense the temperature fluctuation. At Step8, by dividing $M_{op,p}$ by $M_{RT,p}$, we obtain DTR. At Step9, using a translation table (LUT) translating from DTR to BETR, we obtain BETR. Instead of LUT, you could use an empirical equation that expresses the relation between DTR and BETR. At Step10, we finally obtain BET at the operating temperature BET_{op} by multiplying BET_{TT} and BETR.

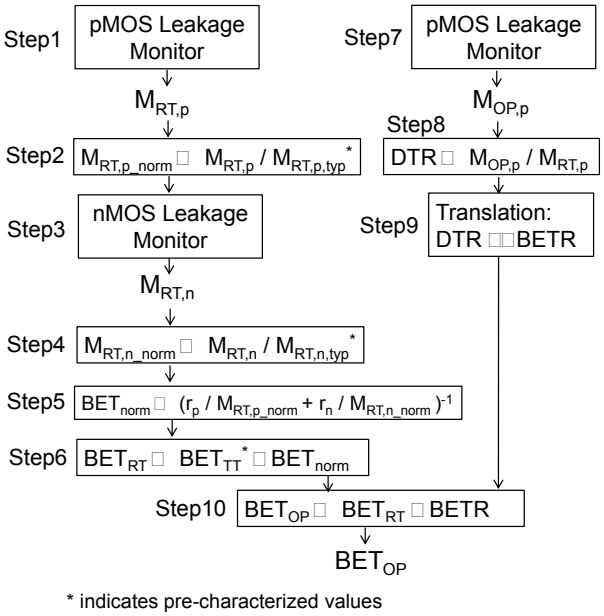

Figure 5. Proposed BET detection methodology

There are two advantages in this methodology. First, you do not need to precisely know the chip temperature itself at the BET detection. Since BET is detected directly from leakage information reflecting temperature/process fluctuations, complicated calibration of temperature-sensing devices is not

required. The second advantage is that the translation from the leakage-monitor response to BET is based on the relation between DTR and BETR. As described, this relation shows clear linearity and hence the required memory size to store the translation table from DTR to BETR can be reduced without sacrificing the accuracy. The linearity between DTR and BETR was observed also at the simulation result for an actual function unit. This will be presented in Section VI.

V. Evaluation Setup

To test our detection methodology, we designed a pMOS/nMOS leakage monitor circuits depicted in Fig. 1 and Fig. 4, respectively. Further, we implemented them with a 32-bit RISC CPU core on the same die using Fujitsu 65nm CMOS technology. In the CPU core, function units such as a multiplier, divider, ALU and shifter are power gated. The layout of the test chip is shown in Fig. 6. Leakage monitors including pairs of pMOS/nMOS leakage-monitor circuits are placed at the corners of the chip. We extracted parasitic resistance and capacitance from the layout data using commercial CAD tools and used at the circuit-level simulations. In this study, we chose the power-gated multiplier as a test bench to evaluate effectiveness of the proposed methodology. This choice is strongly motivated by the fact that BET-aware power gating for the multiplier gives the highest efficiency among the function units [4].

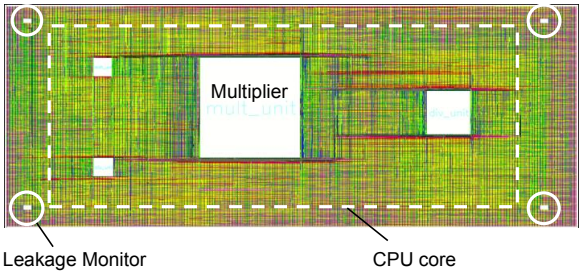

Figure 6. Layout of the test chip

VI. Results

A. Correlation between leakage-monitor response and leakage current of multiplier

First we investigated if the response of the leakage monitor reflects the fluctuation of leakage current of the multiplier. We conducted simulations for the leakage monitor assuming that the detection time of the leakage monitor is sensed by a counter operating at 50MHz. Fig. 7 shows the simulation results on the relationship between leakage current of the multiplier and the inverse of the response of the pMOS/nMOS leakage monitors. As the temperature goes up, leakage current of the multiplier increases. Simultaneously, the response of the leakage monitors reduces and hence the inverse of the response increases. The results shown in Fig. 7 demonstrated that the response of the pMOS/nMOS leakage monitors reflects the fluctuation of leakage current of the multiplier when the temperature changes.

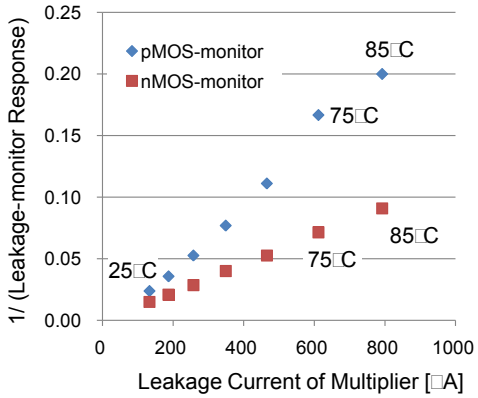

Figure 7. Relationship between leakage current of multiplier and the response of leakage monitors (simulated)

B. Evaluaion of proposed methodology

We investigated BET obtained by our detection methodology by applying the procedure shown in Fig. 5. The detected BET is compared with the BET value which is obtained by the conventional simulation-based technique [3]. In the technique described in [3], energy dissipation is analyzed by simulation at each temperature for the cases that the power gating is enabled and disabled while changing the powered-off cycles. BET is the powered-off cycles where energy dissipations become equal in the power-gating enabled and disabled cases. Now we describe BET obtained by our detection methodology. In proposed procedure depicted in Fig. 5, we pre-characterized the values for $M_{RT,ptyp}$, $M_{RT,n,typ}$ and BET_{TT} by simulations for the pMOS/nMOS monitors and the multiplier. As the result, we obtained $M_{RT,ptyp}$=42, $M_{RT,n,typ}$=67 and BET_{TT}=620ns. Values for r_p and r_n used at Step5 were pre-computed using the equations (11) and (12), along with the leakage-current analysis for the multiplier. This results in the r_p and r_n values of 0.7 and 0.3, respectively. In terms of the translation mechanism at Step9, we investigated the relationship between BETR and DTR through simulations. It turned out that BET actually changes with DTR linearly as depicted in Fig. 3. This fact allowed us to use the following equation

$$\mathrm{BETR} = 0.8921 \times \mathrm{DTR} + 0.1204$$

instead of LUT as the translation mechanism from DTR to BETR. The R^2 value at above linear approximation is 0.996.

The BET values obtained by this procedure are compared with those obtained by the conventional simulation-based technique. Results are shown in Fig. 8(a)-(e). As shown in Fig. 8(a), the proposed methodology enables us to detect BET with good accuracy at all temperatures at the TT corner. The difference between the BET values of the proposed methodology and those of the simulation-based technique was 5% on average. At the FS and SS corners as well, the proposed methodology detects BET with good accuracy. In contrast, it turned out that the accuracy reduces at the FF and SF corners to 17% and to 15% on average, respectively. The potential reason is that the accuracy of the pMOS leakage monitor gets worse when pMOS gets leaky. This is because the rising-speed of the VGND voltage in the pMOS monitor increases and

hence the detection time gets too short to be detected accurately. Improvement of this is the future work.

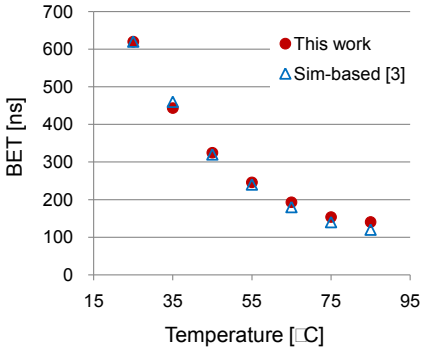

Figure 8(a). Comparison between BET detected by the proposed methodology (This work) and BET obtained by simulations based on [3] at TT corner.

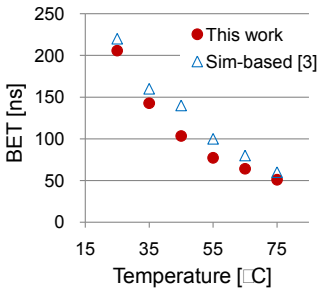

Fig.8(b) Comparison at FF corner

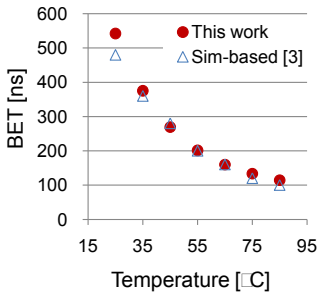

Fig.8(c) Comparison at FS corner

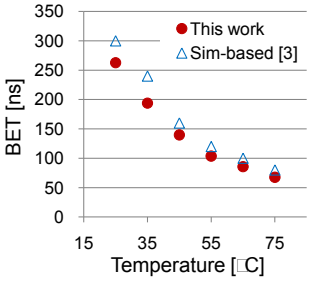

Fig.8(d) Comparison at SF corner

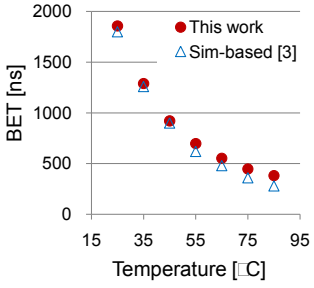

Fig.8(e) Comparison at SS corner

C. *Area and power dissipation*

The area of the leakage monitor including pMOS/nMOS monitors, counters and control circuits is 1400□m^2. This area is 0.4% of that of the multiplier. Simulation results showed that the leakage monitor dissipates 22.5□W at the operation at 50MHz.

D. *Effect of random variation*

We investigated the impact of random variation on the performance of the leakage monitor. The major factor of the random variation is the V_T variation due to random dopant fluctuations in the 65nm technology [11]. We conducted 3000 times of Monte-Carlo SPICE simulations with □10% V_T variations at the room temperature. The result showed that the delays of the model circuit and the voltage comparator are affected by the variation. It also showed that 3□/□ for the pMOS and nMOS monitors can be suppressed to 0.06 and 0.07, respectively, by sizing up the transistors of the model circuit to 12x and the nMOS transistor of the voltage comparator to 6x. This increases the area and power. In terms of the area, since the total area of the model circuit and the voltage comparator occupies 10% in the entire leakage monitor, the sizing-up leads to area increase of the leakage monitor to 2x. In contrast, the penalty for the power dissipation is negligible. This is because the leakage monitor is made to operate once per 10,000 cycles at the same time-granularity as the temperature change.

VII. CONCLUSIONS

We proposed on-chip detection methodology for BET of power-gated function units by using a leakage monitor that senses both temperature fluctuation and process variation. We built analytical models and demonstrated that they support the validity of our methodology. To evaluate the effectiveness, we applied this methodology to the power-gated multiplier. Results showed that our methodology detects BET at 5%-17% difference from that of the conventional simulation-based off-line technique.

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