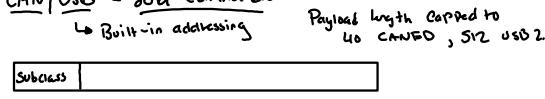
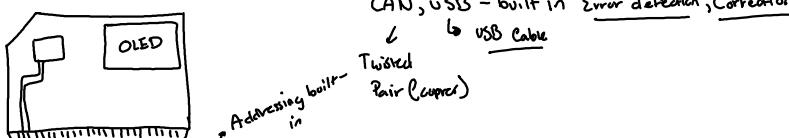
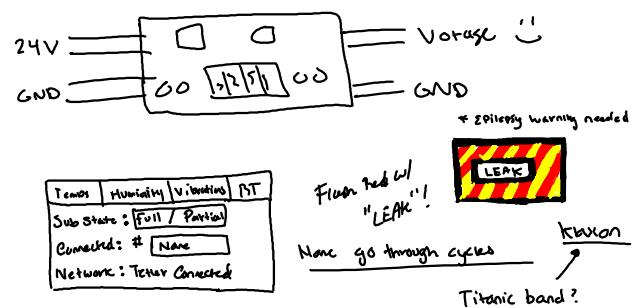
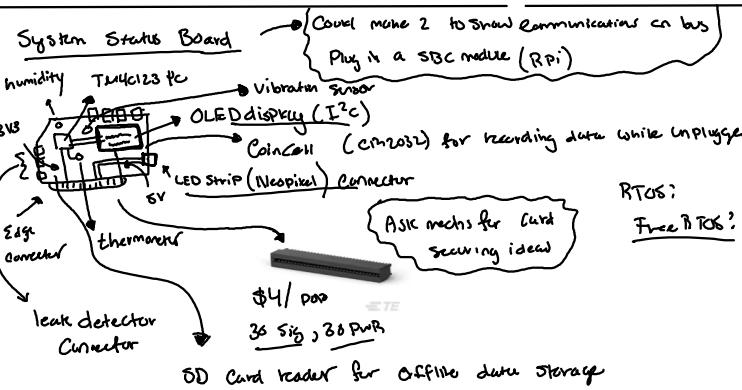
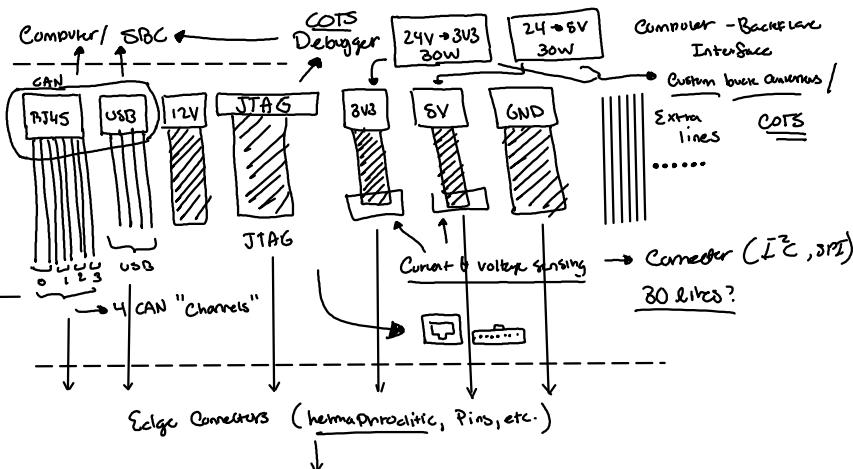
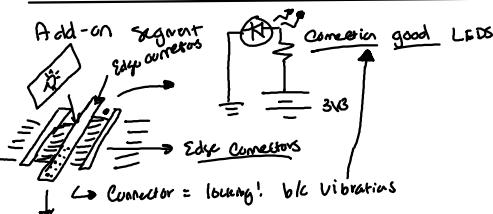


Main Back Plane Segment connections

- CAN Connector (External where Ethernet is not valid / too big)
- JTAG Connector (debugging / flashing)
- USB Connector (internal simpler connection standard)
- Power Connector (3V3, 5V)
- Notes:
 - Extra lines for future use
 - Higher power (12V, etc) through connector on Plugged-in board
 - ↪ PCI-E cable as example
- Thrust Control Servo Control



0x00 = humidity sensor update

↪ 1 byte for frequency

0x01 = humidity sensor output

↪

 (hex)

3: Display on OLED

2: Store in SD Card

1: Send through USB

0: Send through CAN

0x10 = Thermometer update

↪ 1 byte for frequency (0x00 = off)

0x11 = Thermometer output

↪

 (hex)

3: Display on OLED

2: Store in SD Card

1: Send through USB

0: Send through CAN

0x12 = Thermometer Units

↪ 0x00 = °F, 0x01 = °C, 0x02 = K

⋮

0x20 = OLED update

↪ 1 byte for frequency (0x00 = off)

0x21 = OLED Power

↪ 0x00 = Stay off until on battery power
0x01 = Stay on until on battery power

⋮

0x30 = Accelerometer update

↪ 1 byte for frequency (0x00 = off)

0x31 = Accelerometer Output

↪

 (hex)

3: Display on OLED

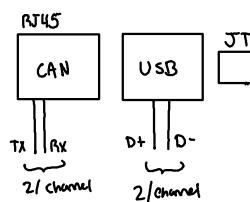
2: Store in SD Card

1: Send through USB

0: Send through CAN

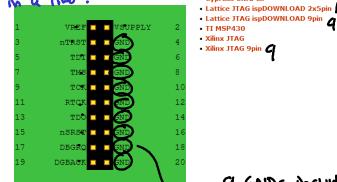
Command	Argument
[0]	[1 - 39]

Addressing & error correction handled by USB & CAN Protocols



Would need some way to jumper signals if one is removed/breaks

Or should we assume that the user will replace/reroute so that they are all decoupling in GND?



$$11 + 2x + 2y = \text{Required Connections}$$

left over = 10 lines

$$11 + 2x + 2y + 10 = 21 + 2(x+y)$$

$$x \geq 1, y \geq 1$$

$$21 + 2(2) = 25 \rightarrow$$

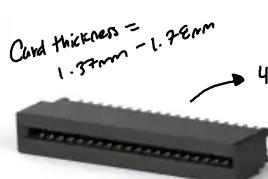
$$21 + 2(3) = 27$$

$$21 + 2(4) = 29 \quad \text{Card thickness} = 1.37\text{mm} - 1.78\text{mm}$$

2 connectors per board
↳ Data ↳ Power

Board guide?

46
1A/Contact which should be fine for most applications
\$3.170/
Digikey
5650719-1



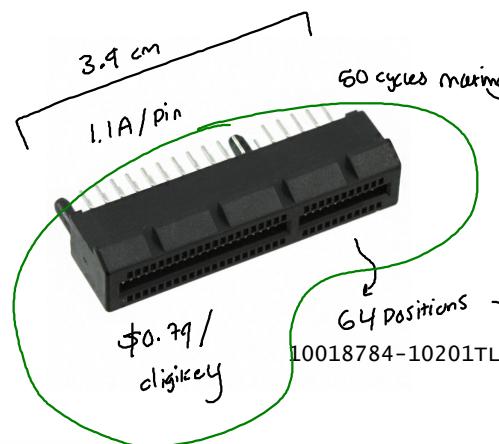
40 positions, 3A/Contact
Not meant for high-speed signals (= poor SI?)
(we could try though...)

5-5530843-4

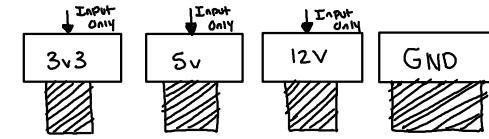
\$3.7/
Digikey

Board Thickness	0.4 - 2.5 mm	Thickness for FR4 are: 0.4/0.6/0.8/1.0/1.2/2.0 mm (2.5 mm only available with 12 layers or more.)
-----------------	--------------	---

25 data → d G d G
(so total 50 total
(25 GNDs for SI)) + PWR Connectors & GND Section



Card thickness for PCI-e = 1.57 mm



(Connect external Converters) or use Power Supply Cards

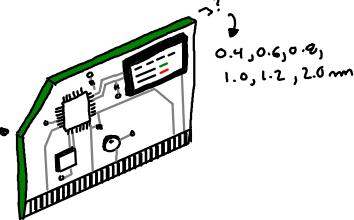
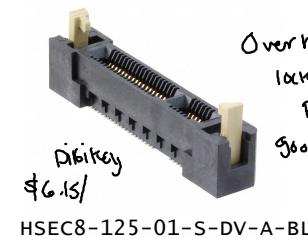
3v3 @ 25W ≈ 6 A
5V @ 25W = 5 A
12 V @ 25W = 2 A

Edge Connectors:

Ampmole MPCI-E
↳ 9A / "beam" = /Connector

depends
25 pins 12.2 = 13 ← 3.3 V @ 20W ≈ 6.1 A
PWR ② ④ ← 5V @ 20W = 4A
← 12V @ 20W ≈ 1.6 A

Over kill,
locking tabs +
polarization
good for 10Ghz
signal



subgeniuskitty • 2 yr. ago

Seconding PCI express connectors. Due to sheer scale of production you're unlikely to find a similarly performing connector at similar prices.

For your backplane, since you'll be plugging and unplugging cards frequently during debugging/bringup, spring for thick hard gold plated connectors. They'll only be a small price increase but the number of insertion cycles skyrockets.

ENIG surface finish, despite being gold, is extremely soft and thin; it will rub through after only a few insertion cycles. Hard gold plating of card edge connectors is available, but expensive for a hobby project that includes several different types of boards in small quantities. I've had good luck with DIY hard gold finger plating at home after 'unplating' suitable ions from existing hard gold fingers, but it was a PITA and is only worth it for the final version of your project, and then only if you want it to run reliably for many years.

Beveling the card edges where they insert into the slot is easily done yourself with a homemade jig. No sense paying the PCB fab for that service and its setup fees.

Consider using the larger x8 or x16 connectors for a couple reasons. (1) This allows you to keep the layer count (and price) down on your backplane PCB by only using every other pin. It's pretty hard to route the inner pins of such a dense connector on something like a 2- or 4-layer PCB and higher layer count PCBs are pretty expensive. (2) By using every other pin, you can tie all the unused pins directly to your ground plane, providing a tightly coupled return path directly alongside every data line. For the long traces of a backplane, this can be significant.

64 - 50 = 14 for power

4 @ 12V 8 @ 5V 5 @ 3.3V
"4.4A "5.5A "5.5A
MAX" MAX" MAX"

<https://jlcpcb.com/quote/pcbborderFAQ/Gold%20Fingers>

Must be ENIG for gold fingers or else it will tin

Jetson Nano:

SODIMM SLOT = 260 Positions

3.4 Jetson Orin Nano Pin List

Jetson SODIMM Signal Name	Jetson Orin Nano Function	Pin # Top Odd	Pin # Bottom Even	Jetson SODIMM Signal Name	Jetson Orin Nano Function
GND	GND	1	2	GND	GND
CSD1_D0_N	CSH1_D0_N	3	4	CSD1_D0_N	CSD1_D0_N
CSD1_D0_P	CSH1_D0_P	5	6	CSD1_D0_P	CSD1_D0_P
GND	GND	7	8	GND	GND
CSD1_CLK_N	CSH1_CLK_N	9	10	CSD1_CLK_N	CSD1_CLK_N
CSD1_CLK_P	CSH1_CLK_P	11	12	CSD1_CLK_P	CSD1_CLK_P
GND	GND	13	14	GND	GND
CSD1_D1_N	CSH1_D1_N	15	16	CSD1_D1_N	CSD1_D1_N
CSD1_D1_P	CSH1_D1_P	17	18	CSD1_D1_P	CSD1_D1_P
GND	GND	19	20	GND	GND
CSD1_D2_N	CSH1_D2_N	21	22	CSD1_D2_N	CSD1_D2_N
CSD1_D2_P	CSH1_D2_P	23	24	CSD1_D2_P	CSD1_D2_P
GND	GND	25	26	GND	GND
CSD1_CLK_N	CSH1_CLK_N	27	28	CSD1_CLK_N	CSD1_CLK_N
CSD1_CLK_P	CSH1_CLK_P	29	30	CSD1_CLK_P	CSD1_CLK_P
GND	GND	31	32	GND	GND
CSD1_D3_N	CSH1_D3_N	33	34	CSD1_D3_N	CSD1_D3_N
CSD1_D3_P	CSH1_D3_P	35	36	CSD1_D3_P	CSD1_D3_P
GND	GND	37	38	GND	GND
DP0_RXD_N	USBS81_RX_N	39	40	PCIE2_RX0_N	PCIE2_RX0_N
DP0_RXD_P	USBS81_RX_P	41	42	PCIE2_RX0_P	PCIE2_RX0_P
GND	GND	43	44	GND	GND
DP0_RXD_N	USBS81_TX_N	45	46	PCIE2_RX0_N	PCIE2_RX0_N
DP0_RXD_P	USBS81_TX_P	47	48	PCIE2_RX0_P	PCIE2_RX0_P
GND	GND	49	50	GND	GND
DP0_RXD_N	USBS82_RX_N	51	52	PCIE2_RX1_N	PCIE2_RX1_N
DP0_RXD_P	USBS82_RX_P	53	54	PCIE2_RX1_P	PCIE2_RX1_P
GND	GND	55	56	GND	GND
DP0_RXD_N	USBS82_TX_N	57	58	PCIE2_D1_N	PCIE2_D1_N
DP0_RXD_P	USBS82_TX_P	59	60	PCIE2_D1_P	PCIE2_D1_P
GND	GND	61	62	GND	GND
DP1_RXD_N	DP1_RXD_N	63	64	PCIE2_D3_N	PCIE2_D3_N
DP1_RXD_P	DP1_RXD_P	65	66	PCIE2_D3_P	PCIE2_D3_P
GND	GND	67	68	GND	GND
DP1_RXD_N	DP1_RXD_N	69	70	DSI_D0_N	RSVD
DP1_RXD_P	DP1_RXD_P	71	72	DSI_D0_P	RSVD
GND	GND	73	74	GND	GND
DP1_RXD_N	DP1_RXD_N	75	76	DSI_CLK_N	RSVD
DP1_RXD_P	DP1_RXD_P	77	78	DSI_CLK_P	RSVD
GND	GND	79	80	GND	GND
DP1_RXD_N	DP1_RXD_N	81	82	DSI_D1_N	RSVD
DP1_RXD_P	DP1_RXD_P	83	84	DSI_D1_P	RSVD
GND	GND	85	86	GND	GND
GPIO00	GPIO00	87	88	DP0_HIRD	RSVD
SP1_MISO	SP1_MISO	89	90	DP0_HIRD_N	RSVD
SP1_SCK	SP1_SCK	91	92	DP0_AUX_P	RSVD
SP1_MISO	SP1_MISO	93	94	AMCI_CEC	
SP10_CSD0	SP10_CSD0	95	96	DP1_HIRD	DP1_HIRD
SP10_CS1*	SP10_CS1*	97	98	DP1_AUX_N	DP1_AUX_N
UART0_RXD	UART0_RXD	99	100	DP1_AUX_P	DP1_AUX_P
UART0_RXD	UART0_RXD	101	102	GND	GND
UART0CTS	UART0CTS	103	104	SP1_MISO	SP1_MISO
UART0CTS	UART0CTS	105	106	SP1_SCK	SP1_SCK
GND	GND	107	108	SP1_MISO	SP1_MISO
USB0_D_N	USB0_D_N	109	110	SP1_CSD0	SP1_CSD0
USB0_D_P	USB0_D_P	111	112	SP1_CSD1_P	SP1_CSD1_P
GND	GND	113	114	CAM0_PWDN	CAM0_PWDN
Jetson SODIMM Signal Name	Jetson Orin Nano Function	Pin # Top Odd	Pin # Bottom Even	Jetson SODIMM Signal Name	Jetson Orin Nano Function
USBS81_RX_N	USBS81_RX_N	115	116	CAM0_MCLK	PCIE0_RX0_N
USBS81_RX_P	USBS81_RX_P	117	118	PCIE0_RX0_P	PCIE0_RX0_P
GND	GND	119	120	CAM0_RXDN	GND
USBS82_RX_N	USBS82_RX_N	121	122	CAM1_MCLK	PCIE0_RX1_N
USBS82_RX_P	USBS82_RX_P	123	124	PCIE0_RX1_P	PCIE0_RX1_P
GND	GND	125	126	PCIE0_RX2_N	PCIE0_RX2_P
GPIO04	GPIO04	127	128	PCIE0_RX3_N	PCIE0_RX3_P
GND	GND	129	130	PCIE0_RX4_N	PCIE0_RX4_P
PCIE0_RX5_N	PCIE0_RX5_N	131	132	PCIE0_RX5_N	PCIE0_RX5_P
PCIE0_RX5_P	PCIE0_RX5_P	133	134	PCIE0_RX5_P	PCIE0_RX5_P
GND	GND	135	136	PCIE0_RX6_N	GND
PCIE0_RX1_N	PCIE0_RX1_N	137	138	PCIE0_RX6_P	PCIE0_RX6_P
PCIE0_RX1_P	PCIE0_RX1_P	139	140	PCIE0_RX7_N	PCIE0_RX7_P
GND	GND	141	142	PCIE0_RX7_P	PCIE0_RX7_P
CAN_RX	CAN_RX	143	144	GND	GND
CAN_RX	CAN_RX	145	146	GND	GND
CAN_RX	CAN_RX	147	148	PCIE0_T2_N	PCIE0_T2_N
PCIE0_RX2_N	PCIE0_RX2_N	149	150	PCIE0_T2_P	PCIE0_T2_P
PCIE0_RX2_P	PCIE0_RX2_P	151	152	GND	GND
GND	GND	153	154	PCIE0_T3_N	PCIE0_T3_N
PCIE0_RX3_N	PCIE0_RX3_N	155	156	PCIE0_T3_P	PCIE0_T3_P
PCIE0_RX3_P	PCIE0_RX3_P	157	158	GND	GND
GND	GND	159	160	PCIE0_CLK_N	PCIE0_CLK_N
USBS85_RX_N	USBS85_RX_N	161	162	PCIE0_CLK_P	PCIE0_CLK_P
USBS85_RX_P	USBS85_RX_P	163	164	GND	GND
GND	GND	165	166	USBS85_RX_N	USBS85_RX_N
PCIE1_RXD_N	PCIE1_RXD_N	167	168	USBS85_RX_P	USBS85_RX_P
PCIE1_RXD_P	PCIE1_RXD_P	169	170	GND	GND
PCIE1_CLK_N	PCIE1_CLK_N	171	172	PCIE1_RX5_N	PCIE1_RX5_P
PCIE1_CLK_P	PCIE1_CLK_P	173	174	PCIE1_RX5_P	PCIE1_RX5_P
GND	GND	175	176	GND	GND
PCIE1_WAKE*	PCIE1_WAKE*	177	178	M0D_SLEEP	M0D_SLEEP
PCIE0_RST*	PCIE0_RST*	179	180	PCIE1_CKREQ*	PCIE1_CKREQ*
PCIE1_RST*	PCIE1_RST*	181	182	PCIE1_CKREQ*	PCIE1_CKREQ*
IC20_SDA	IC20_SDA	183	184	G8E_M0D0_N	G8E_M0D0_N
IC21_SCL	IC21_SCL	185	186	G8E_M0D1_P	G8E_M0D1_P
IC20_SDA	IC20_SDA	187	188	G8E_LED_LINK	G8E_LED_LINK
IC21_SCL	IC21_SCL	189	190	G8E_M0D1_N	G8E_M0D1_N
IC20_SDA	IC20_SDA	191	192	G8E_M0D2_P	G8E_M0D2_P
IC20_DIN	IC20_DIN	193	194	G8E_LED_ACT	G8E_LED_ACT
IC20_DIN	IC20_DIN	195	196	G8E_M0D2_N	G8E_M0D2_N
IC20_FS	IC20_FS	197	198	G8E_M0D2_P	G8E_M0D2_P
IC20_CLK	IC20_CLK	199	200	GND	GND
GND	GND	201	202	G8E_M0D3_N	G8E_M0D3_N
UART1_RXD	UART1_RXD	203	204	G8E_M0D3_P	G8E_M0D3_P
UART1_RXD	UART1_RXD	205	206	GPI007	GPI007
UART1_RTS	UART1_RTS	207	208	GPI008	GPI008
UART1_CTS	UART1_CTS	209	210	CLK_32K_OUT	CLK_32K_OUT
GND	GND	211	212	GPI010	GPI010
CAM1_IC2_SCL	CAM1_IC2_SCL	213	214	FORCE_RECOVERY*	FORCE_RECOVERY*
CAM1_IC2_SDA	CAM1_IC2_SDA	215	216	GPI011	GPI011
GND	MODULE_ID	217	218	GPI012	GPI012
SDMMC_DAT0	SDMMC_DAT0	219	220	I2S1_DOUT	I2S1_DOUT
SDMMC_DAT1	SDMMC_DAT1	221	222	I2S1_DIN	I2S1_DIN
PCIE1_NST*	PCIE1_NST*	223	224	I2S1_F8	I2S1_F8
SDMMC_CMD	SDMMC_CMD	225	226	I2S1_SCK	I2S1_SCK
POC1_CLK_N	POC1_CLK_N	227	228	GPI013	GPI013
POC1_CLK_P	POC1_CLK_P	229	230	GPI014	GPI014
GND	GND	231	232	I2C2_SDA	I2C2_SDA
SHUTDOWN_REQ*	SHUTDOWN_REQ*	233	234	I2C2_SDA	I2C2_SDA
PMIC_BBAT	PMIC_BBAT	235	236	I2C2_SDA	I2C2_SDA
POWER_EN	POWER_EN	237	238	I2C2_RXD	I2C2_RXD
SYS_RESET*	SYS_RESET*	239	240	SLEEPWAKE*	SLEEPWAKE*

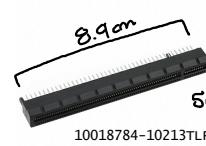
Most likely, will pursue making a Jetson-specific carrier board w/ adapters for our pinout

Add extra lines for possible functionality?

- ↳ 64 Position = \$0.79 /
- ↳ 96 Position = \$0.97 /
- ↳ 164 Position = \$1.04 /
- ↳ 230 Position = \$10.29 /
- ↳ 280 Position = \$10.94 /
- ↳ 341 Position = \$16.01 /

PCI-e
PHY
Support

"On Card"
Have local & bus Extra lines



50 cycles mating,
better finish =
longer lifetime

Differential Pairs = GND b/w Each Pair to net thing
distribute Power

Design revision

More expensive, less coverage = potentially less secure due to more allocated to power.

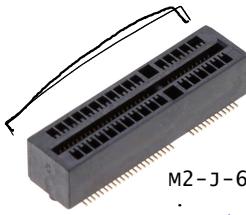
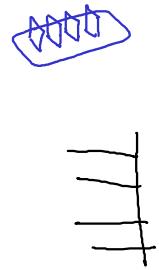
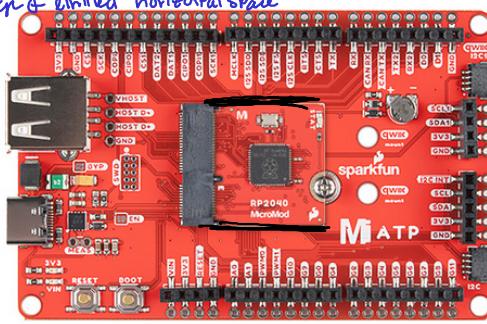
MIL Boards:

24 V
5 V
GND
E-stop
thruster

I think you can go way deeper here, as there are numerous examples of modular electronics on the market. Some other prior art to consider includes the Feather Spec (which you know I adore), the MicroMod system, Arduino "shields", RPi "HATs" etc. Also, the PCI(e) on modern consumer computers. Also thinking about the option of certain mezzanine-style modular boards (like RPi computer modules, Arduino Portenta, etc) will be worthwhile to consider.

I think doing a deeper analysis of the tradeoffs that each of these systems balances, and how that relates to the goals of your system, is worthwhile. Ultimately I want you guys to consider all options, rather than staying tied to the backplane idea since it was your first. The goal is to make a convincing argument that this is the best solution to your problem :)

Sideways connectors are not suitable for application's boards must be vertical to take advantage of limited horizontal space



a Main Board...

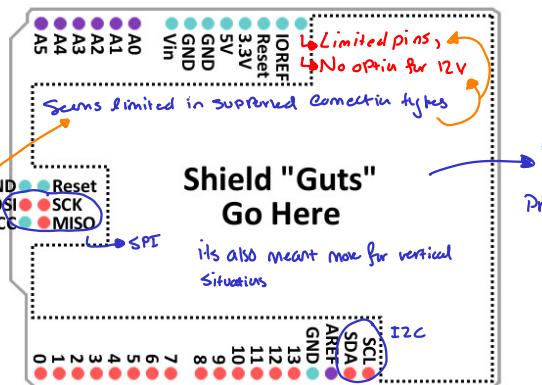
or Board of your choice to a footprint.

...Or use Carrier Boards

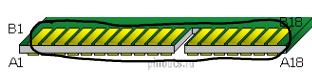
Choose from 8 different Carrier Boards to access specific inputs and outputs based on your specific needs and pair with a Processor Board of your choice.

[SEE AVAILABLE CARRIER BOARDS](#)

- ↳ 67 positions, comparable to Smallest PCI-E I found
- \$1.44 / Digikey > \$0.79 / Digikey
- 0.5A / pin < 1.1A / pin
- ↳ 25-60 cycles
- ↳ 0.8 mm board size = Standard JLC Capability (0.7mm - 0.9mm)
- ↳ Thinner boards needed



Some shields use every pin on the Arduino, while others only use a couple. When stacking shields, it's important to make sure they don't use overlapping pins. Some shields communicate with the Arduino via SPI, I²C, or Serial, and others use the Arduino's interrupts or analog inputs.



Not needed for Subs, but could be included in whatever we use

→ Pins for 12V, GND, SMBus, 3.3V, JTAG, reset, WAKE, PCI differential pair TX, RX, HotPlug (for hot swapping)



Adds extra PCI-e lanes

PCI-e X8, X16 do the same (add more PCI-e lanes)

We would take the main PCI-e Connectors, but change the transmission to USB and CAN (also differential pair)

→ Higher Signal Integrity (Potential) →

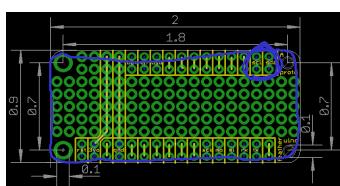
- ↳ 64 position = \$0.79 / \$0.18
- ↳ 96 Position = \$0.97 / \$0.07
- ↳ 164 Position = \$1.04 / \$0.07
- ↳ 230 Position = \$10.21 / \$0.07
- ↳ 280 Position = \$10.44 / \$0.07
- ↳ 314 Position = \$16.01 / \$0.07

→ Additional cost w/ additional needed segment connectors (which also have to be high SI)

→ Additional cost w/ ENIG boards (gold-plating)

HASL, HALT-free





- Like micromod, suffers from fixed dimensions when we have a "maximum size" (limitations of sub enclosure) but want to reduce as much as possible.

- We would also need to modify the Power standard and increase the # pins to allow JTAG, SWD, reset, etc.

↳ Breadboard / Dupont cable compatible

↳ Would have to be horizontal

~~Lower lifecycle than Mezzanine~~

Ribbon cables
↳ Mechanically safe, but no vertical clearance

Connectors
↳ wire-to-wire
↳ wire-to-board
+ Allows easier card/module re-use
+ Designed for high signal integrity
+ Card design does not have to have a fixed

↳ Mezzanine
↳ Board-to-Board

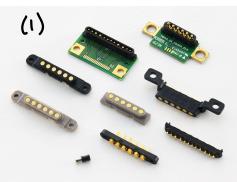
↳ Size + Cost issues
↳ Headers & receptacles better current/contact

+ Probably not designed w/ high-speed diff. signals in mind

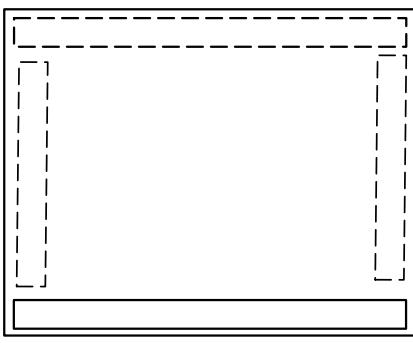
↳ Page-Pins (1)

↳ Probably own, more expensive, same issue

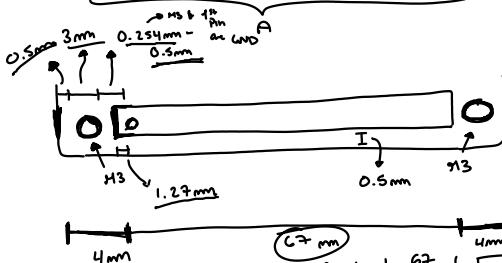
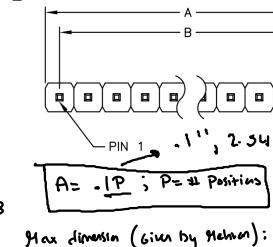
Original idea: ↑ PCB cost due to ENIG/Gold Plating, Reduced lifecycle, less connector options, Easier shippability, Needs 3 connectors / segment + 1 on PCB



Header pins as horizontal connectors



To maintain Breadboard compatibility:
↳ 0.1" (2.54 mm) spacing
↳ .025" (0.64 mm) square contact area



$$A = 2.54P \Rightarrow P = \left\lfloor \frac{A}{2.54} \right\rfloor = \left\lfloor \frac{6.7}{2.54} \right\rfloor = 26 \text{ Positions / Row}$$

for 50 positions, we would need 2 rows. To add SWD we would need three rows

We also need to give plenty of vertical space below boards just in case

What if you don't maintain Breadboard compatibility & move pitch smaller?

↳ Linearly added cost to connectors

$$A = 2P \Rightarrow P = \left\lfloor \frac{A}{2} \right\rfloor = \left\lfloor \frac{6.7mm}{2} \right\rfloor = 33 \text{ Positions / Row}$$

Still need 2 rows

To get a single row, you would need a pitch matching of...

$$A = MP \Rightarrow M \leq \frac{A}{P} \Rightarrow \frac{6.7mm}{50 \text{ pos}} \rightarrow M \leq 1.34 \text{ mm}$$

OK, what if you use M=1.27mm (0.5")

$$A = 1.27P \Rightarrow P = \left\lfloor \frac{A}{1.27} \right\rfloor = \left\lfloor \frac{6.7mm}{1.27} \right\rfloor = 52 \text{ Positions / Row}$$

Not an option, closest is 1 Row @ 50



2 Row header connector (52 pos) used to connect 1 board to 1 board
End = \$3.96 (custom Digikey order)
Vertical = \$3.85

\$6-7 / board

Additional delivery time

↳ 2.5A / contact



Only one option
- 1A / contact
- \$6.18 (Custom DigiKey Order)



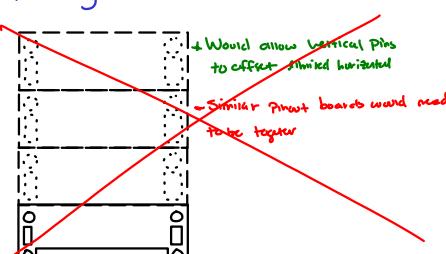
- \$7.01
- 1A / contact

850-10-050-10-001000

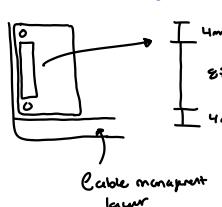
No options exist that meet our space requirements that are also as clear / cheaper than PCI-e, M.2, or Mezzanine.

What can you do to offset pins vertically and provide stability?

Potentially have a set of vertical slots where each slot takes over 9.5mm of space.



Instead of having common horizontal pins, have common vertical pins:



Cable management layer

@ .1", 2.54mm :

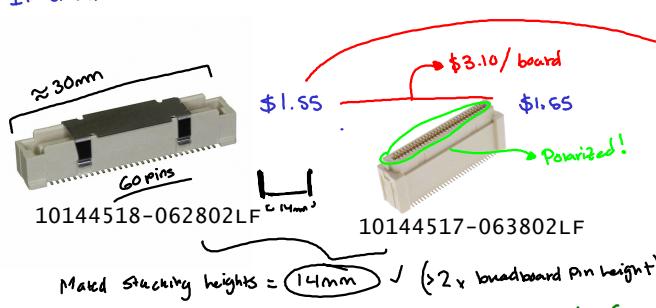
$$P = \left\lfloor \frac{8.2mm}{2.54mm} \right\rfloor = 34 \text{ positions / row}$$

$$\text{Need } M \leq \frac{A}{P} \Rightarrow M \leq \frac{8.2mm}{2.54mm} \rightarrow M \leq 1.74mm$$

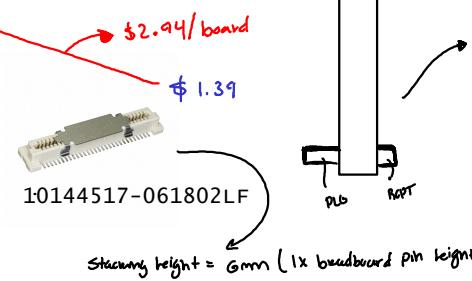
↳ Some issue, M=1.25mm

Mezzanine for horizontal use

It should still have the same profile as pin headers, but to a lesser extent

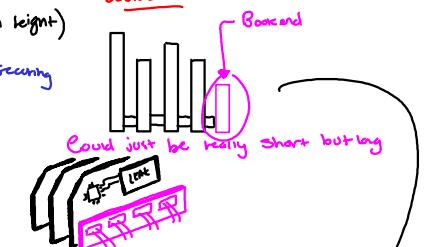


IEEE 1386



Plug or receptacle in bottom left allows for less of a board height + width requirement.

Difficult to "start" / have a bookend



- + Offers different board stacking options; boards can be of different heights as needed = Save even more space!
- + Potential Cost Savings; 2 connects / board + HASL board
- Has the problem of Needing to remove all boards just to remove 1
- + Potentially longer connector lifecycle (50 cycles) than PCI-e
- 0.6A / Contact

Stacking height = 6mm (1x breadboard pin height)

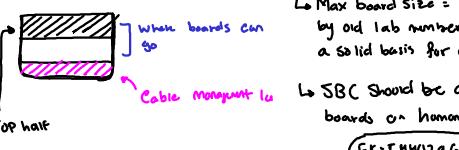
Need to talk to mechanical abt. mounting & securing options

How could you avoid dismantling all boards just to replace one?

↳ We could group boards by function or MTBF so that only a few boards have to be disassembled for the replacement (boards w/ blank separator boards)

↳ We could group them linearly w/o separator boards

Can you also go a bit more in depth about the enclosure size and interconnections between the backplane and the SBC? Is power going to be routed separately to the backplane and the SBC? You should think critically about the tradeoffs regarding cabling complexity and weight, and the challenge of integrating all of this. I think it might be worthwhile to consider the arrangement of all of this in the sub, cable management between the SBC and the backplane, etc. Have you put any thought into making the backplane actually be a carrier board for the SBC?

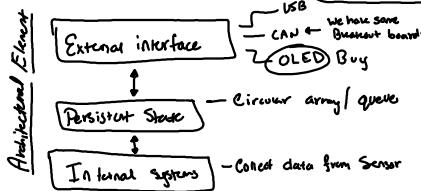


↳ Max board size = 75mm x 95mm determined by old lab number. This may change but provides a solid basis for our decisions

↳ SBC should be as isolated from electrical boards as humanly possible

↳ EK-TM4129GXL Buy

↳ we have some breakout boards. Have CAN+USB available? ↳ CAN+USB do that



↳ dt+, dt-
↳ USB 2.0, CAN & differential + high speed

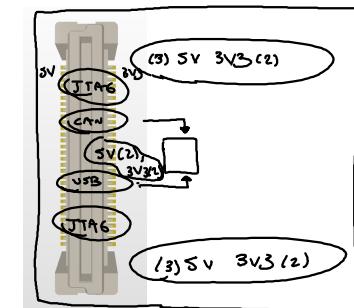
GND	GND
DT	CAN-H
D-	CAN-L
GND	GND
:	:

↳ 12V, Switch-mode power converter
↳ buck, boost, buck/boost
↳ 0.4A/contact
↳ NOISY

3V3 @ 20W ≈ 6.06A = 6 pins = 3A
5V @ 20W ≈ 4A = 8 pins

25 pins

14 + 14 = 28 pins
↳ 32 pins



Front
Spare

Connectors

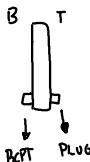
10H4517 (= RCPT) - (06 = 2x30, 08 = 2x40) (1-4) (Plating) (Polarization Poly) (Packaging) (Lead Free)

for 7 mm spacing:

10H4517 - 061826LF (RCPT)
08 3

USB = USB-C
5V, 3.3V = TX/GND TE ones from
CAN = RJ45 Thrust/kill

1044518 - 063826LF (Prog)
08 3

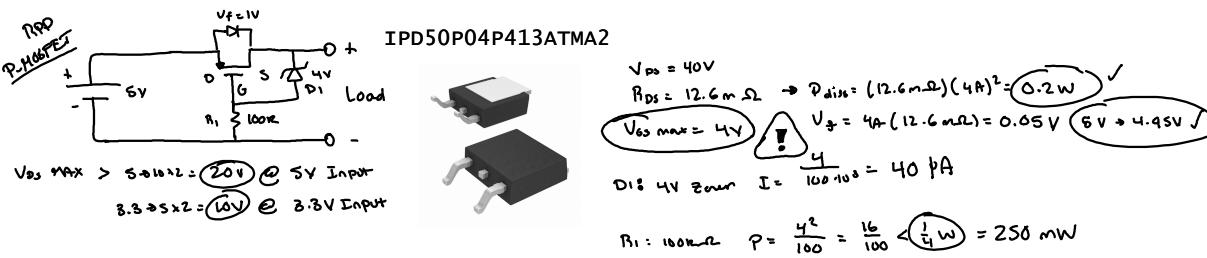


New Layout

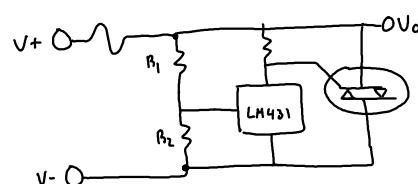
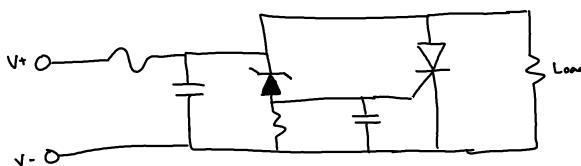
3V3 = 8 pins = 4A = 13.2W

5V = 8 pins = 4A = 20W

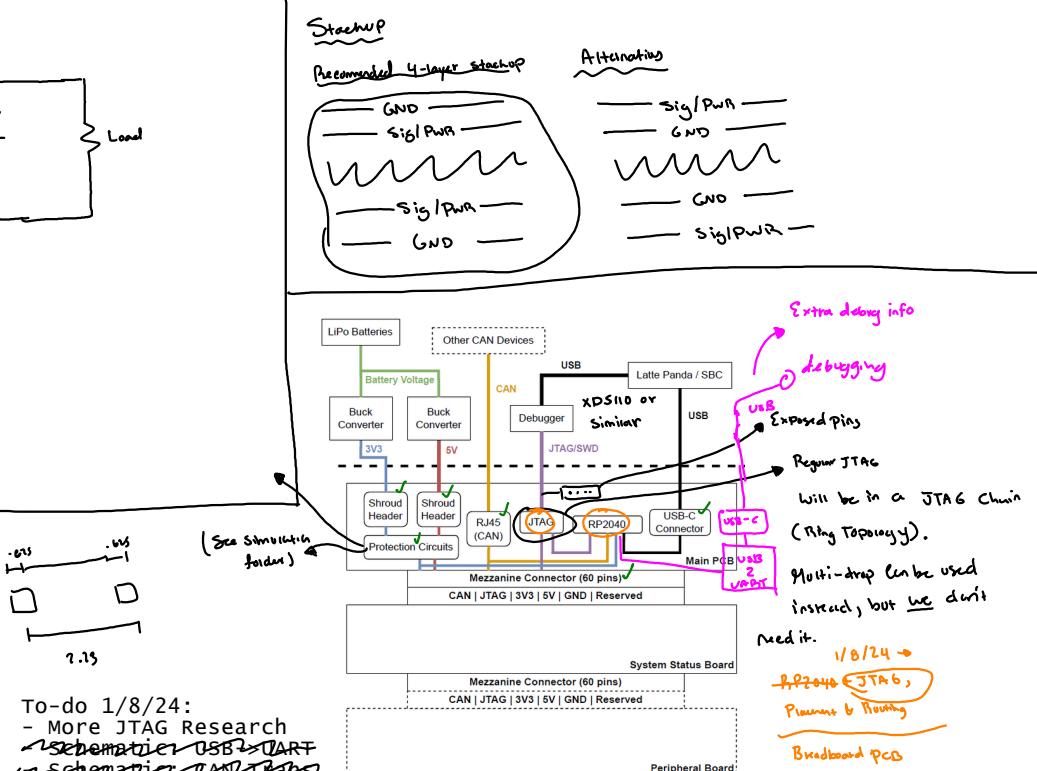
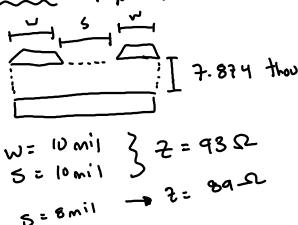
16 GND = 8A



OVP → Crowbar circuit limit = 5.5V & 3.2V



USB Lines target impedance = $90\ \Omega$



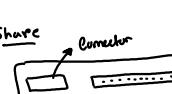
TG1S Breakout

o 3.3V, 5V, GND → 2.54 headers
o CAN, JTAG



Right angle header?

order 5 sets, draw them
see signal degradation?

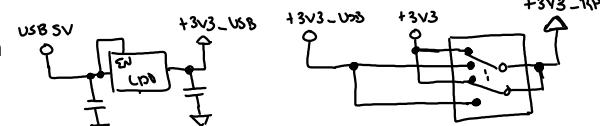


(MAYBE) Research protection circuits with LEDs

Not as accurate as with actual testing RP2040

switching to 80-pin DPAK 50V

switching to 80-pin DPAK 50V
for ST versions (added more grounds
and spaced them for better return paths)



+3V3-RP

Description	Pin Name	Function	Pin # (BTM)	Pin # (TOP)	Function	Pin Name	Description
-	GND	-	1	2	GND	-	-
-	5V	-	3	4	3V3	-	-
-	5V	-	5	6	3V3	-	-
-	5V	-	7	8	3V3	-	-
-	5V	-	9	10	GND	-	-
Voltage Reference	VREF	IC1	11	12	-	RSVTRST	System reset
GND Detect	GNDetect	JTAG	13	14	GND	TRACECLK	Trace clock
Test Mode Select Input	JTDI	JTAG	15	16	GND	-	-
Data Out	JTDQ[3:0]	JTAG	19	20	JTAG	TRD0	Trace 00
Test Clock	JTCK	JTAG	21	22	JTAG	TRD1	Trace 01
Test Data In	JTMISW[3:0]	JTAG	23	28	JTAG	TRD2	Trace 02
Test Data In	JTMISW[3:0]	JTAG	29	30	GND	TRD3	Trace 03
Reserved	-	RSVD	31	32	RSVD	-	Reserved
Reserved	-	RSVD	33	34	RSVD	-	Reserved
Differential High CAN-H	CAN-H	JAN	37	38	GND	-	Reserved
Differential Low CAN-L	CAN-L	JAN	41	42	GND	-	Reserved
-	5V	43	44	3V3	-	-	-
-	5V	45	46	3V3	-	-	-
-	5V	47	48	GND	-	-	-
Received	RSVD	49	50	RSVD	-	Reserved	
Received	RSVD	51	52	RSVD	-	Reserved	
Received	RSVD	53	54	RSVD	-	Reserved	
Received	RSVD	55	56	RSVD	-	Reserved	
Received	RSVD	57	58	RSVD	-	Reserved	
Received	RSVD	59	60	GND	-	Reserved	
Received	RSVD	61	62	RSVD	-	Reserved	
Received	RSVD	63	64	RSVD	-	Reserved	
Received	RSVD	65	66	GND	-	Reserved	
Received	RSVD	67	68	RSVD	-	Reserved	
Received	RSVD	69	70	RSVD	-	Reserved	
-	GND	71	72	GND	-	-	-
-	3V3	73	74	3V3	-	-	-
-	3V3	75	76	3V3	-	-	-
-	3V3	77	78	3V3	-	-	-
-	GND	79	80	GND	-	-	-

I isolated SWD from JTAG.
XDS110, J-link
be aware of layout & both but SWD
cannot be easily shared!

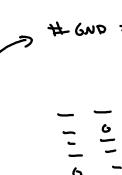
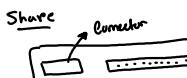
How many headers?

↳ Power (2)

↳ Ground (2) (22 pins)

↳ CAN bus (2)

↳ JTAG (12?)



$2^2 + 2 + 12$

$= 36$

$36 / 2 = 18$ Pairs

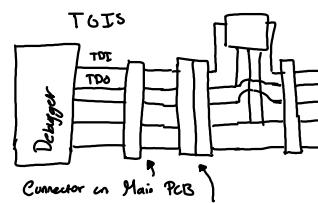
JTAG Chain

Topologies include

- o Ring (IEEE 1149.1)

- o Star (Needs multiple sites)

- o Multidrop ← Nice, but Extra hardware (\$\$\$), not widely supported or discussed, and won't work if a board fails the entire robot will fail (all boards are essential) or will at least be checked out before continuing.



Return path for TDI
Most儿 built into
Every board
(Early termination header
resistor)

SWD Chain

SWD 2.0 is the standard for Multidrop SWD

Introduced a long time ago - Still no widespread adoption or support.

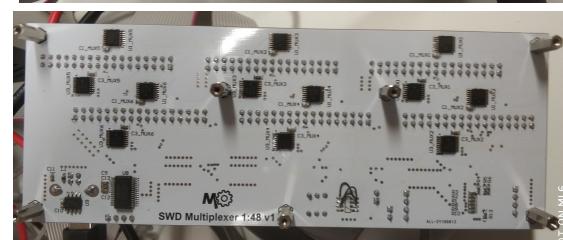
PProteo supports chaining in a Star topology (multiple Subbus lines)

Can be multiplexed using an SWD multiplexer (Custom hardware design, no IC's or decs)

Constructed using Analog multiplexers = Another separate project!

Instead using Custom Software = Too complex to fit in this one :-;

<https://devzone.nordicsemi.com/f/nordic-q-a/35094/what-is-the-swd-driver-impedance-of-swdio-line>

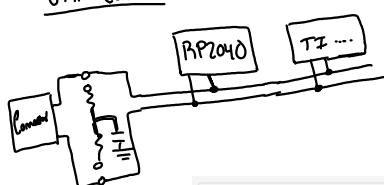


L. Bogdanov, "Multiple Microcontroller Programming Using the SWD Interface,"
2020 XXIX International Scientific Conference Electronics (ET), Sozopol, Bulgaria, 2020,
pp. 1-4, doi: 10.1109/ET50336.2020.9238282.

& Software.

Same Idea, but with clearer schematics & Design could be replicated with more widely supported
Microcontrollers...

CAN Connector



Each device must provide optional
termination resistors

Trace Type

- Microstrip
- Stripline
- Embedded Microstrip
- Asymmetric Stripline
- Edge Coupled Microstrip
- Broadside Coupled Stripline
- Edge Coupled Stripline

Solve For

- Impedance
- Trace Width

TRACE THICKNESS (t)

HEIGHT (h)

TRACE WIDTH (w)

TRACE SPACING (s)

DIELECTRIC CONSTANT (ϵ_r)

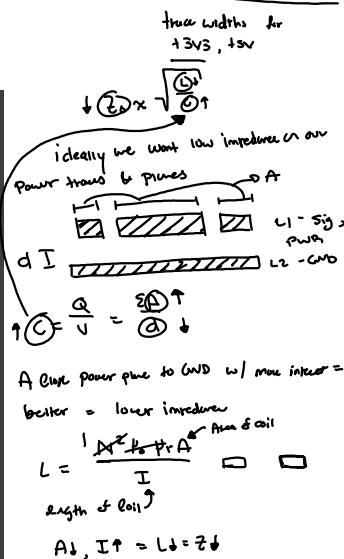
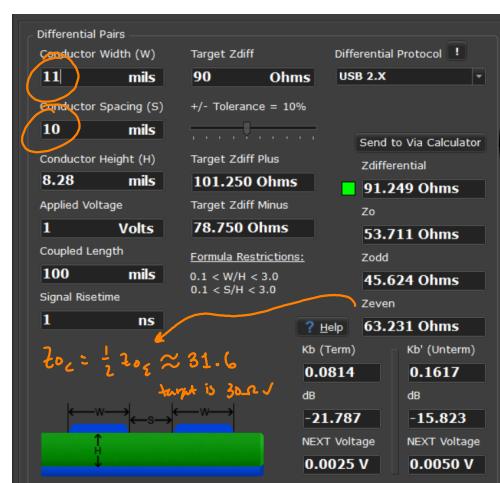
DIFFERENTIAL IMPEDANCE (Z_0)

Good Enough results for someone
who does not know TF he's doing :)

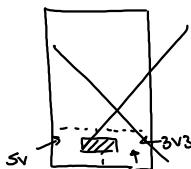
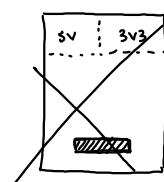
$Z_d \approx \frac{174}{\sqrt{\epsilon_r + 1.41}} \times \ln \left(\frac{5.98h}{(0.8w + t)} \right) \times [1 - 0.48 \exp(-0.98 \frac{s}{h})]$

$Z_d = \frac{1}{2} Z_{0d} \approx 31.6$ target is 30 ohms

USB



Layout



$L_1 = \text{SV/SV}$
 $L_2 = \text{GND}$
 $L_3 = \text{GND}$
 $L_4 = \text{SV/3V3}$

won't fit! Split both boards

↳ Power board (3V3, 5V + protection circuits for both) ↳ Right angle connectors for everything

↳ USB to CAN board (USB side input, CAN side input)