







Pin-to-pin connection diagram for the 10144517-061802LF connector. The diagram shows two columns of pins, 1 through 59 on the left and 2 through 60 on the right. Various signals are connected to specific pins, including power (5V, 3V3), ground (GND), and control signals (VREF, JnRST, JnRSTCLK, TRD0, TRD1, TRD2, TRD3, CANO_P, CANO_N).

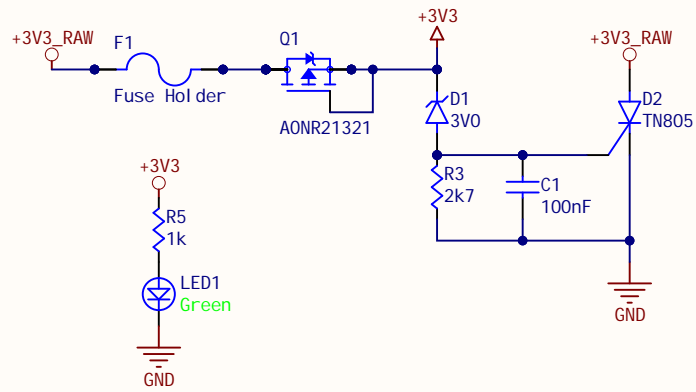
| Signal | Pin(s) |
|----------|---|
| +5V | 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60 |
| +3V3 | 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60 |
| GND | 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60 |
| VREF | 13 |
| JnRST | 12 |
| JnRSTCLK | 14 |
| TRD0 | 16 |
| TRD1 | 18 |
| TRD2 | 20 |
| TRD3 | 22 |
| CANO_P | 25 |
| CANO_N | 26 |

The top diagram shows the USB + POWER module (J2) with connections for +5V USB, USB D_N, USB D_P, and GND. The bottom diagram shows the SERIAL DEBUG module (J7) with connections for USB D_N, USB D_P, and GND. Both diagrams show the module's internal pins and their connections to external components like resistors and ground.

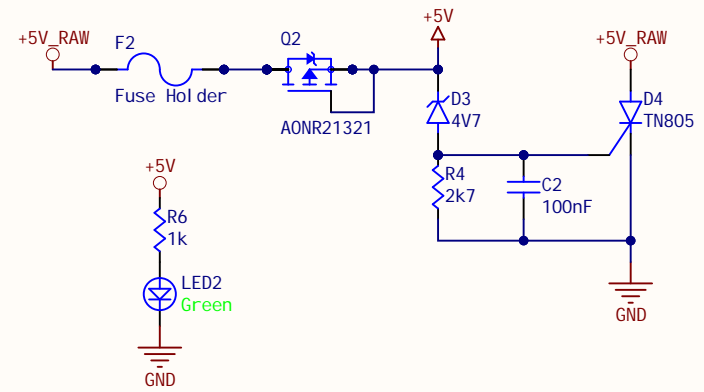
| | | |
|------------|------------|---|
| USBO_D_P | USBO_D_P |  |
| USBO_D_N | USBO_D_N |  |
| USB1_D_P | USB1_D_P |  |
| USB1_D_N | USB1_D_N |  |
| CANO_P | CANO_P |  |
| CANO_N | CANO_N |  |
| CANO_YLW | CANO_YLW | |
| CANO_GRN | CANO_GRN | |
| JTMS/SWDIO | JTMS/SWDIO | |
| JTCK/SWCLK | JTCK/SWCLK | |

| Description | Pin Name | Function | Pin # (SWP) | Pin # (TOP) | Function | Pin Name | Description |
|------------------------|------------|----------|----------------|----------------|----------|----------|--------------|
| - | - | GND | 1 | 2 | GND | - | - |
| - | - | SV | 3 | 4 | SV3 | - | - |
| - | - | SV | 5 | 6 | SV3 | - | - |
| - | - | SV | 7 | 8 | SV3 | - | - |
| - | - | GND | 9 | 10 | GND | - | - |
| Voltage reference | VREF | JTAG | 11 | 12 | JTAG | JRefST | System reset |
| - | - | GND | 13 | 14 | GND | - | - |
| GNDDetect | GNDetect | JTAG | 15 | 16 | JTAG | TRACCLK | Trace Clock |
| - | - | GND | 17 | 18 | GND | - | - |
| Test Mode Select Input | JTDI | JTAG | 19 | 20 | JTAG | TRD0 | Trace D0 |
| Data Out | JTD0/SWIO | SVIO | 21 | 22 | JTAG | TRD1 | Trace D1 |
| - | - | GND | 23 | 24 | GND | - | - |
| Test Clock | JTCK/SWCLK | SVIO | 25 | 26 | JTAG | TRD2 | Trace D2 |
| Test data in | JTMS/SWIO | JTAG | 27 | 28 | JTAG | TRD3 | Trace D3 |
| - | - | GND | 29 | 30 | GND | - | - |
| Reserved | - | RSVD | 31 | 32 | RSVD | - | Reserved |
| Reserved | - | RSVD | 33 | 34 | RSVD | - | Reserved |
| - | - | GND | 35 | 36 | GND | - | - |
| Differential High | CAN HI | CAN | 37 | 38 | RSVD | - | Reserved |
| Differential Low | CAN LO | CAN | 39 | 40 | RSVD | - | Reserved |
| - | - | GND | 41 | 42 | GND | - | - |
| - | - | SV | 43 | 44 | SV3 | - | - |
| - | - | SV | 45 | 46 | SV3 | - | - |
| - | - | GND | 47 | 48 | GND | - | - |
| Reserved | - | RSVD | 49 | 50 | RSVD | - | Reserved |
| Reserved | - | RSVD | 51 | 52 | RSVD | - | Reserved |
| Reserved | - | GND | 53 | 54 | GND | - | - |
| Reserved | - | RSVD | 55 | 56 | RSVD | - | Reserved |
| Reserved | - | RSVD | 57 | 58 | RSVD | - | Reserved |
| - | - | GND | 59 | 60 | GND | - | - |
| Reserved | - | RSVD | 61 | 62 | RSVD | - | Reserved |
| Reserved | - | RSVD | 63 | 64 | RSVD | - | Reserved |
| - | - | GND | 65 | 66 | GND | - | - |
| Reserved | - | RSVD | 67 | 68 | RSVD | - | Reserved |
| Reserved | - | RSVD | 69 | 70 | RSVD | - | Reserved |
| - | - | GND | 71 | 72 | GND | - | - |
| - | - | SV3 | 73 | 74 | SV | - | - |
| - | - | SV3 | 75 | 76 | SV | - | - |
| - | - | SV3 | 77 | 78 | SV | - | - |
| - | - | GND | 79 | 80 | GND | - | - |

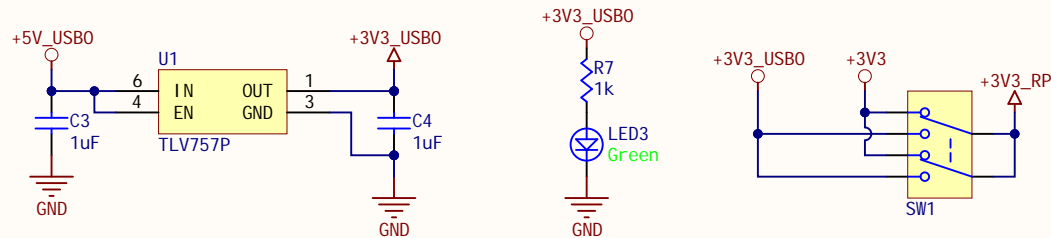
3. 3V PROTECTION CIRCUIT



5V PROTECTION CIRCUIT



RP2040 POWER



NOTES:
 [1] SEE SIMULATION FOLDER FOR DETAILS.
 [2] FUSE HOLDER ACCEPTS 4A AUTOMOTIVE FUSE (E.G. https://www.napaonline.com/en/p/BK_7822086)
 [3] POWER FOR THE RP2040 CAN COME FROM THE USB HOST OR AN EXTERNAL REGULATOR.

Project/Vehicle: TGIS - Main PCB

Author(s):
 -Yovany Molina
 -Blake Sanders

Revisor(s):
 -*
 -*
 -*
 -*

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Git Repo: <https://github.com/yomole/TailGator>
 Git Hash: bbabc1c7



Date: 1/9/2024

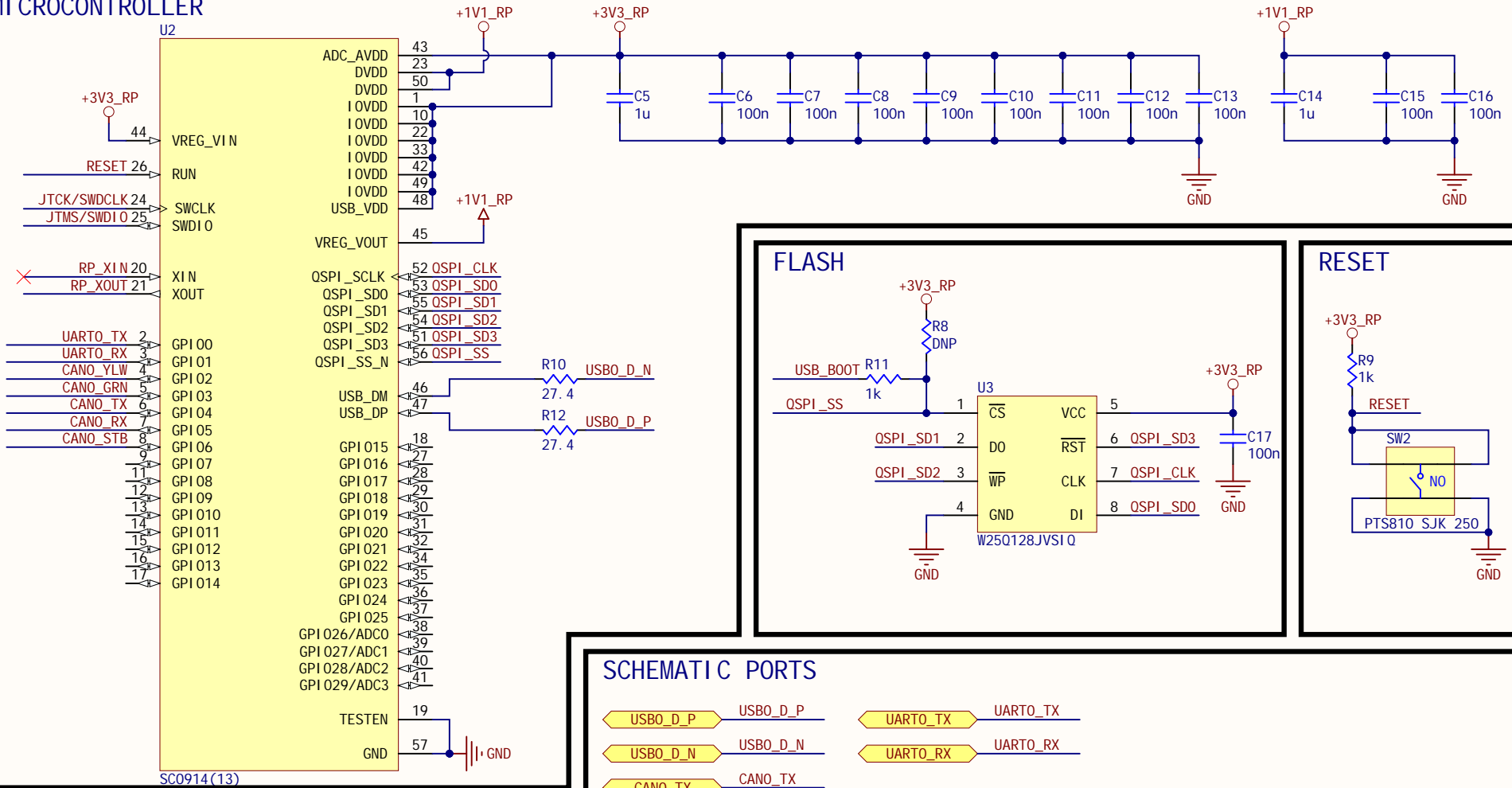
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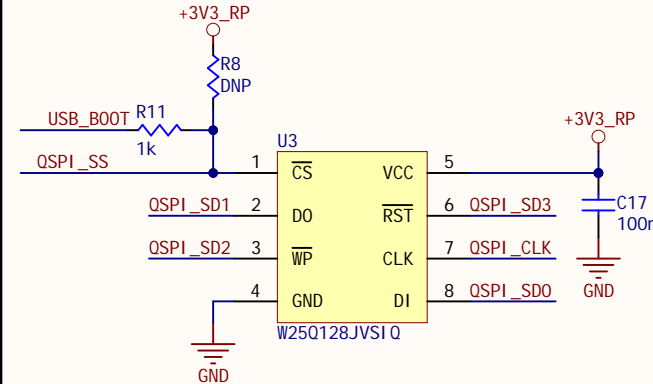
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Sheet 2 of 4

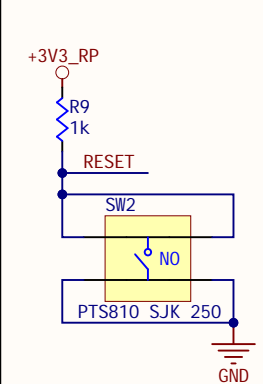
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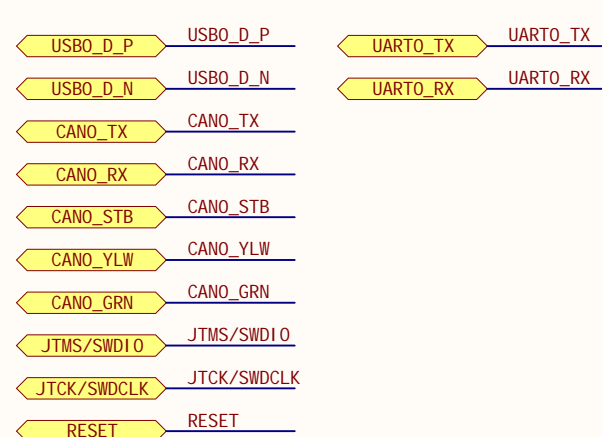
FLASH



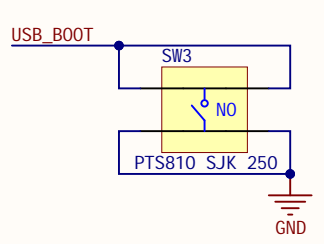
RESET



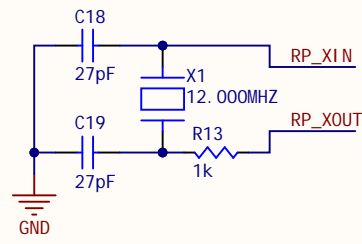
SCHEMATIC PORTS



BOOTSEL



OSCILLATOR



NOTES:

- SEE RP2040 DATASHEET AND THE RP2040 HARDWARE DESIGN GUIDE FOR DETAILS.
- 1UF BULK DECOUPLING CAPS HAVE PRIORITY PLACEMENT.
- USE 10K RESISTOR FOR DNP IF CS IS NOT AT VCC ON STARTUP.
- RP2040 USES FLASH CS AS BOOTSEL.
- CANO COMMUNICATION RELIES ON "CAN2040" PIO IMPLEMENTATION (KevinConnor/can2040 ON GITHUB).

Project/Vehicle: TGIS - Main PCB

Author(s):
-Yovany Molina
-Blake Sanders

Revisor(s):
-
-
-
-

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Git Repo: <https://github.com/yomole/TailGator>
Git Hash: bbabc1c7



Date: 1/9/2024

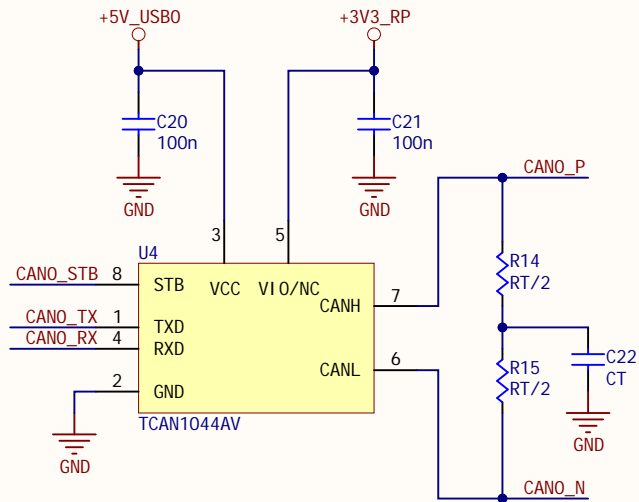
Revision: A

Size: A

File: Microcontroller.SchDoc

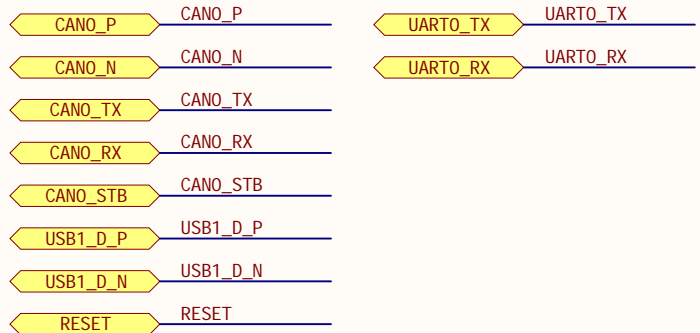
Sheet 3 of 4

CAN TRANSCEIVER



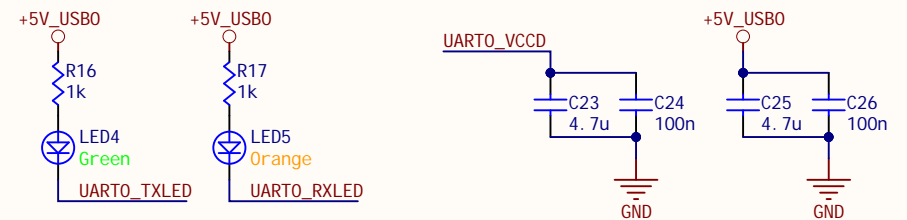
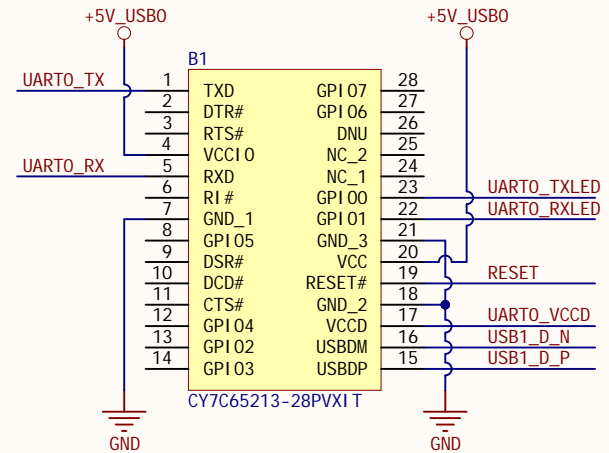
Notes:
 [1] REPLACE RT, CT (IF NEEDED) WITH APPROPRIATE TERMINATION RESISTORS AND SPLIT TERMINATION CAPACITORS FOR THE GIVEN CAN NETWORK.
 [2] IO SUPPLY VOLTAGE IS 3.3V TO WORK WITH ANY EXISTING SN65HVD230 CAN TRANSCEIVERS.

SCHEMATIC PORTS



Notes:
 [1] CAN FD IS BACKWARDS COMPATIBLE WITH CAN 2.0, BUT NOT VICE-VERSA.

UART TRANSCEIVER



| | | | |
|--|-------------------------------------|---|---------------------------|
| Project/Vehicle: TGIS - Main PCB | | Machine Intelligence Laboratory 1889 Museum Rd Room 3001 Gainesville, FL, 32611 | |
| Author(s): -Yovany Molina -Blake Sanders | Revison(s): -* -* -* -* | Git Repo: https://github.com/yomole/TailGator Git Hash: bbabc1c7 | |
| Date: 1/9/2024 | Revision: A | Size: A | File: Transceivers.SchDoc |



| Comment | Description | Designator | Footprint | LibRef | Quantity |
|-------------------|---|--|---------------------------------|----------------------------|----------|
| CY7C65213-28PVXIT | USB Interface IC 32KB USB-UART LP Bridge Controller | B1 | SOP65P780X200-28N | CY7C65213-28PVXIT | 1 |
| Cap | | C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26 | CAPC0805 | Cap | 26 |
| 3V0 | DIODE ZENER 3.0V 500MW SOD123 | D1 | DIO_BZT52C4V7S_R9 | BZT52C3V0 | 1 |
| TN805 | SCR 600 V 8 A Standard Recovery Surface Mount DPAK | D2, D4 | DPAK_TN | TN805-600B-TR | 2 |
| 4V7 | DIODE ZENER 4.7V 500MW SOD123 | D3 | DIO_BZT52C4V7S_R9 | BZT52C4V7S_R9 | 1 |
| Fuse Holder | Fuse Holder 30 A 500V 1 Circuit Blade Through Hole | F1, F2 | FUSE_3568 | 3568 | 2 |
| 10144517-061802LF | CONN RCPT 60POS SMD GOLD | J1 | AMPHENOL_1014451 7-061802LF | 10144517-061802LF | 1 |
| USB4120-03 | USB-C (USB TYPE-C) USB 2.0 Receptacle Connector 24 (16+8 Dummy) Position Surface Mount, Through Hole | J2, J7 | GCT_USB4120-03- C_REVA | USB4120-03 | 2 |
| 1877285-2 | | J3, J4 | TE_1877285-2 | 1877285-2 | 2 |
| RJHSE-3381 | Jack Modular Connector 8p8c (RJ45, Ethernet) Vertical Shielded | J5 | AMPHENOL_RJHSE33 81 | RJHSE-3381 | 1 |
| FTSH-110 | Connector Header Surface Mount 20 position 0.050" (1.27mm) | J6 | SAMTEC_FTSH-110-01- L-DV-007 | FTSH-110-01-L-DV- 007-K | 1 |
| LED | | LED1, LED2, LED3, LED4, LED5 | LED0603 | LED | 5 |
| AONR21321 | P-Channel 30 V 24A (Tc) 4.1W (Ta), 24W (Tc) Surface Mount 8- DFN-EP (3x3) | Q1, Q2 | TRANS_AONR21321 | AONR21321 | 2 |
| Res | | R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13 | RES0805 | Res | 13 |
| Res | | R14, R15, R16, R17 | RES0603 | Res | 4 |
| JS202011SCON | Slide Switch DPDT Surface Mount | SW1 | SW_JS202011SCON | JS202011SCON | 1 |
| PTS810 SJK 250 | Tactile Switch SPST- NO Top Actuated Surface Mount | SW2, SW3 | SW_PTS810_SJM_250 _SMTR_LFS | PTS810 SJK 250 SMTR LFS | 2 |
| TLV757P | Linear Voltage Regulator IC Positive Fixed 1 Output 1A 6- WSO (2x2) | U1 | VREG_TLV75733PDRV R | TLV75733PDRV | 1 |
| SC0914(13) | ARM® Cortex®-M0+ - Microcontroller IC 32- Bit Dual-Core 133MHz External Program Memory 56-QFN (7x7) | U2 | QFN40P700X700X90- 57N | SC0914(13) | 1 |
| W25Q128JVSQ | FLASH - NOR Memory IC 128Mbit SPI - Quad I/O, QPI, DTR 133 MHz 8-SOIC | U3 | SOIC127P790X216-8N | W25Q128JVSQ | 1 |
| TCAN1044AV | 1/1 Transceiver Half CANbus TSOT-23-8 | U4 | SOT65P280X110-8N | TCAN1044AVDDFRQ1 | 1 |
| 12.000MHZ | 12 MHz ±20ppm Crystal 18pF 50 Ohms HC-49/US | X1 | ABLS-12.000MHZ | ABLS-12.000MHZ | 1 |