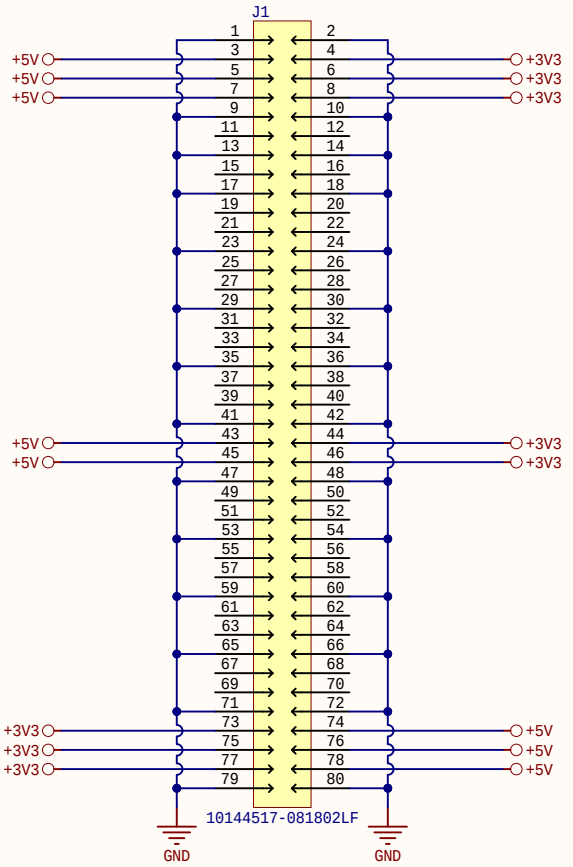
BOARD CONNECTOR



Description	Pin Name	Function	Pin # (BTM)	Pin # (TOP)	Function	Pin Name	Description
-	-	GND	1	2	GND	-	-
-	-	5V	3	4	3V3	-	-
-	-	5V	5	6	3V3	-	-
-	-	5V	7	8	3V3	-	-
-	-	GND	9	10	GND	-	-
Voltage reference	VREF	JTAG	11	12	JTAG	JnSRST	System reset
-	-	GND	13	14	GND	-	-
GNDDetect	GNDetect	JTAG	15	16	JTAG	TRACECLK	Trace Clock
-	-	GND	17	18	GND		
Test Mode Select Input	JTDI	JTAG	19	20	JTAG	TRD0	Trace D0
Data Out	JTDO	JTAG	21	22	JTAG	TRD1	Trace D1
-	-	GND	23	24	GND	-	-
Test Clock	JTCK	JTAG	25	26	JTAG	TRD2	Trace D2
Test data in	JTMS	JTAG	27	28	JTAG	TRD3	Trace D3
-	-	GND	29	30	GND	-	-
Serial Wire Debug Clock	SWDCLK	SWD	31	32	RSVD	-	Reserved
Serial Wire Debug IO	SWDIO	SWD	33	34	RSVD	-	Reserved
-	-	GND	35	36	GND	-	-
Differential High	CAN-HI	CAN	37	38	RSVD	-	Reserved
Differential Low	CAN-LO	CAN	39	40	RSVD	-	Reserved
-	-	GND	41	42	GND	-	-
-	-	5V	43	44	3V3	-	-
-	-	5V	45	46	3V3	-	-
-	-	GND	47	48	GND	-	-
Reserved	-	RSVD	49	50	RSVD	-	Reserved
Reserved	-	RSVD	51	52	RSVD	-	Reserved
-	-	GND	53	54	GND	-	-
Reserved	-	RSVD	55	56	RSVD	-	Reserved
Reserved	-	RSVD	57	58	RSVD	-	Reserved
-	-	GND	59	60	GND	-	-
Reserved	-	RSVD	61	62	RSVD	-	Reserved
Reserved	-	RSVD	63	64	RSVD	-	Reserved
-	-	GND	65	66	GND	-	-
Reserved	-	RSVD	67	68	RSVD	-	Reserved
Reserved	-	RSVD	69	70	RSVD	-	Reserved
-	-	GND	71	72	GND	-	-
-	-	3V3	73	74	5V	-	-
-	-	3V3	75	76	5V	-	-
-	-	3V3	77	78	5V	-	-
-	-	GND	79	80	GND	-	-

NOTES:

Project/Vehicle: TGIS - Main PCB

Author(s):
-Yovany Molina
-Blake Sanders
-*
-*

Revisor(s):
-*
-*
-*
-*

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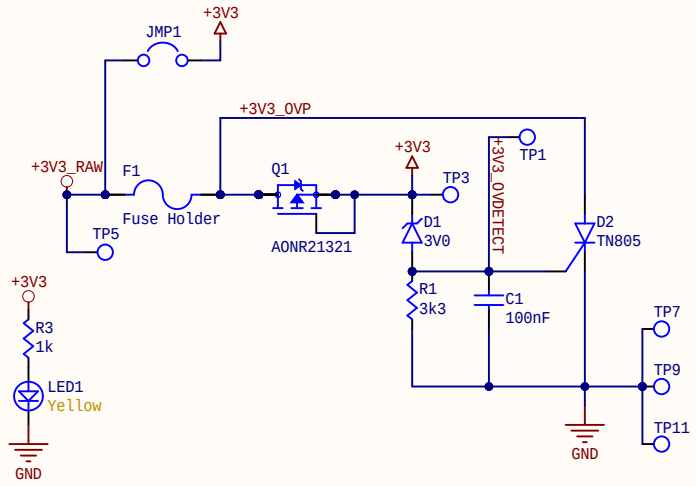
1889 Museum Rd.
Room 3001
Gainesville, FL, 32611

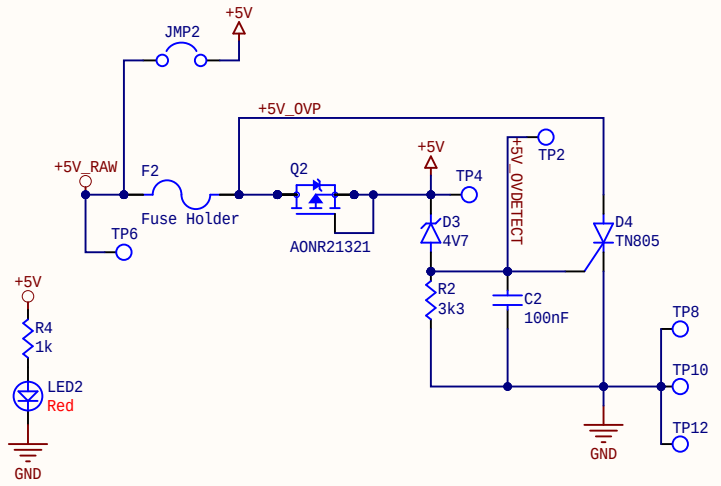
Git Repo: https://github.com/yomole/TailGator
Git Hash: 20141556

Date: 1/18/2024 | Revision: - | Size: A | File: Connectors.SchDoc | Sheet 1 of 2

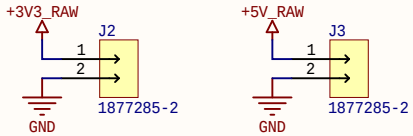
3.3V PROTECTION CIRCUIT



5V PROTECTION CIRCUIT



CONNECTORS



NOTES:
[1] POWER RAILS NEED VOLTAGES 0.6V HIGHER THAN THEIR RAILS BECAUSE OF PROTECTION CIRCUITS.
[2] OVERVOLTAGE PROTECTION APPLIES AT VOLTAGES HIGHER THAN 4.5V AND 6V FOR 3.3V AND 5V INPUTS.

NOTES:
[1] SEE SIMULATION FOLDER FOR DETAILS.
[2] FUSE HOLDER ACCEPTS 4A AUTOMOTIVE FUSE (E.G. https://www.napaonline.com/en/p/BK_7822086)
[3] JUMPERS PROVIDED FOR BYPASSING PROTECTION DURING PROTOTYPING STAGE. THE PIN HEADER AND JUMPER SHOULD BE RATED FOR AT LEAST 4A (E.G. SNT-100-BK-T).

Project/Vehicle: TGIS - Main PCB	
Author(s): -Yovany Molina -Blake Sanders -* -*	Revisor(s): -* -* -* -*
Date: 1/18/2024	Revision: A
Size: A	File: Power.SchDoc
Sheet 2 of 2	

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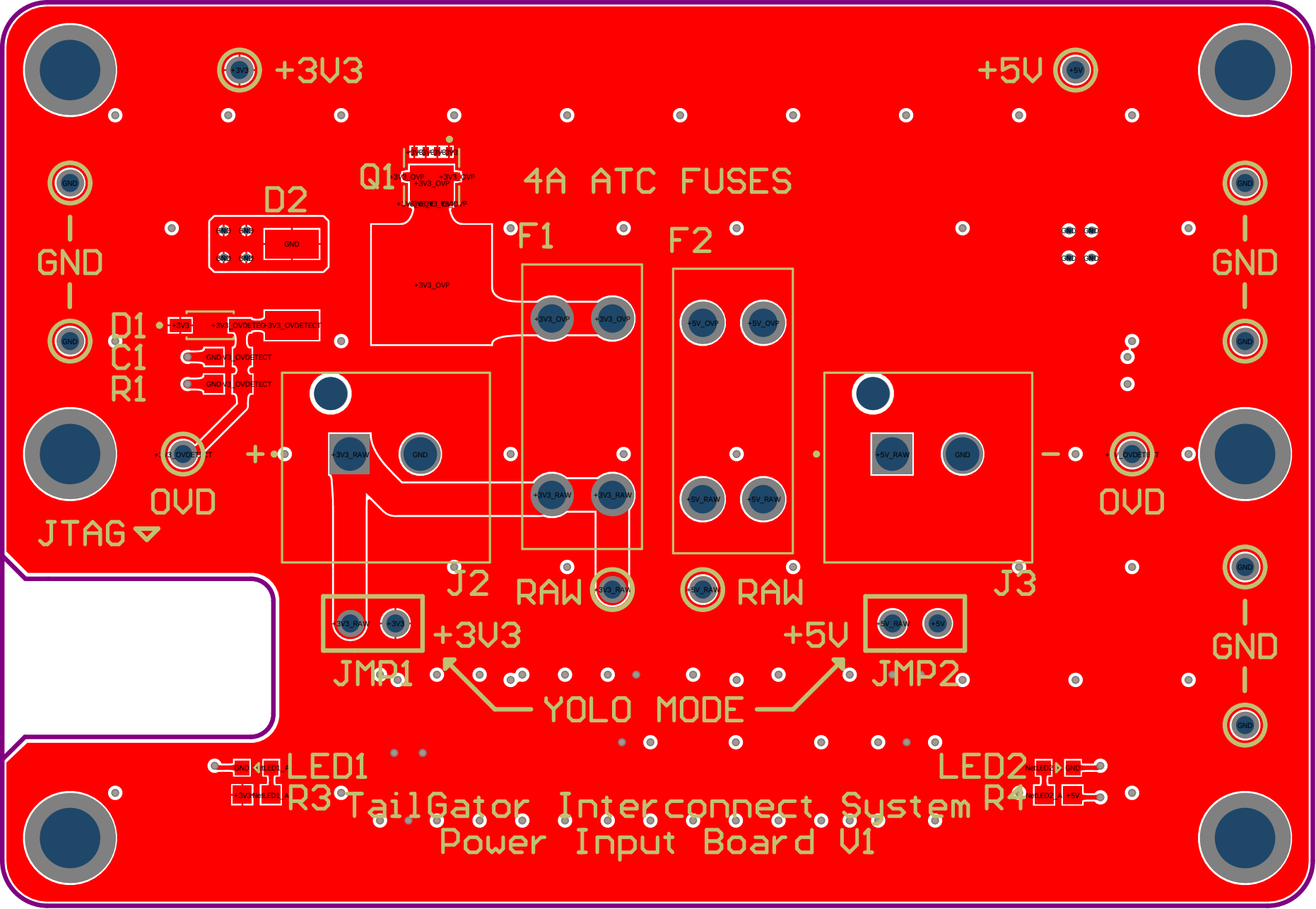
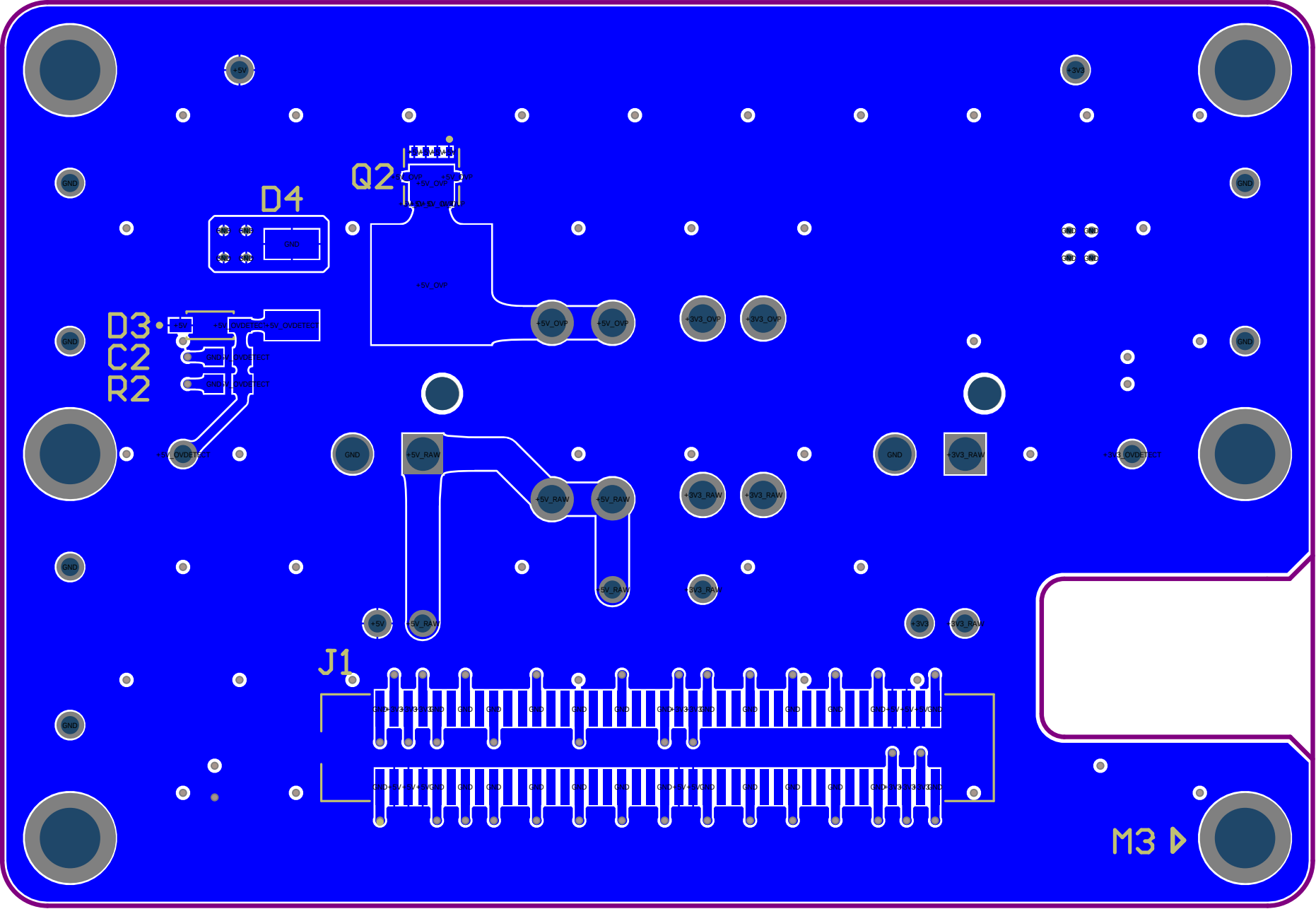
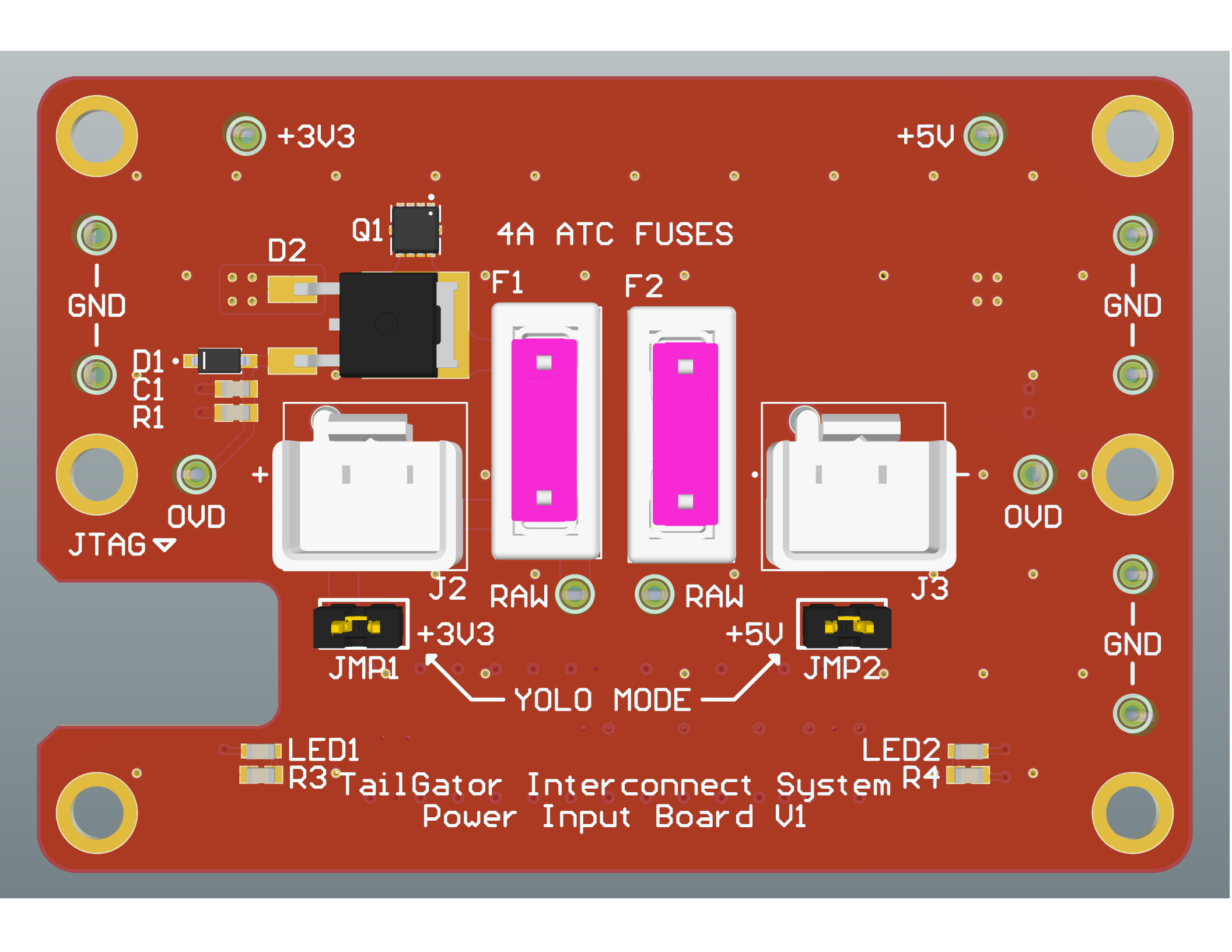
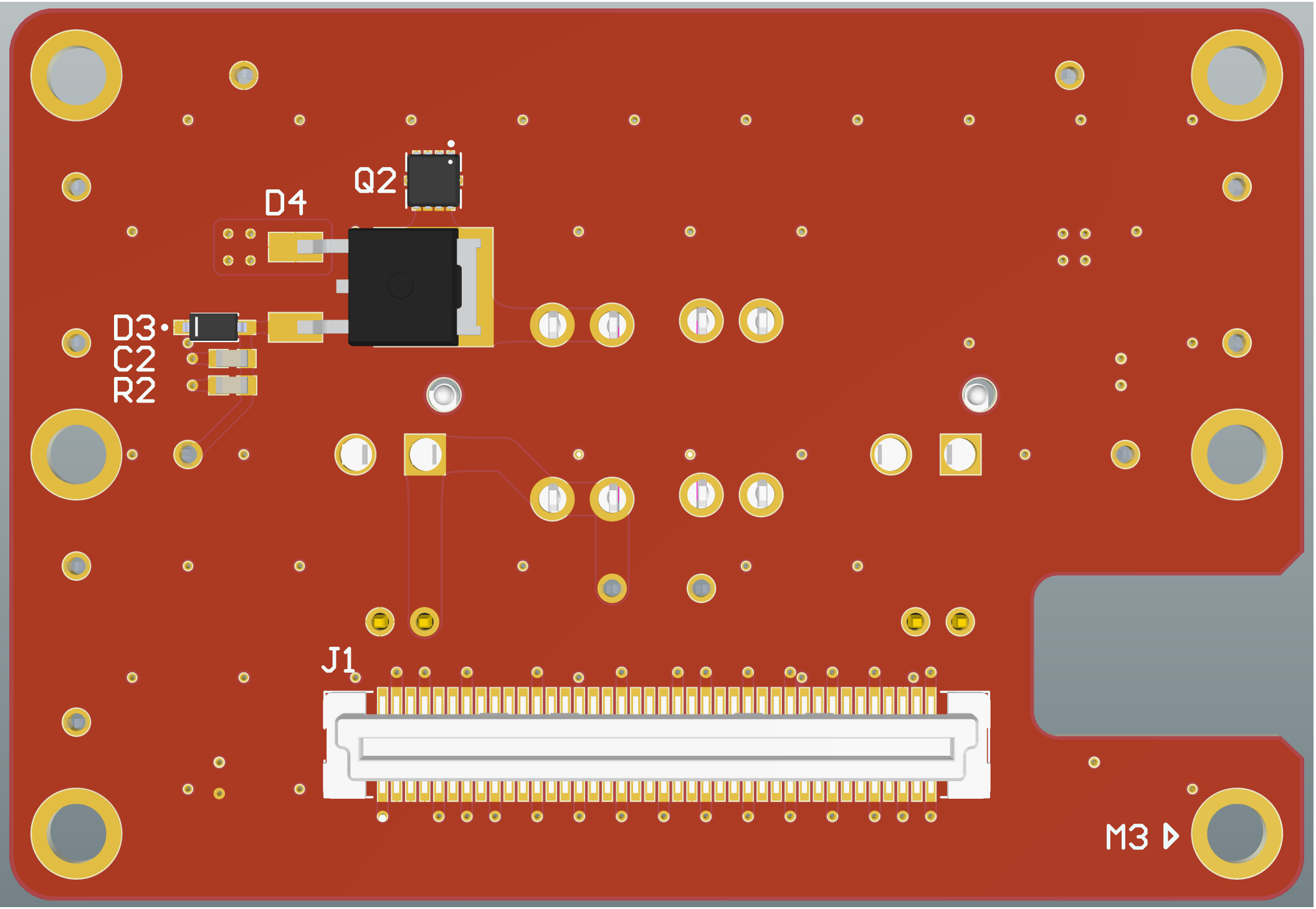
Git Hash: 20141556


+3V3
+5V
GND
GND
GND
GND
Q1
D2
4A ATC FUSES
F1
F2
D1
C1
R1
OVD
OVD
JTAG
J2
RAW
RAW
J3
+3V3
+5V
JMP1
JMP2
YOLO MODE
LED1
R3
LED2
R4
TailGator Interconnect System
Power Input Board V1


Q2
D4
D3
C2
R2
J1
M3
+5V
+3V3
GND
+5V_OVP
+3V3_OVP
+5V_RAW
+3V3_RAW
+5V_OVDETECT
+3V3_OVDETECT


+3V3
+5V
Q1
4A ATC FUSES
D2
F1
F2
GND
GND
D1
C1
R1
OVD
OVD
JTAG
J2
RAW
RAW
J3
+3V3
+5V
JMP1
JMP2
YOLO MODE
GND
LED1
R3
LED2
R4
TailGator Interconnect System
Power Input Board V1


Q2
D4
D3
C2
R2
J1
M3

Comment	Description	Designator	Footprint	LibRef	Quantity
Cap		C1, C2	CAPC0603	Cap	2
3V0	DIODE ZENER 3.0V 500MW SOD123	D1	SOD3715X135N	BZT52C3V0	1
TN805	SCR 600 V 8 A Standard Recovery Surface Mount DPAK	D2, D4	DPAK_TN	TN805-600B-TR	2
4V7	DIODE ZENER 4.7V 500MW SOD123	D3	SOD3715X135N	BZT52C4V7	1
Fuse Holder	Fuse Holder 30 A 500V 1 Circuit Blade Through Hole	F1, F2	FUSE_3568	3568	2
10144517-081802LF	CONN RCPT 1 80POS SMD GOLD	J1	AMPHENOL_10144517-081802LF	10144517-081802LF	1
1877285-2		J2, J3	TE_1877285-2	1877285-2	2
LED		LED1, LED2	LED0603	LED	2
AONR21321	P-Channel 30 V 24A (Tc) 4.1W (Ta), 24W (Tc) Surface Mount 8-DFN-EP (3x3)	Q1, Q2	TRANS_AONR21321	AONR21321	2
Res		R1, R2, R3, R4	RES0603	Res	4
TP		TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12	TPTH-100mil	TP	12

Electrical Rules Check Report

Class	Document	Message
		Successful Compile for TGIS Main.PrjPcb

Design Rules Verification Report

Filename : C:\Users\molyo\OneDrive\Desktop\MIL\TailGator\PCB\TailGator Interconnect Syste

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=4mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=4mil) (Max=71497.938mil) (Preferred=4mil) (All)	0
Power Plane Connect Rule(Direct Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Power Plane Connect Rule(Relief Connect)(Expansion=11.811mil) (Conductor Width=4mil) (Air Gap=4mil) (Entries=4)	0
Minimum Annular Ring (Minimum=3mil) (All)	0
Hole Size Constraint (Min=7.874mil) (Max=248.031mil) (All)	0
Hole To Hole Clearance (Gap=9.842mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0mil) (All),(All)	0
Silk To Solder Mask (Clearance=4mil) (IsPad),(All)	0
Silk to Silk (Clearance=0mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Board Clearance Constraint (Gap=0mil) (All)	0
Height Constraint (Min=0mil) (Max=71497.938mil) (Prefered=500mil) (All)	0
Total	0