APPLICATION NOTE

AT07216: SAM G55 Schematic Checklist

Atmel | SMART SAM G55

Introduction

A good hardware design comes from a proper schematic. Since SAM G55 devices have a fair number of pins and functions, the schematic for these devices can be large and quite complex.

This application note describes a common checklist which should be used when building and reviewing the schematics of a SAM G55 application design.

The document covers the following general aspect:

- Power supply strategies
- Clock and crystal oscillators
- JTAG and SWD debug ports
- USB port
- Bootloader driven pins
- Suggested reading

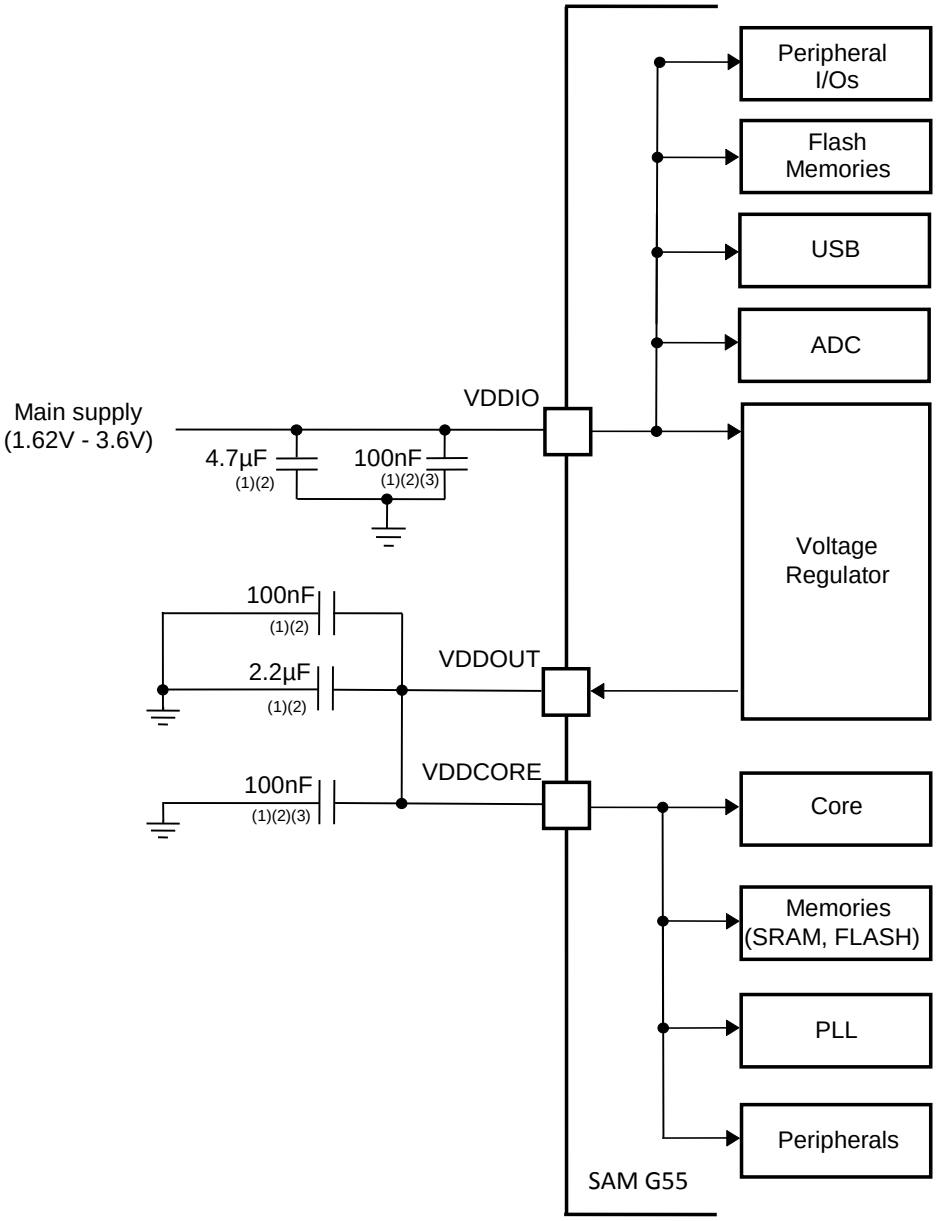
1 Schematic Checklist

1.1 Power Supply Strategy

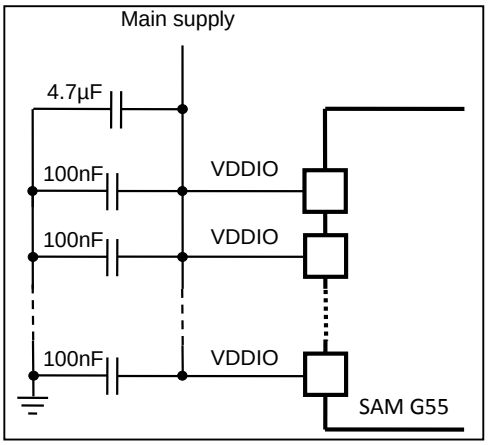
1.1.1 49-pin WLCSP Package

Single power supply strategy is mandatory on SAM G55. VDDCORE should always be connected to VDDOUT. Figure 1-1 shows the standard power supply for the 49-pin WLCSP package. It is mandatory to guarantee a minimum of 3.0V on VDDIO if USB functionality is used. Otherwise VDDIO can be lowered down to 1.62V.

Figure 1-1. Power Supply Schematic Example for 49-pin WLCSP Package



Note:
1. These values are given only as a typical example.
2. Capacitors should be placed as close as possible to each pin in the signal group, vias should be avoided.
3. Decoupling capacitors must be connected as close as possible to the microcontroller and on each concerned pin.



The checklist, Table 1-1, must be followed in order to ensure correct hardware configuration for power supply.

Table 1-1. Single Power Supply Checklist

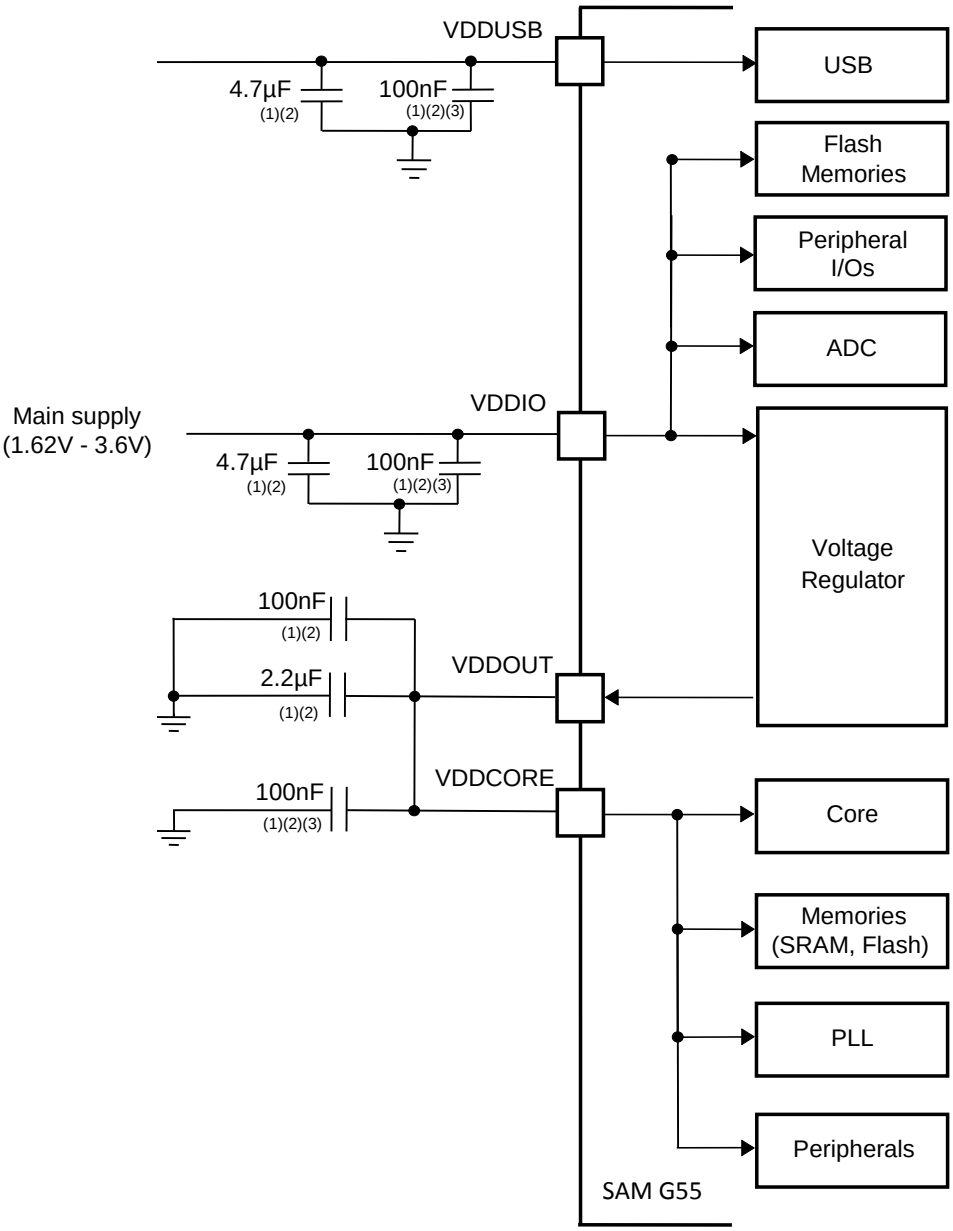
☑	Signal name	Recommended pin connection	Description
	VDDIO	**3.0 to 3.6V if USB is used** 1.62V to 3.6V otherwise Decoupling/Filtering capacitors (100nF and 4.7µF)(1)(2)	Powers the peripheral I/Os, USB, Flash memory (dual rail), ADC, 32kHz crystal oscillator and oscillator pads. Decoupling/Filtering capacitors must be added to improve start-up stability and reduce source voltage drop.
	VDDOUT	Decoupling/filtering capacitor (100nF and 2.2µF)(1)(2)	1.2V output of the main voltage regulator. Decoupling/Filtering capacitors must be added to guarantee stability.
	VDDCORE	Must be connected directly to VDDOUT pin. Decoupling/filtering capacitor (100nF)(1)(2)	Powers the Core, the embedded memories (SRAM, Flash), the PLL and integrated peripherals.
	GND	Ground	Ground pins GND are common to VDDIO and VDDCORE

Note: 1. These values are given only as a typical example.
2. Capacitors should be placed as close as possible to each pin in the signal group, vias should be avoided.

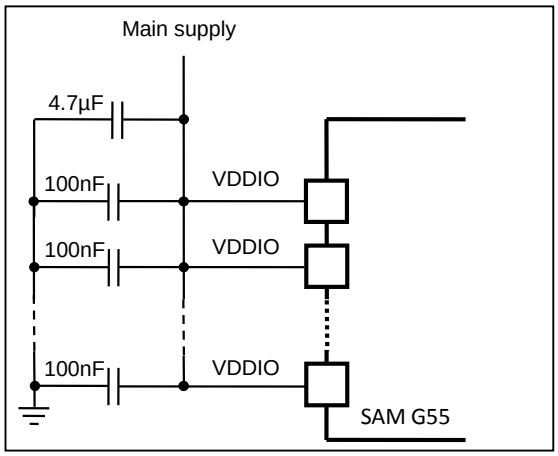
1.1.2 64-pin LQFP/LQFN Packages

The 64-pin packages have VDDUSB pin which needs to be powered independently if USB functionality is required. If not, VDDUSB can be directly connected to the Main Supply. VDDCORE should always be connected to VDDOUT. Figure 1-2 shows the standard power supply for the 64-pin LQFP/LQFN packages.

Figure 1-2. Power Supply Schematic Example for 64-pin LQFP/LQFN Packages



Note:
1. These values are given only as a typical example.
2. Capacitors should be placed as close as possible to each pin in the signal group, vias should be avoided.
3. Decoupling capacitors must be connected as close as possible to the microcontroller and on each concerned pin.



The checklist, Table 1-2, must be followed in order to ensure correct hardware configuration for power supply.

Table 1-2. Single Power Supply Checklist

☑	Signal name	Recommended pin connection	Description
	VDDIO	1.62V to 3.6V Decoupling/Filtering capacitors (100nF and 4.7µF)(1)(2)	Powers the peripheral I/Os, Flash memory (dual rail), ADC, 32kHz crystal oscillator and oscillator pads. Decoupling/Filtering capacitors must be added to improve start-up stability and reduce source voltage drop.
	VDDUSB	3.0V to 3.6V If USB is not used, VDDUSB can be connected to Main Supply. Decoupling/Filtering capacitors (100nF and 4.7µF)(1)(2)	Powers USB cells. Decoupling/Filtering capacitors must be added to improve start-up stability and reduce source voltage drop.
	VDDOUT	Decoupling/filtering capacitor (100nF and 2.2µF)(1)(2)	1.2V output of the main voltage regulator. Decoupling/Filtering capacitors must be added to guarantee stability.
	VDDCORE	Must be connected directly to VDDOUT pin. Decoupling/filtering capacitor (100nF)(1)(2)	Powers the Core, the embedded memories (SRAM, Flash), the PLL, and integrated peripherals.
	GND	Ground	Ground pins GND are common to VDDIO and VDDCORE

Note: 1. These values are given only as a typical example.
2. Capacitors should be placed as close as possible to each pin in the signal group, vias should be avoided.

1.2 Clocks and Oscillators Configuration

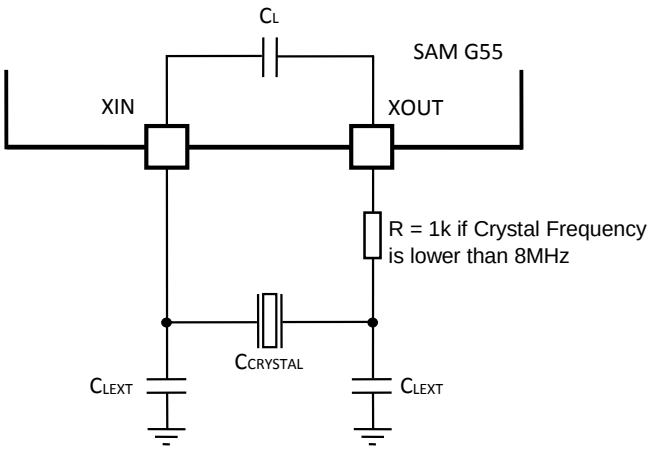
There are three possible configurations for Main and 32kHz clocks:

- Oscillator in Normal Mode
- Oscillator in Bypass
- Internal RC Oscillator

1.2.1 Main Clock/Oscillators

Figure 1-3 shows a standard main crystal hardware implementation.

Figure 1-3. Main Crystal Schematic Example



The checklist, Table 1-3, must be followed in order to ensure correct hardware configuration for main Clock/Oscillators.

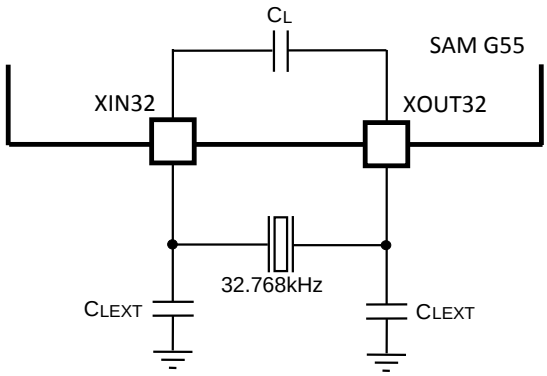
Table 1-3. Main Clock, Oscillators Checklist

☑	Signal name	Recommended pin connection	Description
	PB9/XIN PB8/XOUT **Main Oscillator in Normal Mode**	Crystals between 3 and 20MHz Capacitors on XIN and XOUT (crystal load capacitance dependent) 1kΩ resistor on XOUT only required for crystals with frequencies lower than 8MHz.	Internal Equivalent Load Capacitance (C_L = 12.5pF to 17.5pF): Crystal Load Capacitance, ESR, Drive Level, and Shunt Capacitance to validate. The external load capacitance is calculated with the following formula: $C_{LEXT}=2\ (C_{crystal}-C_L-C_{PCB})$ Refer to the *Crystal Oscillators Design Consideration Information* section of the SAM G5x Series Datasheet. **By default, at start-up the chip runs out of the Master Clock using the fast RC oscillator running at 8MHz.**
	PB9/XIN PB8/XOUT **Main Oscillator in Bypass Mode**	PB9/XIN: external clock source PB8/XOUT: can be left unconnected or used as GPIO.	1.62V to 3.6V Square wave signal (V_{DDIO}) External Clock Source up to 50MHz Duty Cycle: 40 to 60% **By default, at start-up the chip runs out of the Master Clock using the fast RC oscillator running at 8MHz.**
	8/16/24MHz **Fast Internal RC Oscillator**	PB9/XIN and PB8/XOUT: can be left unconnected or used as GPIO	Powered up by V_{DDIO} The output frequency is configurable through the PMC registers. The Fast RC oscillator is calibrated in production. The frequency can be trimmed by software. Duty Cycle: 40 to 60% **By default, at start-up the chip runs out of the Master Clock using the fast RC oscillator running at 8MHz.**

1.2.2 32kHz Clock/Oscillators

Figure 1-4 shows a standard 32kHz crystal hardware implementation.

Figure 1-4. 32kHz Crystal Schematic Example



The checklist, Table 1-4, must be followed in order to ensure correct hardware configuration for 32kHz Clock/Oscillator.

Table 1-4. 32kHz Clock, Oscillators Checklist

☑	Signal name	Recommended pin connection	Description
	PA7/XIN32 PA8/XOUT32 **32kHz crystal used**	32.768kHz Crystal Capacitors on XIN32 and XOUT32 (crystal load capacitance dependent).	Internal parasitic capacitance C_{para}=0.5pF (typ.) Crystal Load Capacitance, ESR, Drive Level and Shunt Capacitance to validate. C_{LEXT}max=24pF C_{LEXT}= 2x($C_{crystal}$-C_{para}- C_{pcb}) Refer to the *Crystal Oscillators Design Consideration Information* section of the SAM G5x Series Datasheet. **By default, at start-up the chip runs out of the embedded 32kHz RC oscillator**
	PA7/XIN32 PA8/XOUT32 **32kHz oscillator in bypass mode**	PA7/XIN32: external clock source PA8/XOUT32: can be left unconnected or use as GPIO.	1.62V to 3.6V Square wave signal (V_{DDIO}) External Clock Source up to 50MHz Duty Cycle: 40 to 60% **By default, at start-up the chip runs out of the Master Clock using the fast RC oscillator running at 8MHz.**

1.3 Serial Wire and JTAG

Figure 1-5, Figure 1-6, Figure 1-7, and Figure 1-8 show a standard JTAG/SWD hardware implementation with 10-pin Cortex-M connector and 20-pin connector. It is recommended to establish accessibility to a JTAG/SWD connector for debug in any case.

Figure 1-5. JTAG Schematic Example: 10-pin Cortex-M Connector

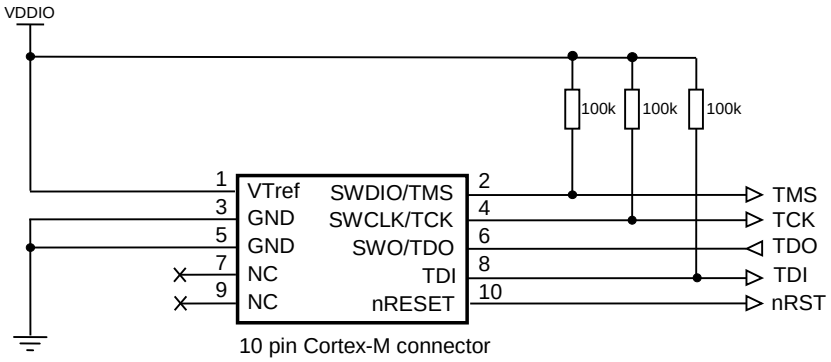


Figure 1-6. JTAG Schematic Example: JTAG 20-pin Connector

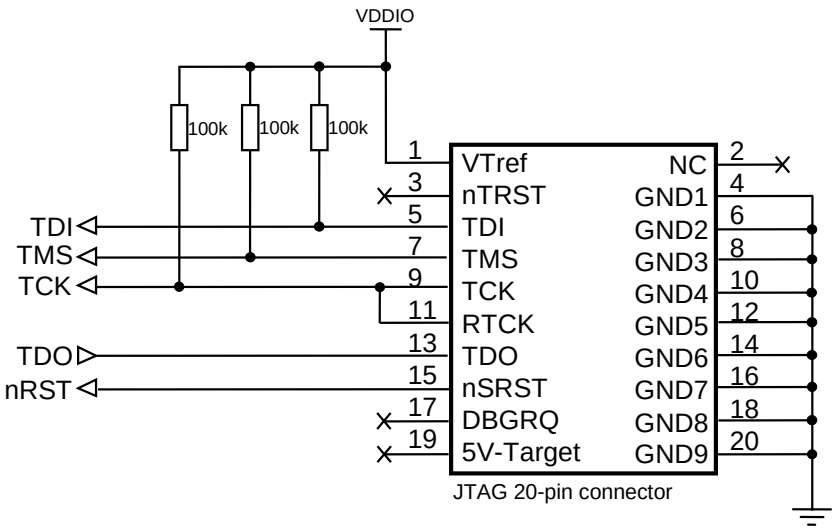


Figure 1-7. SWD Schematic Example: 10-pin Cortex-M Connector

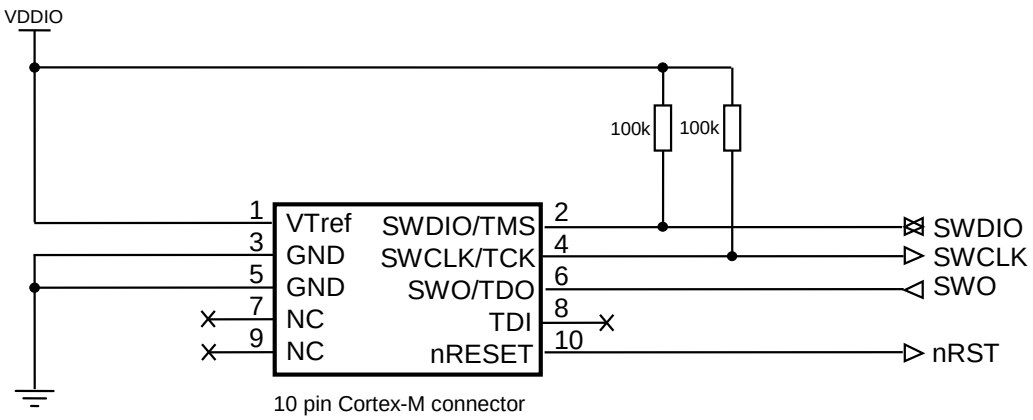
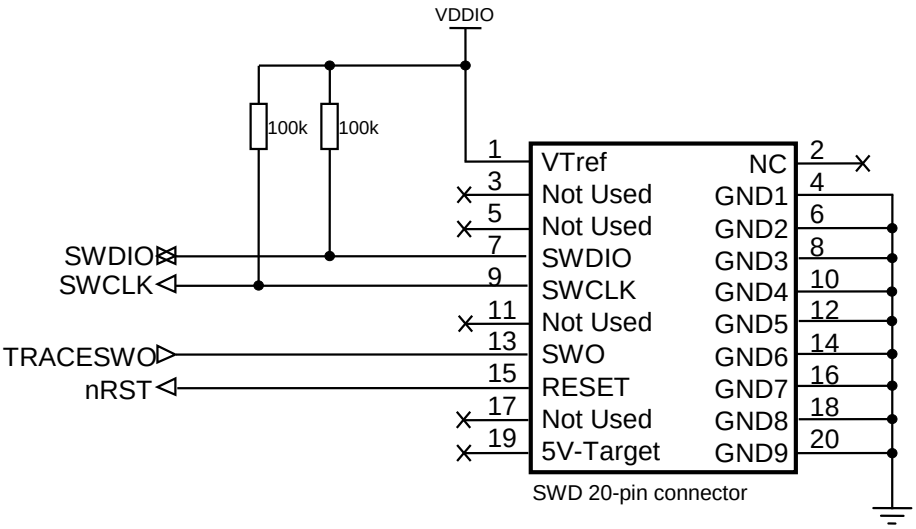


Figure 1-8. SWD Schematic Example: SWD 20-pin Connector



The checklist, Table 1-5, must be followed in order to ensure correct hardware configuration for JTAG/SWD.

Table 1-5. Serial Wire and JTAG Checklist

☑	Signal name	Recommended pin connection	Description
	TCK/SWCLK/PB7	Application dependent. If debug mode is not required this pin can be use as GPIO.	Reset State: - SWJ-DP Mode - Internal pull-up disabled - Schmitt Trigger enabled
	TMS/SWDIO/PB6	Application dependent. If debug mode is not required this pin can be use as GPIO.	Reset state: - SWJ-DP Mode - Internal pull-up disabled - Schmitt Trigger enabled
	TDI/PB4	Application dependent. If debug mode is not required this pin can be use as GPIO.	Reset state: - SWJ-DP Mode - Internal pull-up disabled - Schmitt Trigger enabled
	TDO/TRAC-ESWO/PB5	Application dependent. If debug mode is not required this pin can be use as GPIO.	Reset state: - SWJ-DP Mode - Internal pull-up disabled - Schmitt Trigger enabled
	JTAGSEL	Application dependent. Must be tied to VDDIO to enter JTAG Boundary Scan. **In harsh environments, It is strongly recommended to tie this pin to GND.**	Permanent Internal pull-down resistor (15kΩ)

1.4 Flash Memory

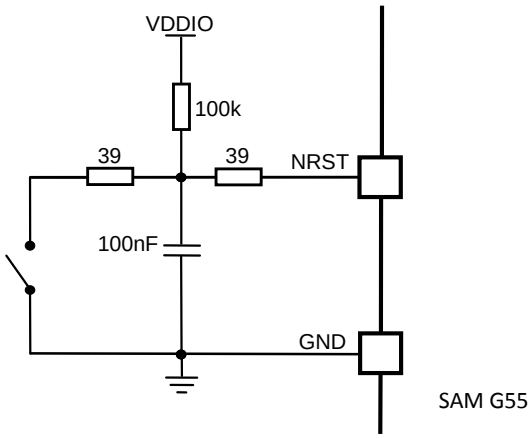
☑	Signal name	Recommended pin connection	Description
	ERASE/PB12	Application dependent. If hardware erase is not required this pin can be use as GPIO.	Internal pull-down resistor (15kΩ). Must be tied to VDDIO to erase the General Purpose NVM bits (GPNVMx), the whole Flash content and the security bit. Reset state: Erase Input, with a 15kΩ Internal pull down and Schmitt trigger enabled

Note: The minimum erase pin assertion for erase effectiveness is 200ms.

1.5 Reset and Test Pins

Figure 1-9, shows a standard reset hardware implementation.

Figure 1-9. Reset Hardware Implementation



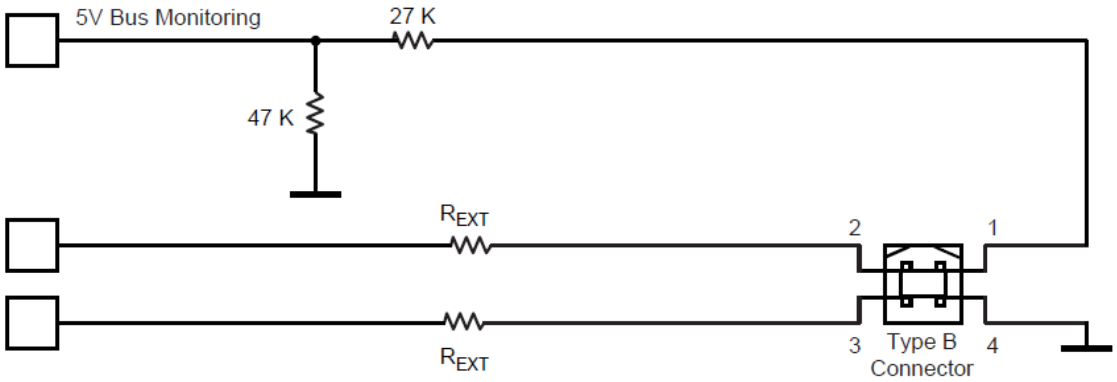
☑	Signal name	Recommended pin connection	Description
	NRST	Application dependent. Can be connected to a push button for hardware reset.	By default, the NRST pin is configured as an input Permanent internal pull-up resistor to VDDIO. NRST pin is also used to enter in bootloader mode if toggled according to a specific sequence (see the Bootloader section)
	TST	TST pin can be left unconnected in normal mode. **In harsh environments, It is strongly recommended to tie this pin to GND.**	Permanent internal pull-down resistor (15kΩ).

1.6 USB

1.6.1 USB Device Port

Figure 1-10 shows a typical USB device port hardware implementation. VBUS monitoring is done using a standard PIO with internal pull-up disabled.

Figure 1-10. USB Device Typical Implementation

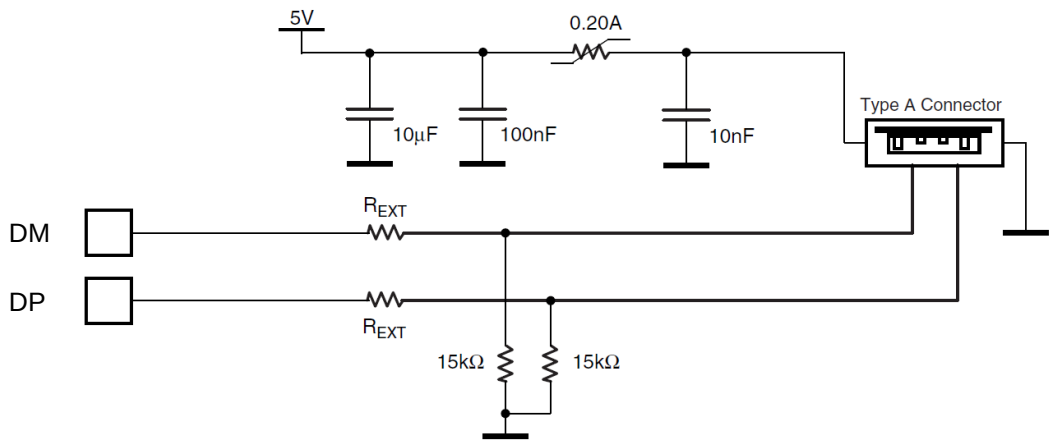


☑	Signal name	Recommended pin connection	Description
	DM/PA21	Application dependent (see figure above) If USB device support is not required this pin can be use as GPIO.	Reset State: - USB Mode - Internal Pull-down
	DP/PA22	Application dependent (see figure above) If USB device support is not required this pin can be use as GPIO.	Reset State: - USB Mode - Internal Pull-down

1.6.2 USB Host Port

Figure 1-11 shows a typical USB host port hardware implementation.

Figure 1-11. USB Host Typical Implementation



☑	Signal name	Recommended pin connection	Description
	DM/PA21	Application dependent (see above figure) In USB Host mode, an external pull-down is required. If USB host support is not required this pin can be use as GPIO.	Reset State: - USB Mode - Internal Pull-down
	DP/PA22	Application dependent (see above figure) In USB Host mode, an external pull-down is required. If USB host support is not required this pin can be use as GPIO.	Reset State: - USB Mode - Internal Pull-down

1.7 PIOs

☑	Signal name	Recommended pin connection	Description
	PAx – PBx	Application dependent (Pulled-up on V_{DDIO})	At reset, all PIOs are in IO or System IO mode with Schmitt trigger inputs and internal pull-up enabled. To reduce power consumption, if not used, the concerned PIO can be configured as an output and driven at '0' with internal pull-up disabled.

1.8 Bootloader

The SAM G55 embeds a bootloader in ROM memory. The table below gives the pins driven by the bootloader.

☑	Signal name	Recommended pin connection	Description
	NRST	Application dependent	Bootloader entry line / Reset Line
	NCHG/PA01	Application dependent	Bootloader handshake
	TWD/PA03	Application dependent	TWI3 data line
	TWCK/PA04	Application dependent	TWI3 clock
	NPCS0/PA11	Application dependent	SPI chip select
	MISO/PA12	Application dependent	SPI master IN, slave OUT
	MOSI/PA13	Application dependent	SPI master OUT, slave IN
	SPCK/PA14	Application dependent	SPI clock

For more information on the bootloader, refer to the application note mentioned in Chapter 2 Suggested Reading.

2 Suggested Reading

2.1 Device Datasheet

The device datasheet contains block diagrams of the peripherals and details about implementing firmware for the device. It also contains the electrical specifications and expected characteristics of the device.

The datasheet is available on http://www.atmel.com/ in the Datasheets section of the product page.

2.2 Xplained Pro User Guide

The SAM G55 Xplained Pro user guide contains schematics that can be used as a starting point when designing with the SAM G55 devices. This user guide is available on http://www.atmel.com/ in the documents section of the SAM G55 Xplained Pro.

2.3 Bootloader

This application note describes how to use the SPI/TWI bootloader embedded in internal ROM, its entry sequence, and how to use the available tool coming with this application note (firmware file generator).

The application note is available on http://www.atmel.com/ in the Application Note section of the product page (literature number is AT09002).

2.4 ARM Documentation on Cortex-M4 Core

- Cortex-M4 Devices Generic User Guide for revision r0p1
- Cortex-M4 Technical Reference Manual for revision r0p1

These documents are available at http://www.arm.com/ in the infocenter section.

3 Revision History

Doc Rev.	Date	Comments
42392C	04/2016	Section 1.5: removed reference to FFPI
42392B	09/2015	Section 1.8: TWI0 has been corrected to TWI3. Some typos fixed.
42392A	01/2015	Initial document release.

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