

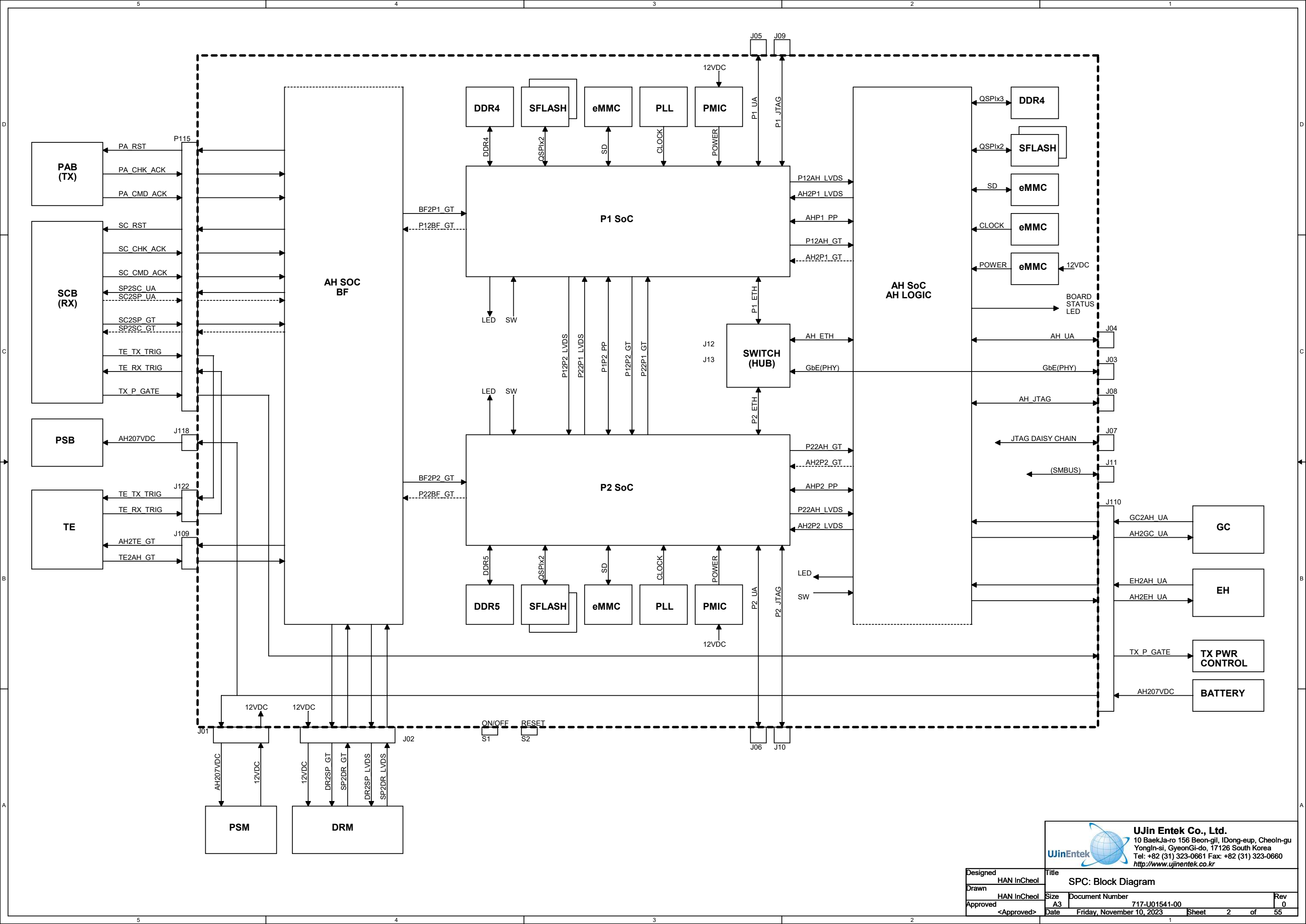
Blue Shark - II

신호처리보드


(Signal Processing Circuit)

Rev.	Date	Description	Page	Remark
0	2023.10.04	Initial design		16Layers, t=2.4

Todo





		UJin Entek Co., Ltd. 10 BaekJa-ro 156 Beon-gil, IDong-eup, Cheoln-gu YongIn-si, GyeonGi-do, 17126 South Korea Tel: +82 (31) 323-0661 Fax: +82 (31) 323-0660 http://www.ujinentek.co.kr	
Designed HAN InCheol		Title SPC: Block Diagram	
Drawn HAN InCheol		Size A3	Document Number 717-U01541-00
Approved <Approved>		Date Friday, November 10, 2023	Rev 0
		Sheet 3	of 55

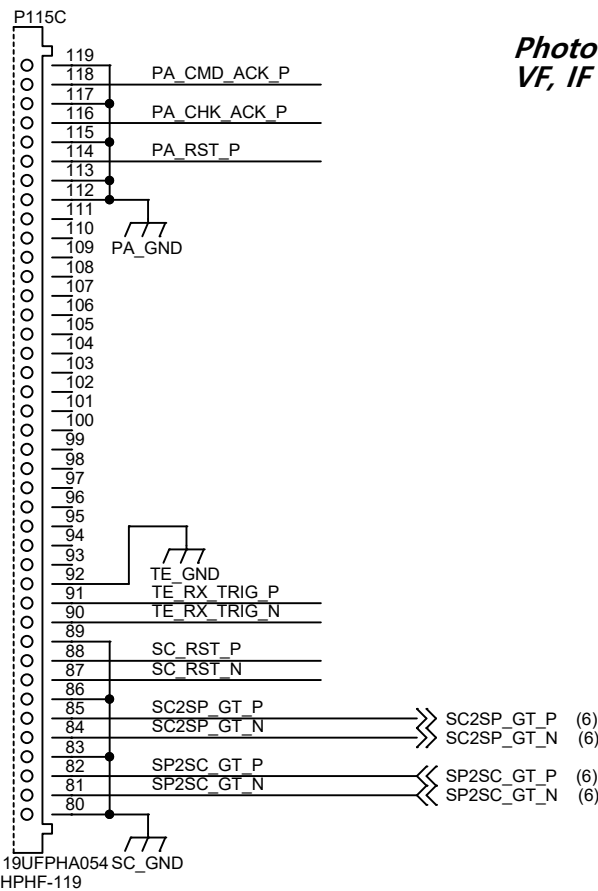
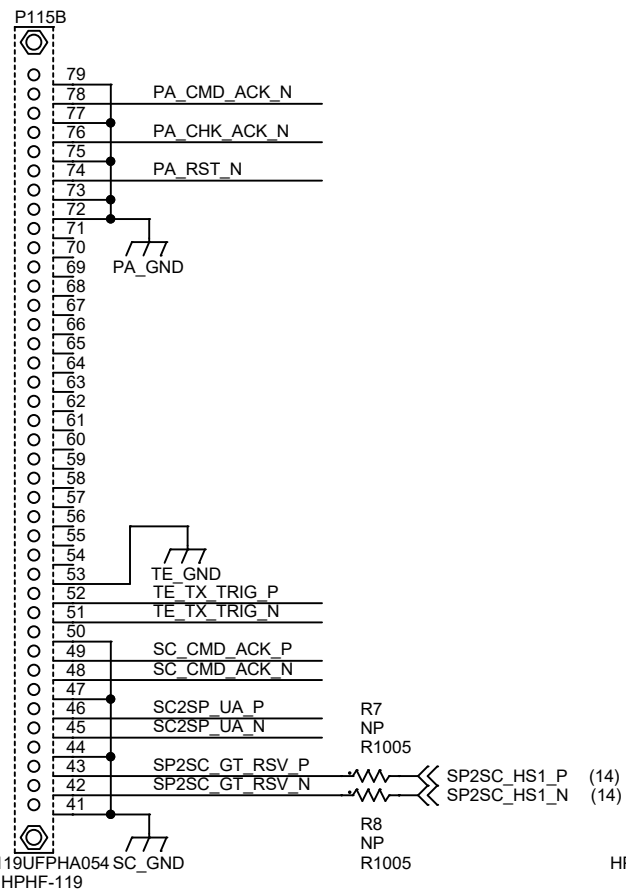
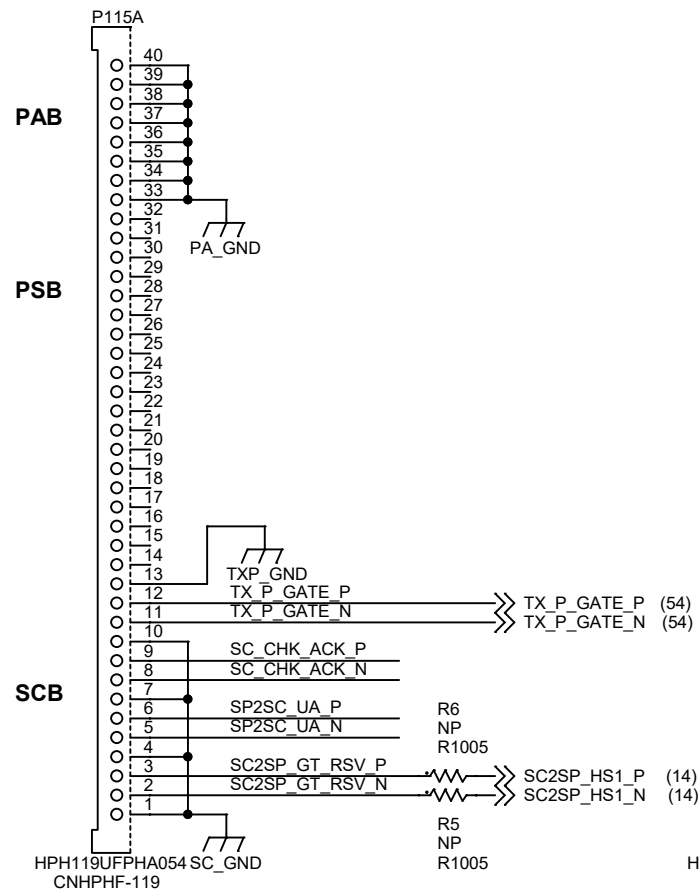
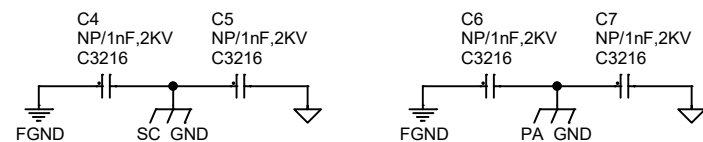
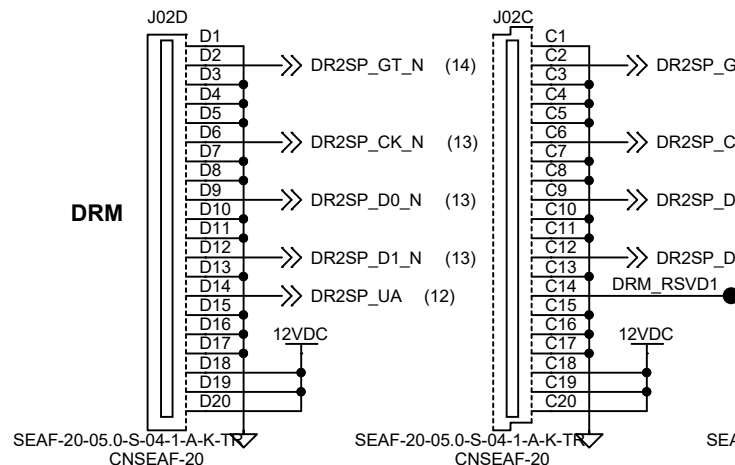
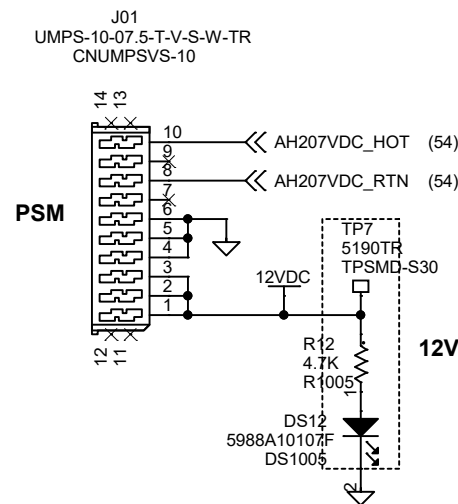
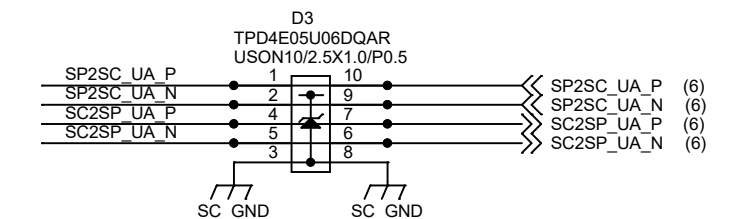
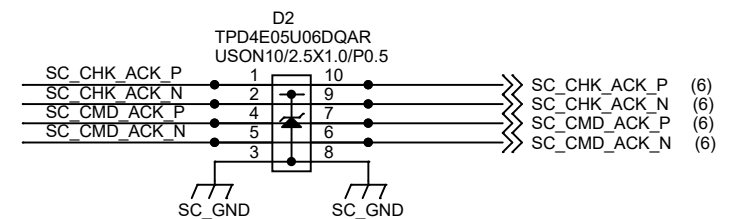
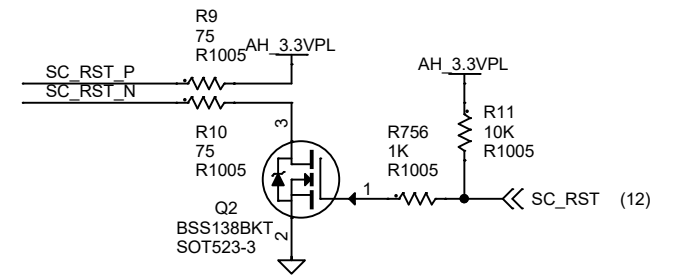
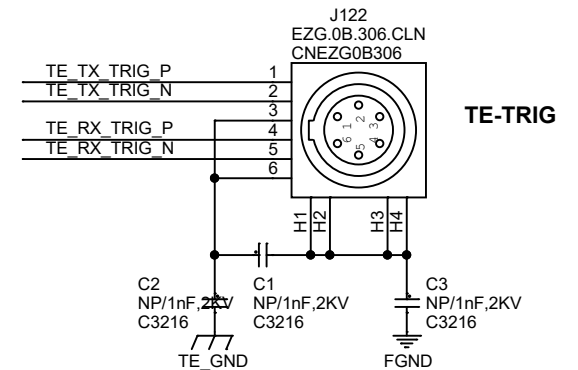
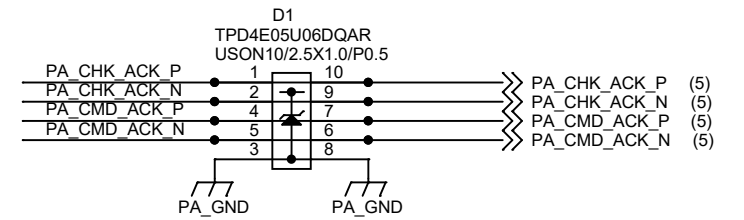
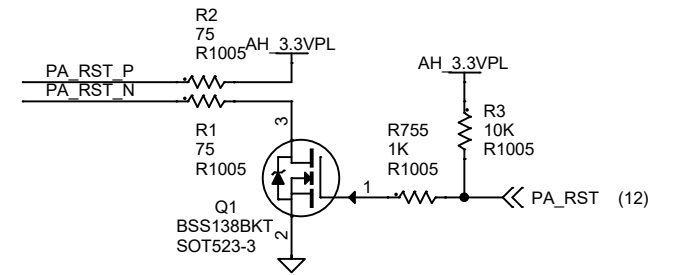
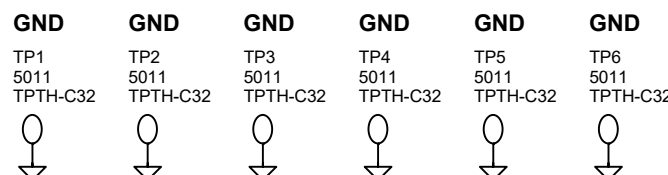
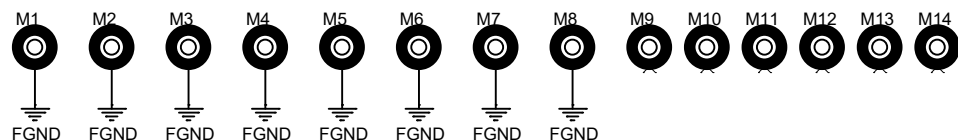


Photo coupler의
VF, IF 확인 필요

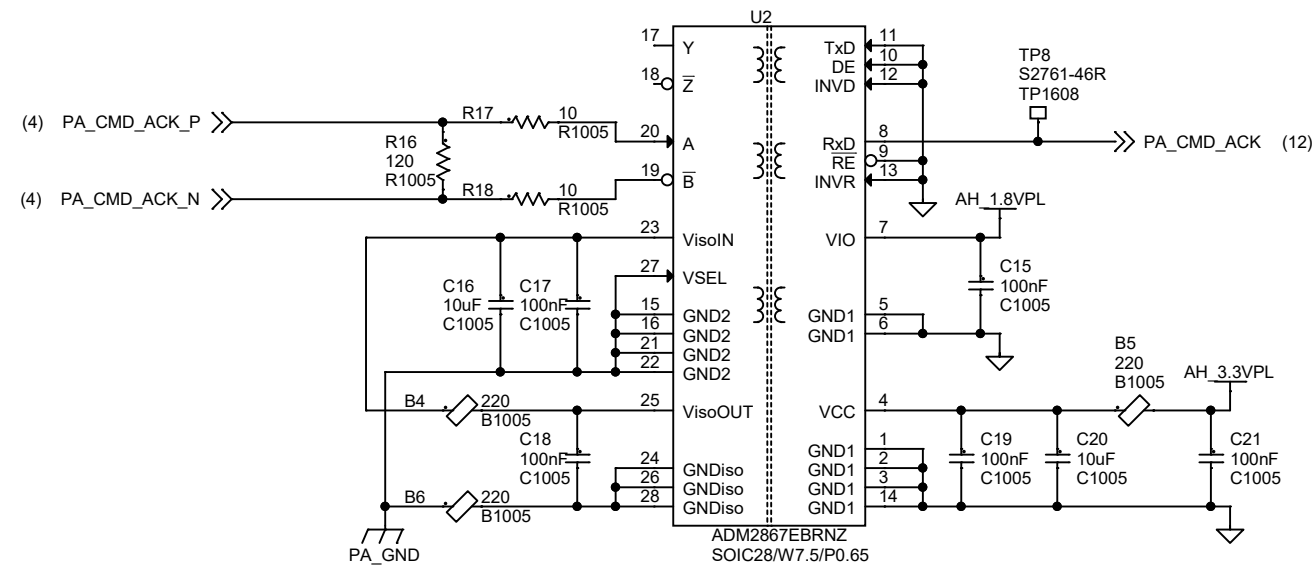
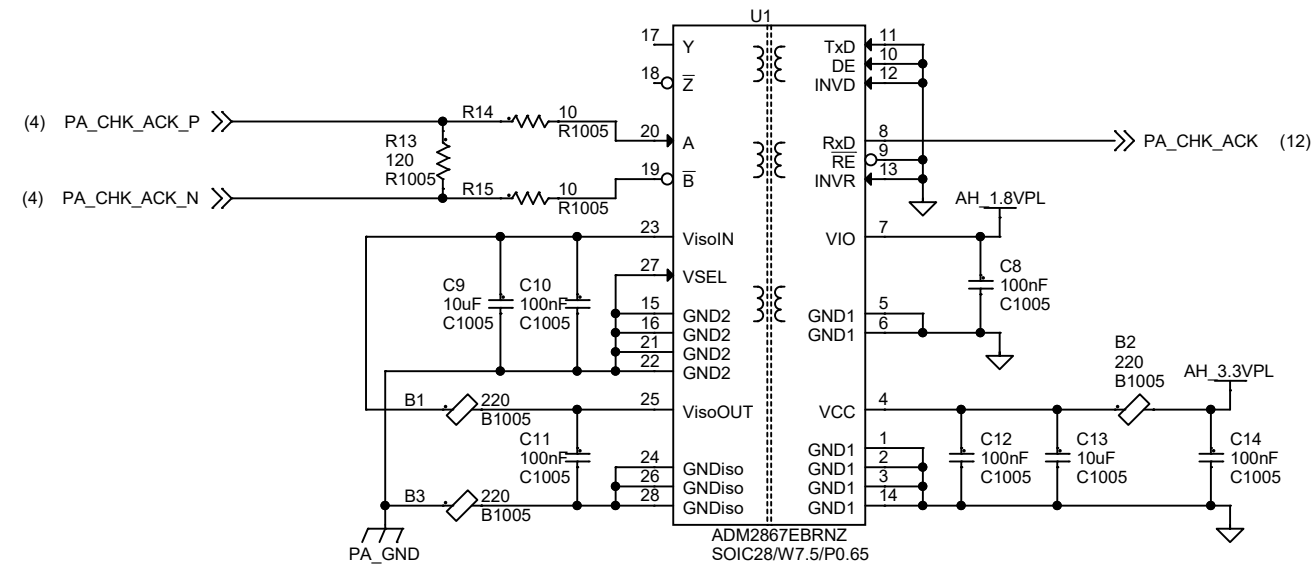


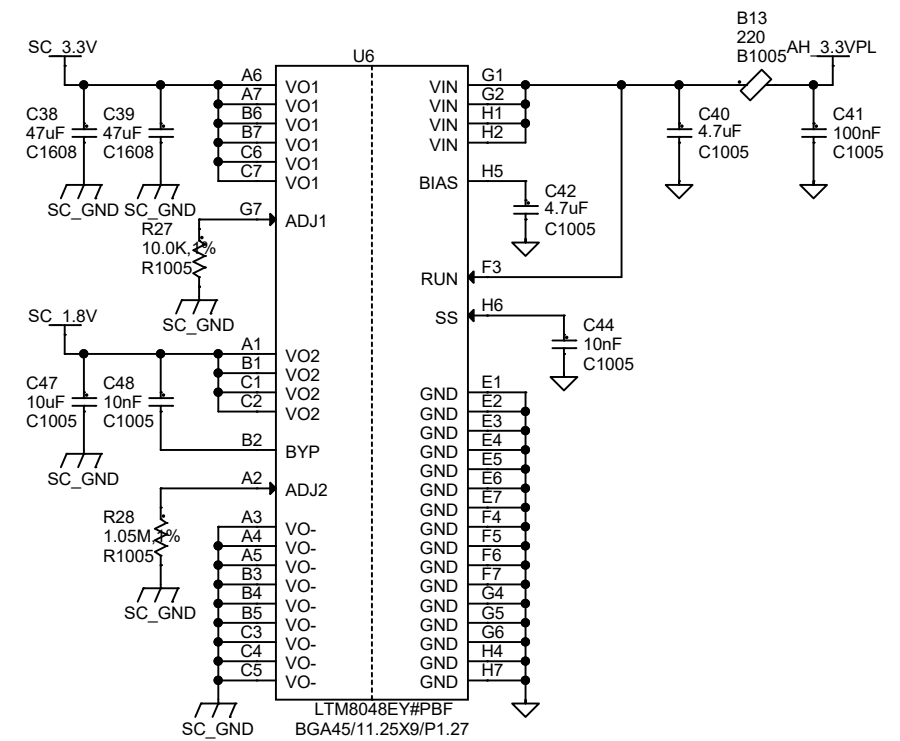
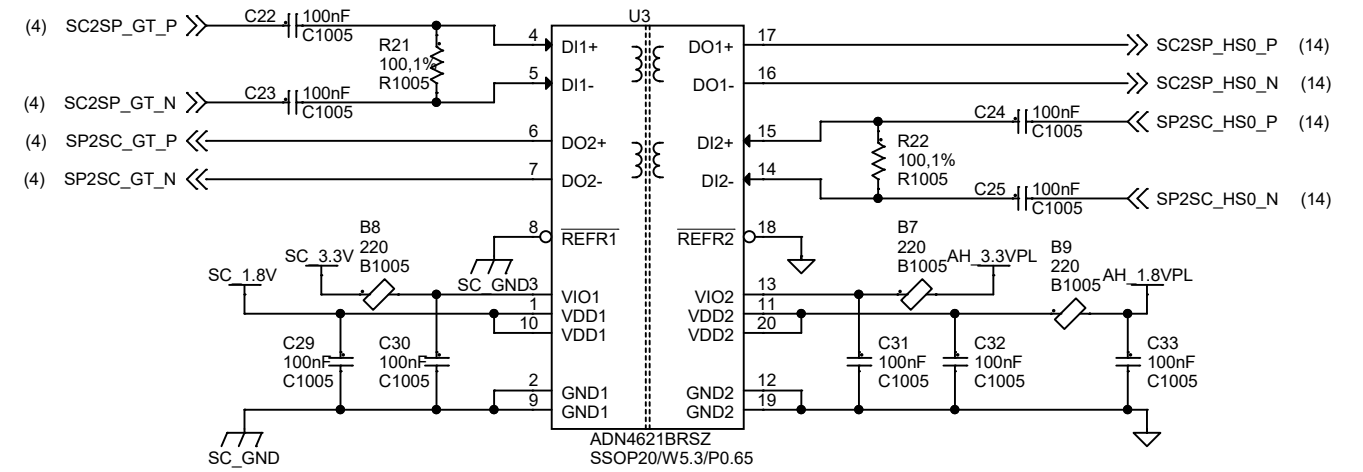
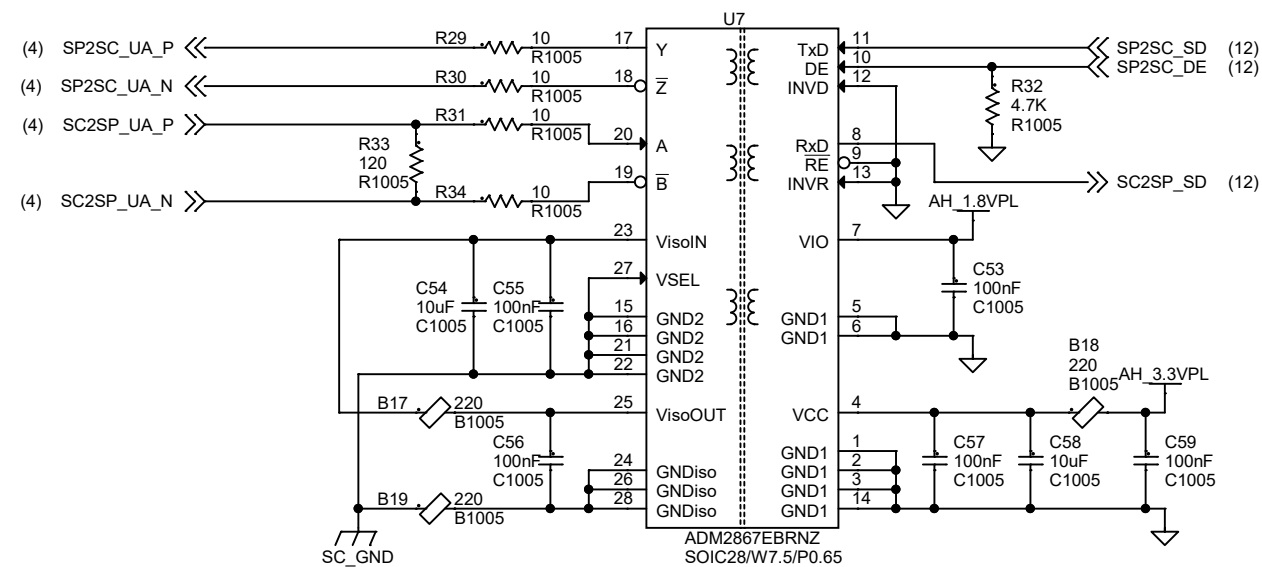
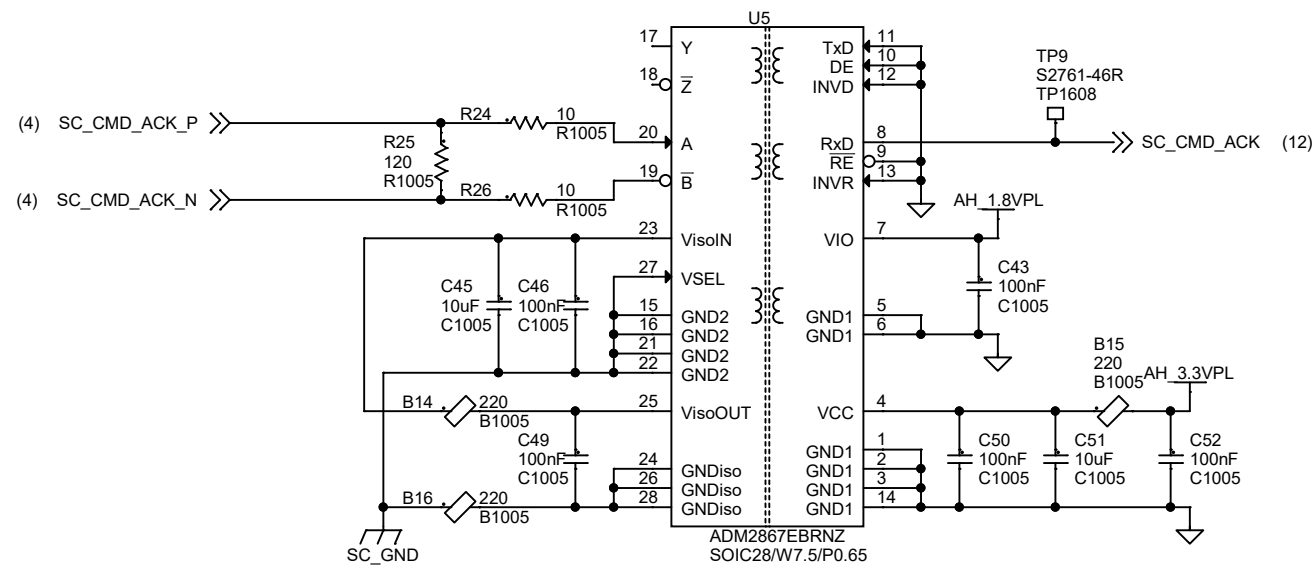
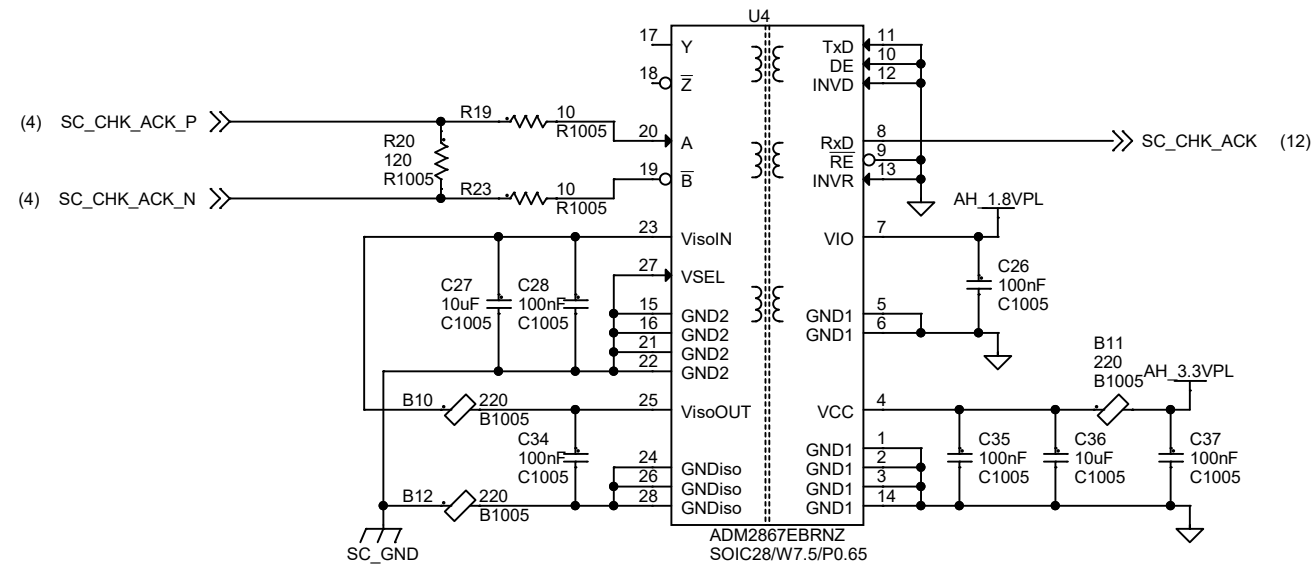
모두 NTH로 수정



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Designed	HAN InCheol	Title	SPC: PAB & SCB Interface
Drawn	HAN InCheol	Size	A3
Approved	<Approved>	Document Number	717-U01541-00
		Date	Friday, November 10, 2023
		Sheet	4 of 55
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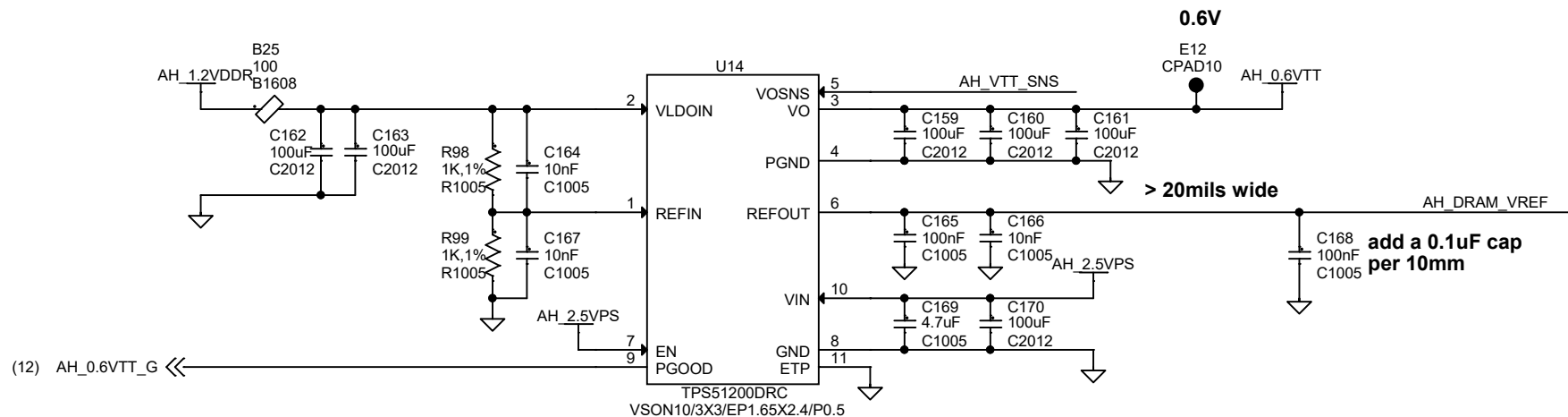
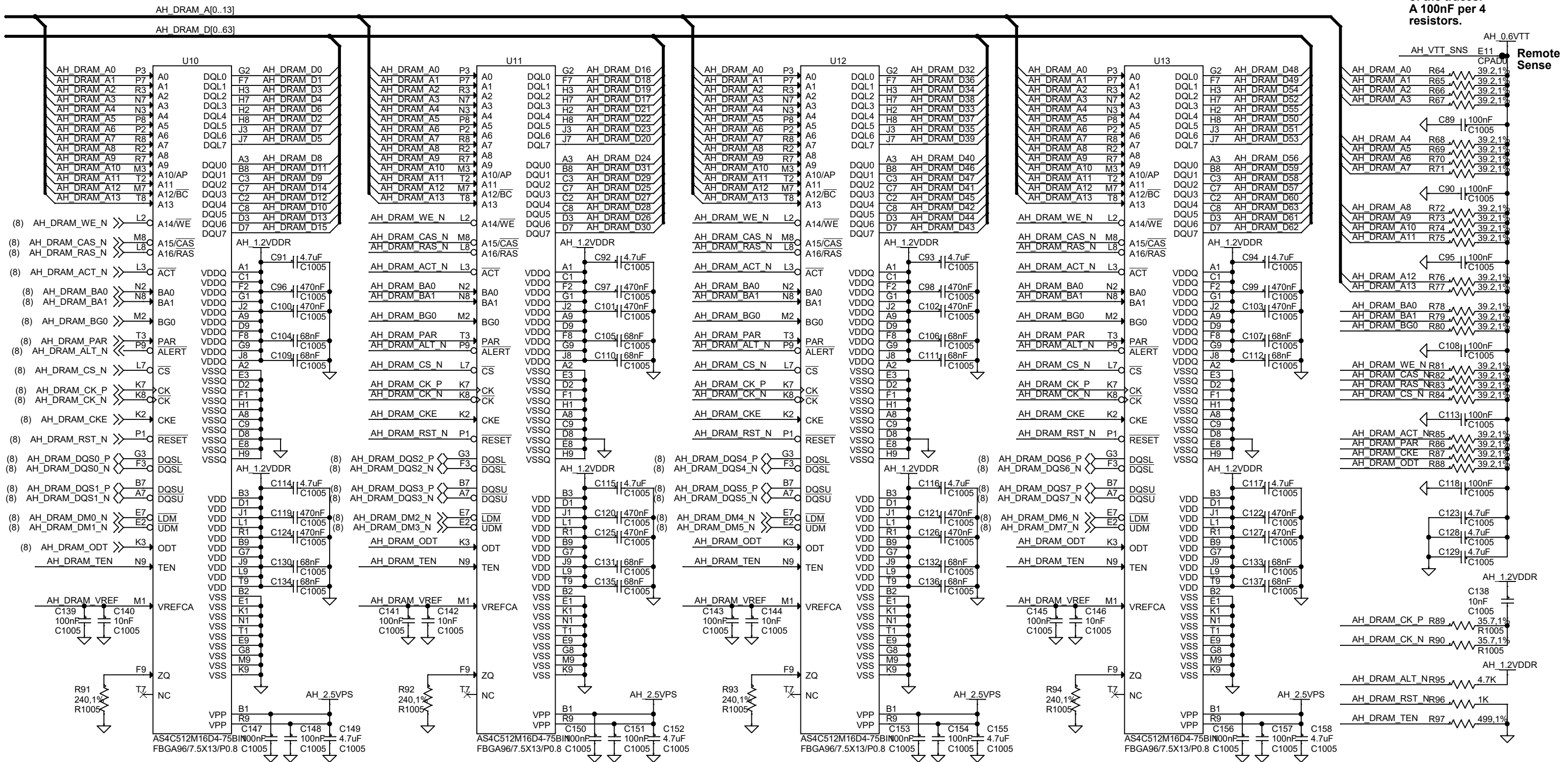


(8) AH_DRAM_A[0..13] >> AH_DRAM_A[0..13]
(8) AH_DRAM_D[0..63] << AH_DRAM_D[0..63]

Fly-by topology

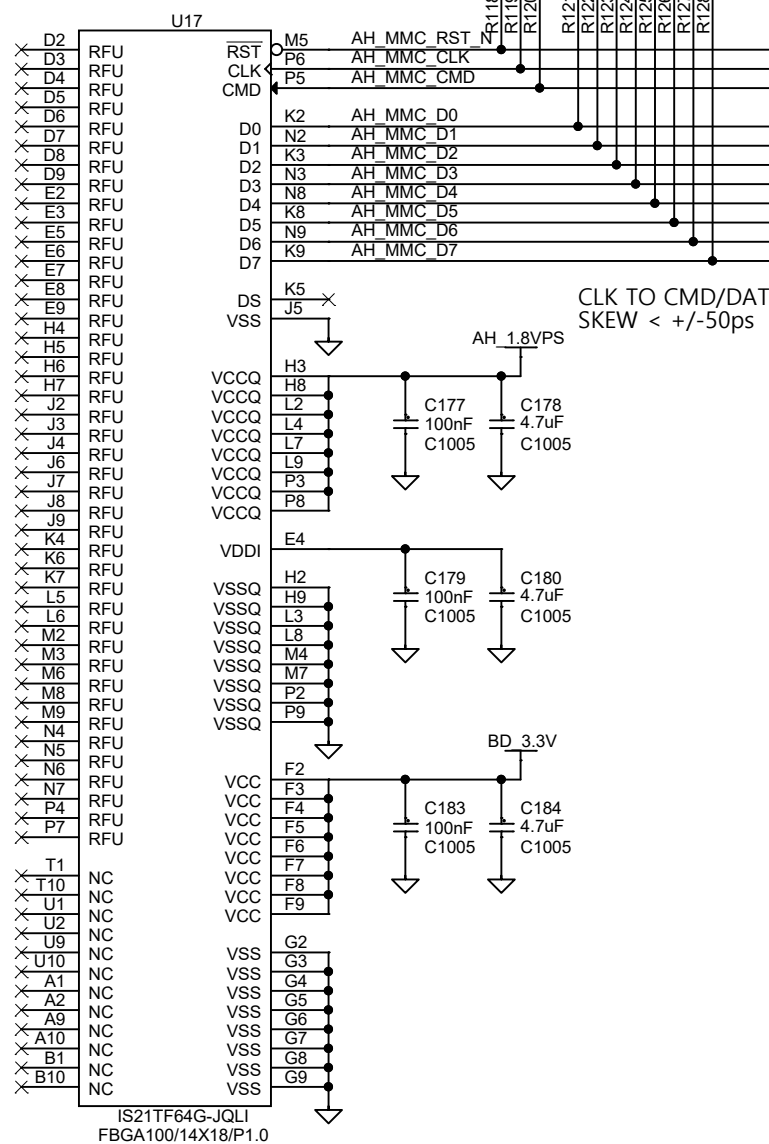
<----- < 0.5" ----->

Place at the end of the traces.
A 100nF per 4 resistors.



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Drawn	HAN InChool	Size	A3
Approved	<Approved>	Document Number	717-U01541-00
		Date	Thursday, November 16, 2023
		Sheet	9 of 55
		Rev	0

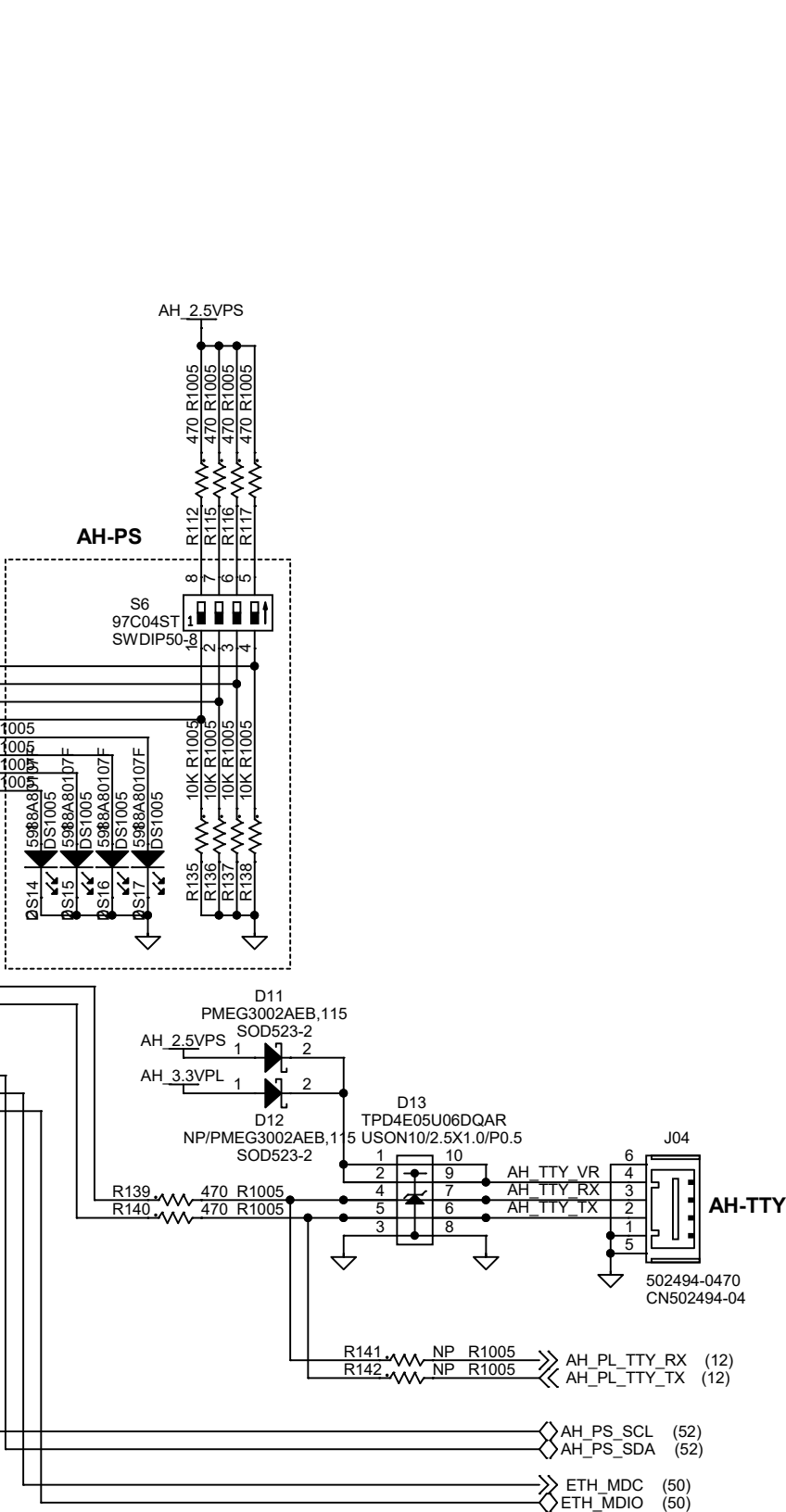
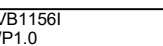
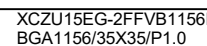


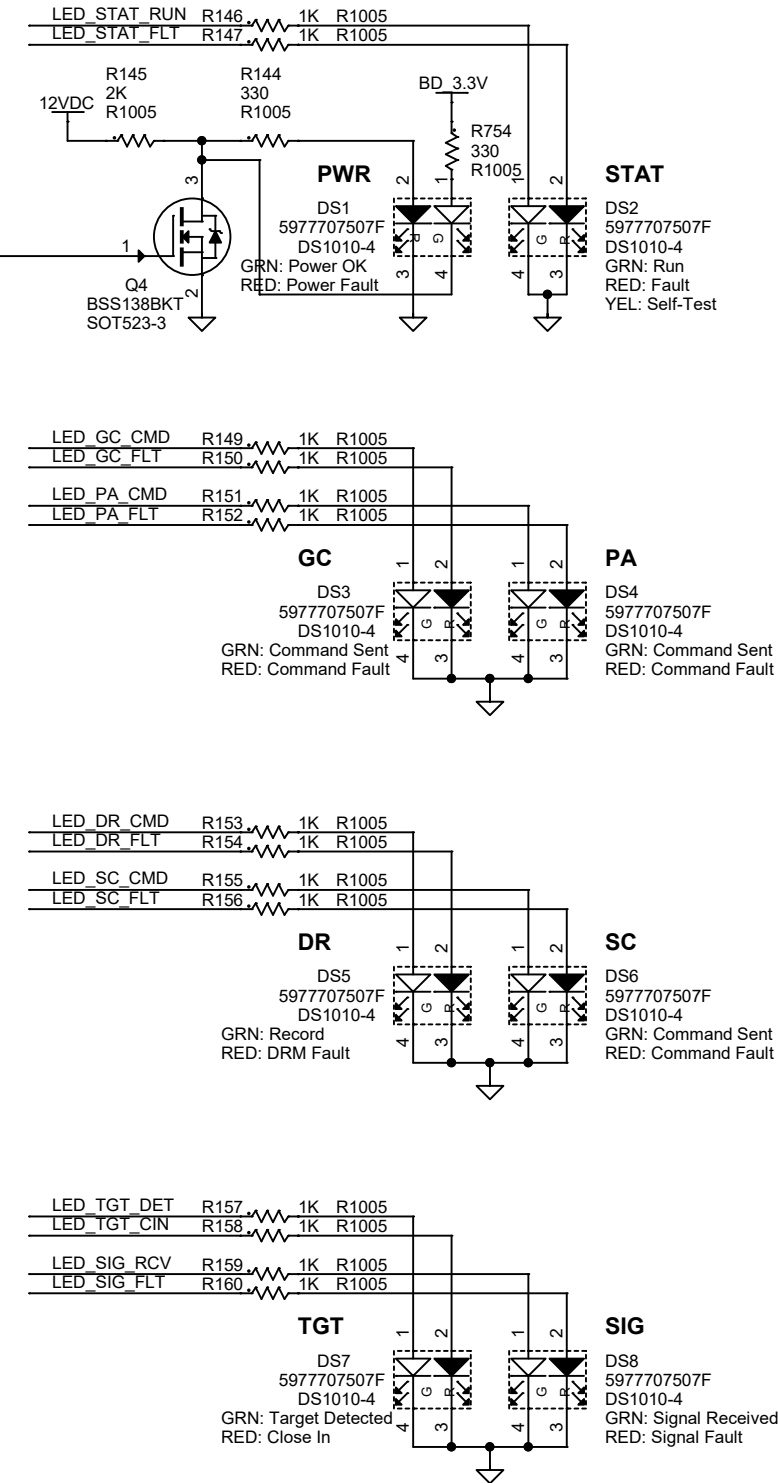
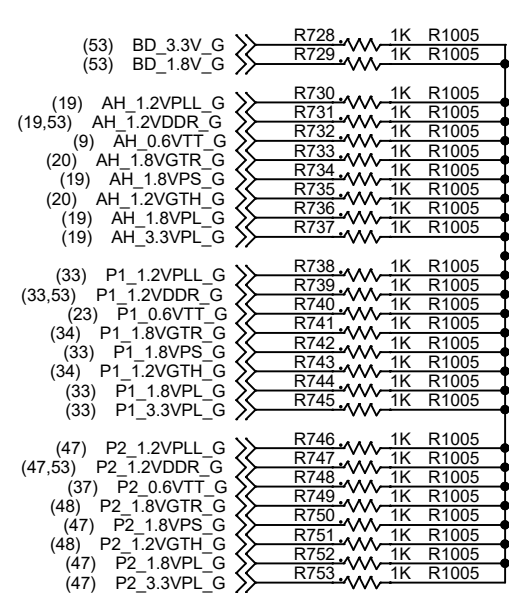
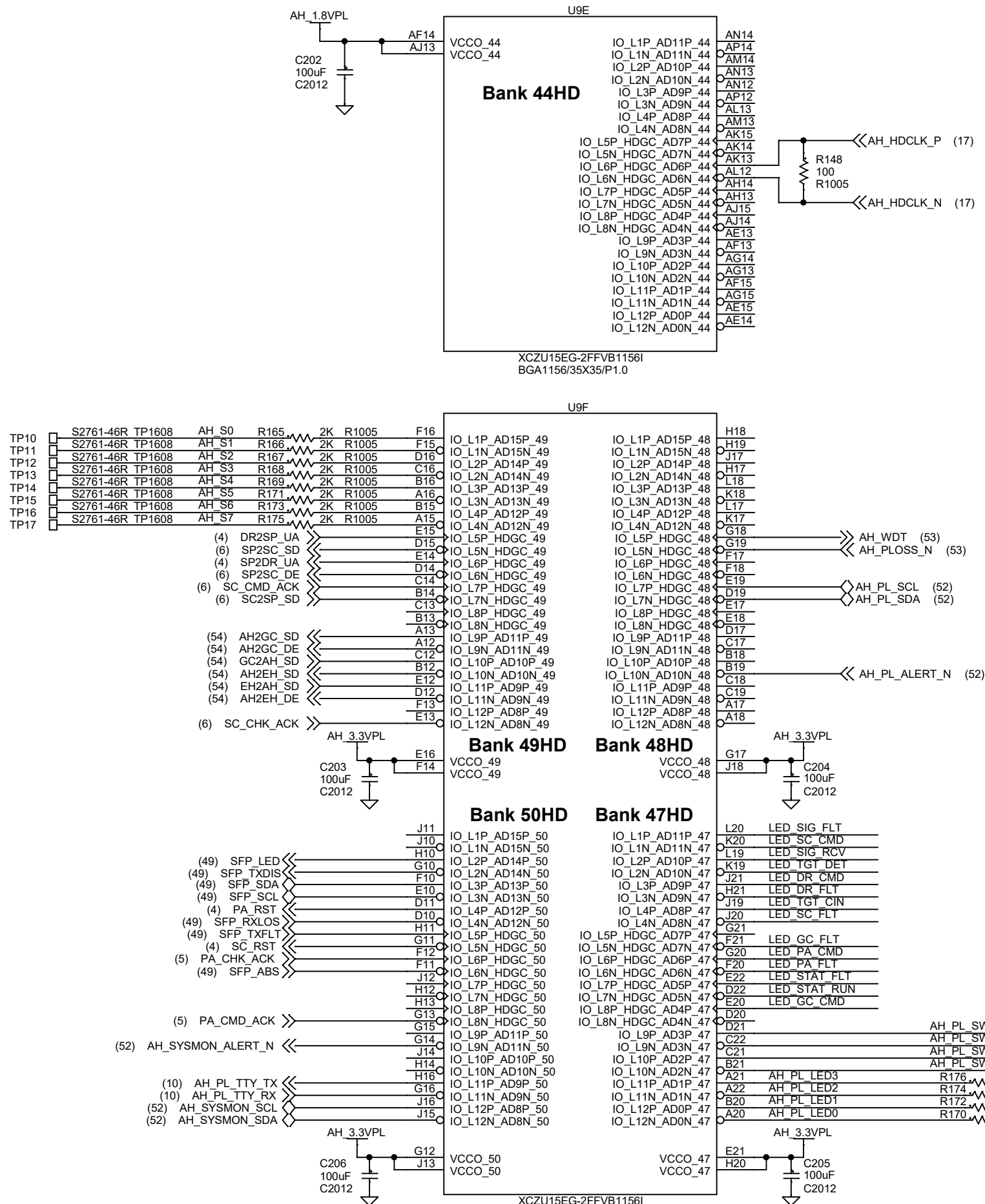
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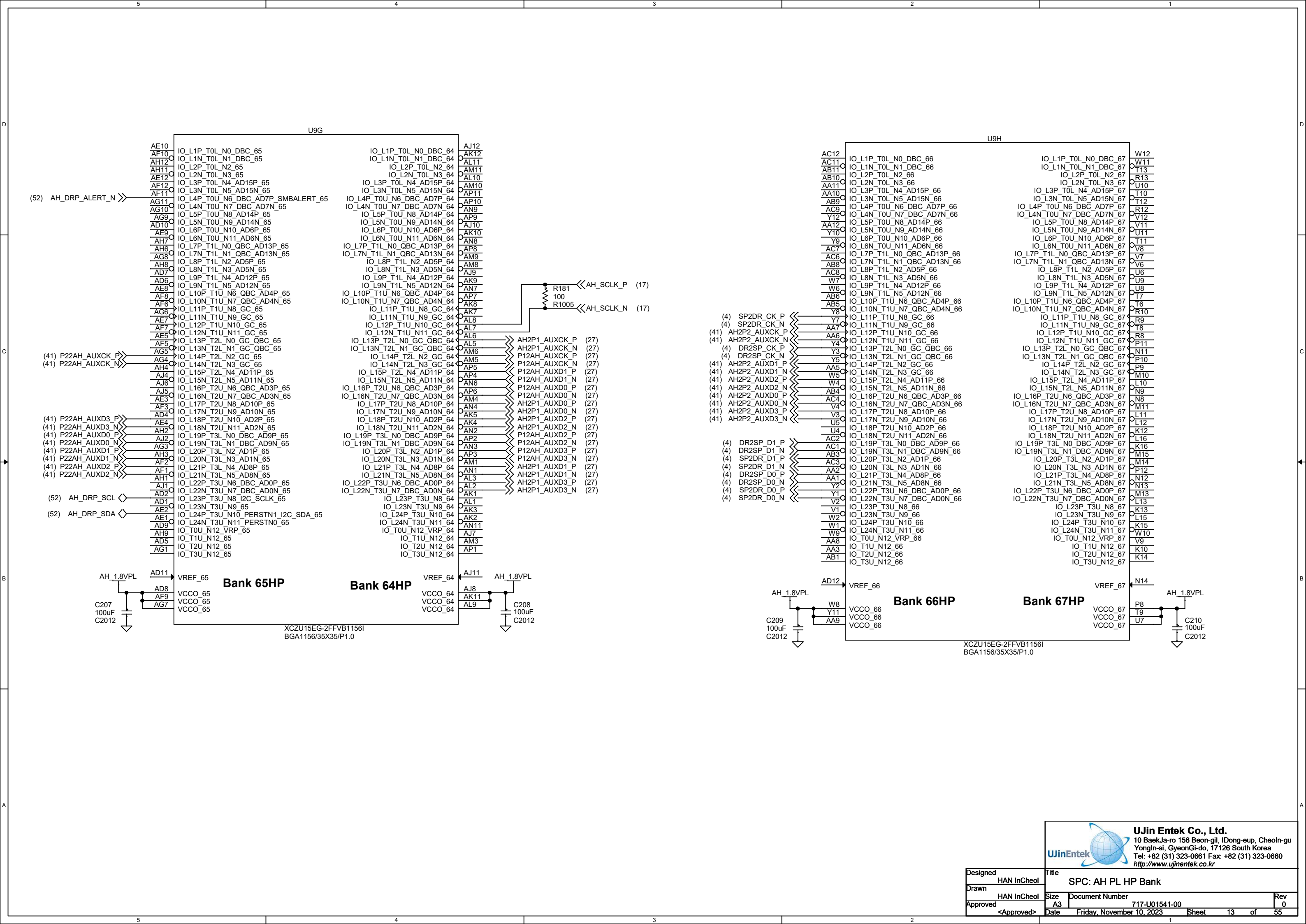
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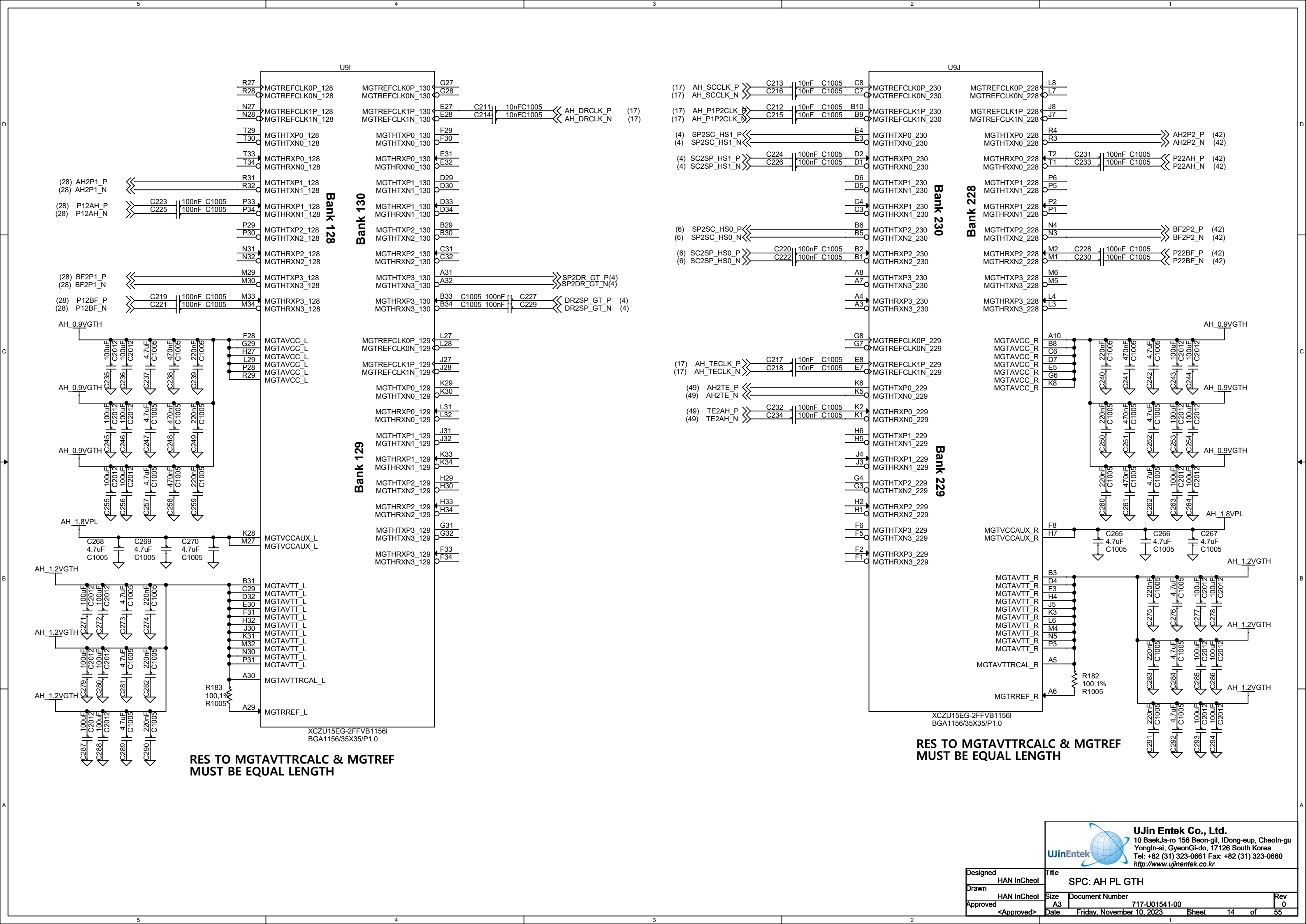
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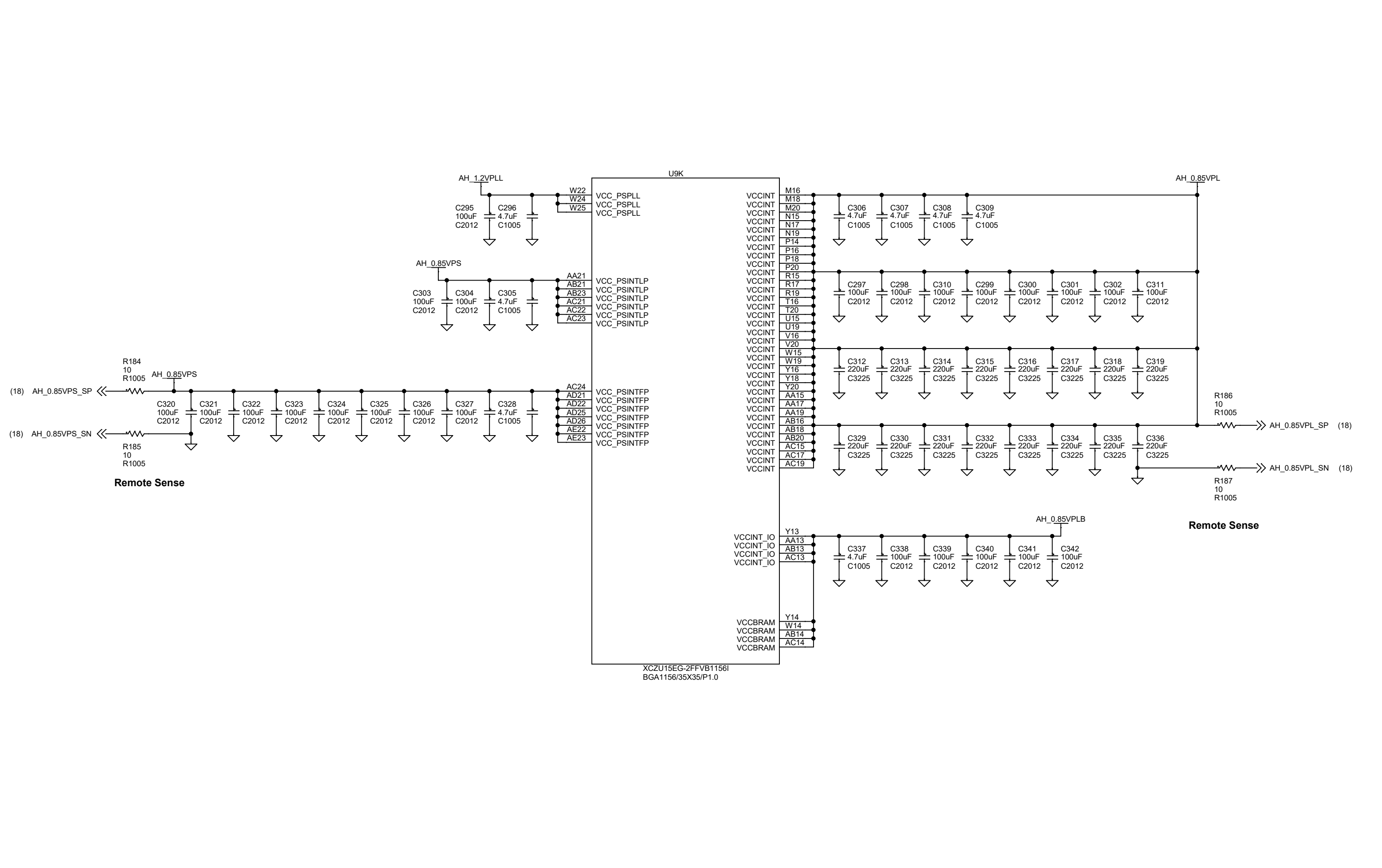
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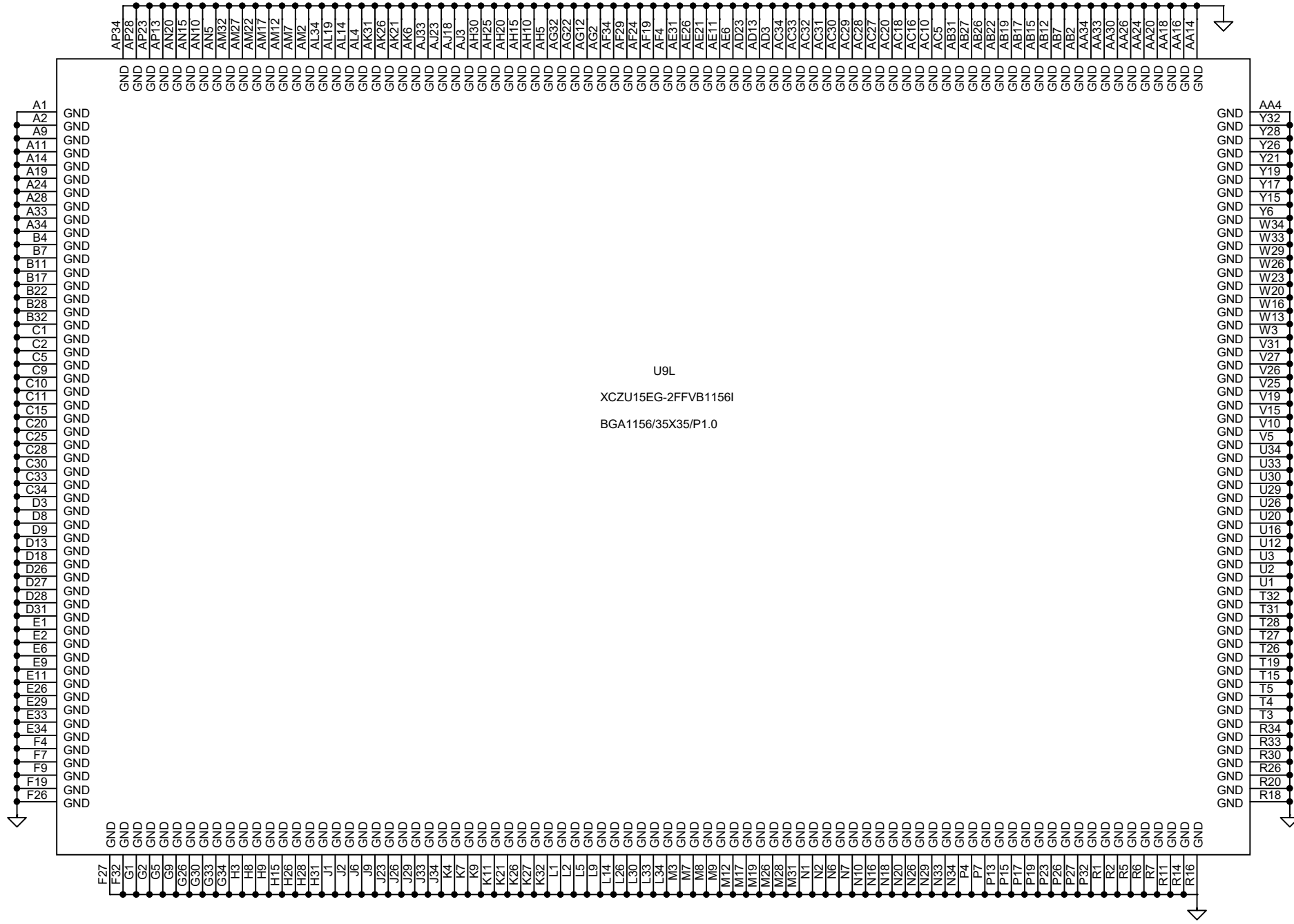








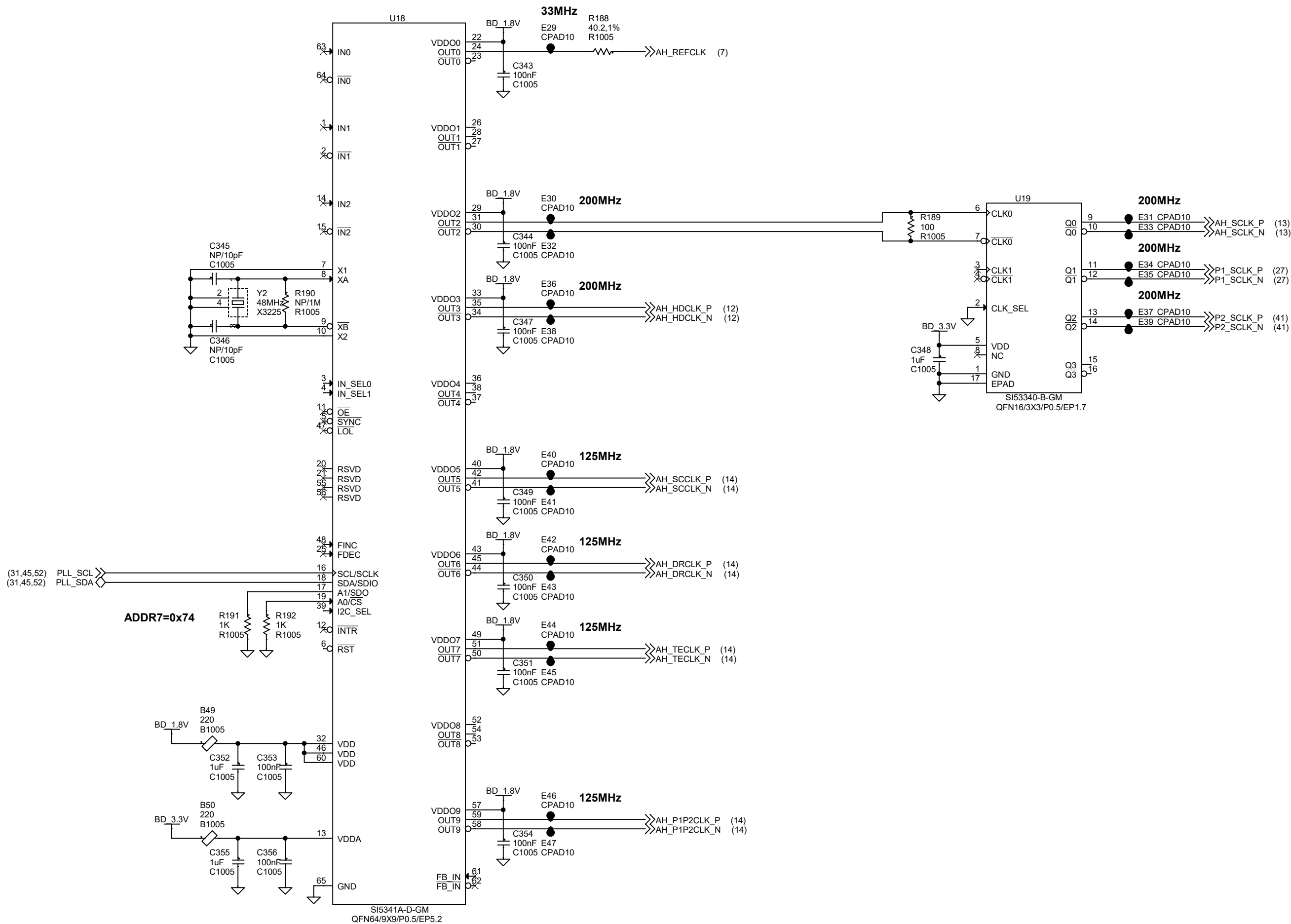






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Designed	HAN InCheol	Title		SPC: AH SoC Ground
Drawn	HAN InCheol	Size	Document Number	Rev
Approved	<Approved>	A3	717-U01541-00	0
		Date	Friday, November 10, 2023	Sheet 16 of 55

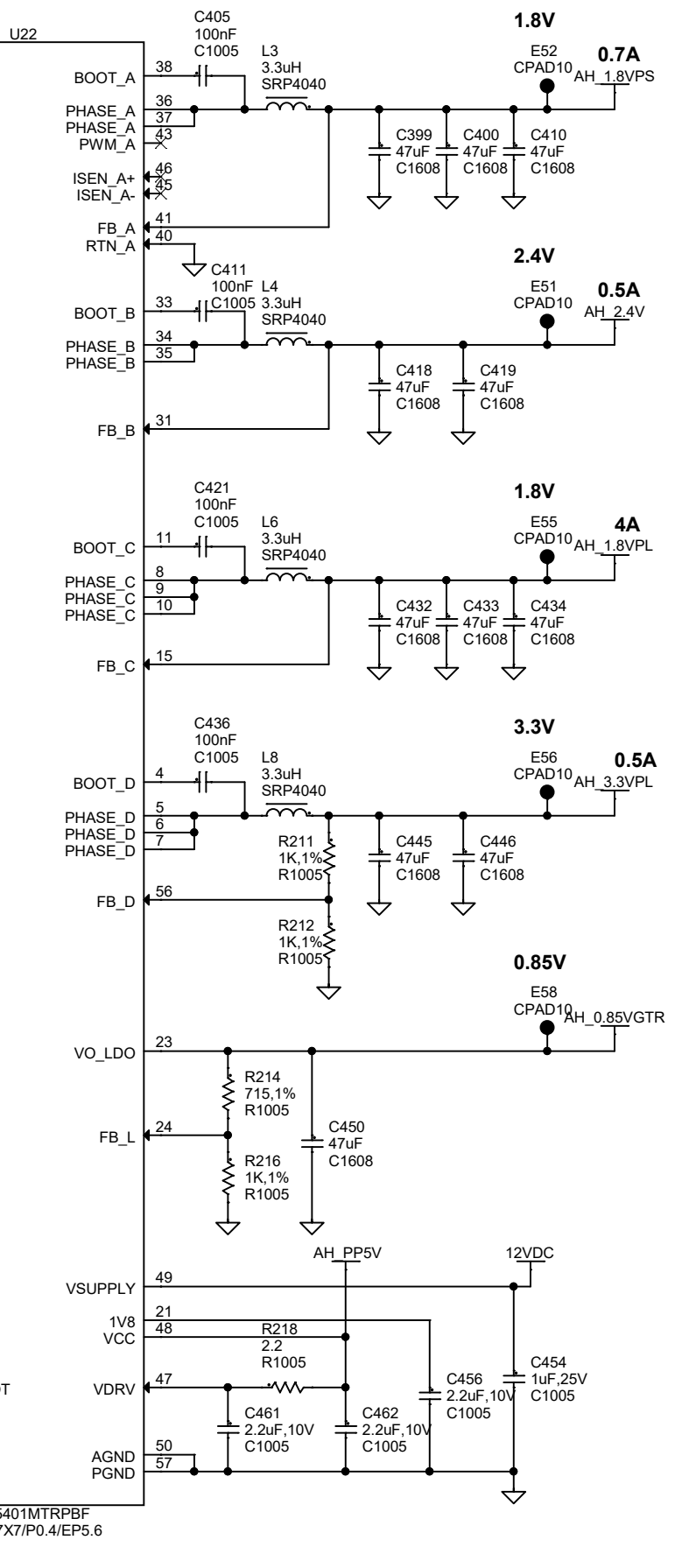
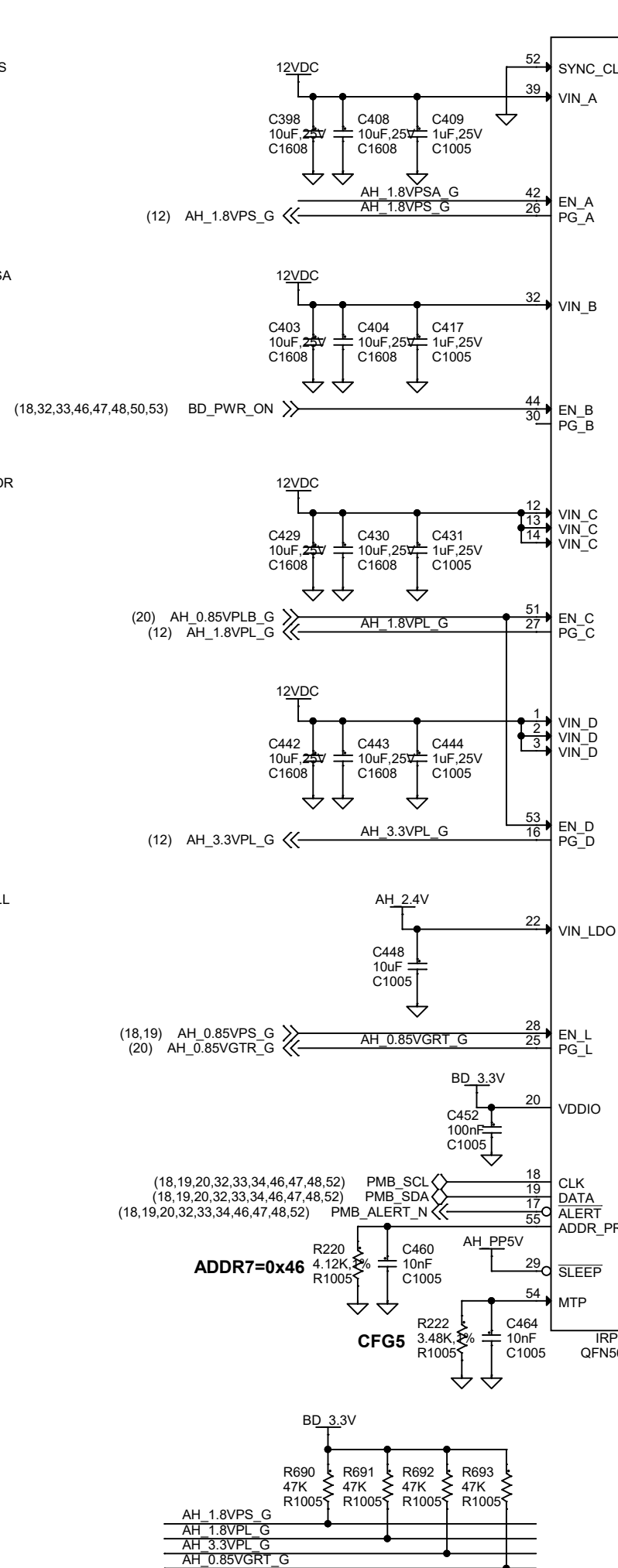
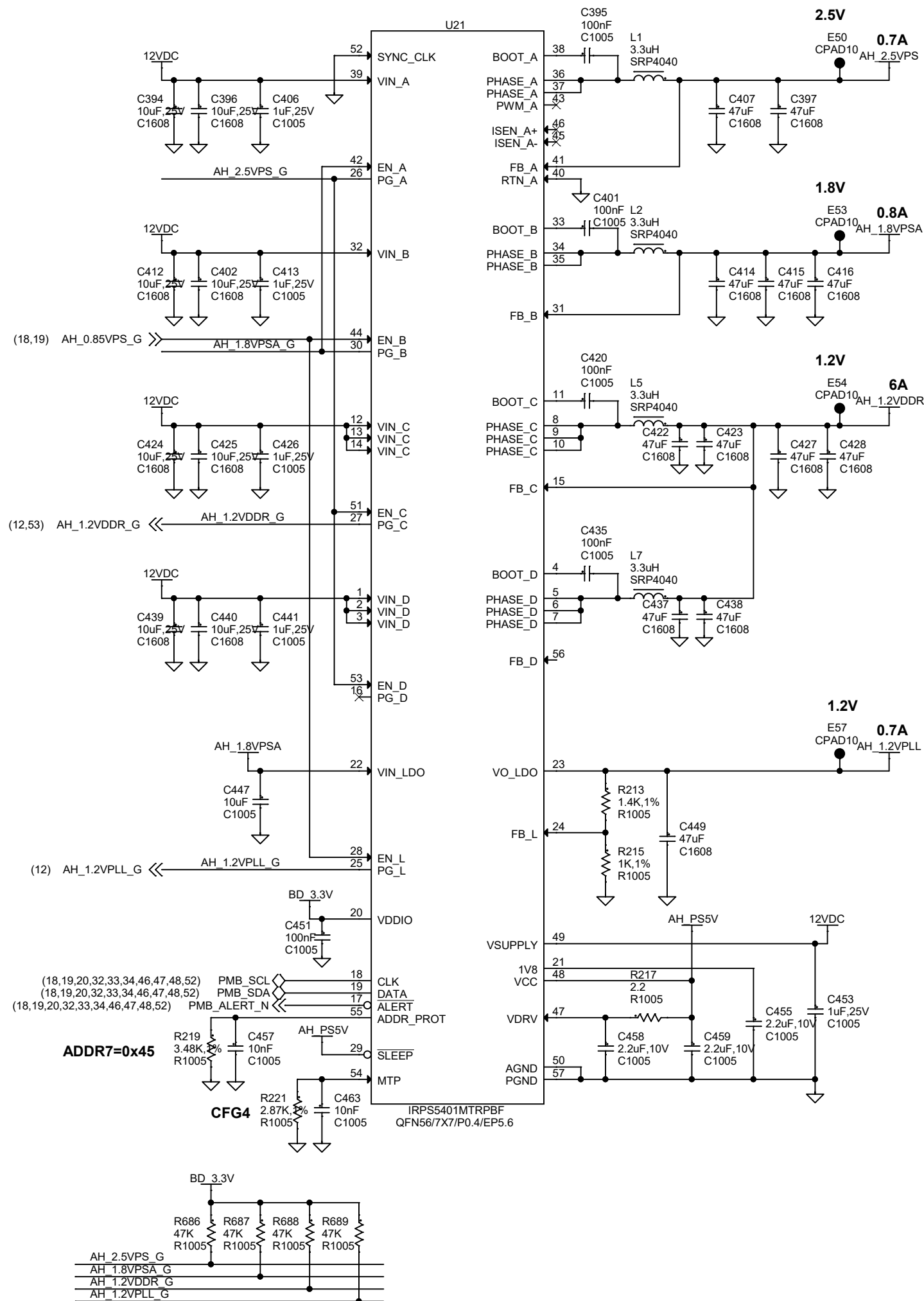


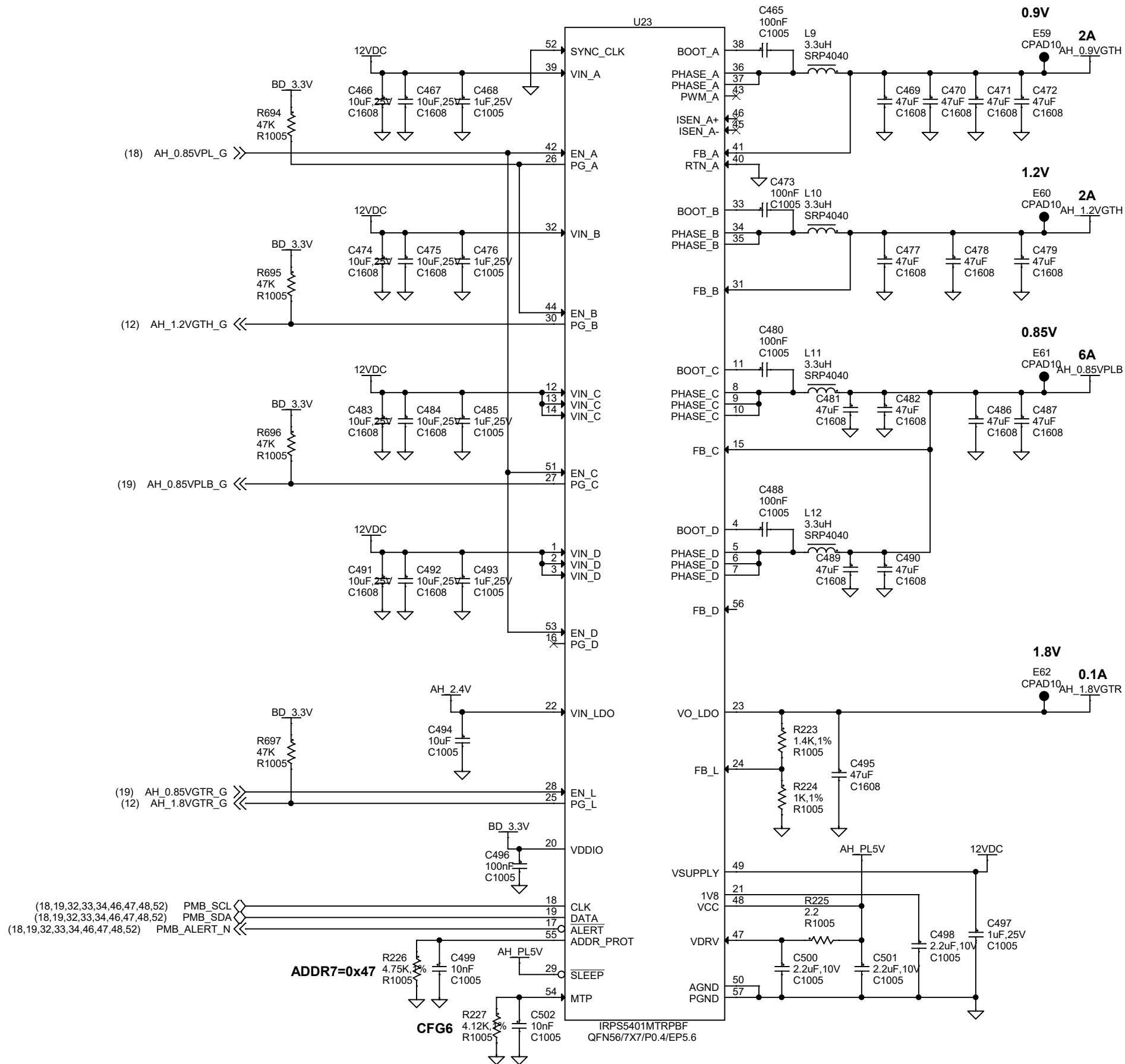
Programmer: ClockBuilder Field Programmer Kit (CBPROG-DONGLE)



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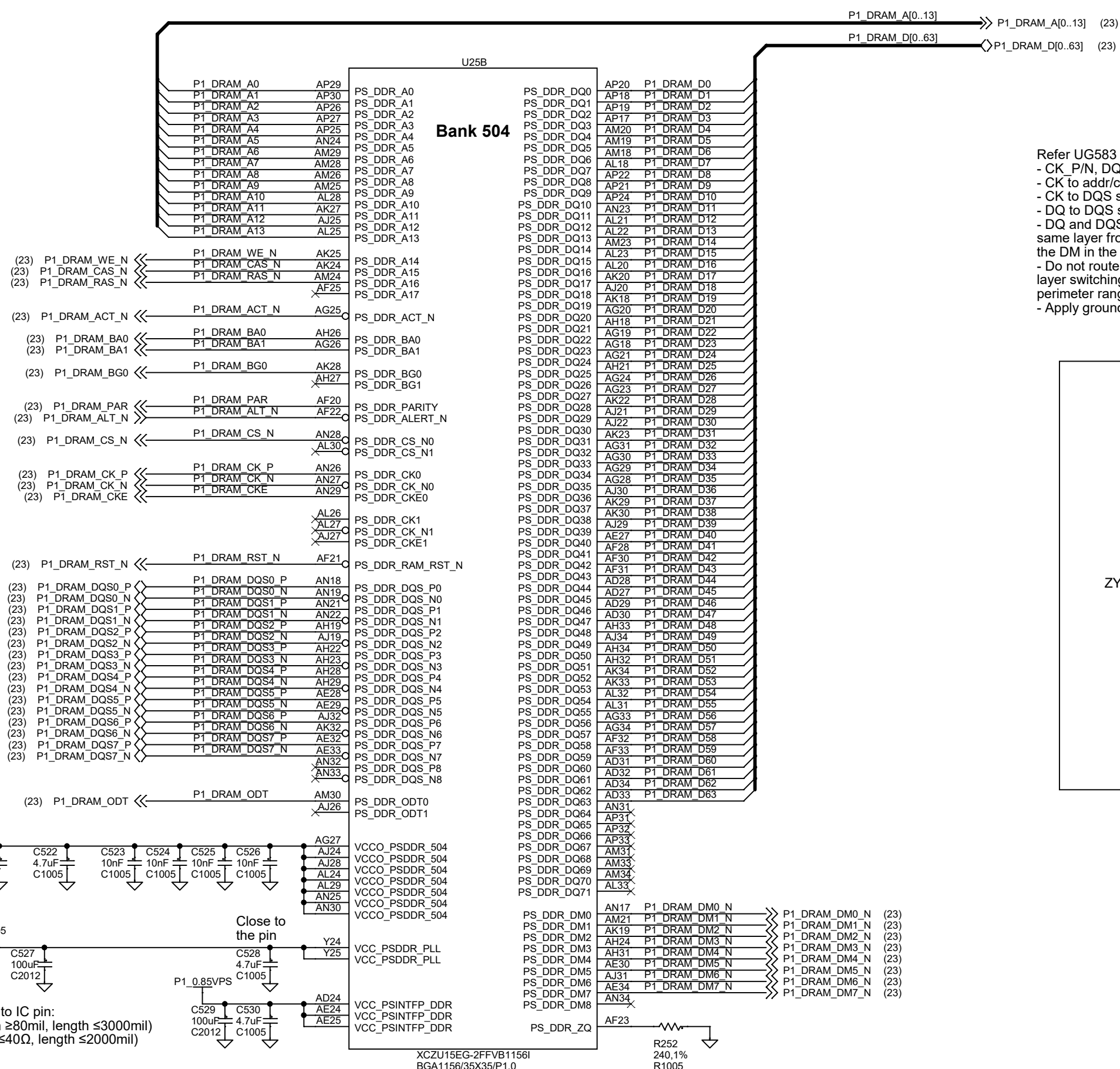
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Drawn	HAN InCheol	Size	A3	Document Number	717-U01541-00
Approved	<Approved>	Date	Friday, November 10, 2023		Rev 0
		Sheet	17	of	55





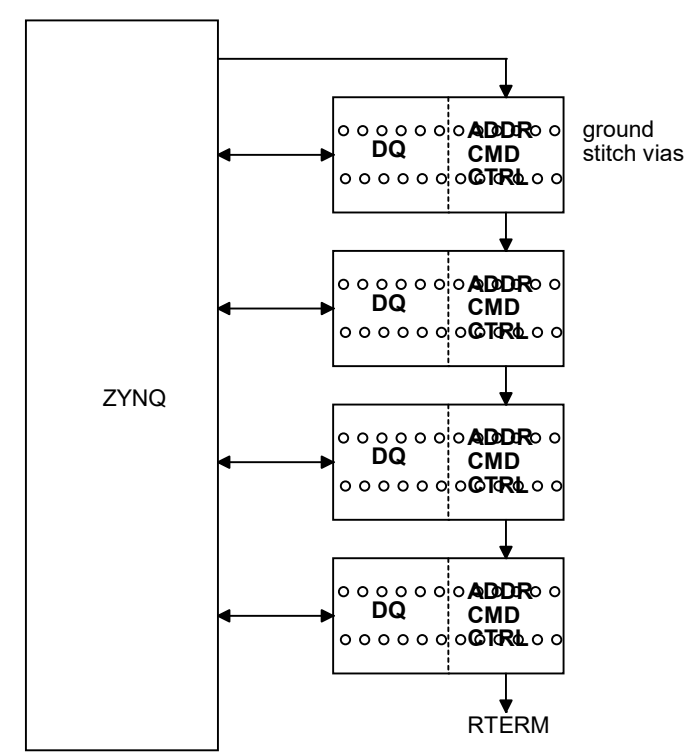


Designed	Title			
Drawn	SPC: P1 Configuration & AUX			
Approved	Size	Document Number	Rev	
<Approved>	A3	717-U01541-00	0	
	Date	Friday, November 10, 2023	Sheet	21 of 55



Refer UG583 p.34~64)

- CK_P/N, DQS_P/N skew < ±2ps, ±12mil
- CK to addr/cmd/ctrl skew < ±8ps, ±47mil
- CK to DQS skew < -149~+1796ps, -879~+10600mil
- DQ to DQS skew < ±5ps, ±29mil
- DQ and DQS signals in the same byte group should be routed in the same layer from Zynq to DRAM, except in the breakout areas. Include the DM in the byte group as applicable.
- Do not route any individual signal on more than two layers. Any signal layer switching via needs to have one ground via within a 50 mil perimeter range
- Apply ground stitch vias under DRAM



Bead to IC pin:
(width ≥80mil, length ≤3000mil)
or (Z ≤40Ω, length ≤2000mil)

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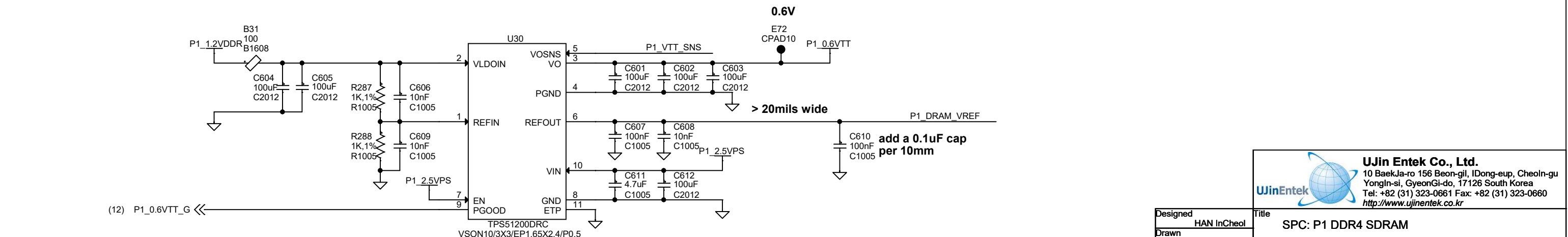
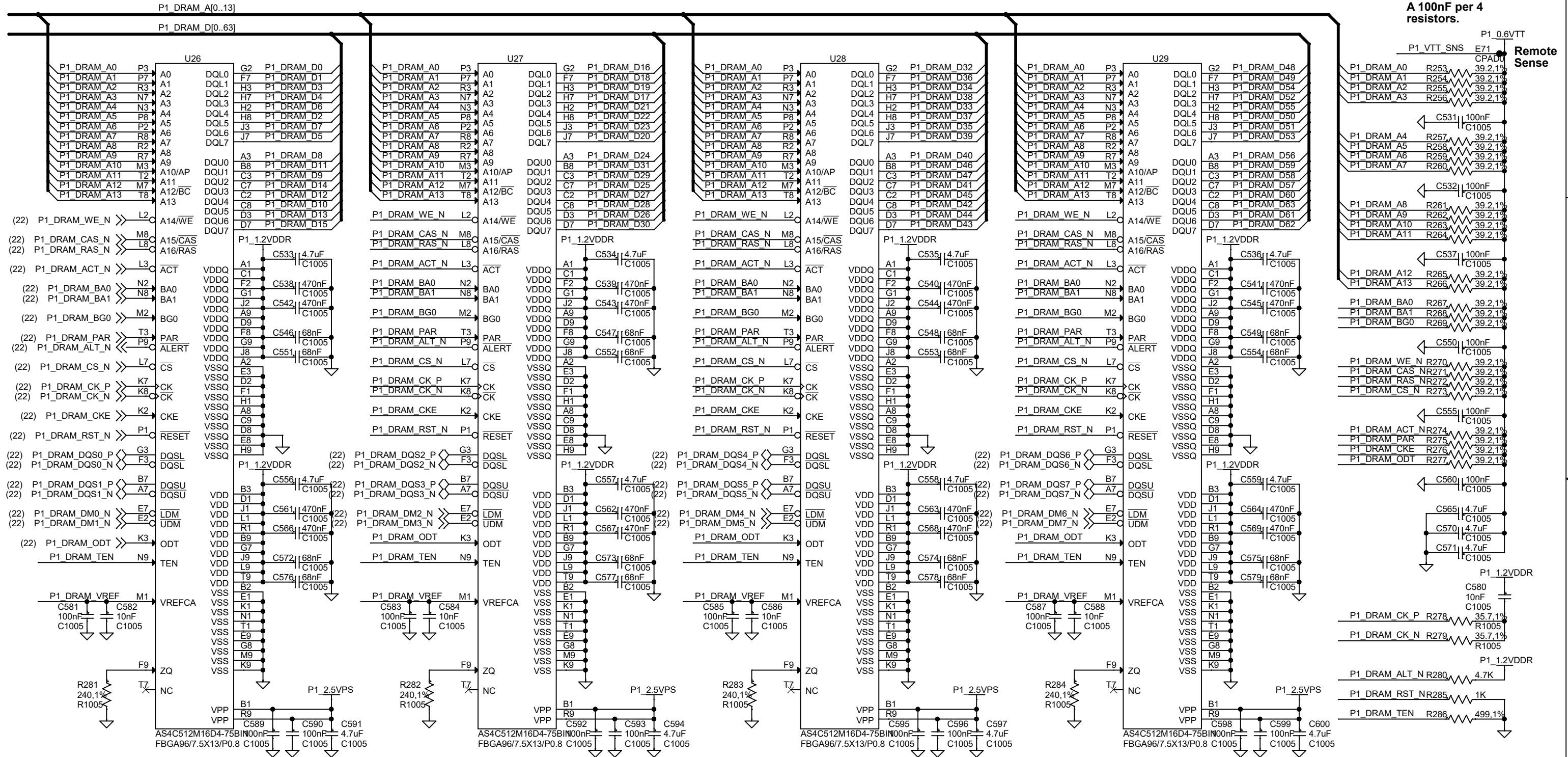
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Drawn	HAN InCheol	Size	A3
Approved	<Approved>	Document Number	717-U01541-00
		Date	Thursday, November 16, 2023
		Sheet	22 of 55
		Rev	0


(22) P1_DRAM_A[0..13] >> P1_DRAM_A[0..13]
(22) P1_DRAM_D[0..63] << P1_DRAM_D[0..63]

Fly-by topology

<----- < 0.5" ----->

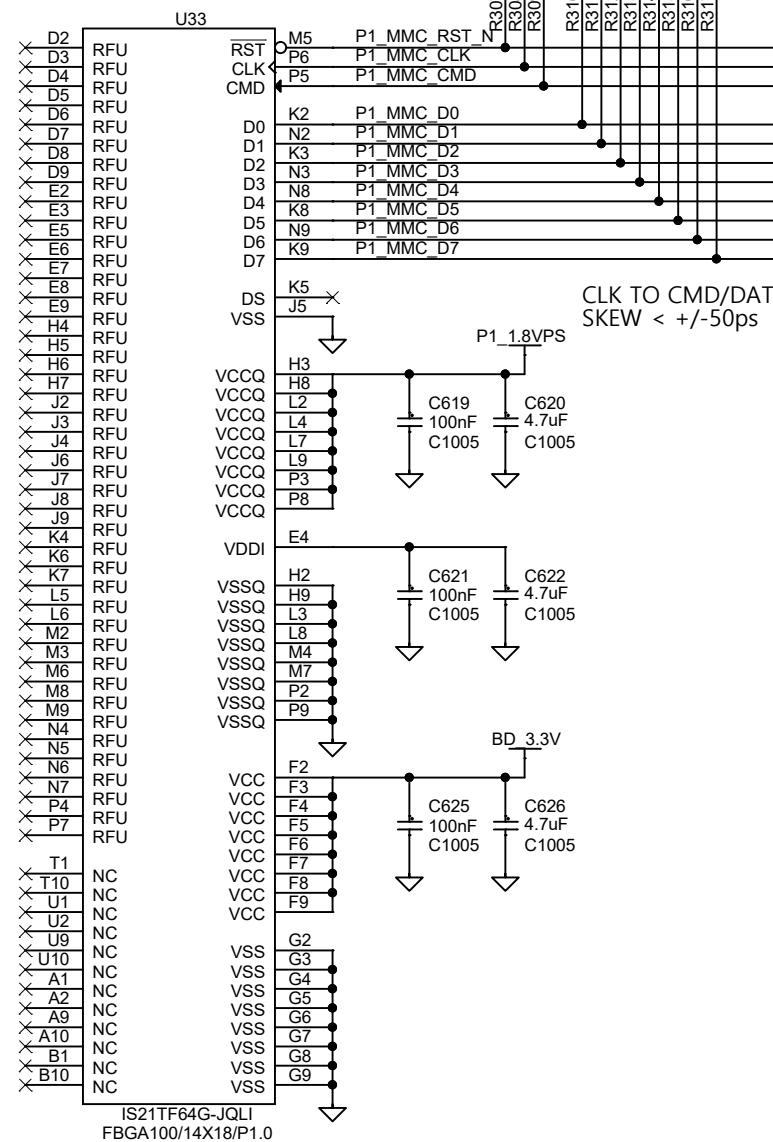
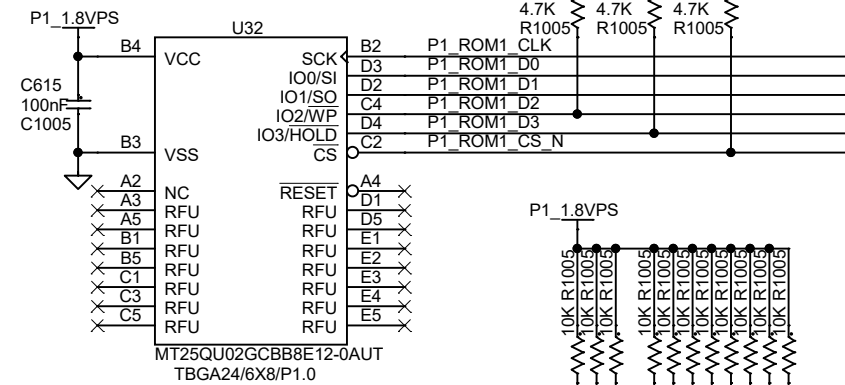
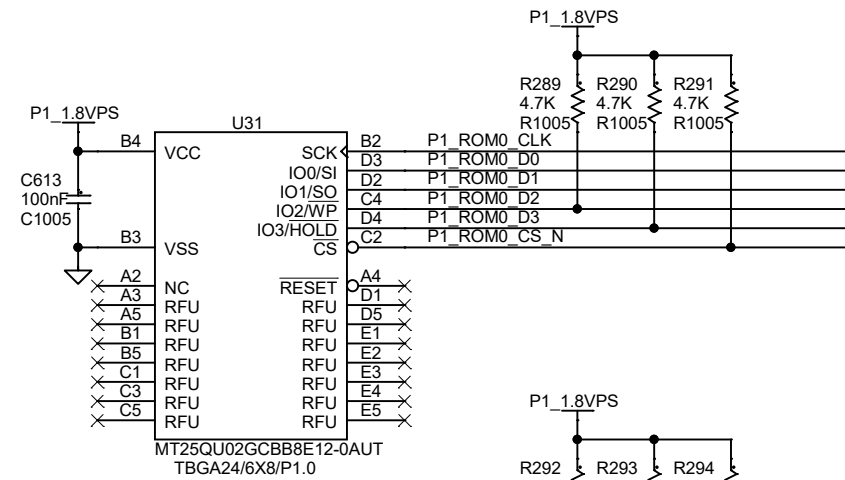
Place at the end of the traces.
A 100nF per 4 resistors.



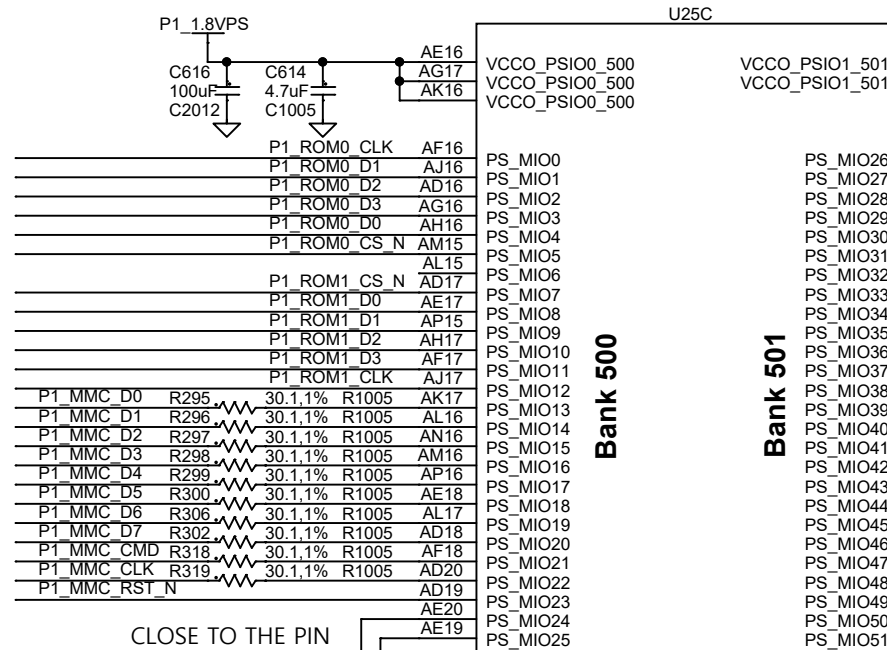


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Drawn	HAN InChol	Size	A3	Document Number
Approved	<Approved>	Date	Thursday, November 16, 2023	
		Sheet	23	of 55



CLK TO CS/DATA
SKEW < +/-50ps
TRACE DELAY < 500ps

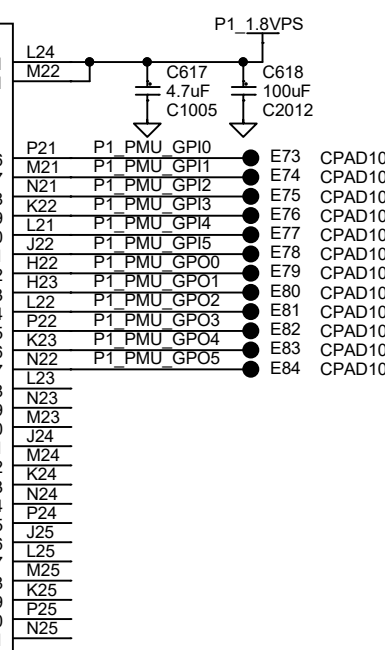


CLOSE TO THE PIN

Bank 500

Bank 501

Bank 502

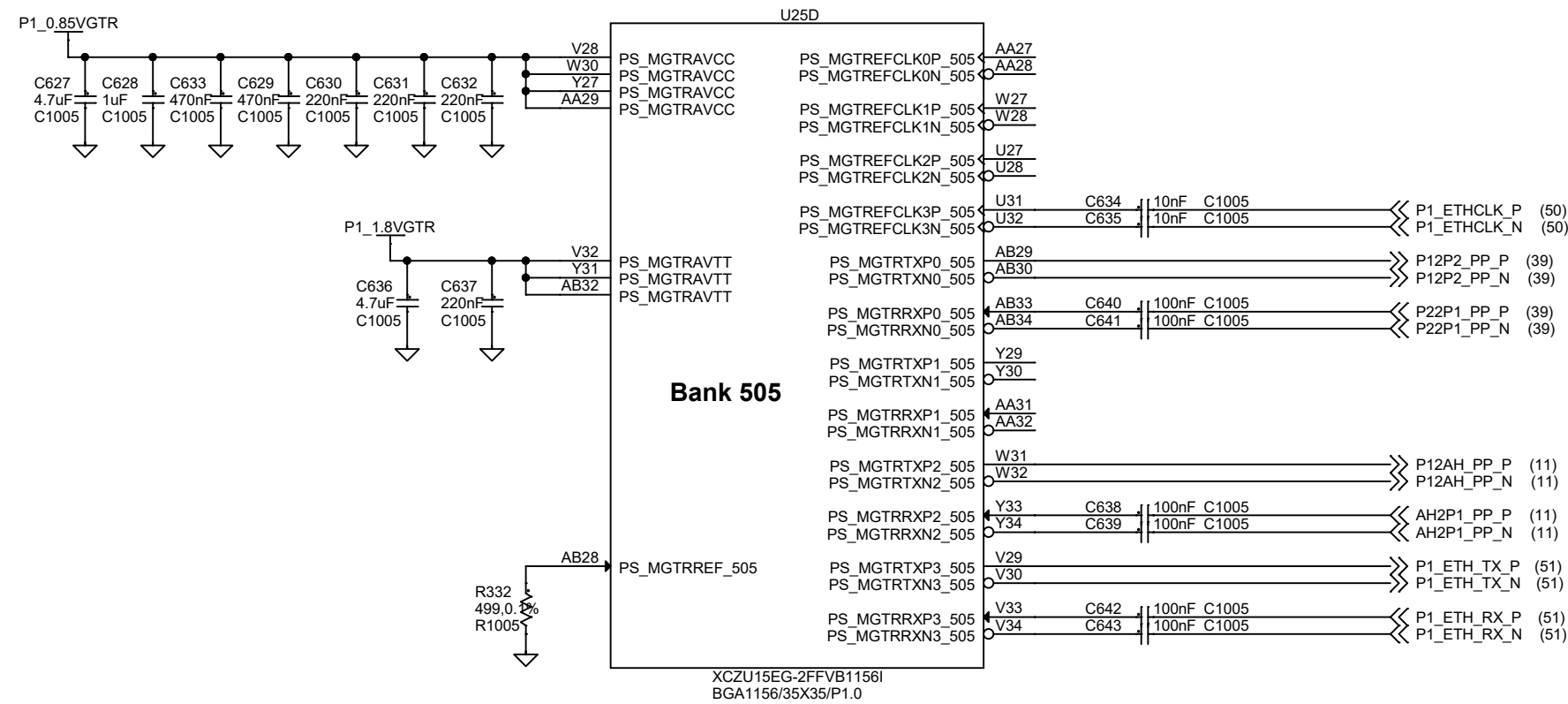


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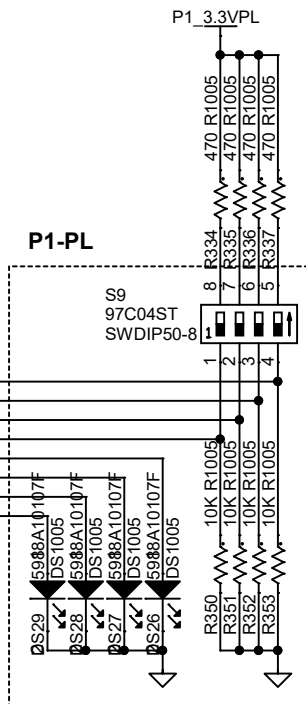
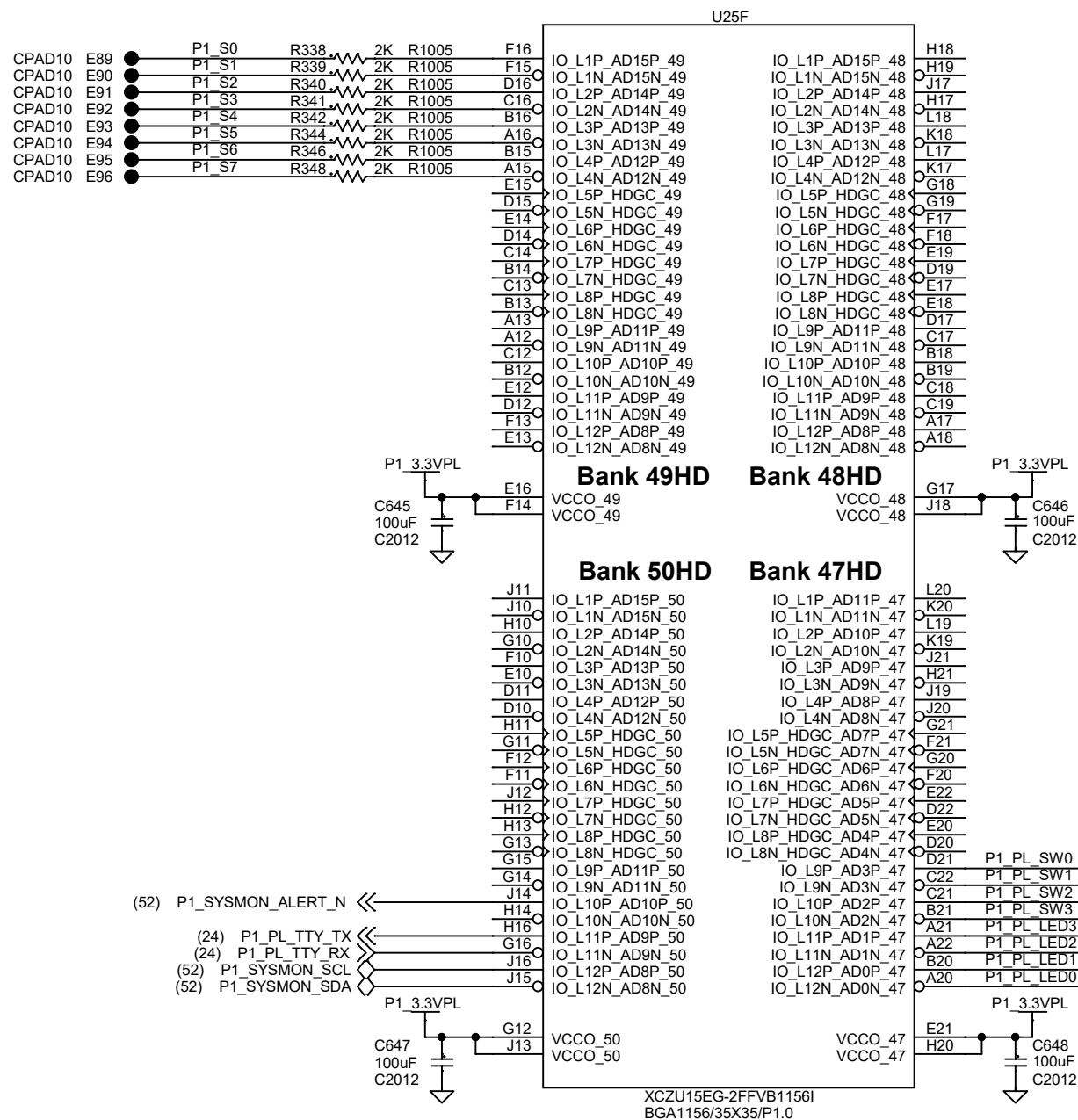
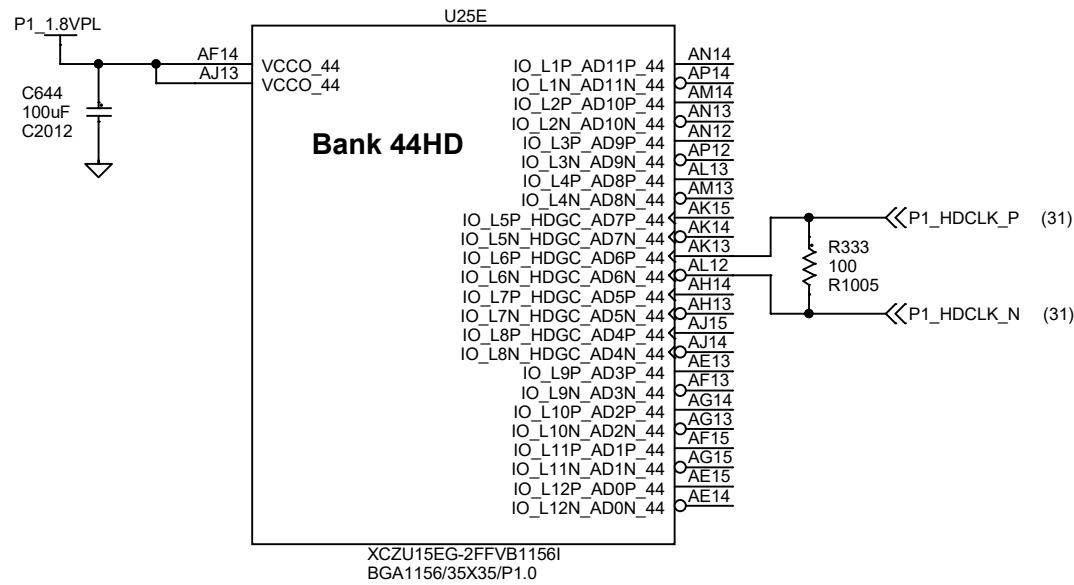
P1-TTY

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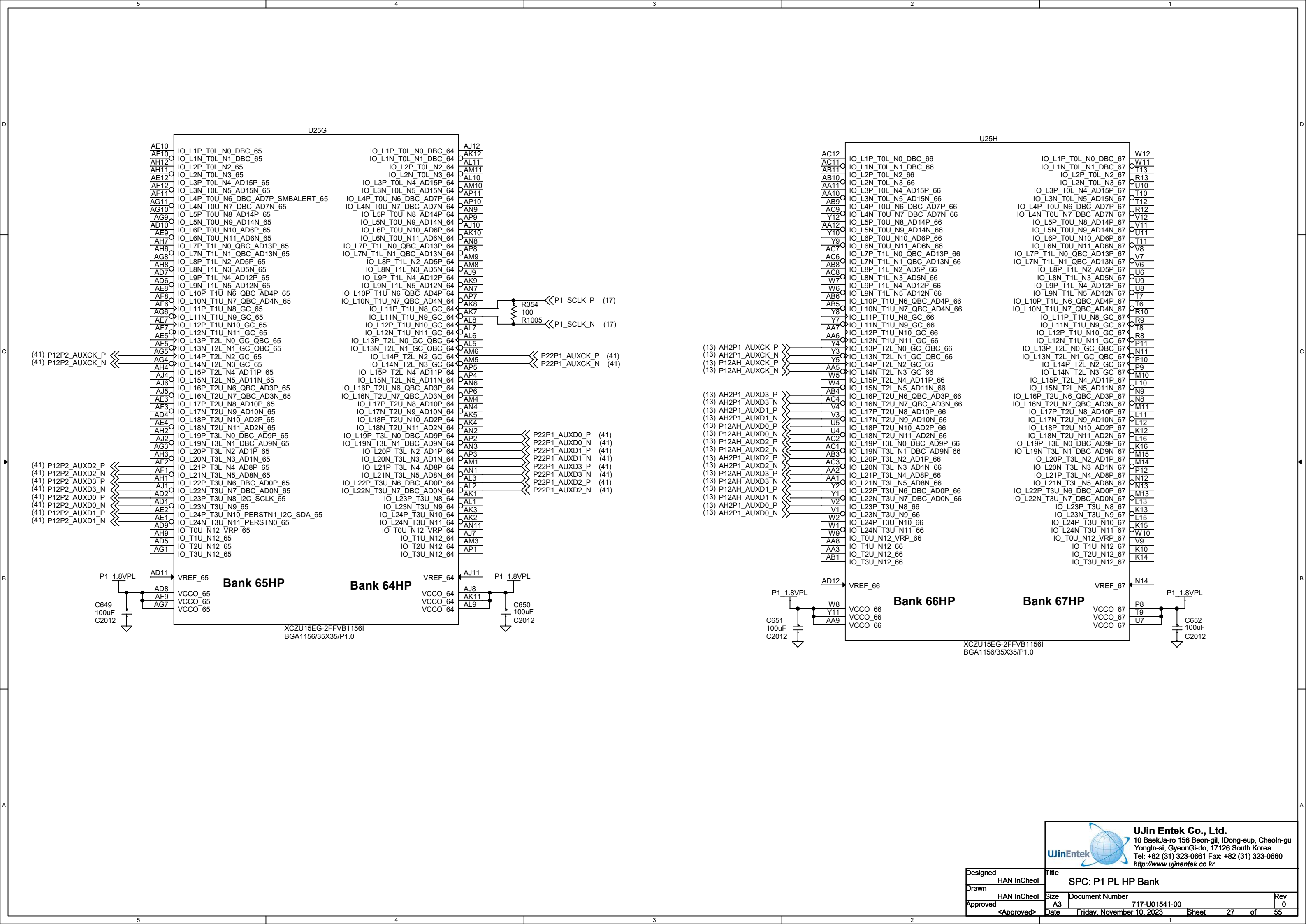
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Drawn	HAN InCheol	Size	A3
Approved	<Approved>	Document Number	717-U01541-00
		Date	Friday, November 10, 2023
		Sheet	24 of 55
		Rev	0

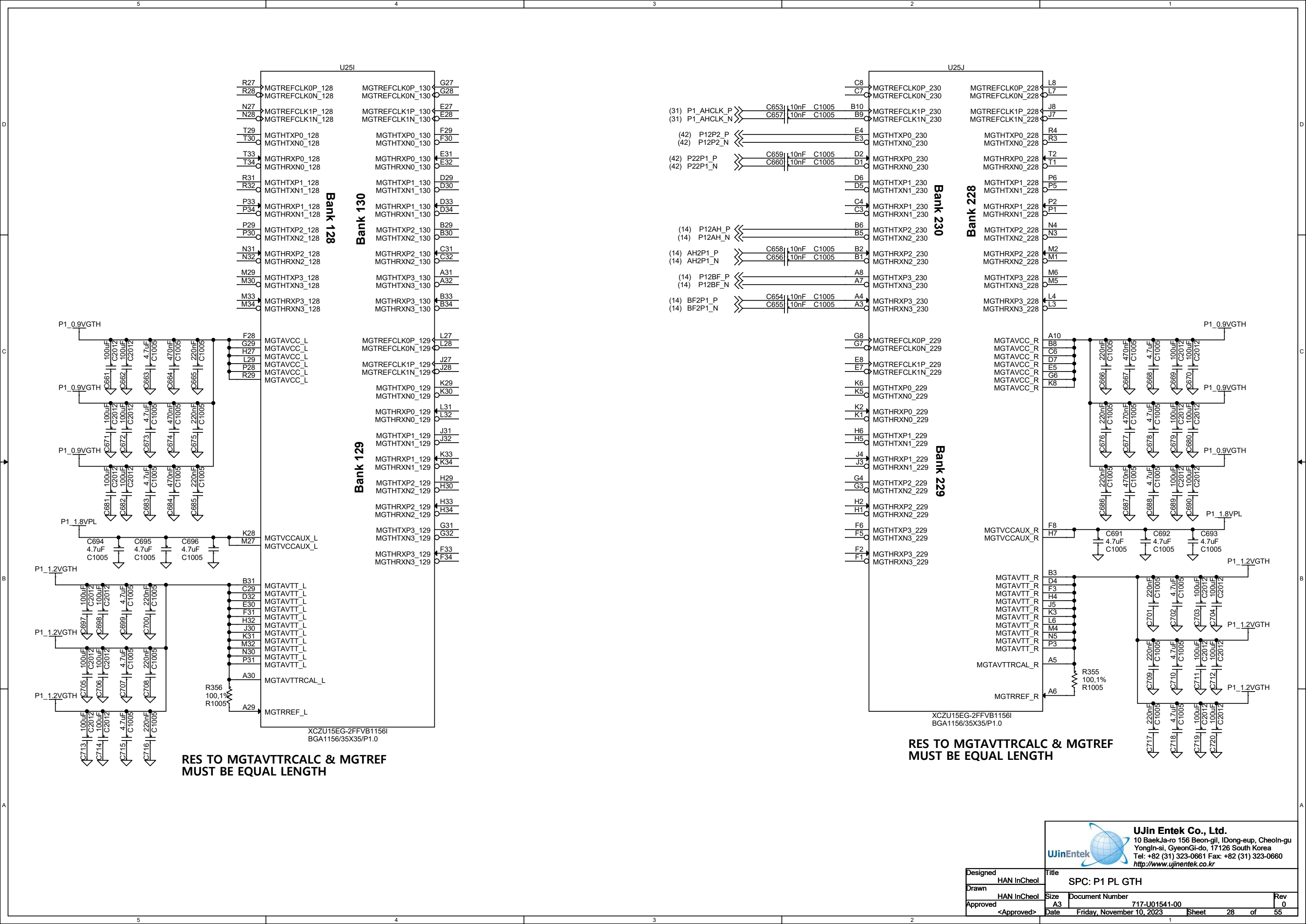


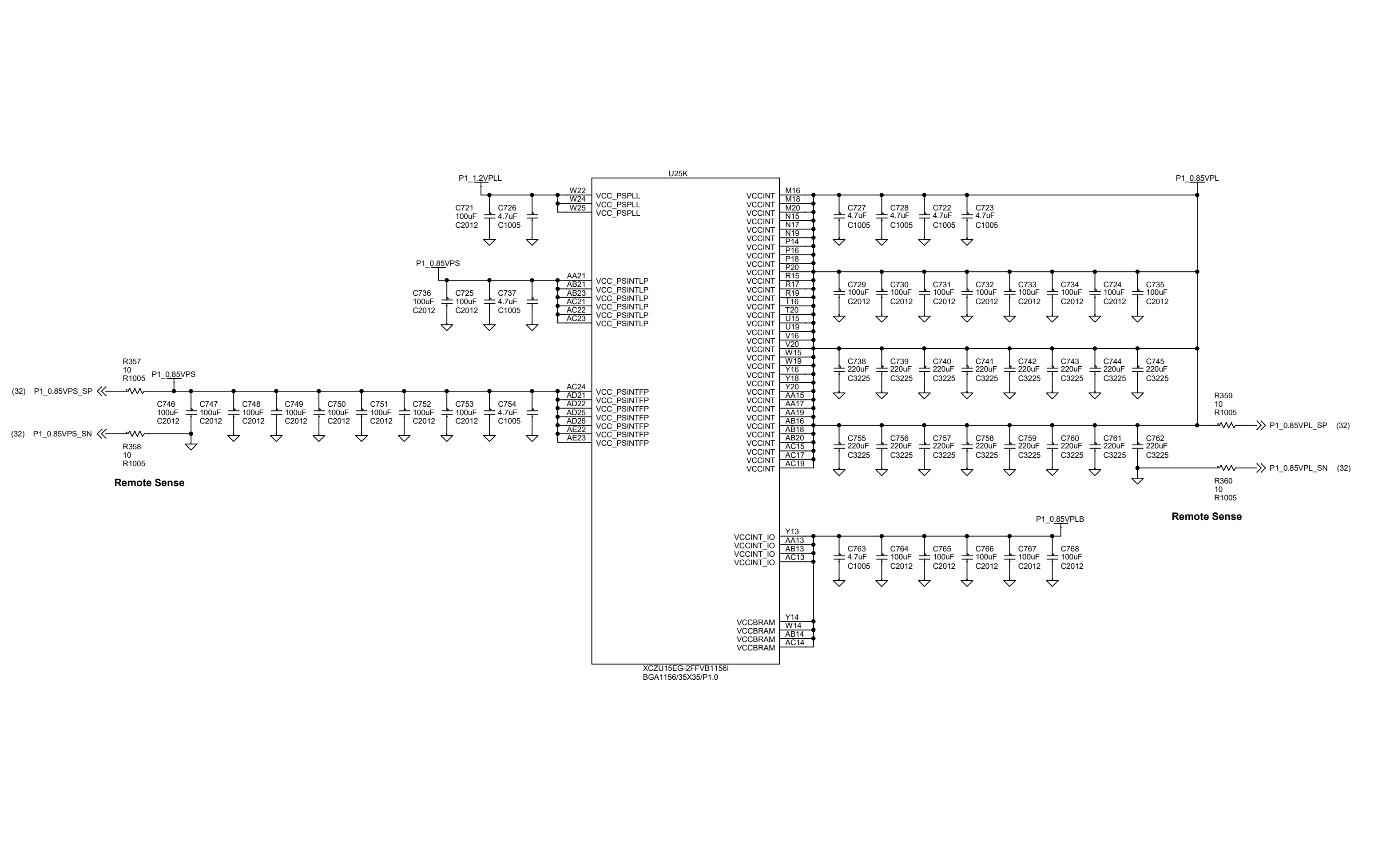
6Gbps max
Z = 50Ω single-ended / 100Ω differential
Trace match P/N < 2ps
Trace length < 254mm



Designed	HAN InCheol	Title	SPC: P1 PL HD Bank
Drawn	HAN InCheol	Size	A3
Approved	<Approved>	Document Number	717-U01541-00
		Date	Friday, November 10, 2023
		Sheet	26 of 55
		Rev	0



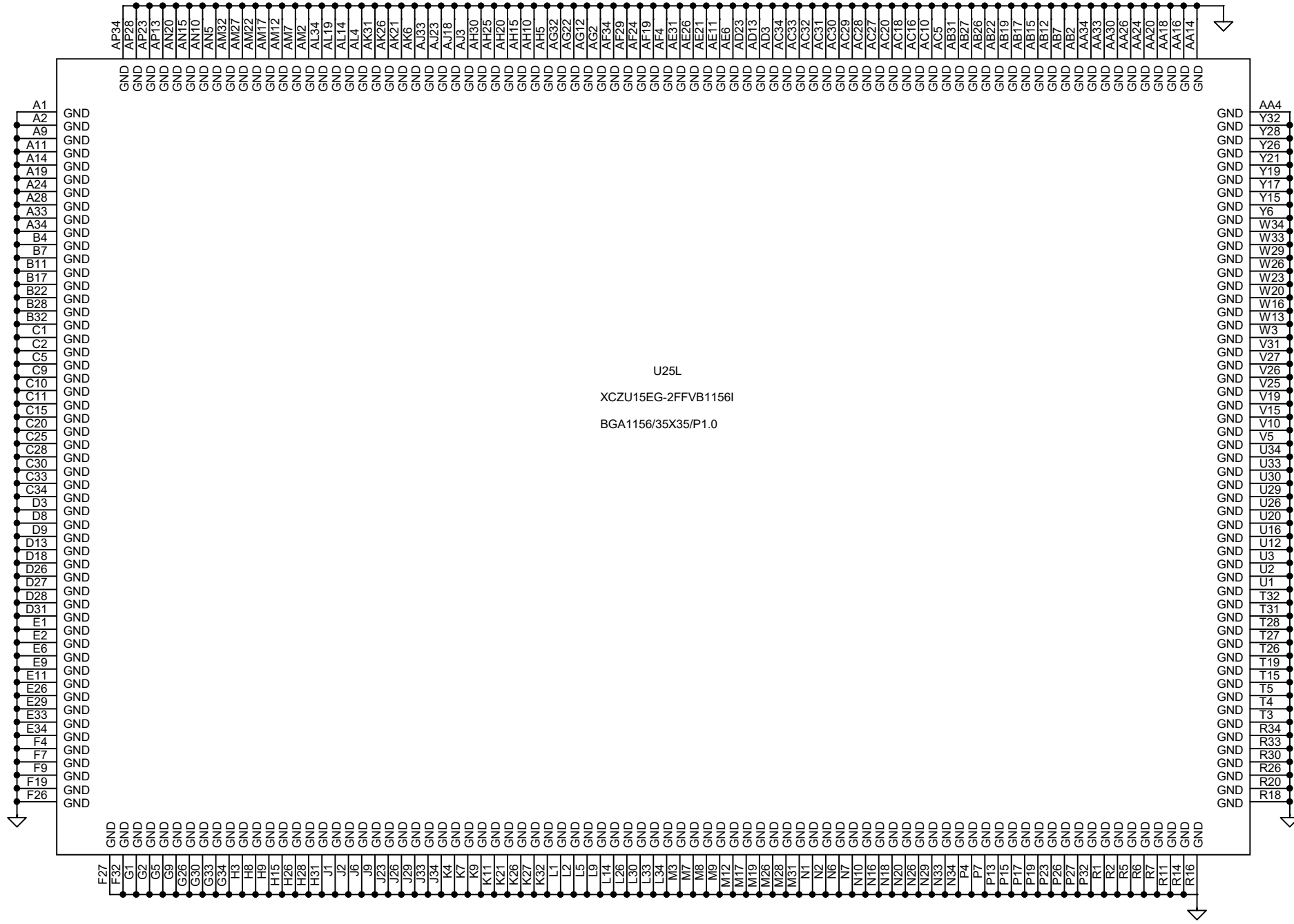






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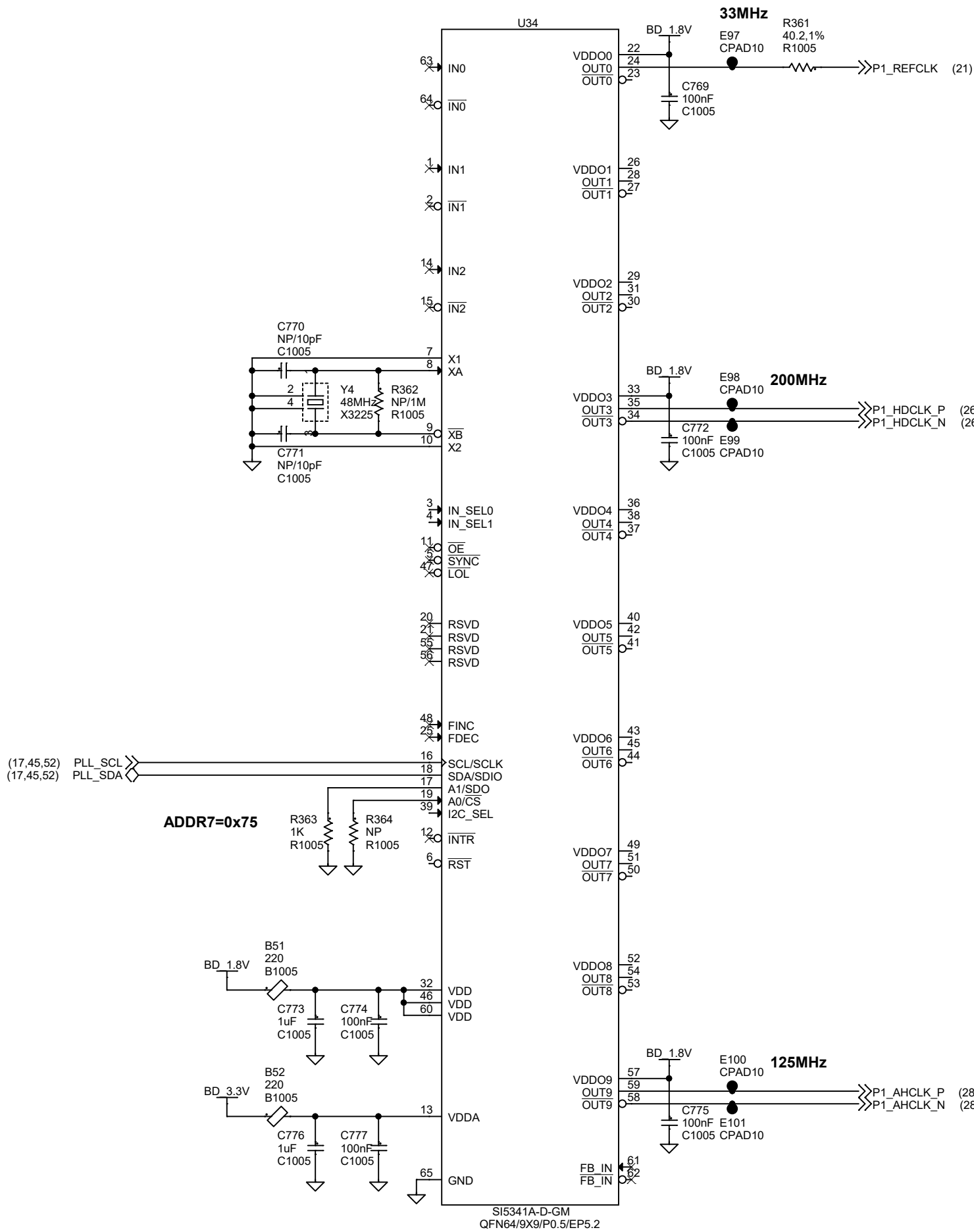
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Drawn	HAN InCheol	SPC: P1 SoC Power				
Approved	<Approved>	Size	Document Number			
		A3	717-U01541-00			
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Designed	HAN InCheol	Title			SPC: P1 SoC Ground		
Drawn	HAN InCheol	Size	A3	Document Number	717-U01541-00	Rev	0
Approved	<Approved>	Date	Friday, November 10, 2023	Sheet	30	of	55

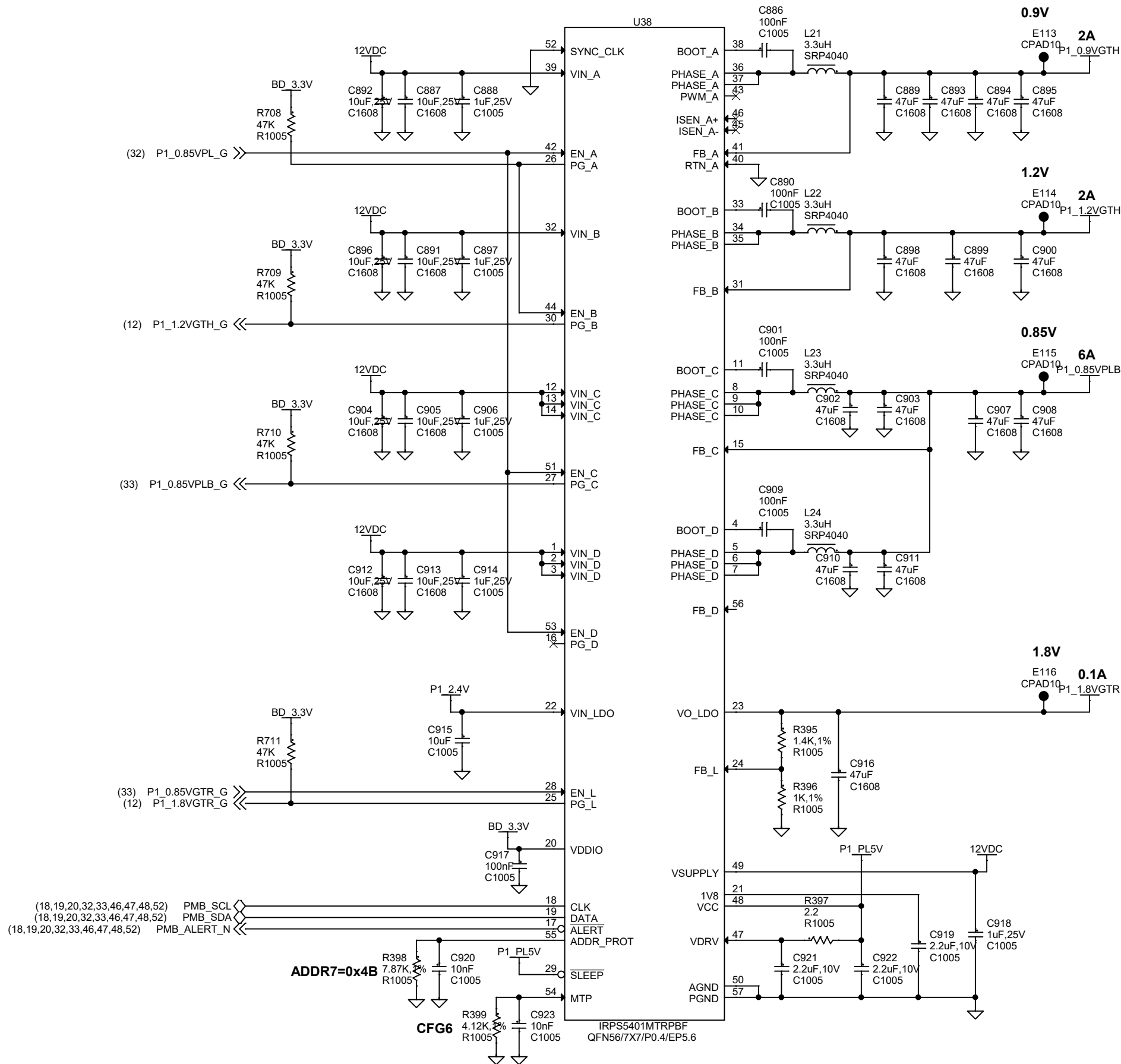


Programmer: ClockBuilder Field Programmer Kit (CBPROG-DONGLE)



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Designed	HAN InCheol	Title		SPC: P1 Clock Generator
Drawn	HAN InCheol	Size	Document Number	Rev
Approved	<Approved>	A3	717-U01541-00	0
		Date	Friday, November 10, 2023	Sheet 31 of 55



Programmer: USB005

(18,19,20,32,33,46,47,48,52) PMB_SCL
(18,19,20,32,33,46,47,48,52) PMB_SDA
(18,19,20,32,33,46,47,48,52) PMB_ALERT_N

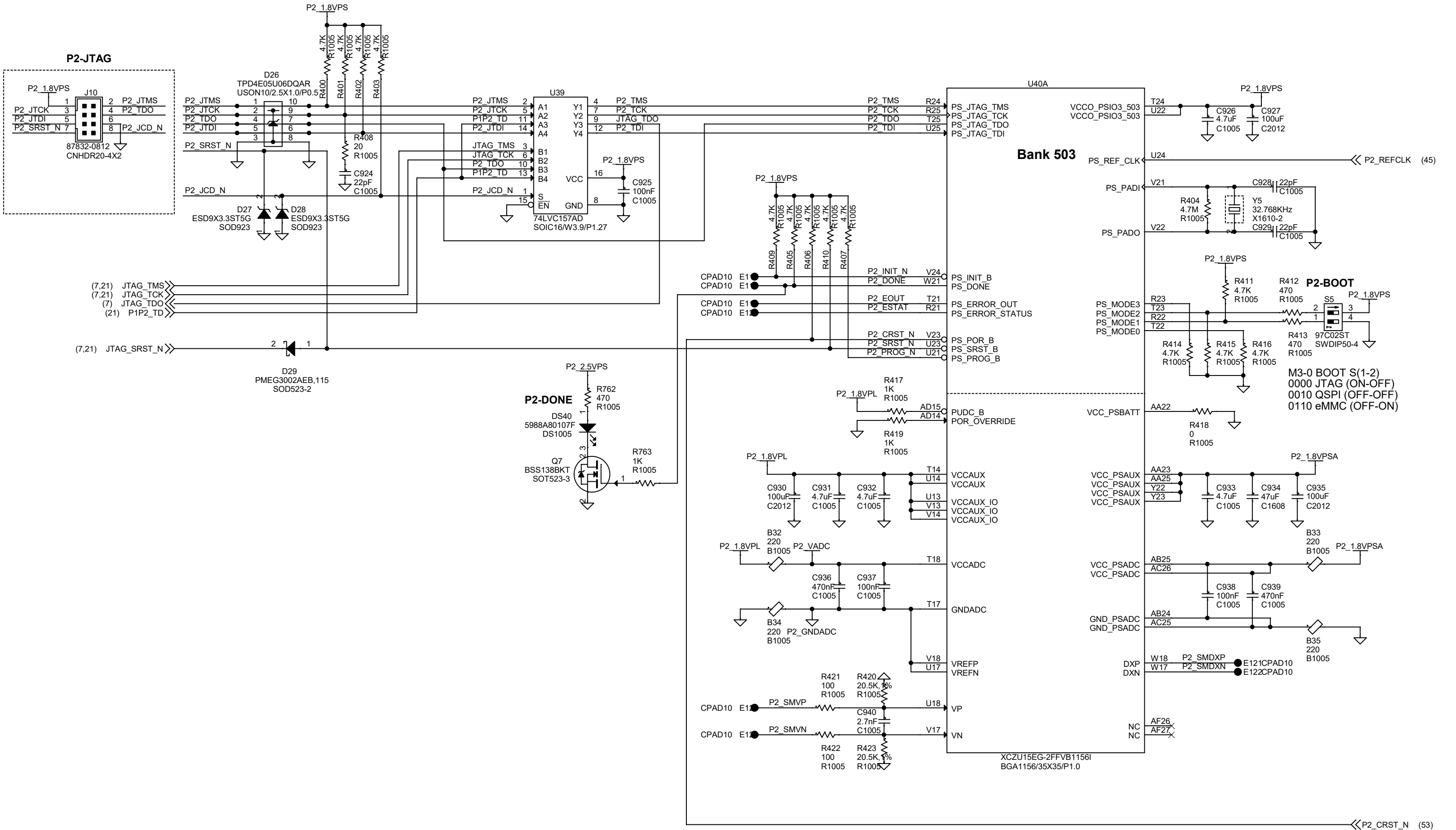
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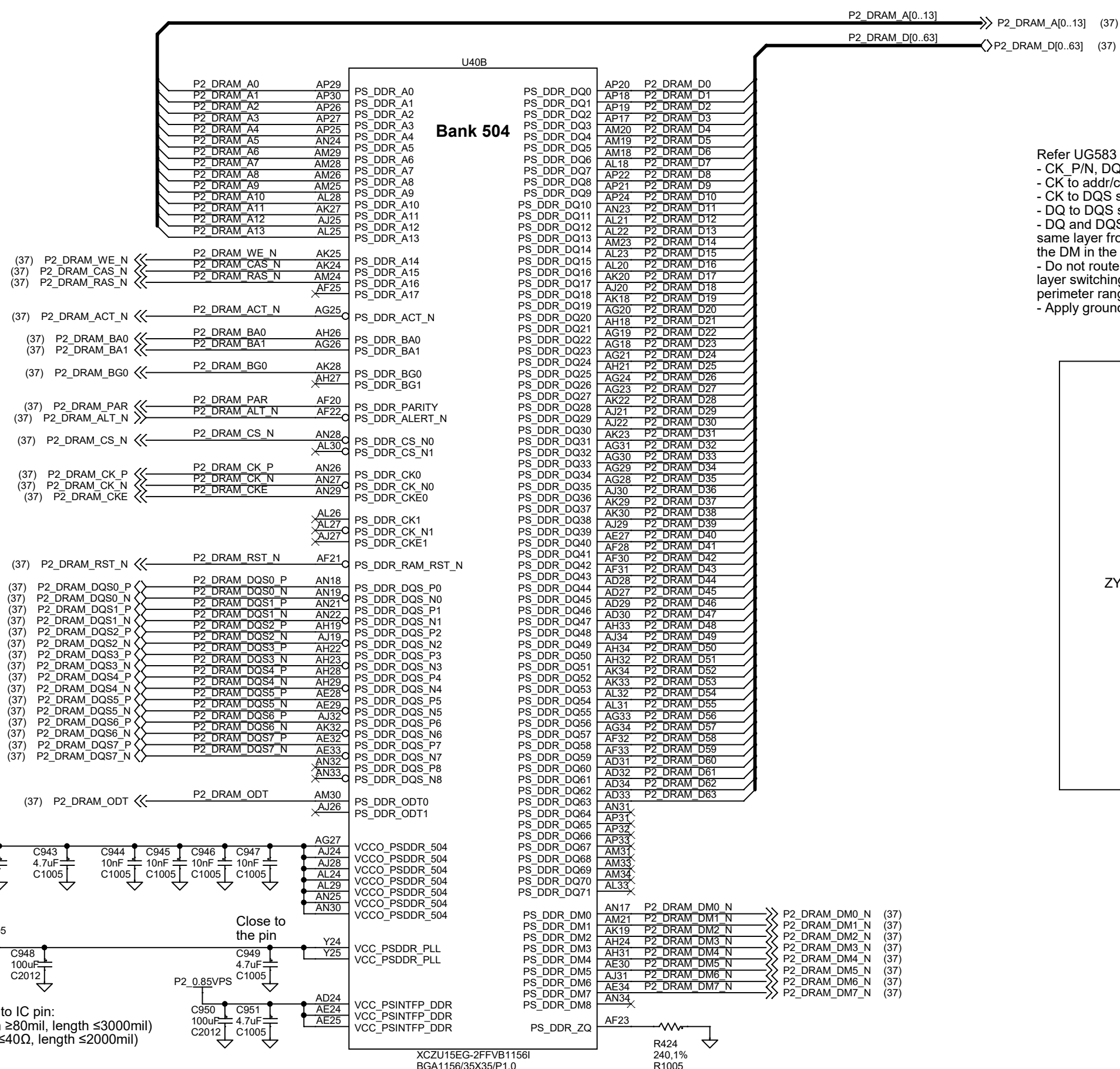
CFG6



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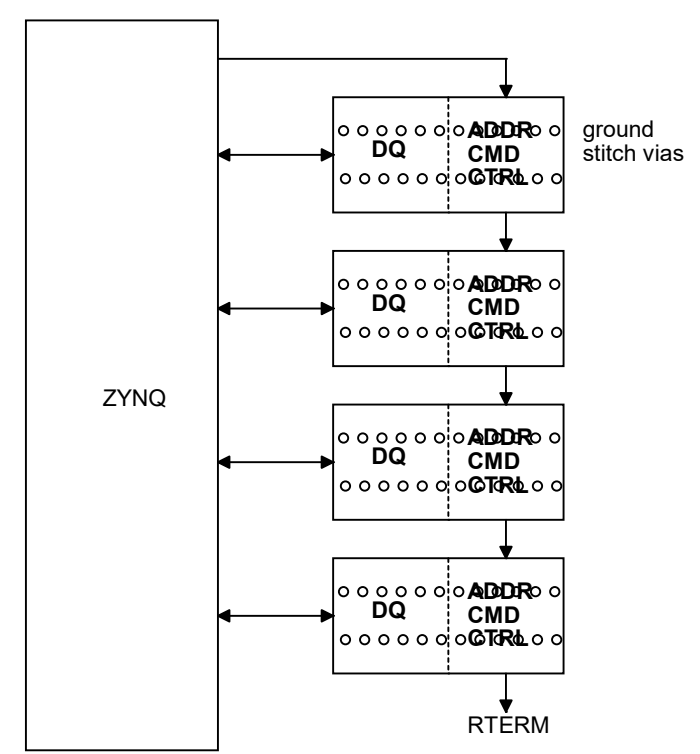
Designed	HAN InCheol	Title			SPC: P1 Power for PL		
Drawn	HAN InCheol	Size	A3	Document Number	717-U01541-00	Rev	0
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Refer UG583 p.34~64)

- CK_P/N, DQS_P/N skew < ±2ps, ±12mil
- CK to addr/cmd/ctrl skew < ±8ps, ±47mil
- CK to DQS skew < -149~+1796ps, -879~+10600mil
- DQ to DQS skew < ±5ps, ±29mil
- DQ and DQS signals in the same byte group should be routed in the same layer from Zynq to DRAM, except in the breakout areas. Include the DM in the byte group as applicable.
- Do not route any individual signal on more than two layers. Any signal layer switching via needs to have one ground via within a 50 mil perimeter range
- Apply ground stitch vias under DRAM

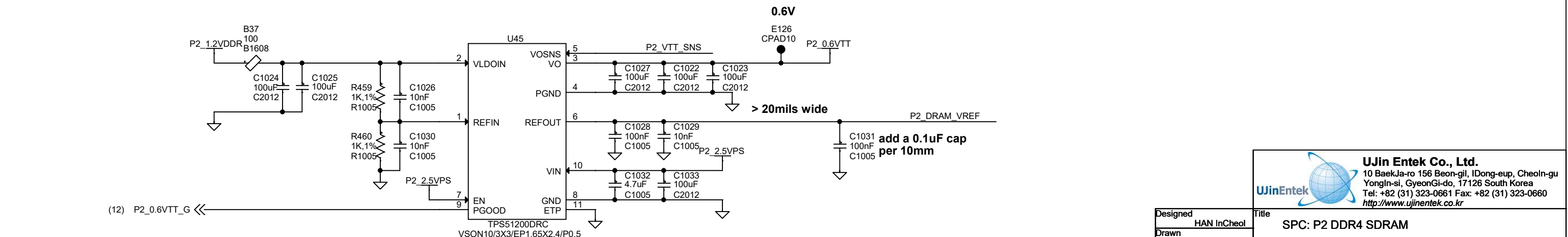
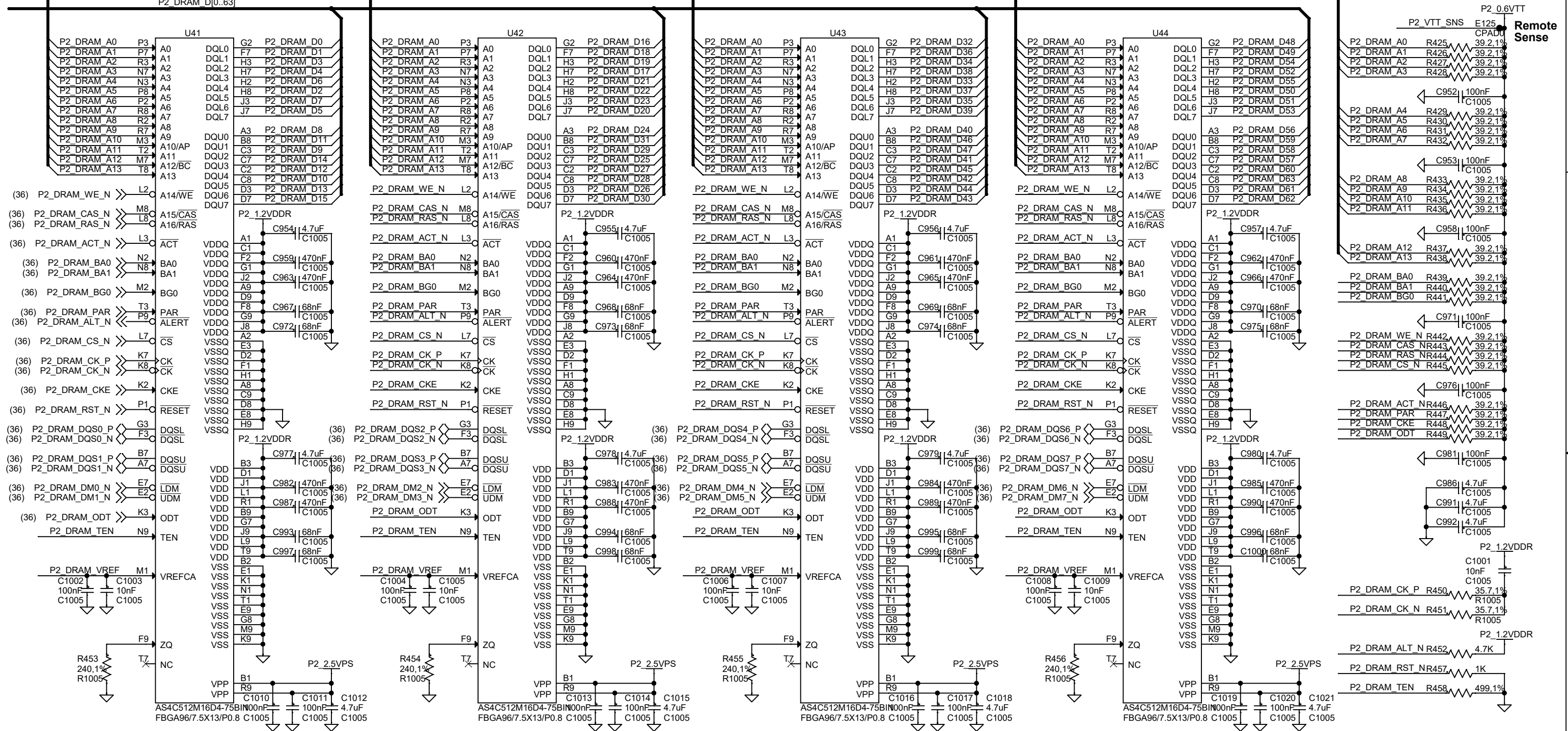


(36) P2_DRAM_A[0..13] >> P2_DRAM_A[0..13]
(36) P2_DRAM_D[0..63] << P2_DRAM_D[0..63]

Fly-by topology

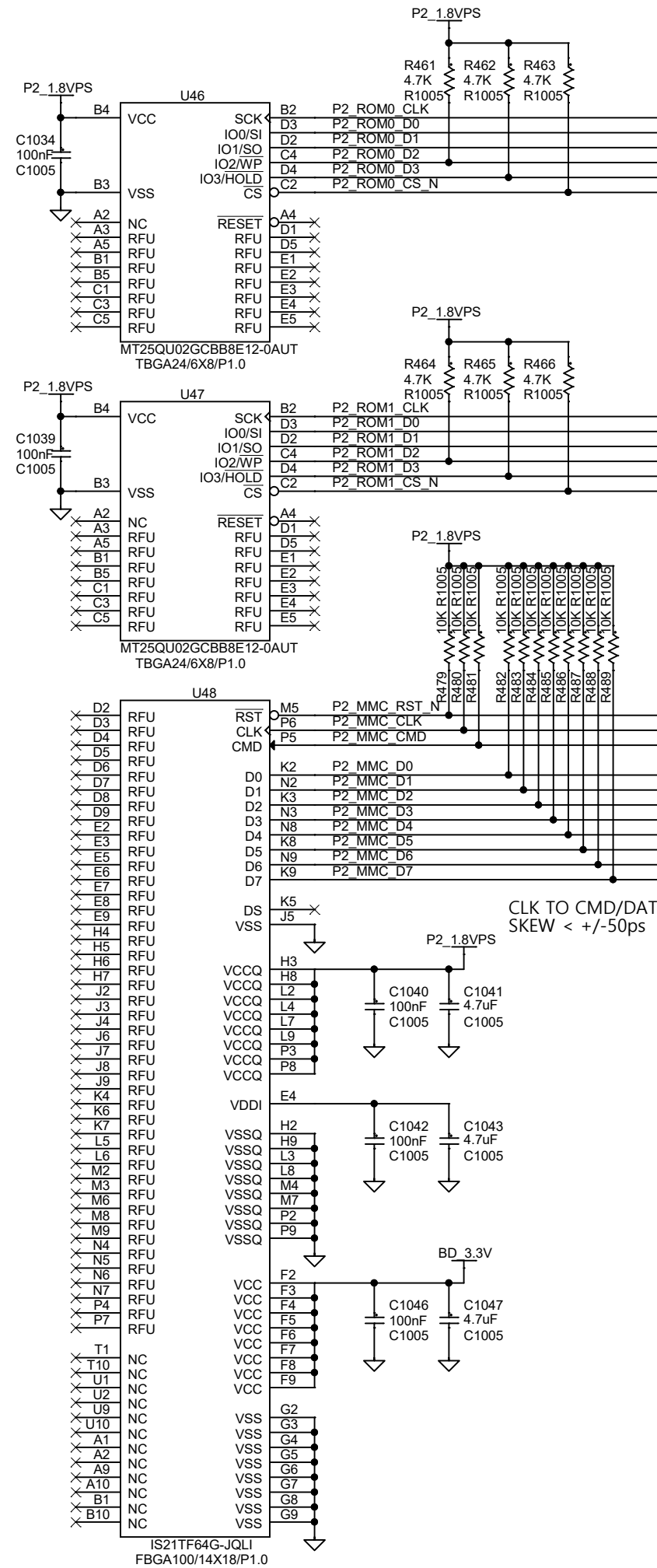
<----- < 0.5" ----->

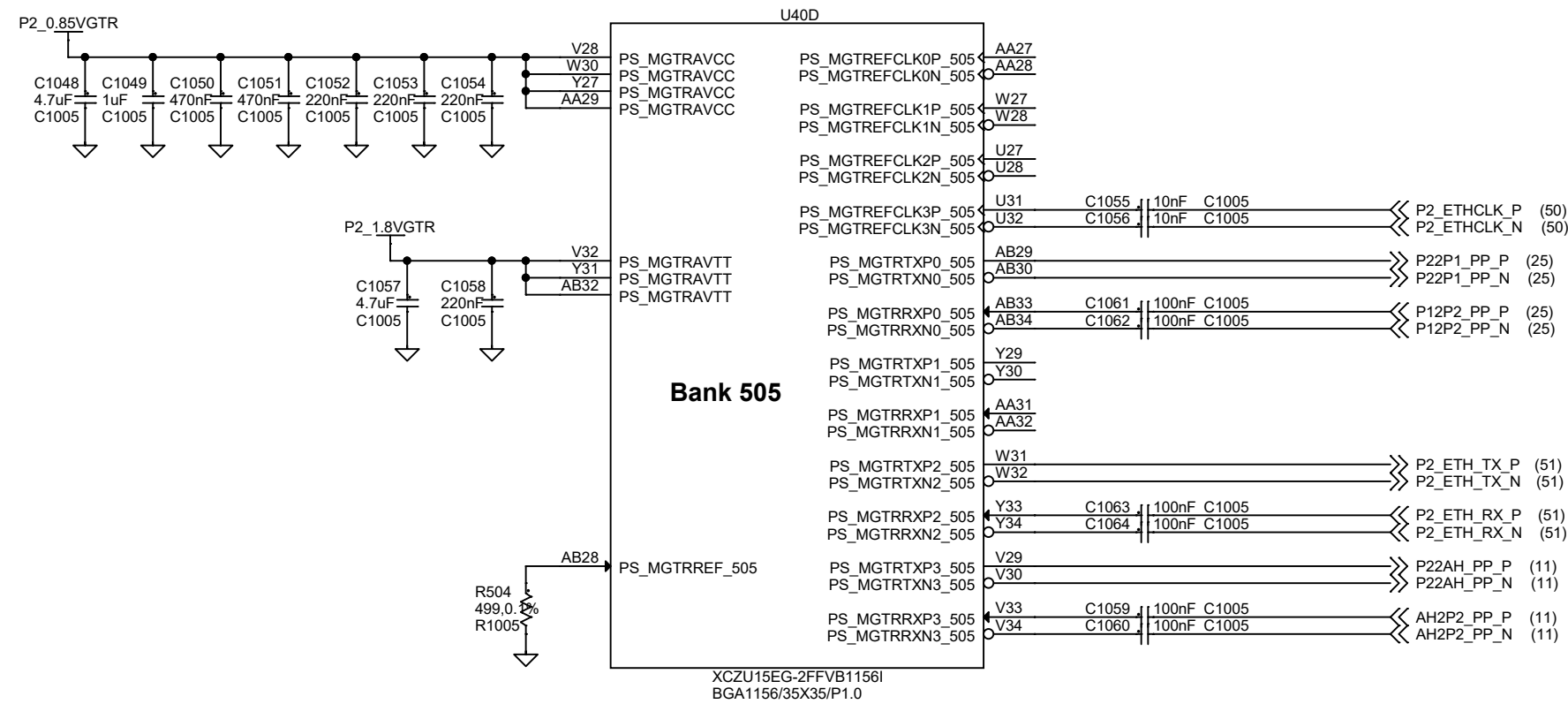
Place at the end of the traces.
A 100nF per 4 resistors.



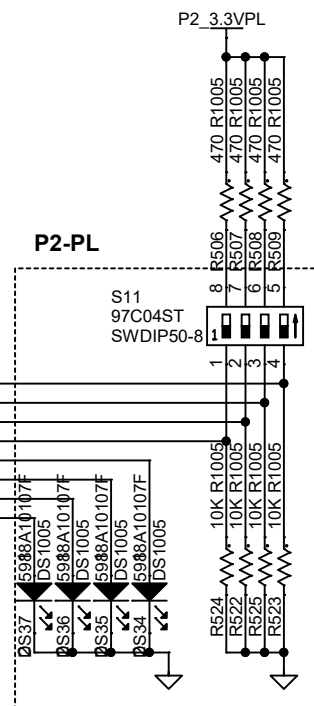
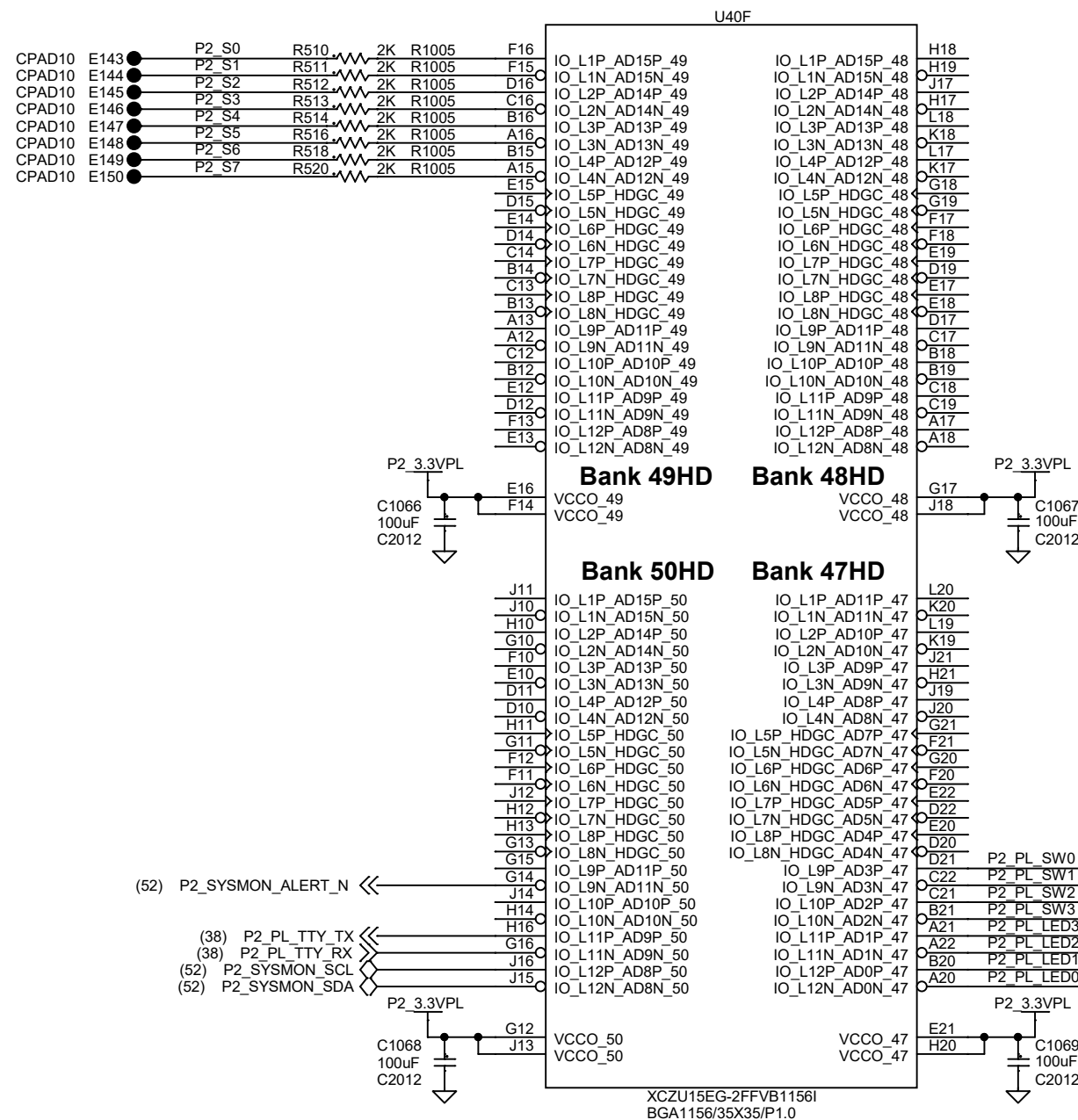
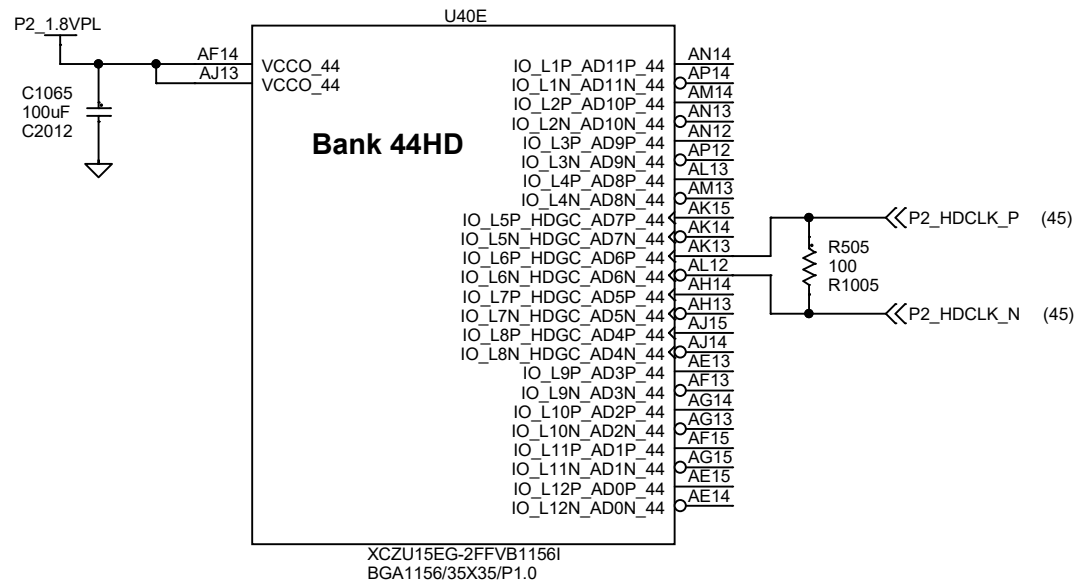
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Designed	HAN InChol	Title	SPC: P2 DDR4 SDRAM
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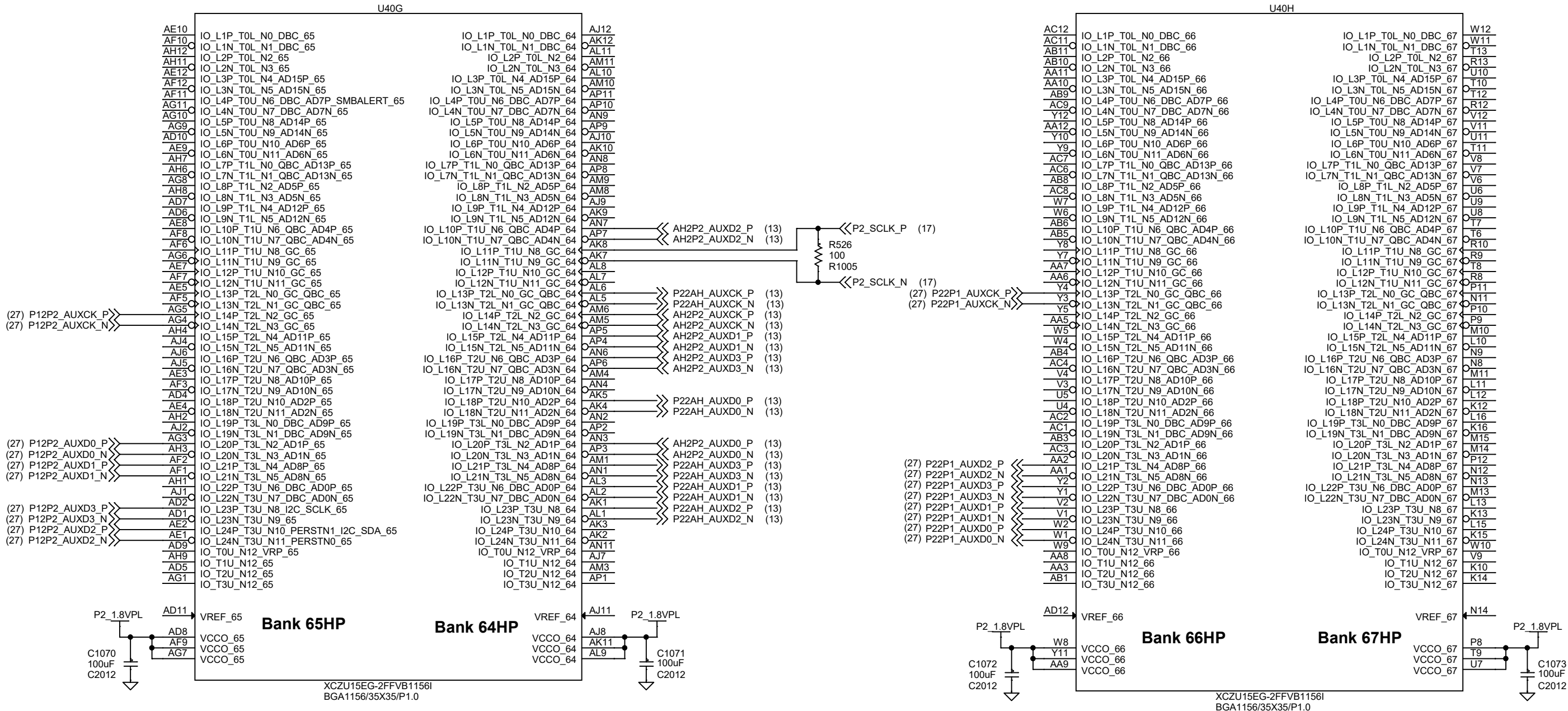


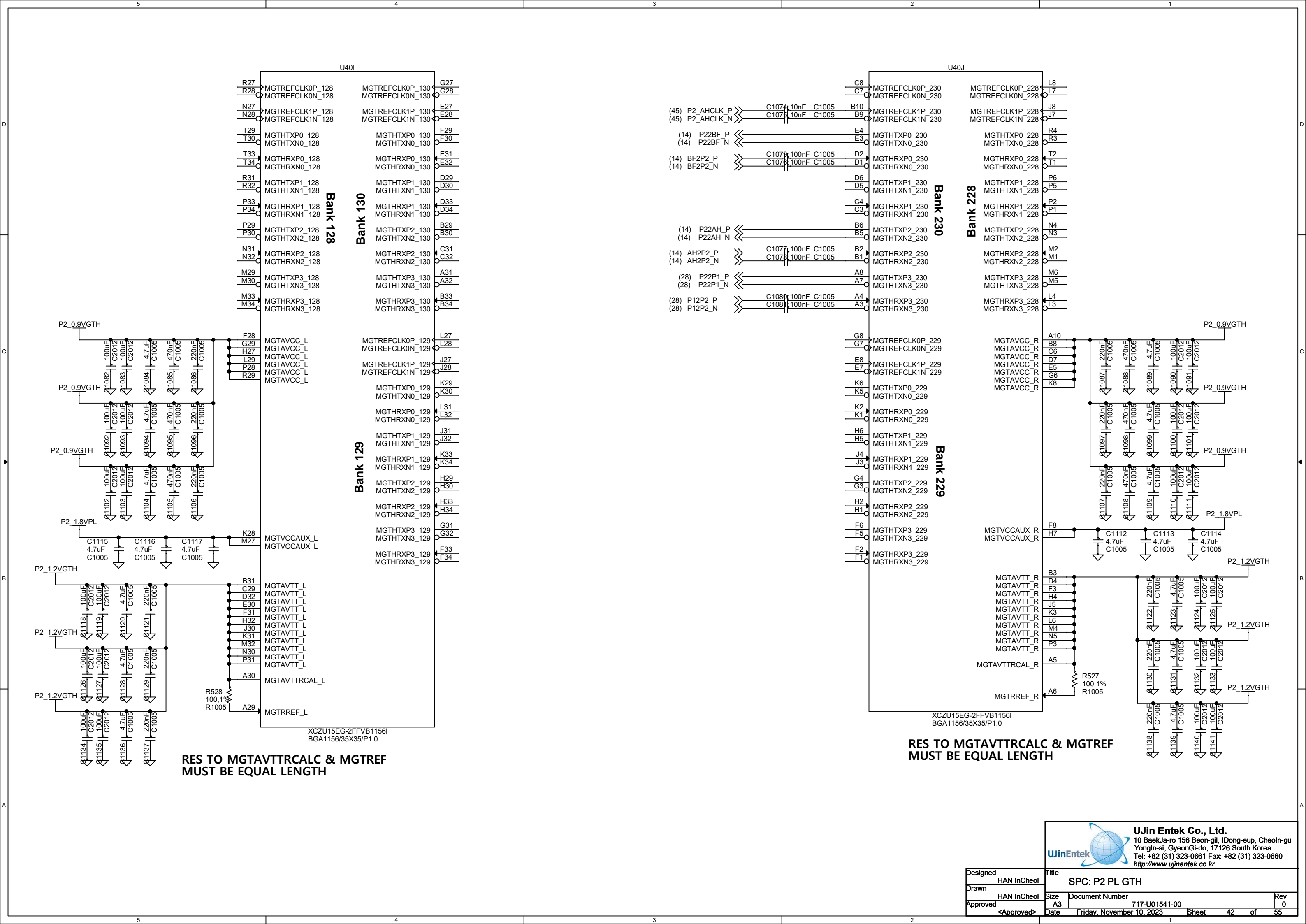


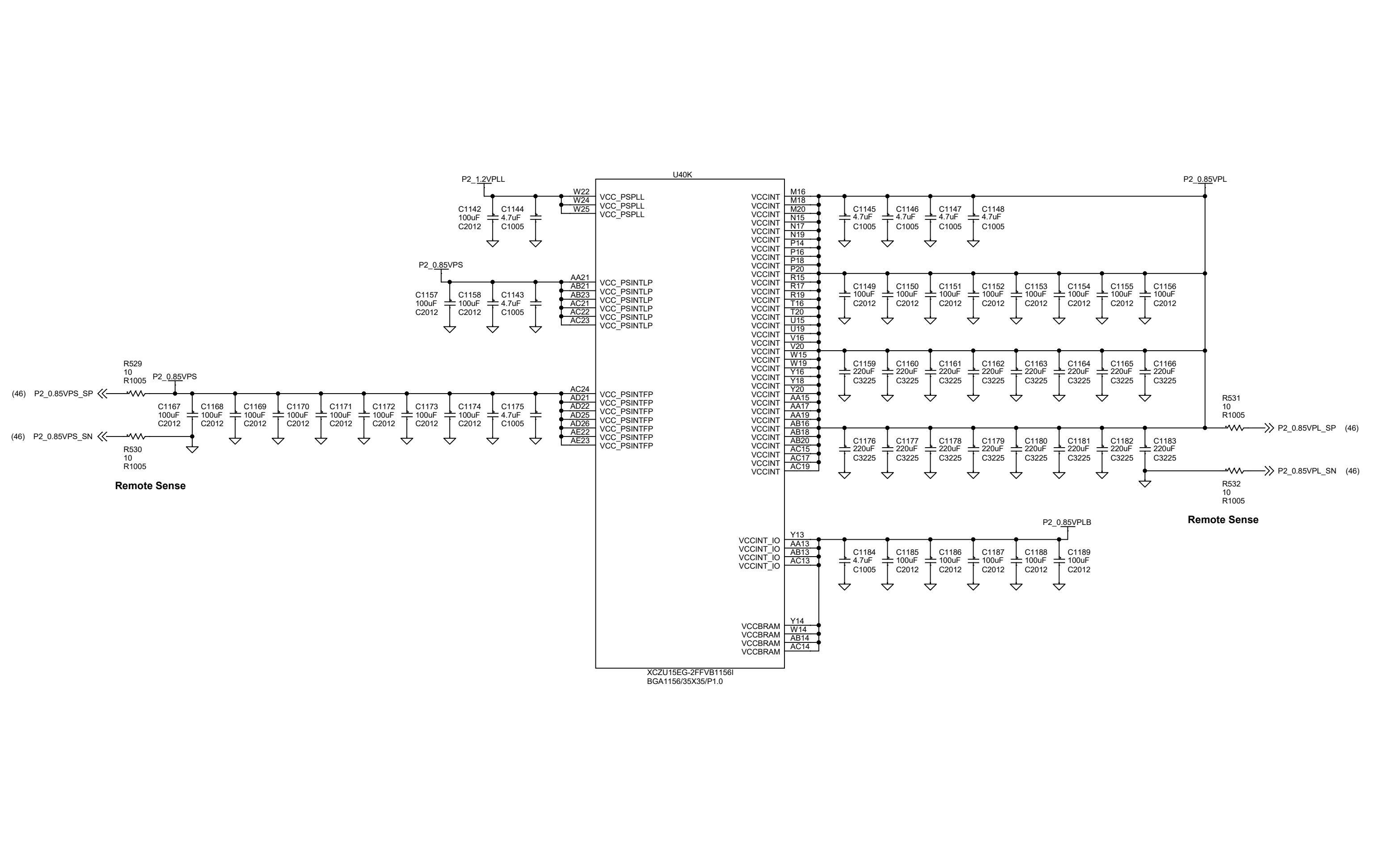
6Gbps max
Z = 50Ω single-ended / 100Ω diffenential
Trace match P/N < 2ps
Trace length < 254mm

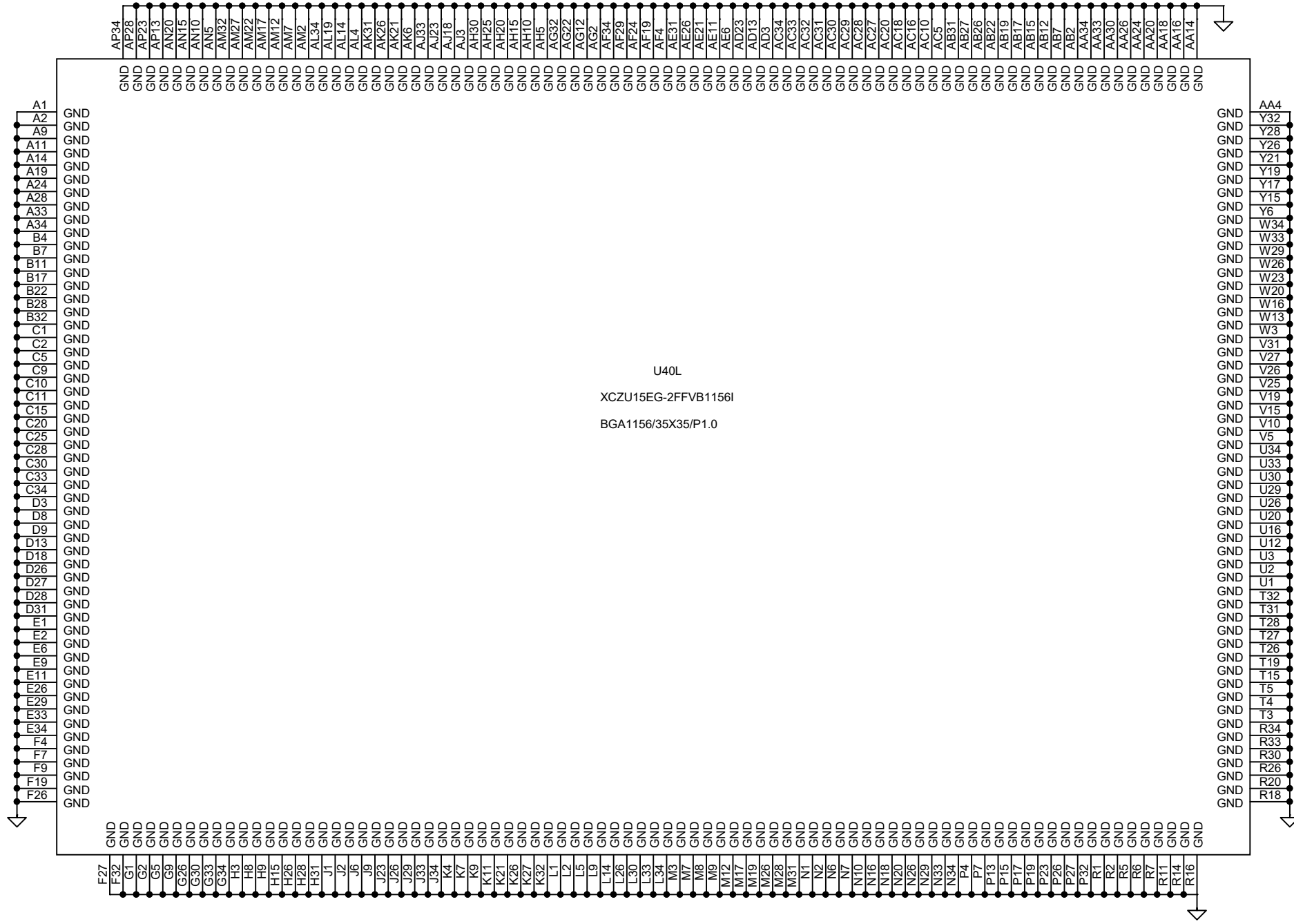


Designed	HAN InCheol	Title	SPC: P2 PL HD Bank
Drawn	HAN InCheol	Size	A3
Approved	<Approved>	Document Number	717-U01541-00
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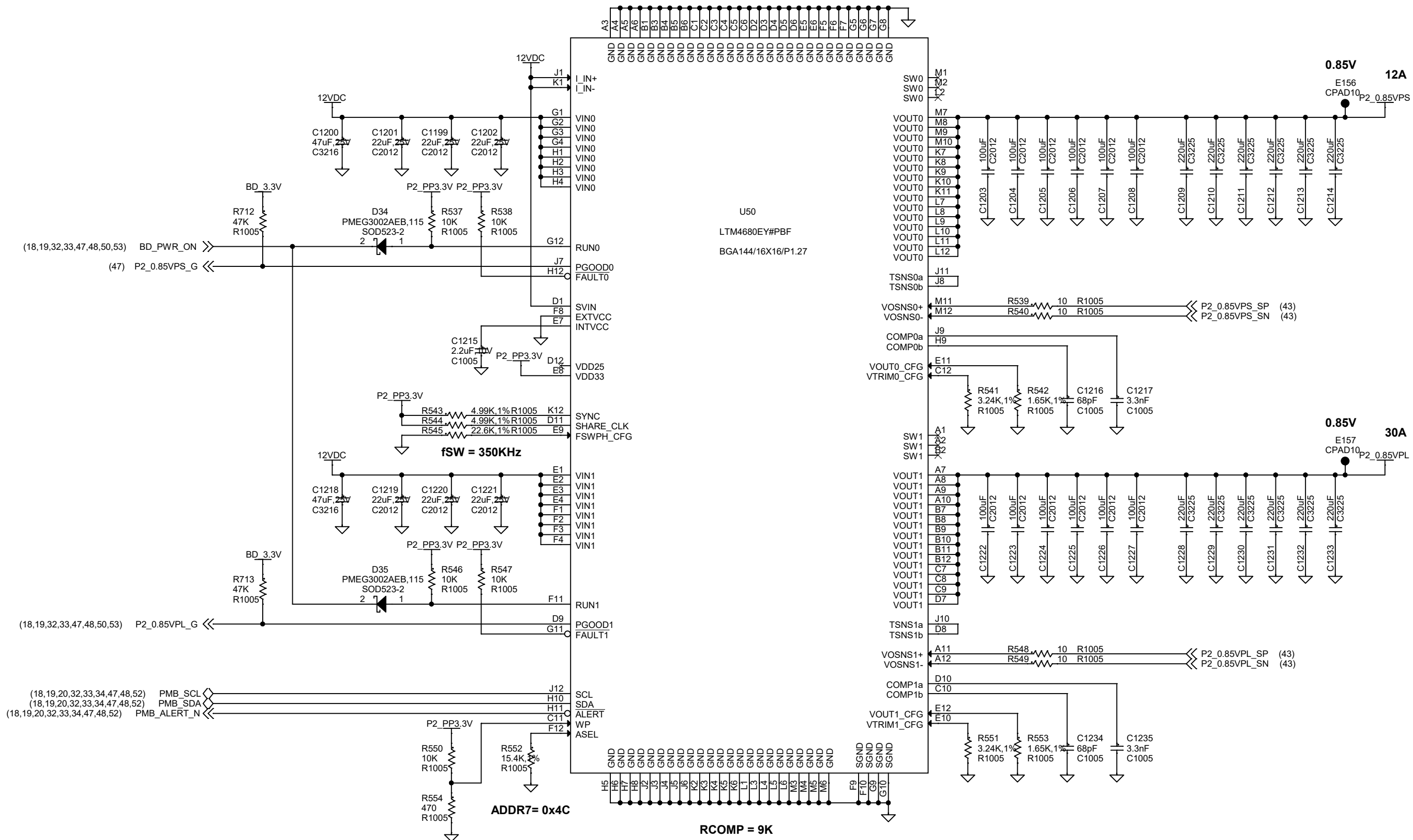


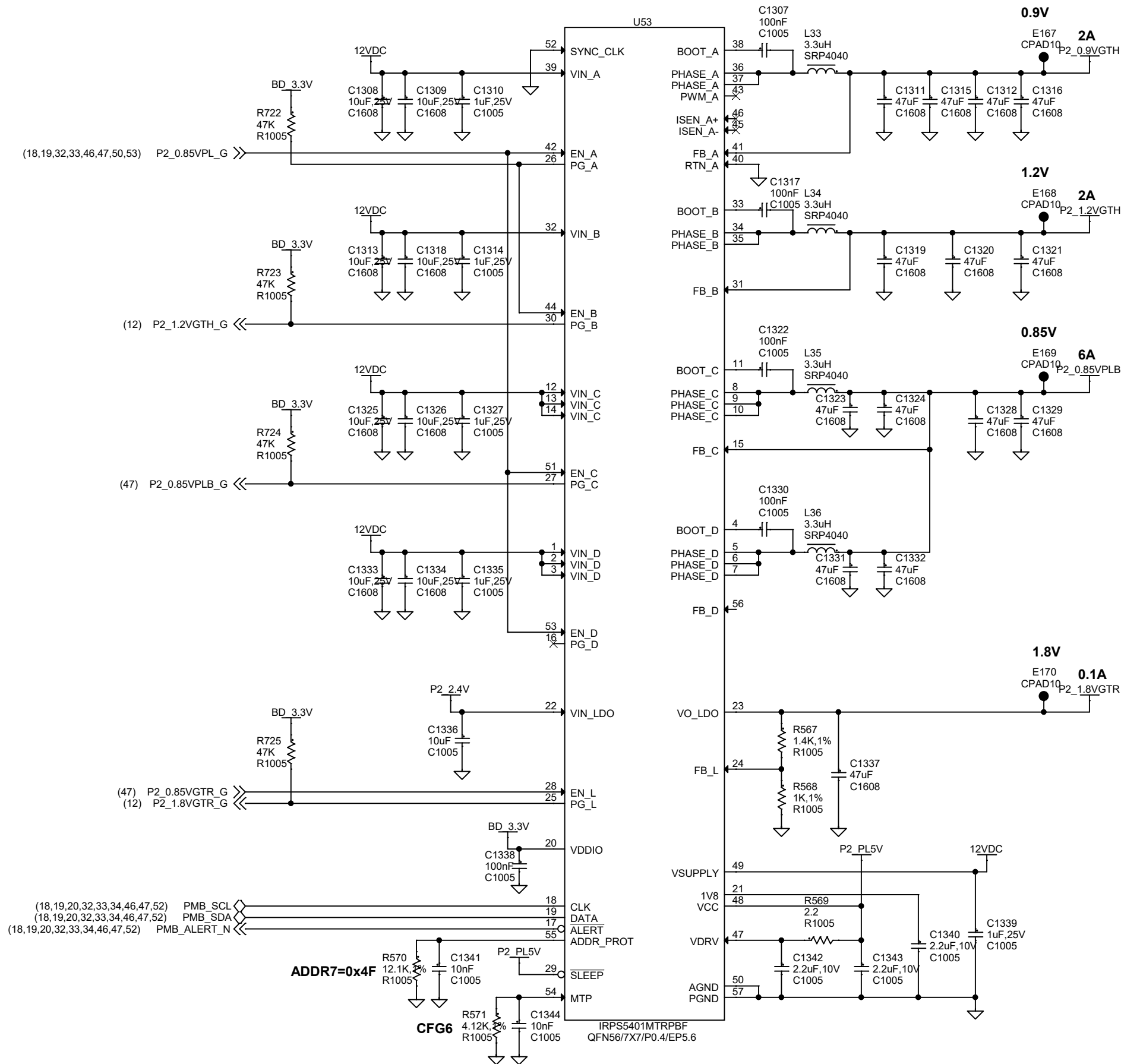




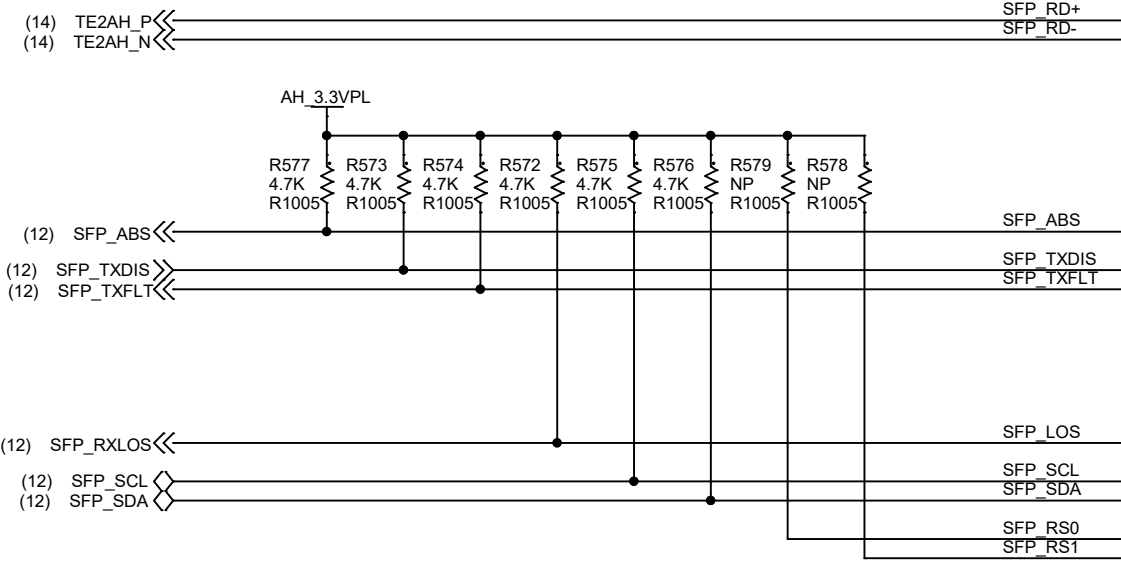
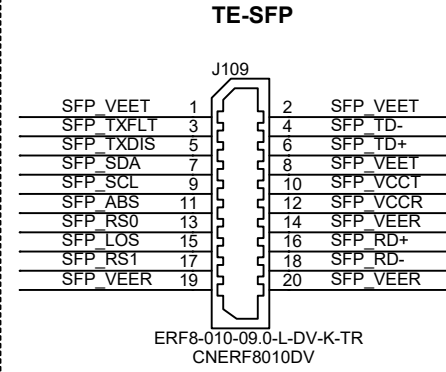
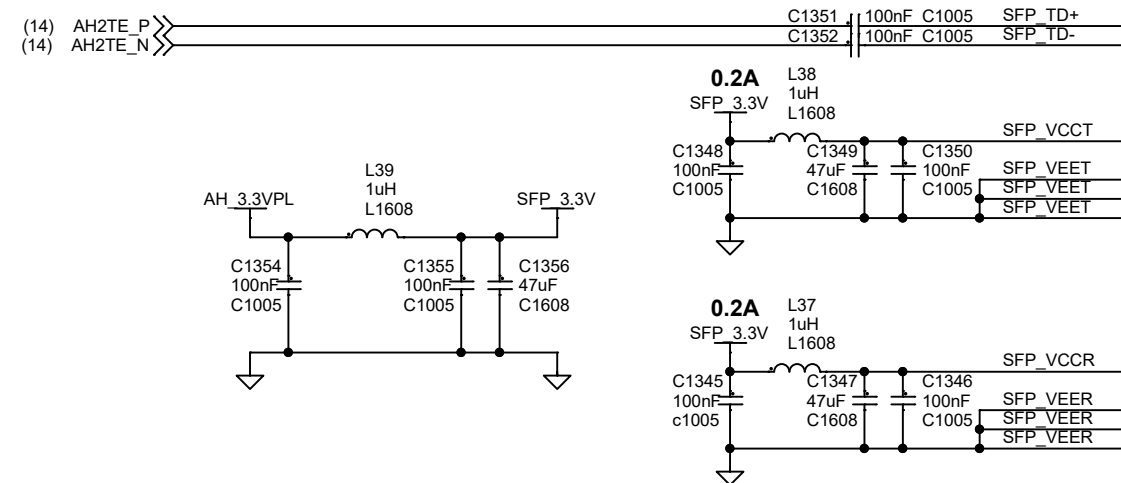
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Designed	HAN InCheol	Title		
Drawn	HAN InCheol	SPC: P1 SoC Ground		
Approved	<Approved>	Size	Document Number	Rev
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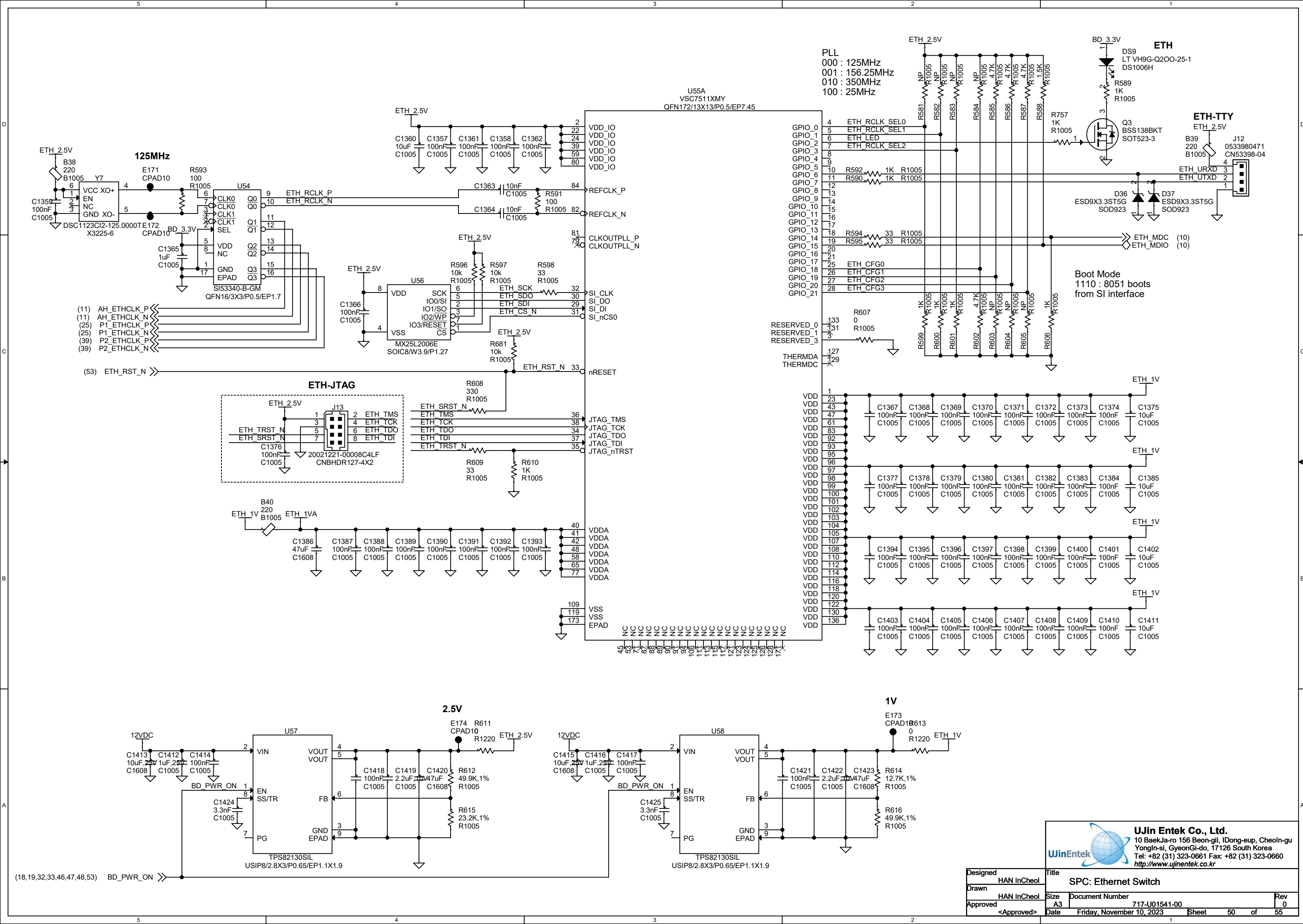


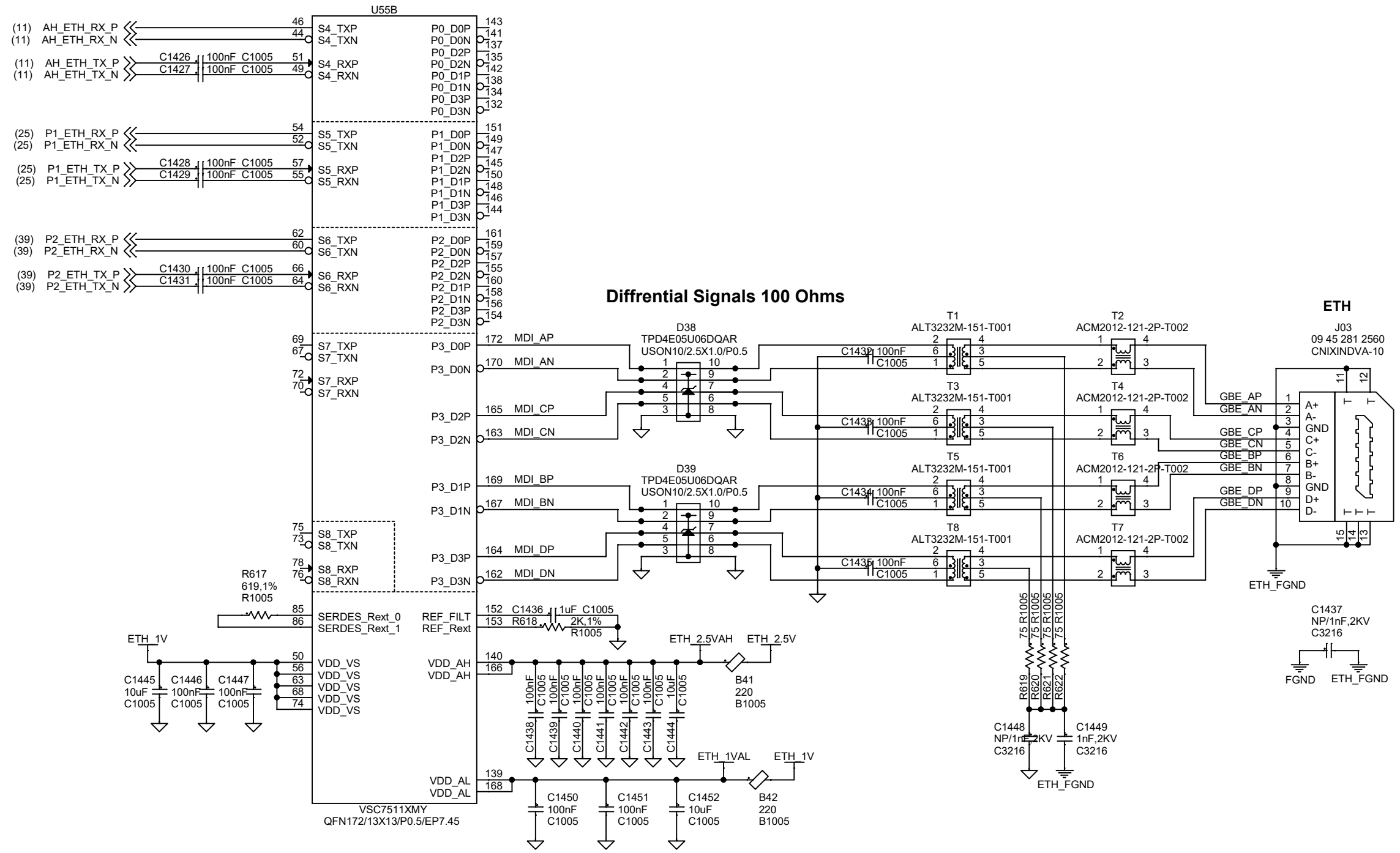
Programmer: USB005

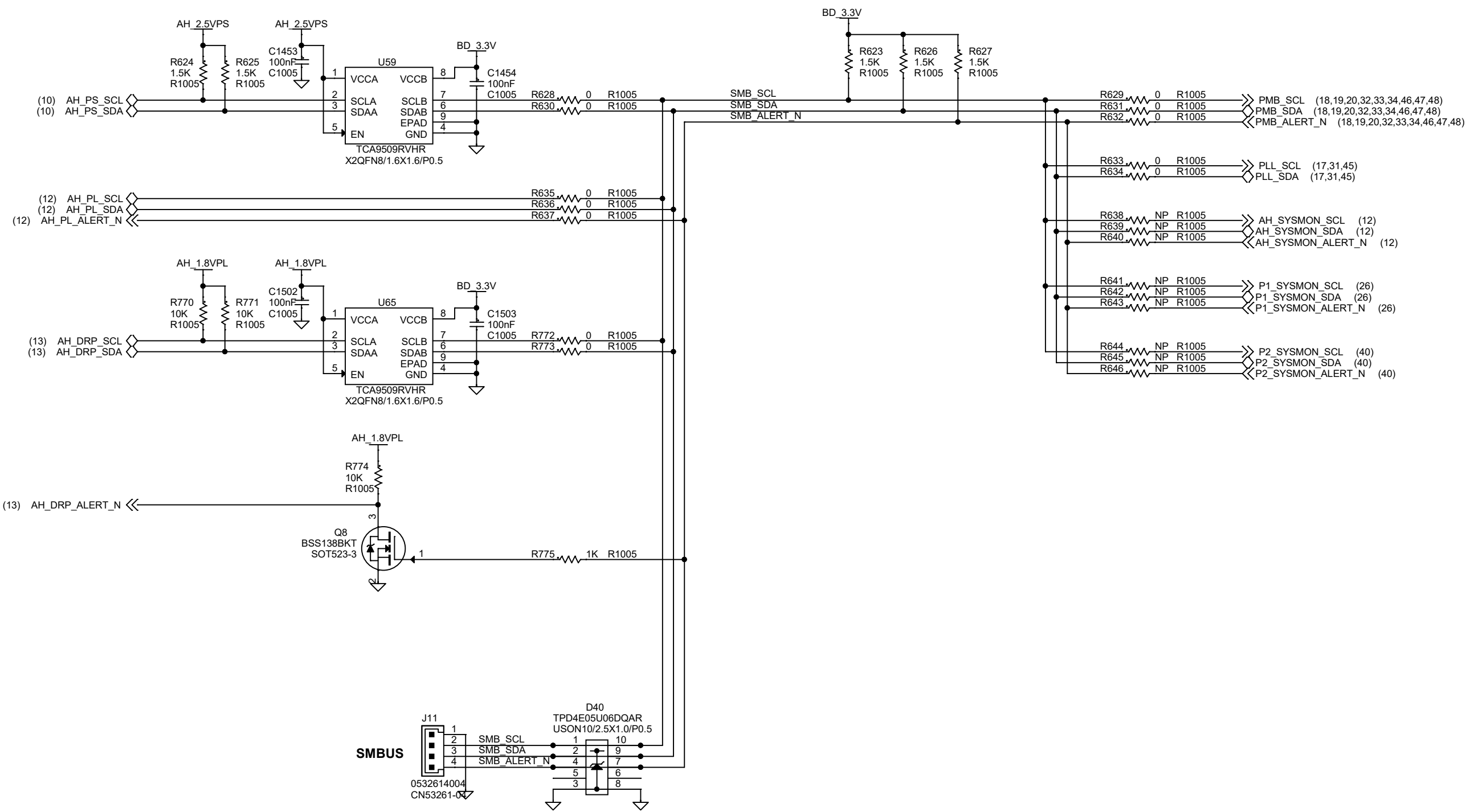


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Designed	HAN InCheol	Title		SPC: SMBus
Drawn	HAN InCheol	Size	Document Number	Rev
Approved	<Approved>	A3	717-U01541-00	0
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(18,19,32,33,46,47,48,50)

