

Blue Shark - II


신호처리보드

(Signal Processing Circuit)

Rev.	Date	Description	Page	Remark
0	2023.10.04	Initial design		16Layers, t=2.4

Todo

UJinEntek



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Digned

Drawn

Approved

HAN InCheol

HAN InCheol

<Approved>

Title

Signal Processing Circuit

Size

A3

Document Number

717-U01541-00

Date

Friday, November 10, 2023

Sheet

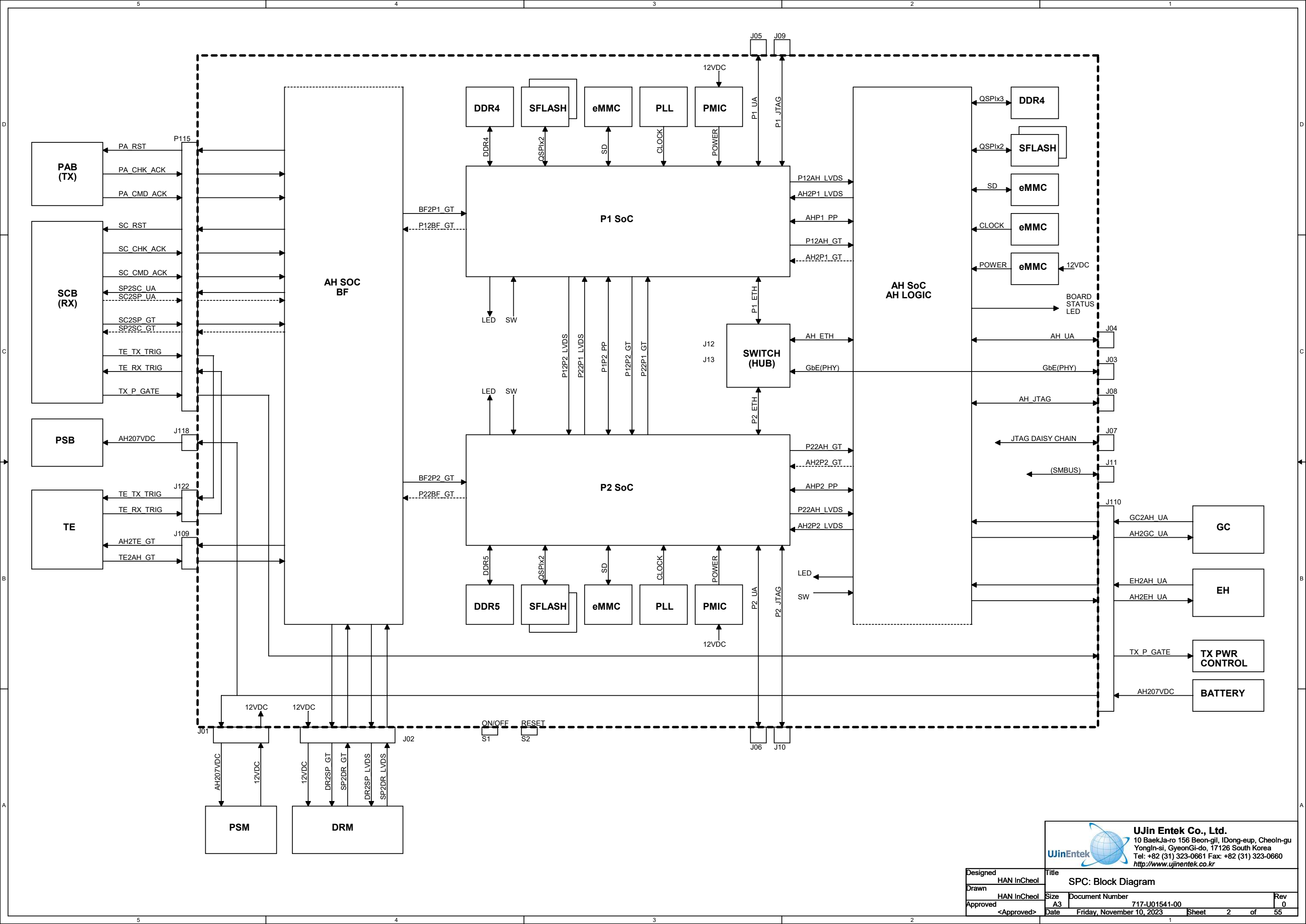
1

of


55

Rev

0





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Designed HAN InCheol		Title SPC: Block Diagram	
Drawn HAN InCheol		Size A3	Document Number 717-U01541-00
Approved <Approved>		Date Friday, November 10, 2023	Rev 0
		Sheet 3	of 55

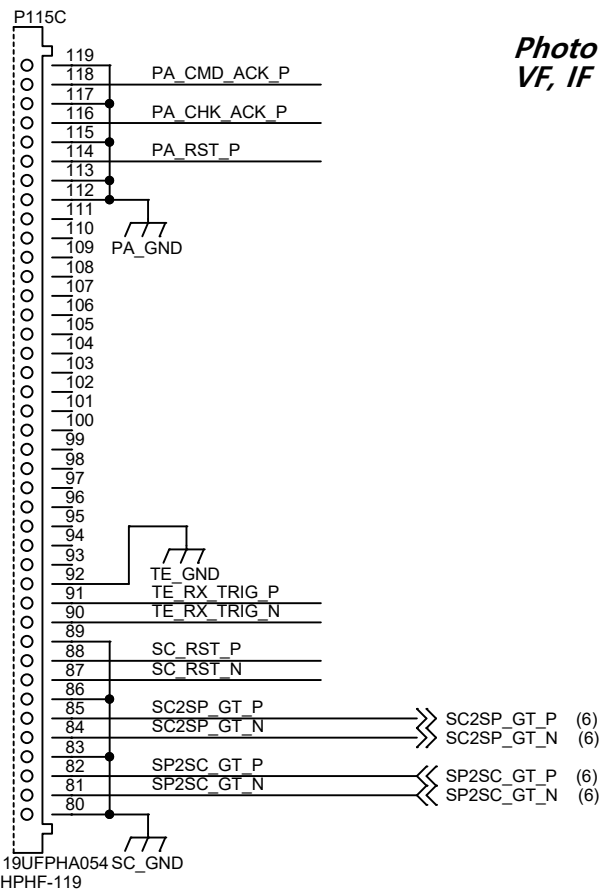
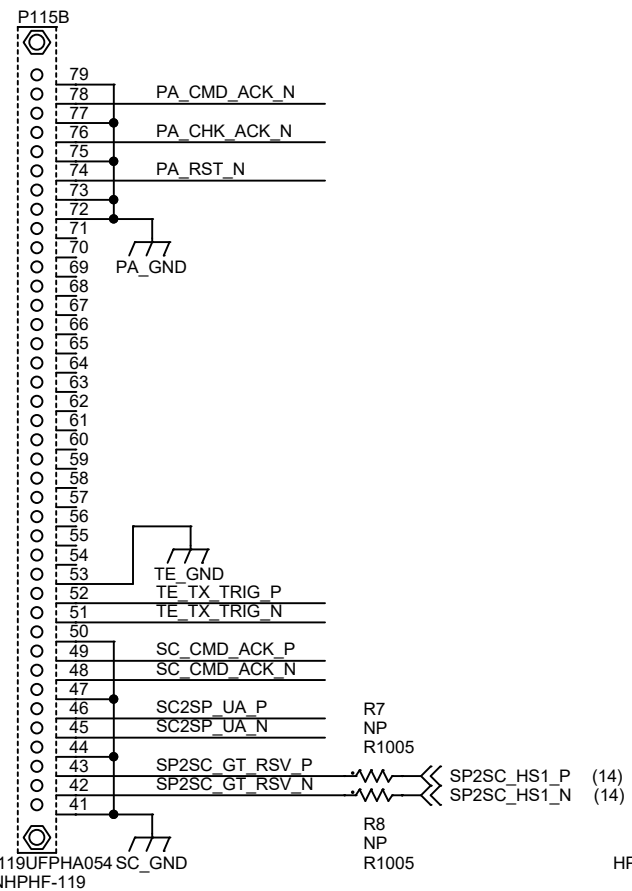
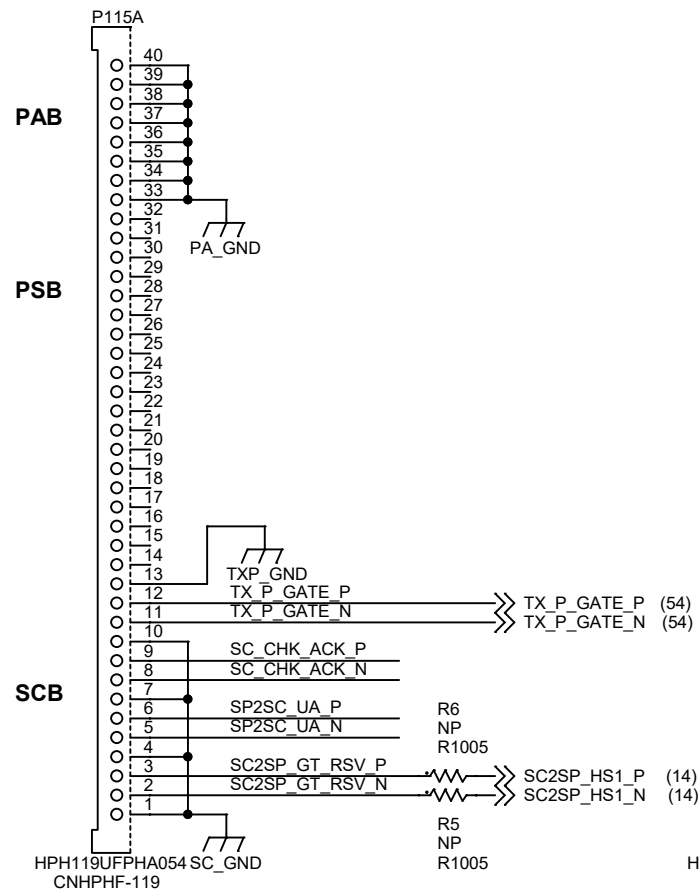
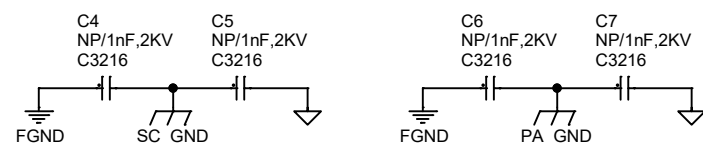
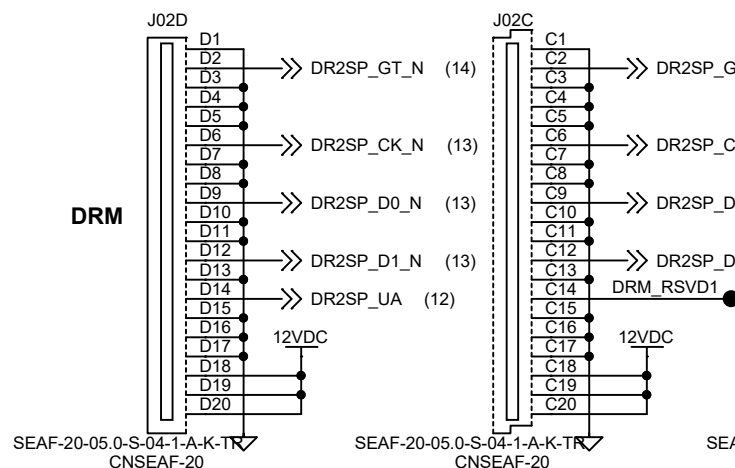
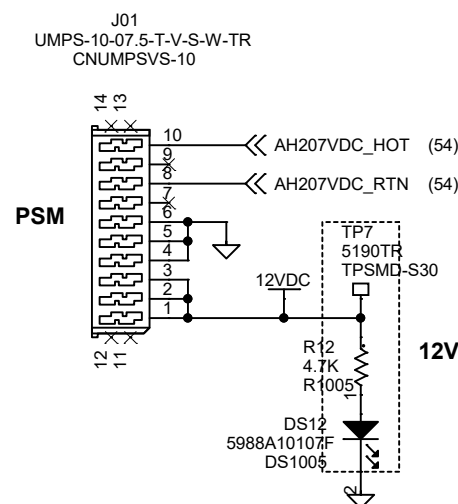
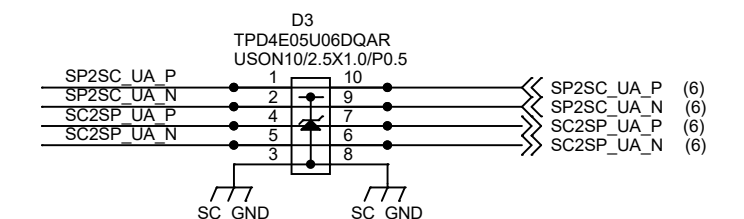
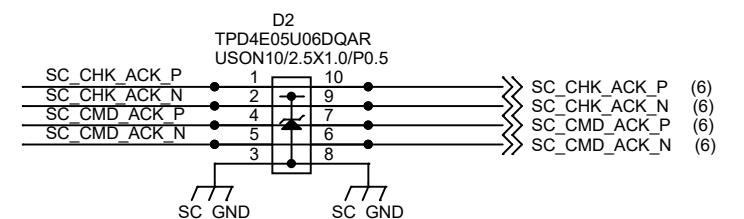
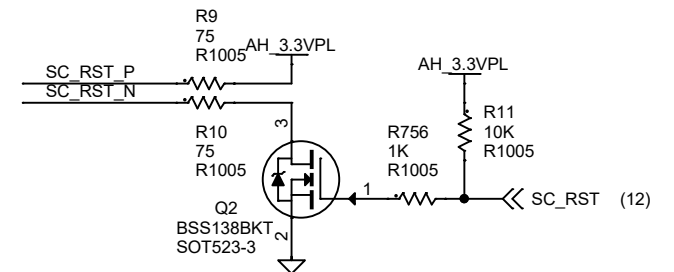
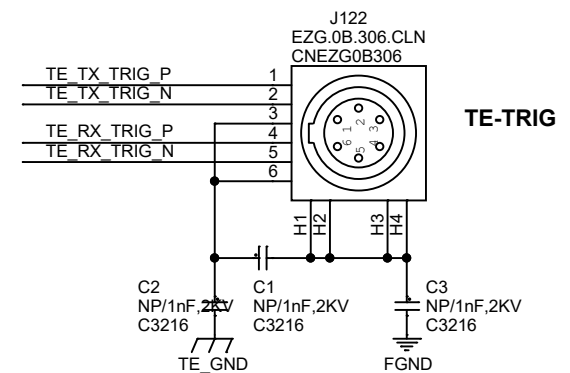
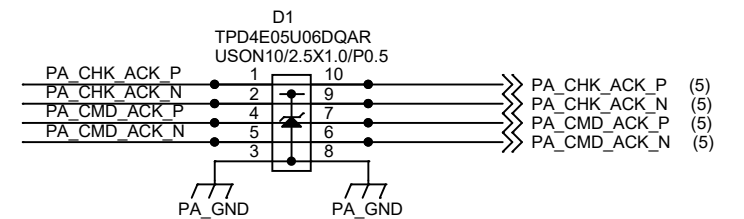
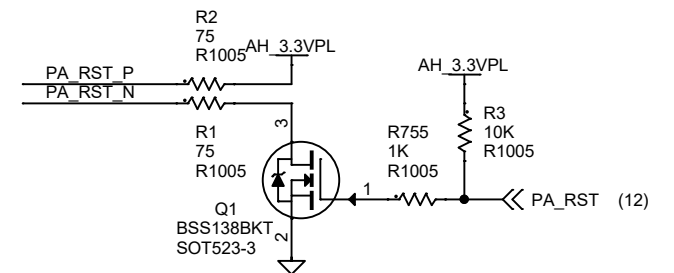
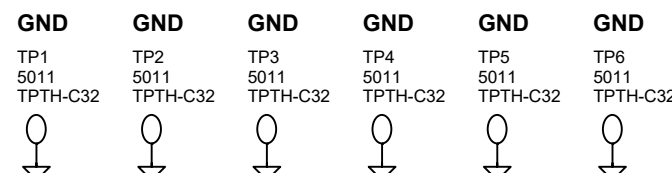
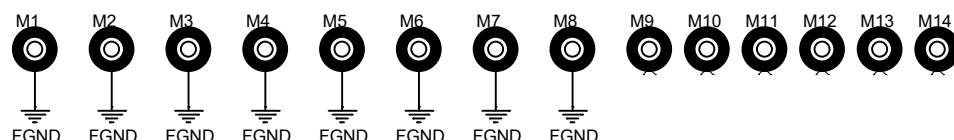


Photo coupler의
VF, IF 확인 필요

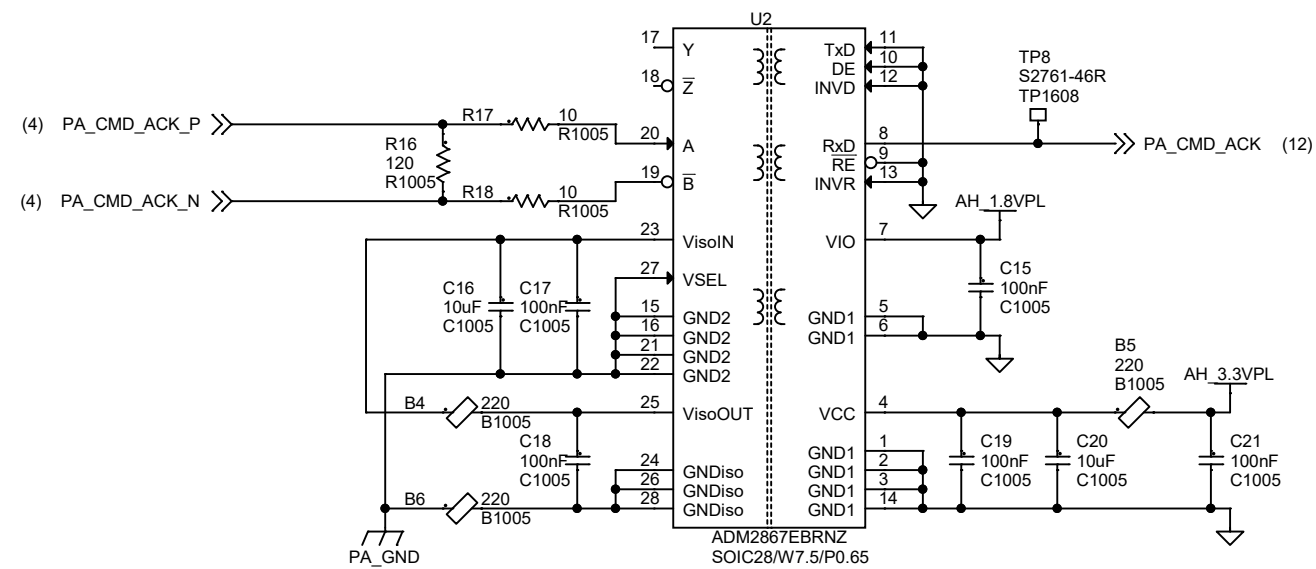
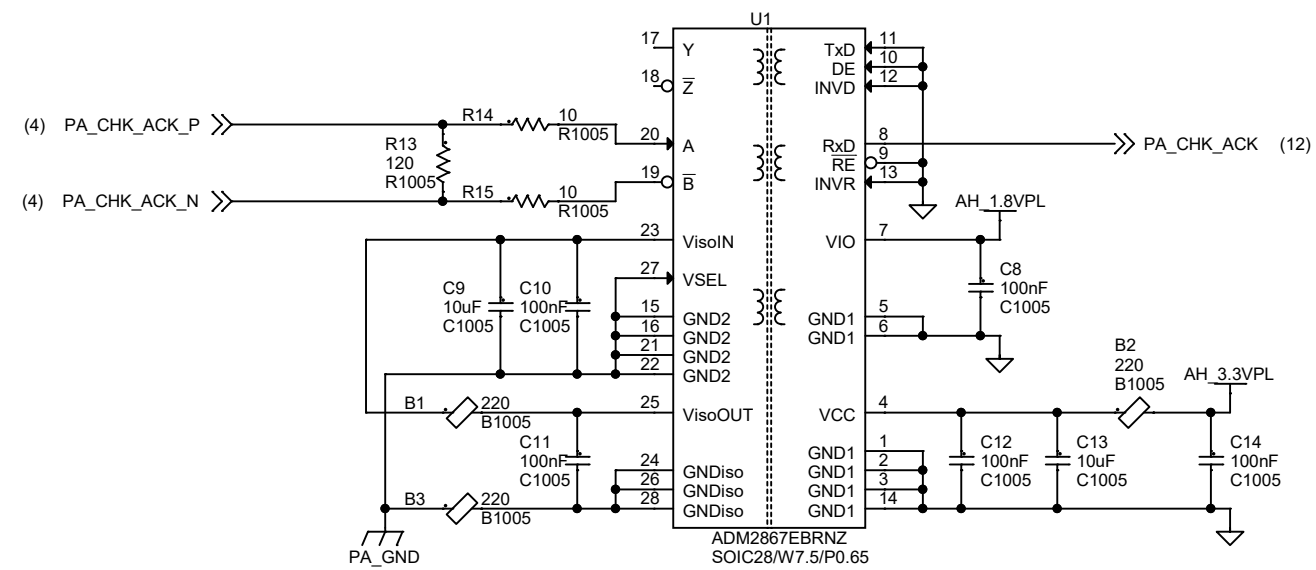


모두 NTH로 수정

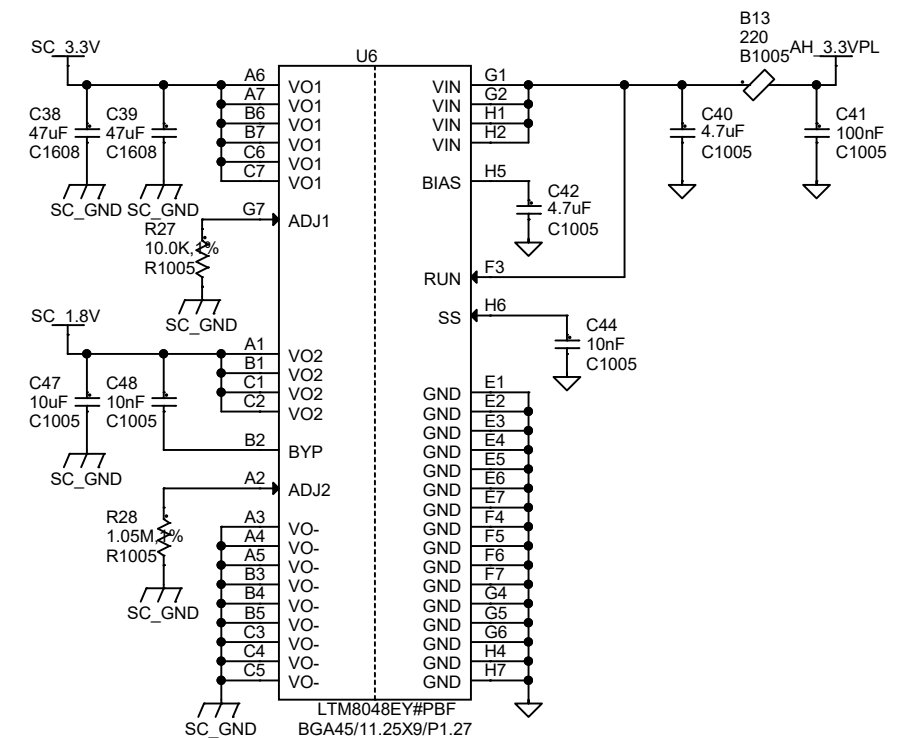
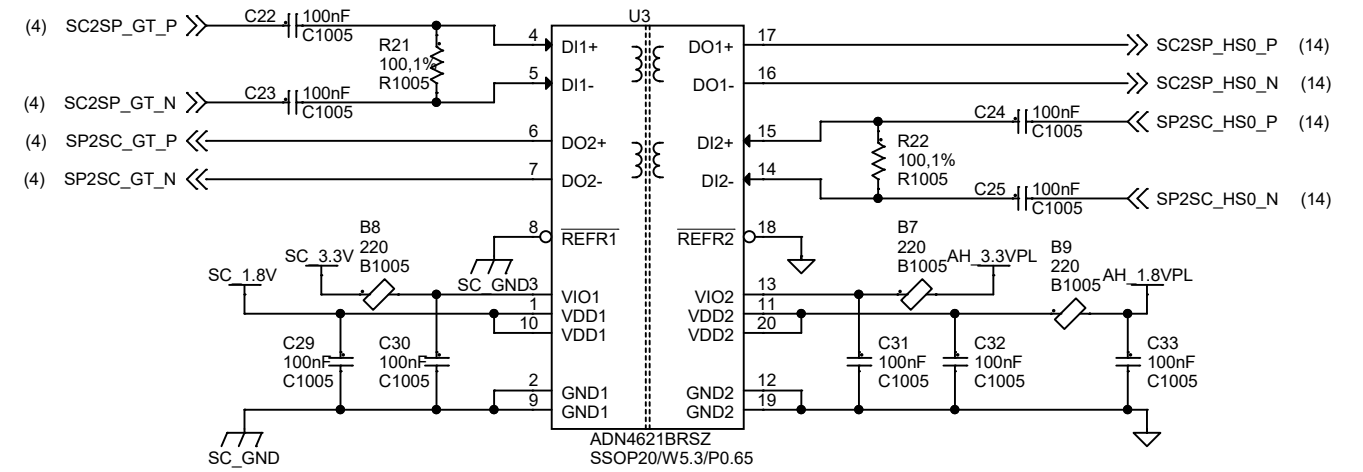
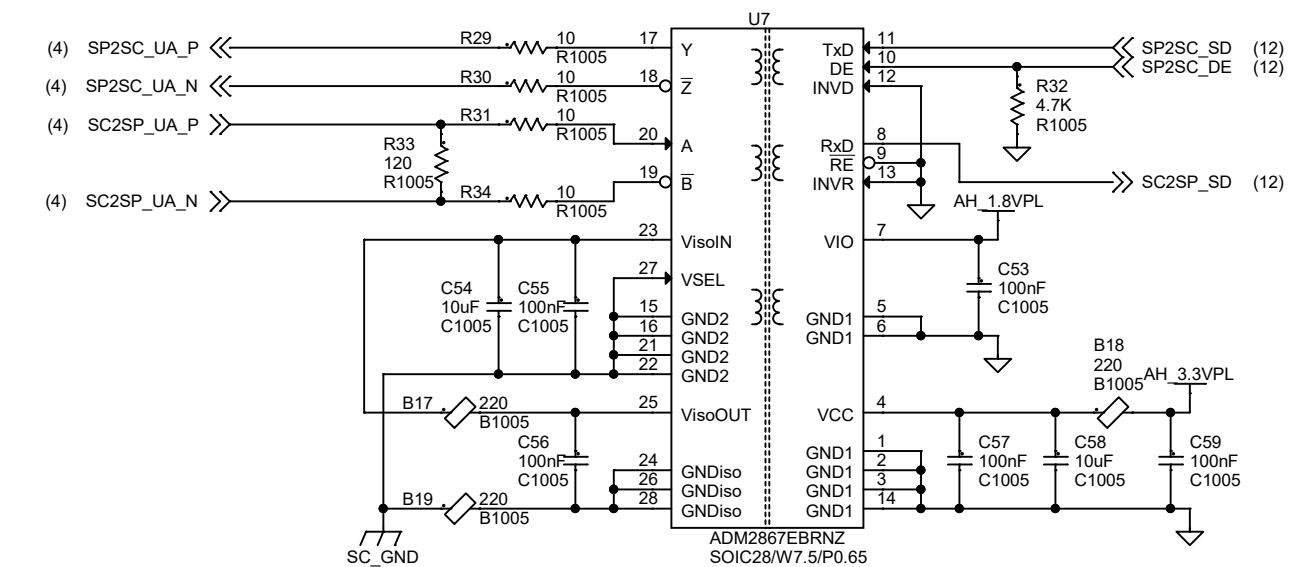
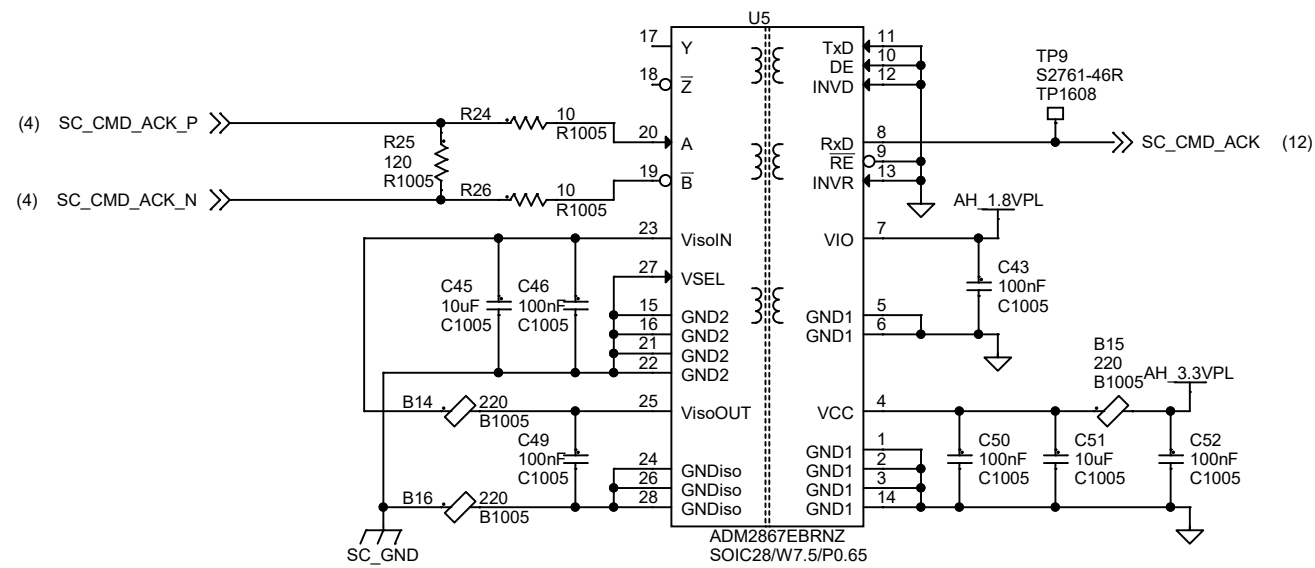
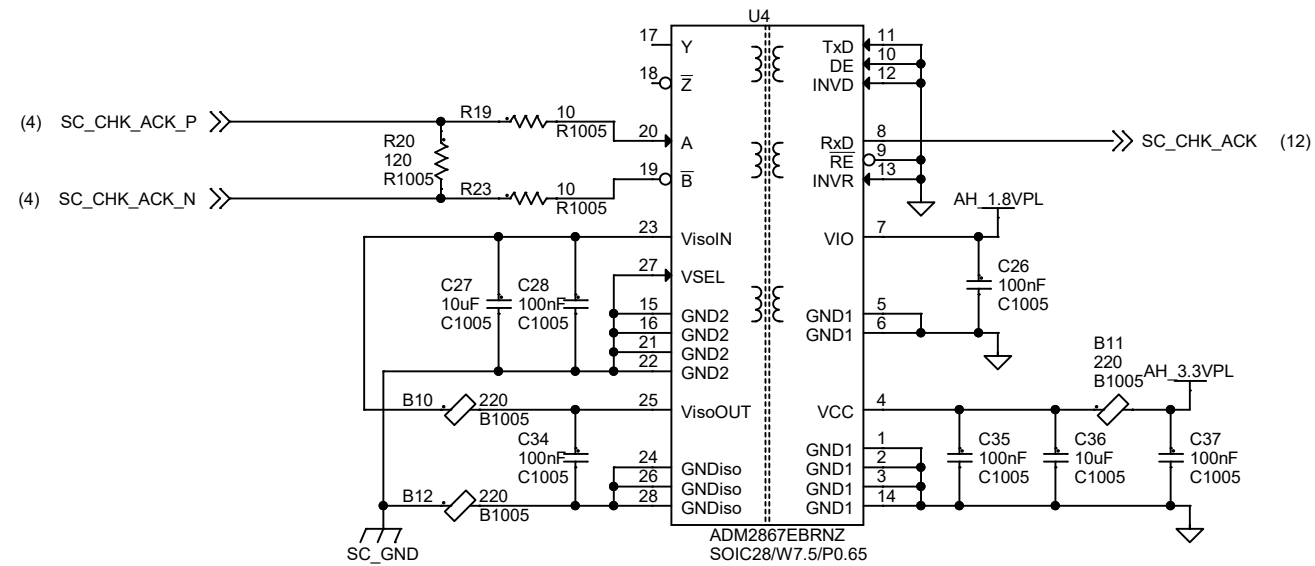


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Designed	HAN InCheol	Title	SPC: PAB & SCB Interface
Drawn	HAN InCheol	Size	A3
Approved	<Approved>	Document Number	717-U01541-00
		Date	Friday, November 10, 2023
		Sheet	4 of 55
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Designed	HAN InCheol		Title		SPC: PAB Transceiver	
Drawn	HAN InCheol		Size		A3	
Approved	<Approved>		Document Number		717-U01541-00	
			Date		Friday, November 10, 2023	
			Sheet		5 of 55	

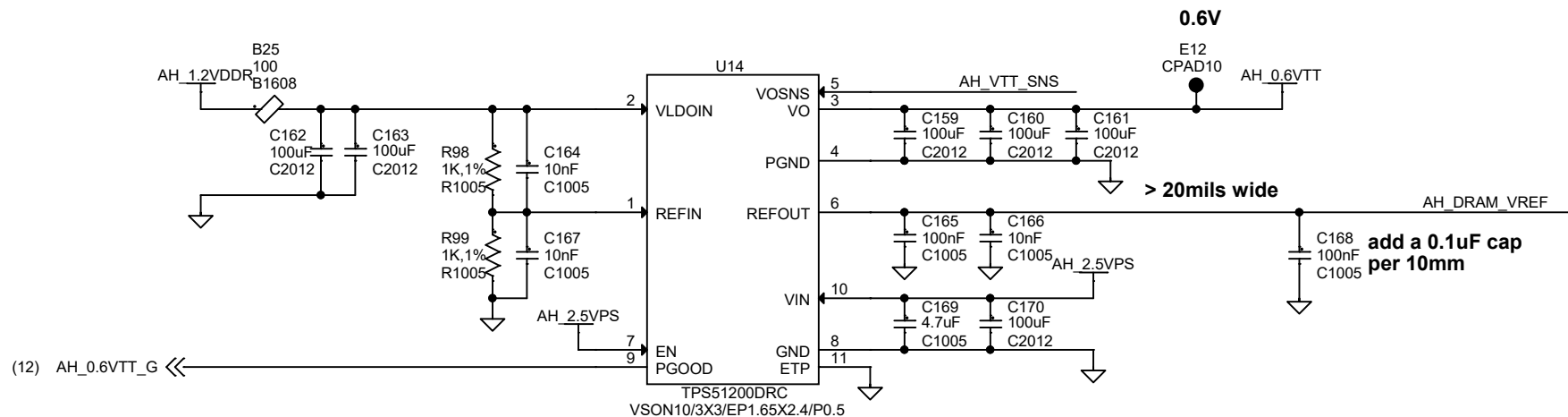
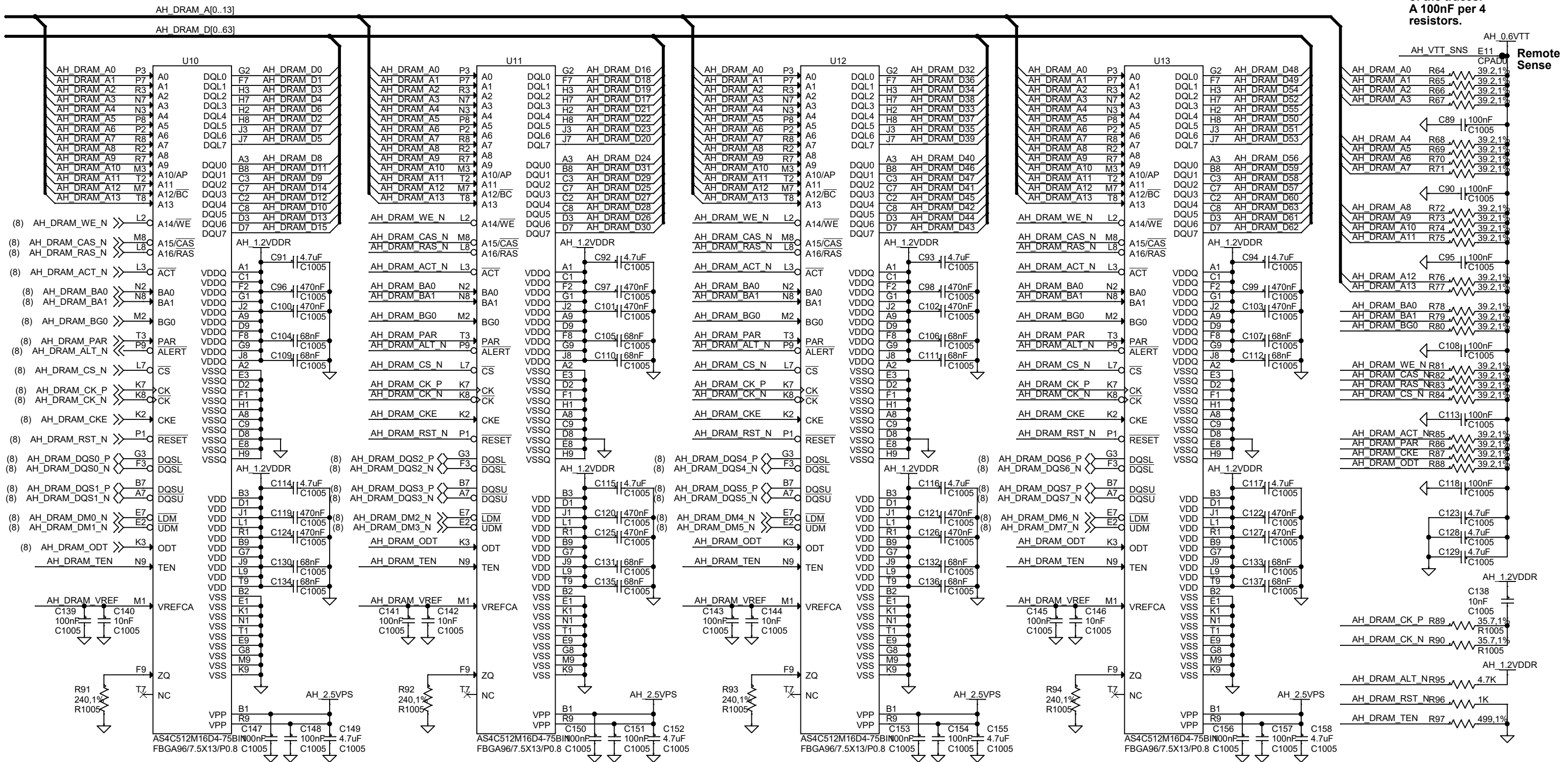


(8) AH_DRAM_A[0..13] >> AH_DRAM_A[0..13]
(8) AH_DRAM_D[0..63] << AH_DRAM_D[0..63]

Fly-by topology

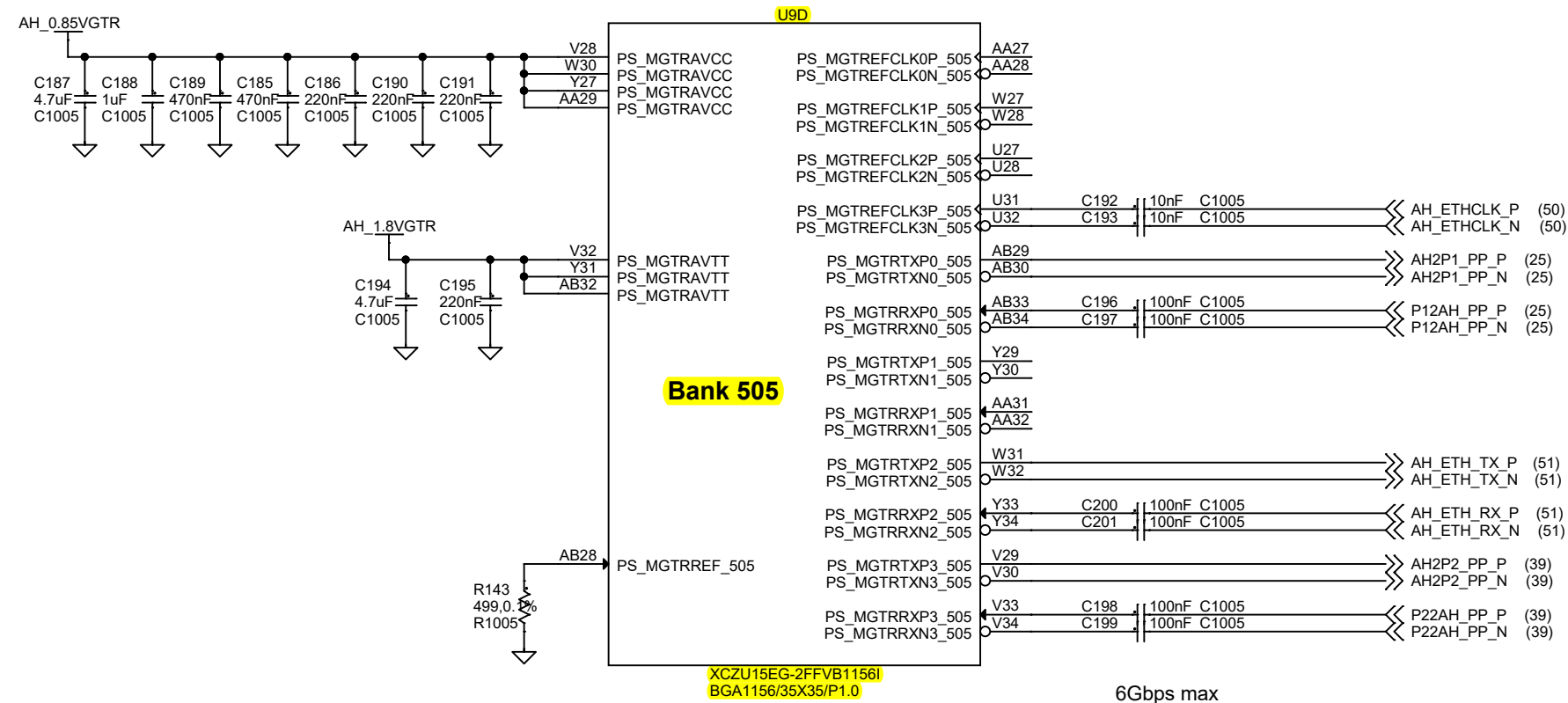
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Place at the end of the traces.
A 100nF per 4 resistors.

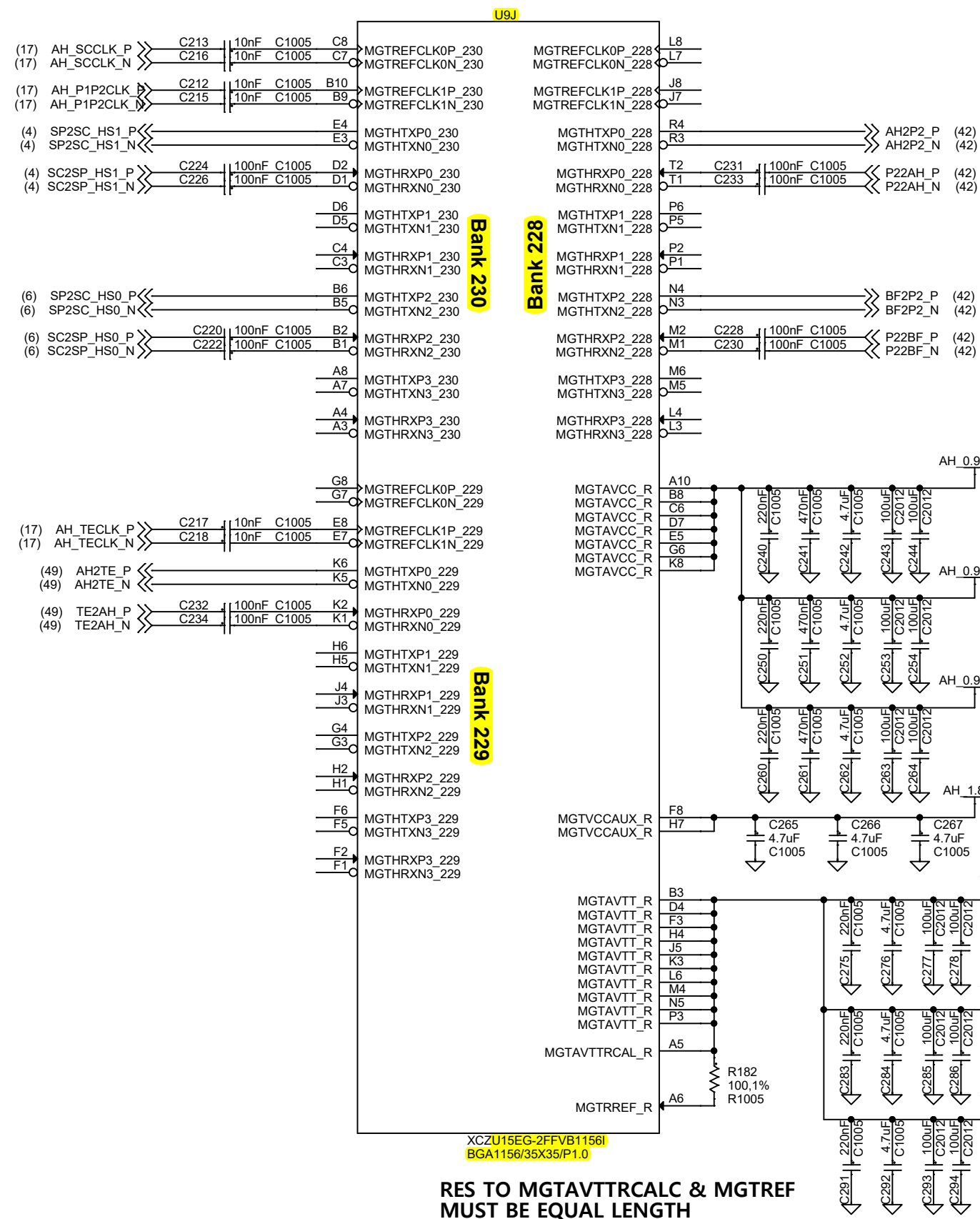
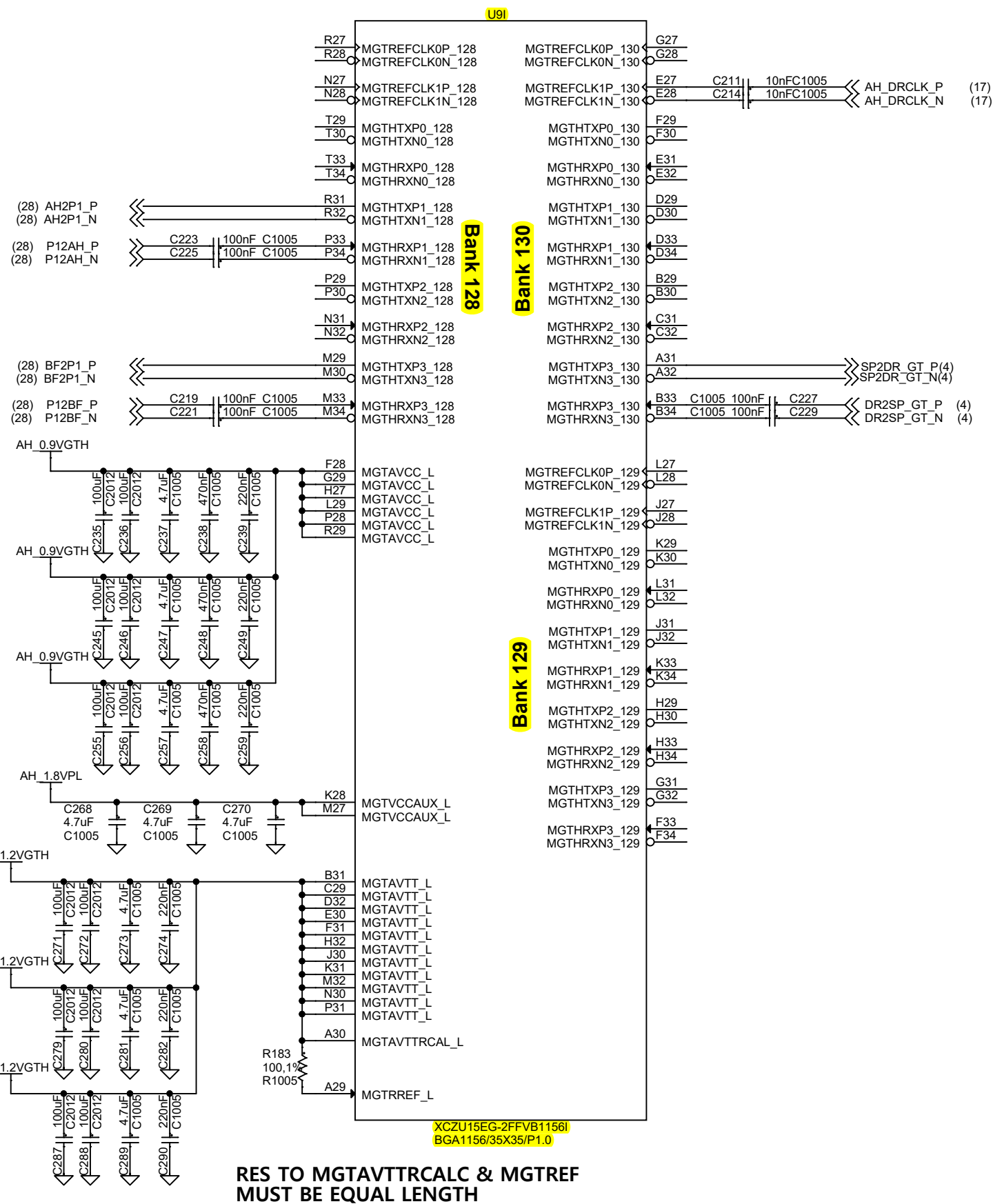


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Designed	HAN InChol	Title	SPC: AH DDR4 SDRAM
Drawn	HAN InChol	Size	A3
Approved	<Approved>	Document Number	717-U01541-00
		Date	Thursday, November 16, 2023
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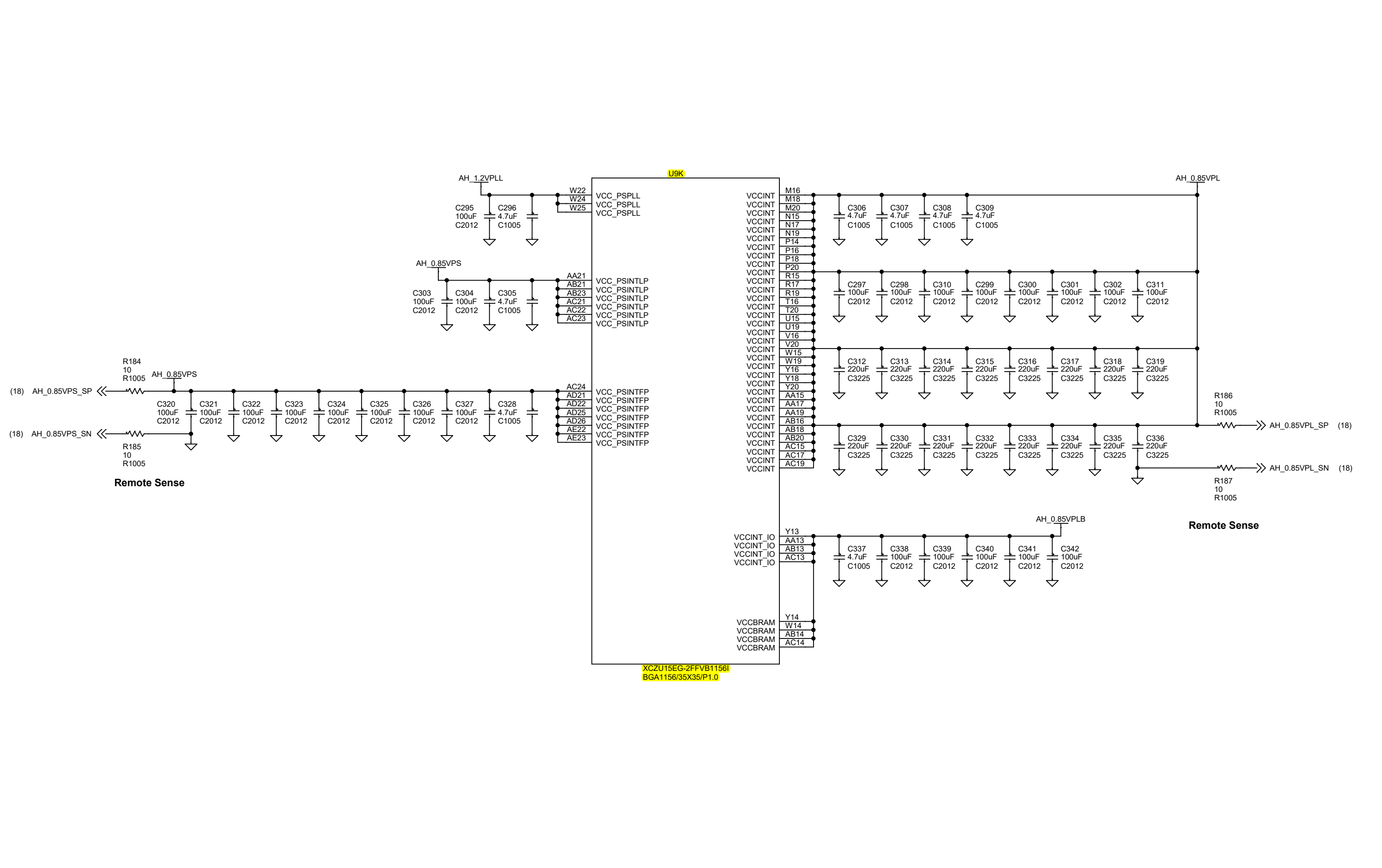


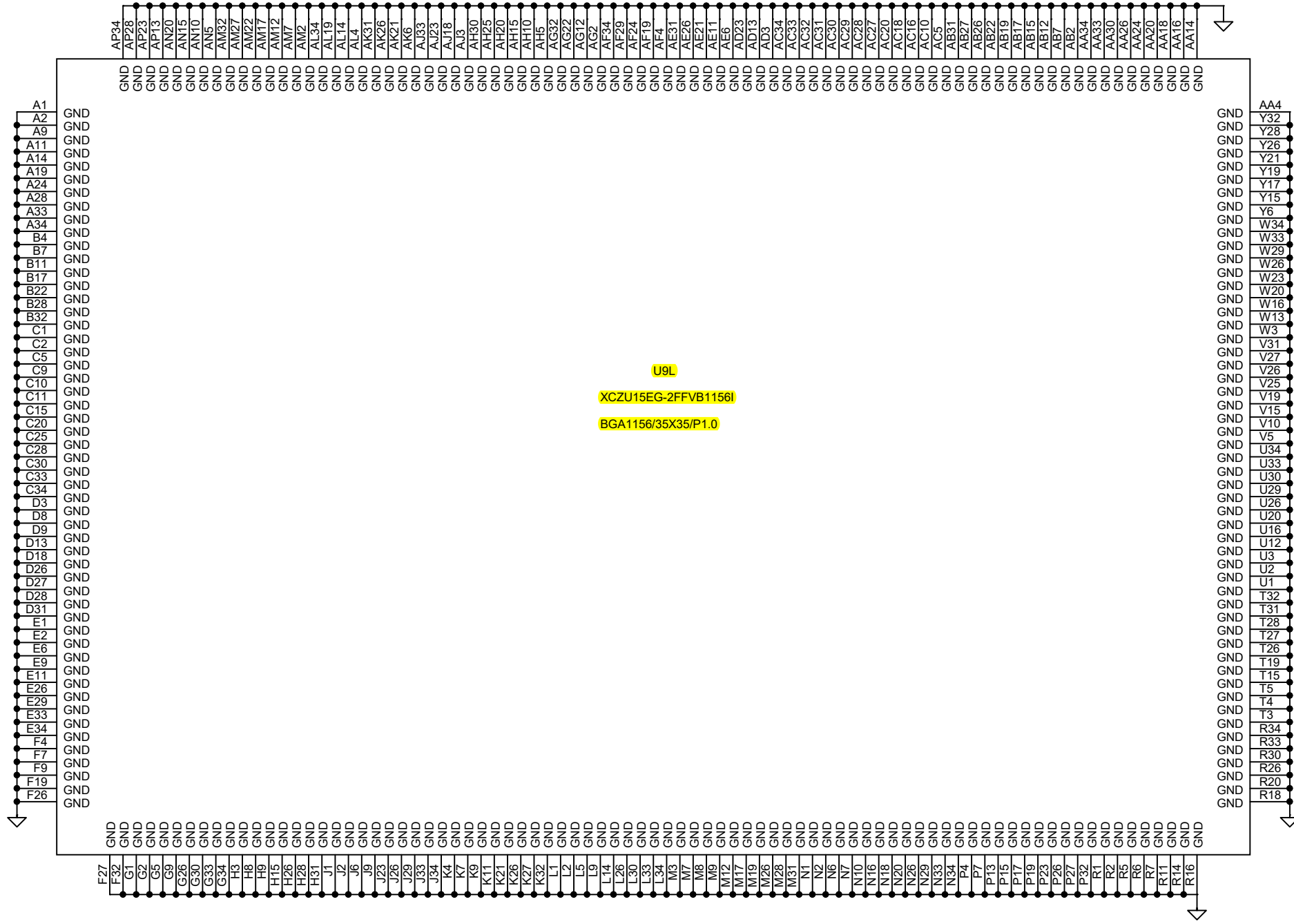
6Gbps max
Z = 50Ω single-ended / 100Ω diffenential
Trace match P/N < 2ps
Trace length < 254mm



RES TO MGTAVTTRCALC & MGTREF
MUST BE EQUAL LENGTH

Designed	Title			
HAN InCheol	SPC: AH PL GTH			
Drawn				
HAN InCheol	Size	Document Number	Rev	
Approved	A3	717-U01541-00	0	
<Approved>	Date	Friday, November 10, 2023	Sheet	14 of 55

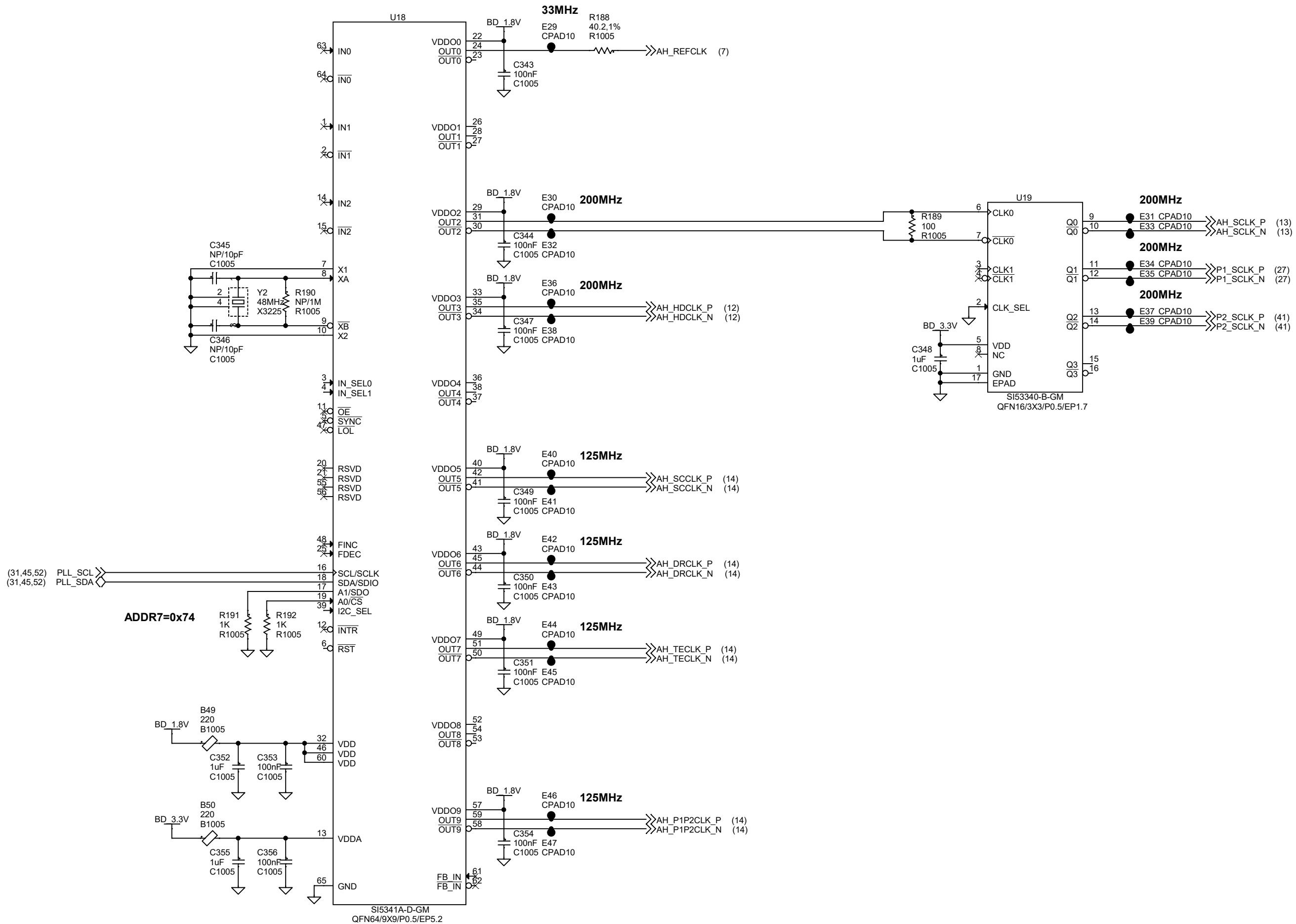







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Designed	HAN InCheol	Title		
Drawn	HAN InCheol	SPC: AH SoC Ground		
Approved	<Approved>	Size	Document Number	Rev
		A3	717-U01541-00	0
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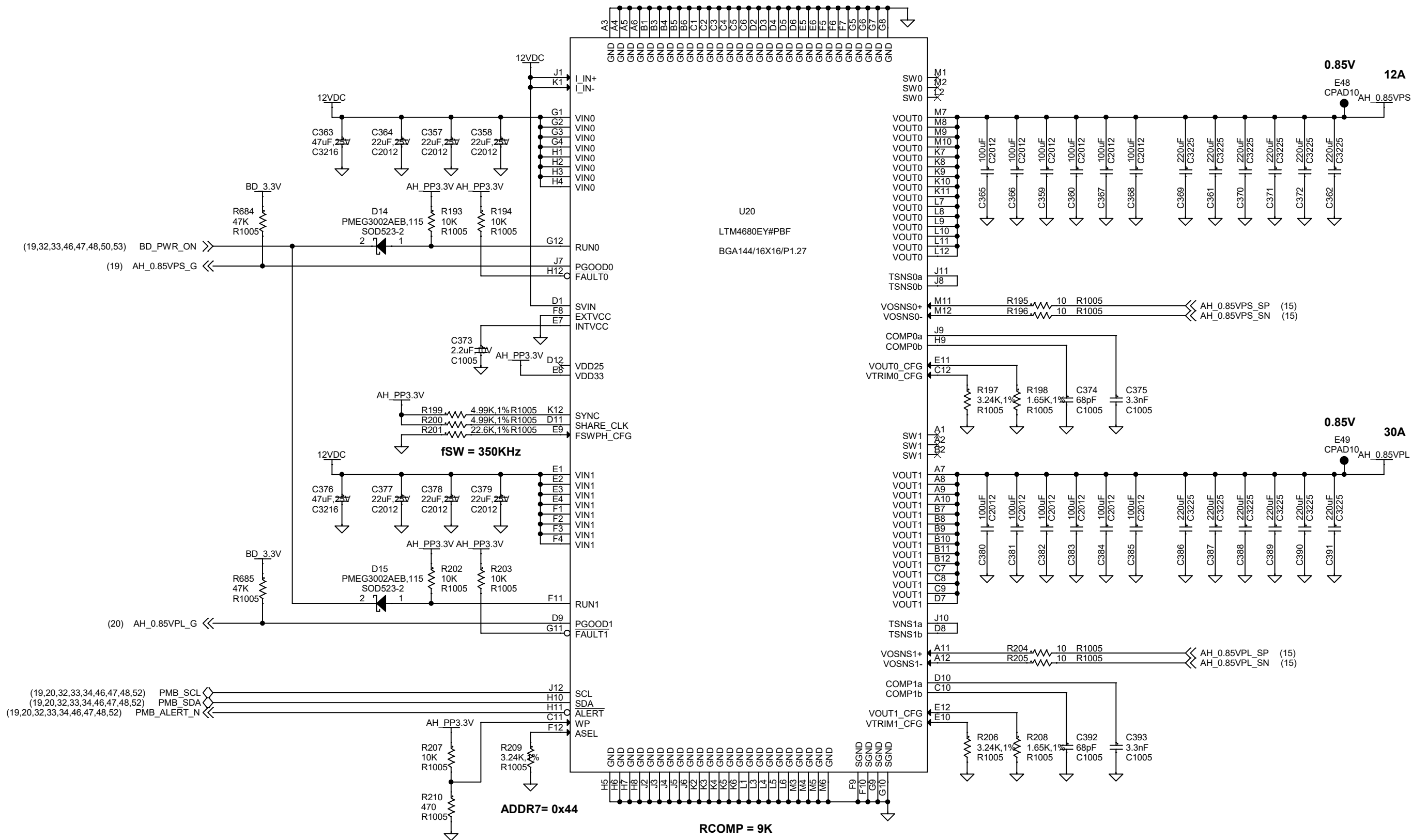


Programmer: ClockBuilder Field Programmer Kit (CBPROG-DONGLE)




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Designed	HAN InCheol	Title		SPC: AH Clock Generator	
Drawn	HAN InCheol	Size	A3	Document Number	717-U01541-00
Approved	<Approved>	Date	Friday, November 10, 2023	Sheet	17 of 55
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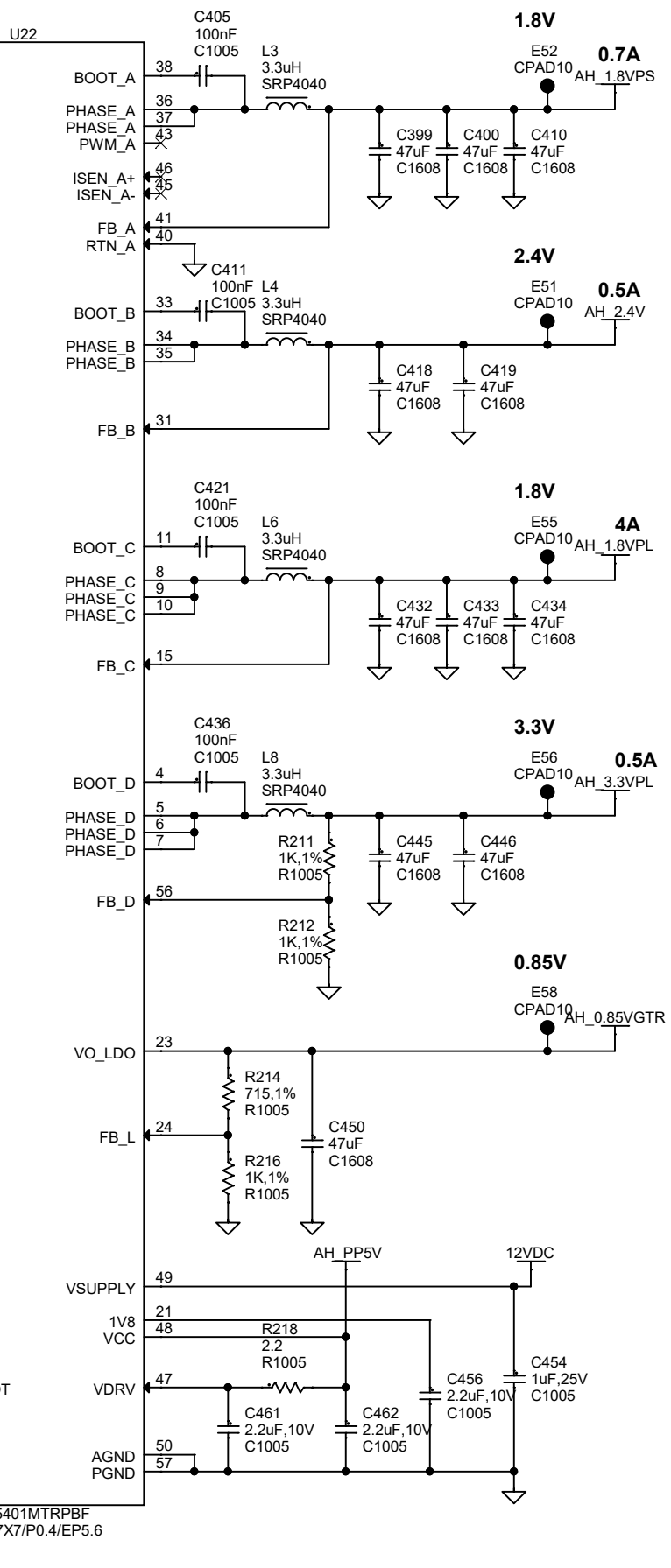
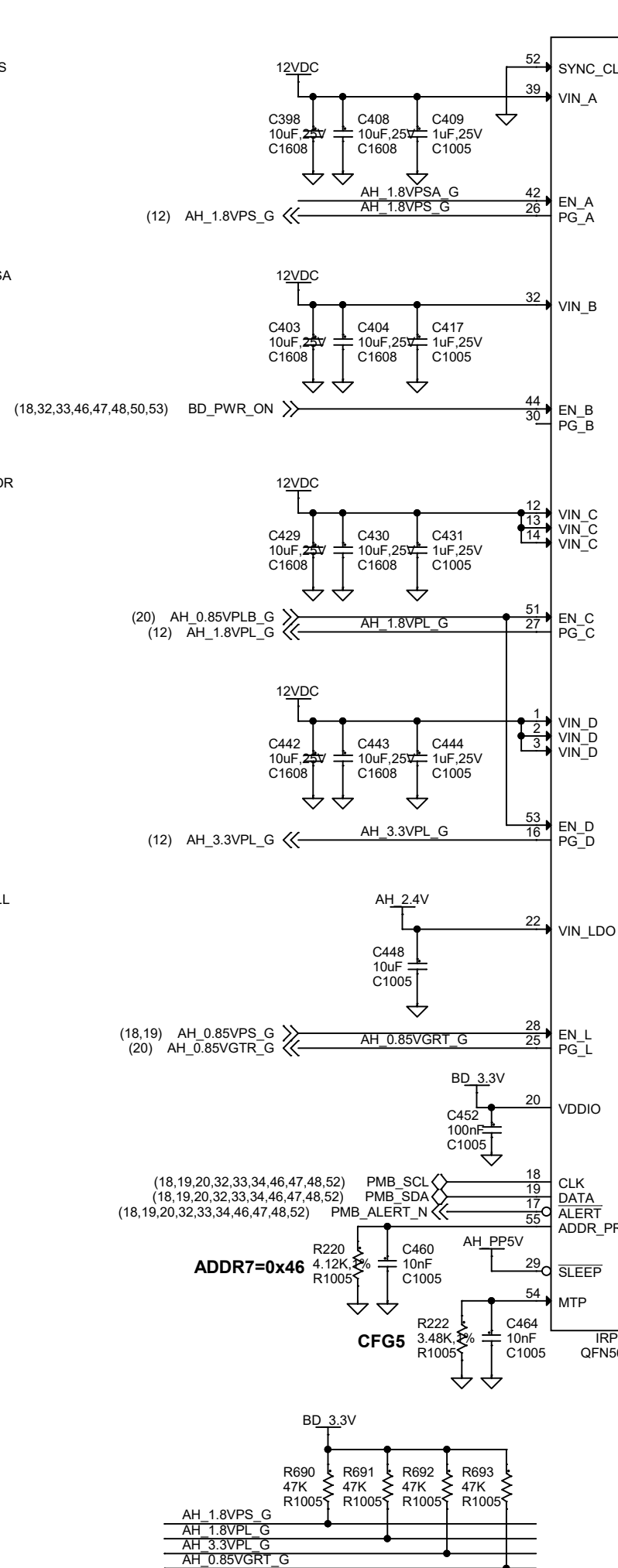
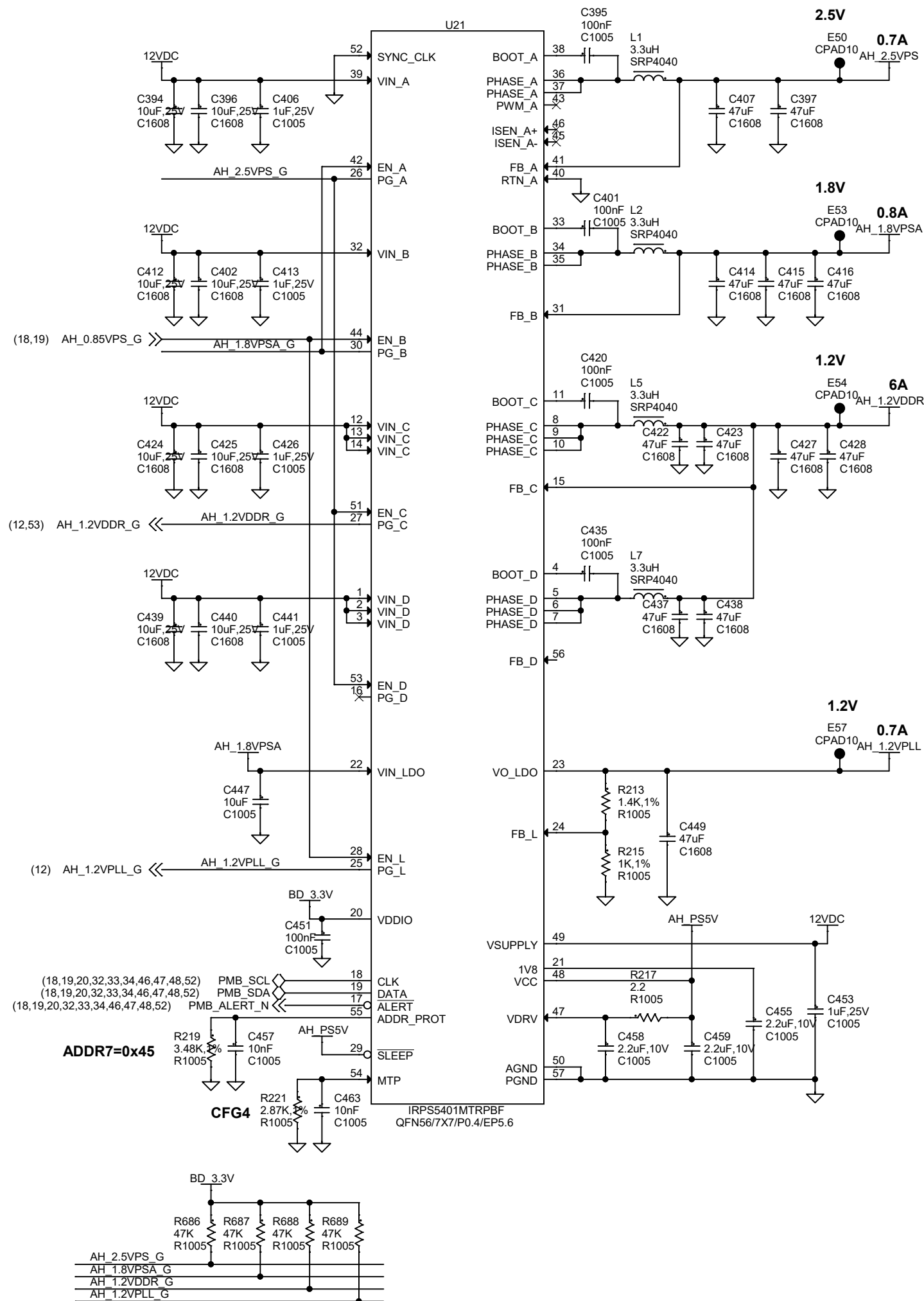


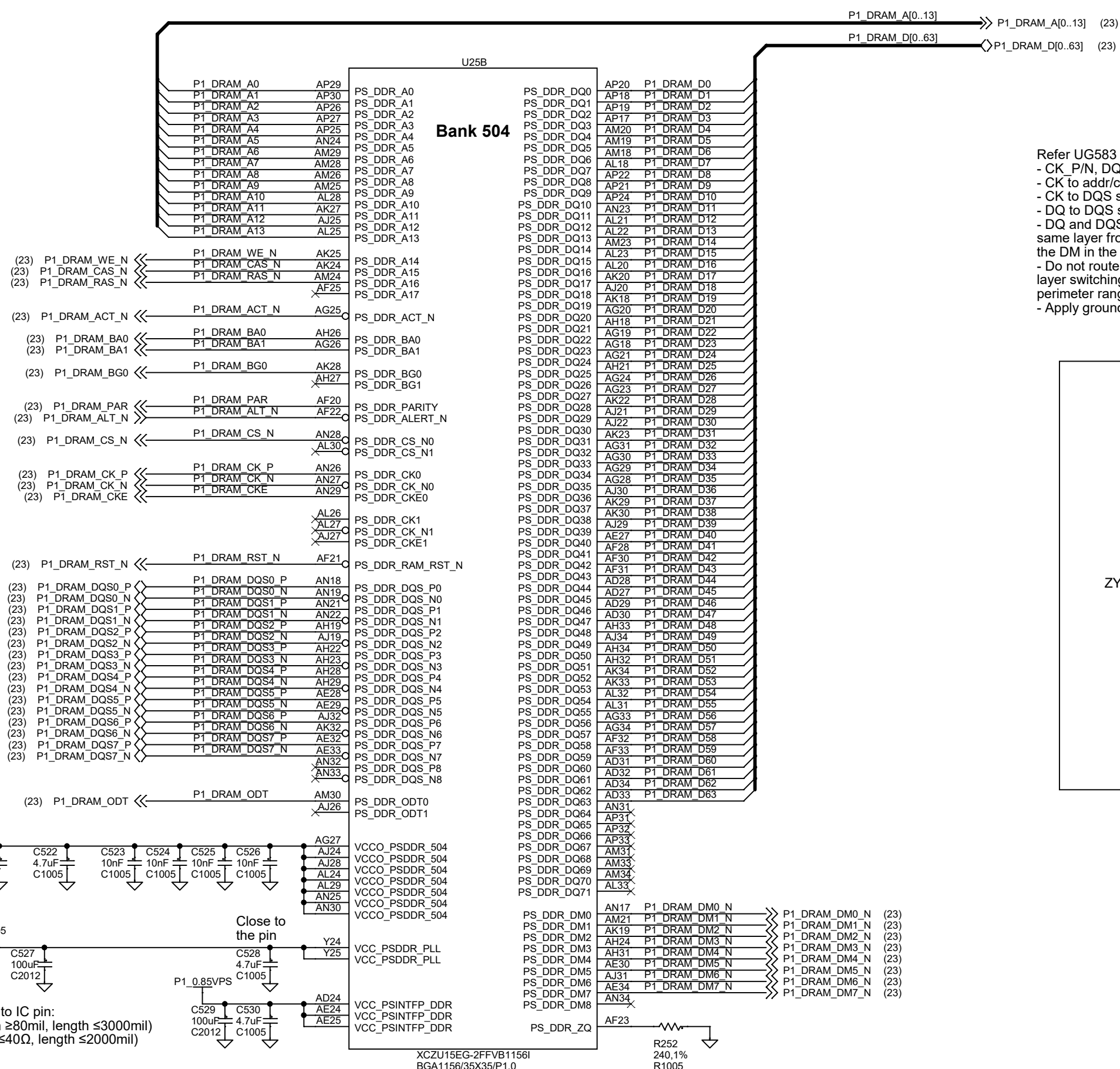
Programmer: DC1613A



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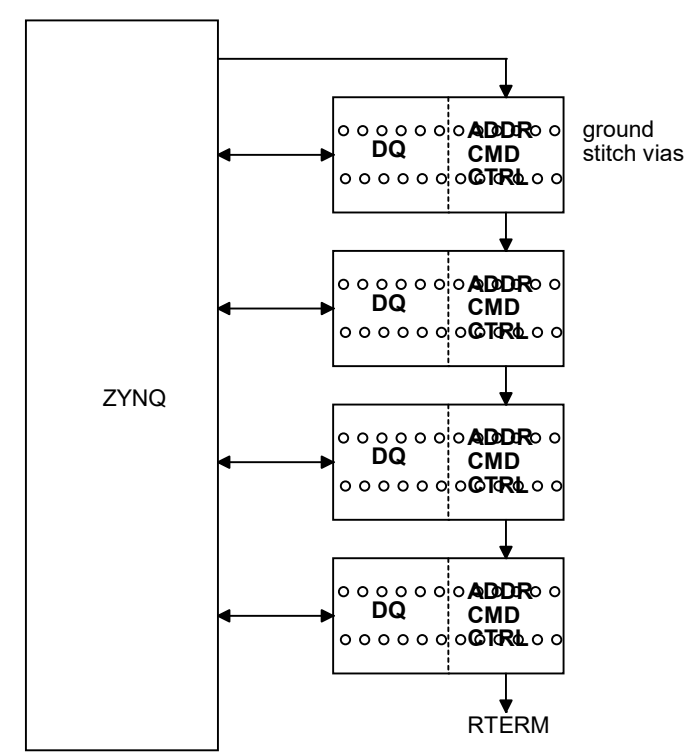
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Drawn	HAN InCheol	Size	Document Number	Rev
Approved	<Approved>	A3	717-U01541-00	0
		Date	Friday, November 10, 2023	Sheet 18 of 55





Refer UG583 p.34~64)

- CK_P/N, DQS_P/N skew < ±2ps, ±12mil
- CK to addr/cmd/ctrl skew < ±8ps, ±47mil
- CK to DQS skew < -149~+1796ps, -879~+10600mil
- DQ to DQS skew < ±5ps, ±29mil
- DQ and DQS signals in the same byte group should be routed in the same layer from Zynq to DRAM, except in the breakout areas. Include the DM in the byte group as applicable.
- Do not route any individual signal on more than two layers. Any signal layer switching via needs to have one ground via within a 50 mil perimeter range
- Apply ground stitch vias under DRAM

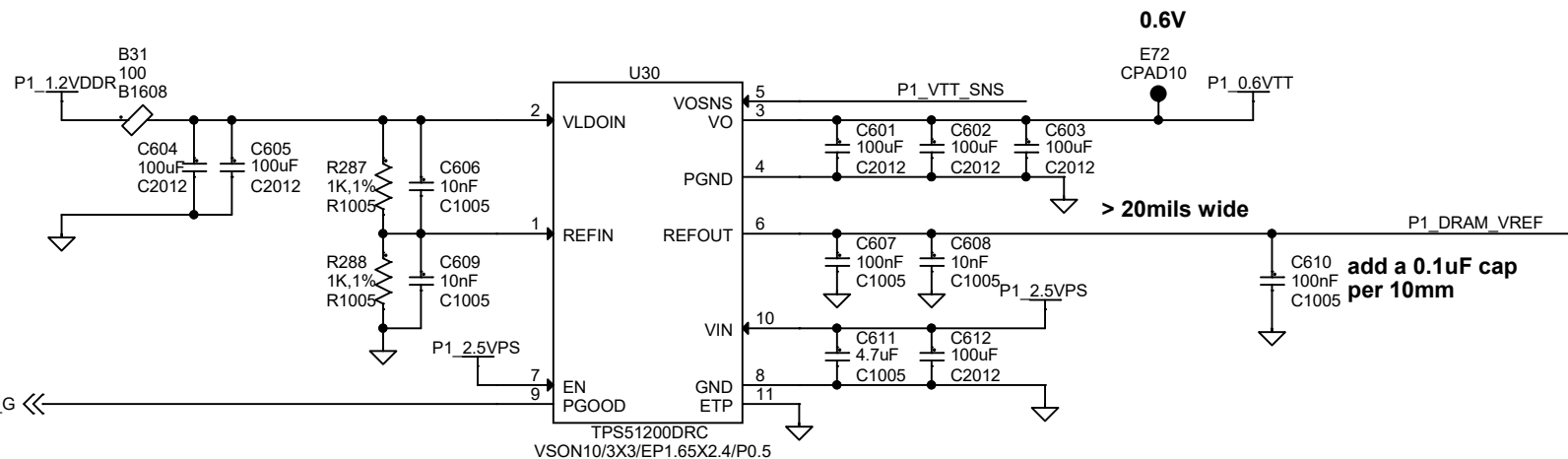
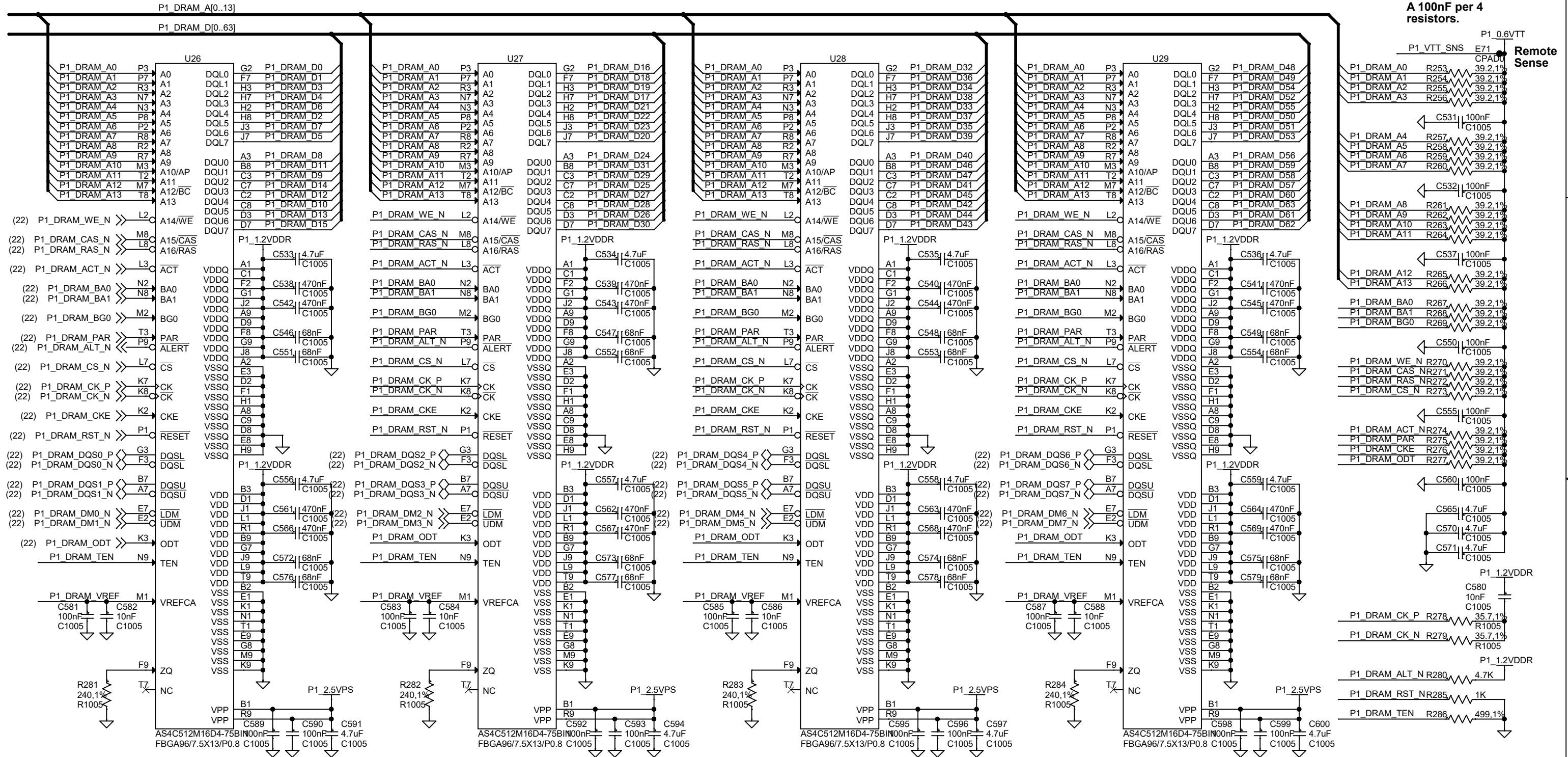


(22) P1_DRAM_A[0..13] >> P1_DRAM_A[0..13]
(22) P1_DRAM_D[0..63] << P1_DRAM_D[0..63]

Fly-by topology

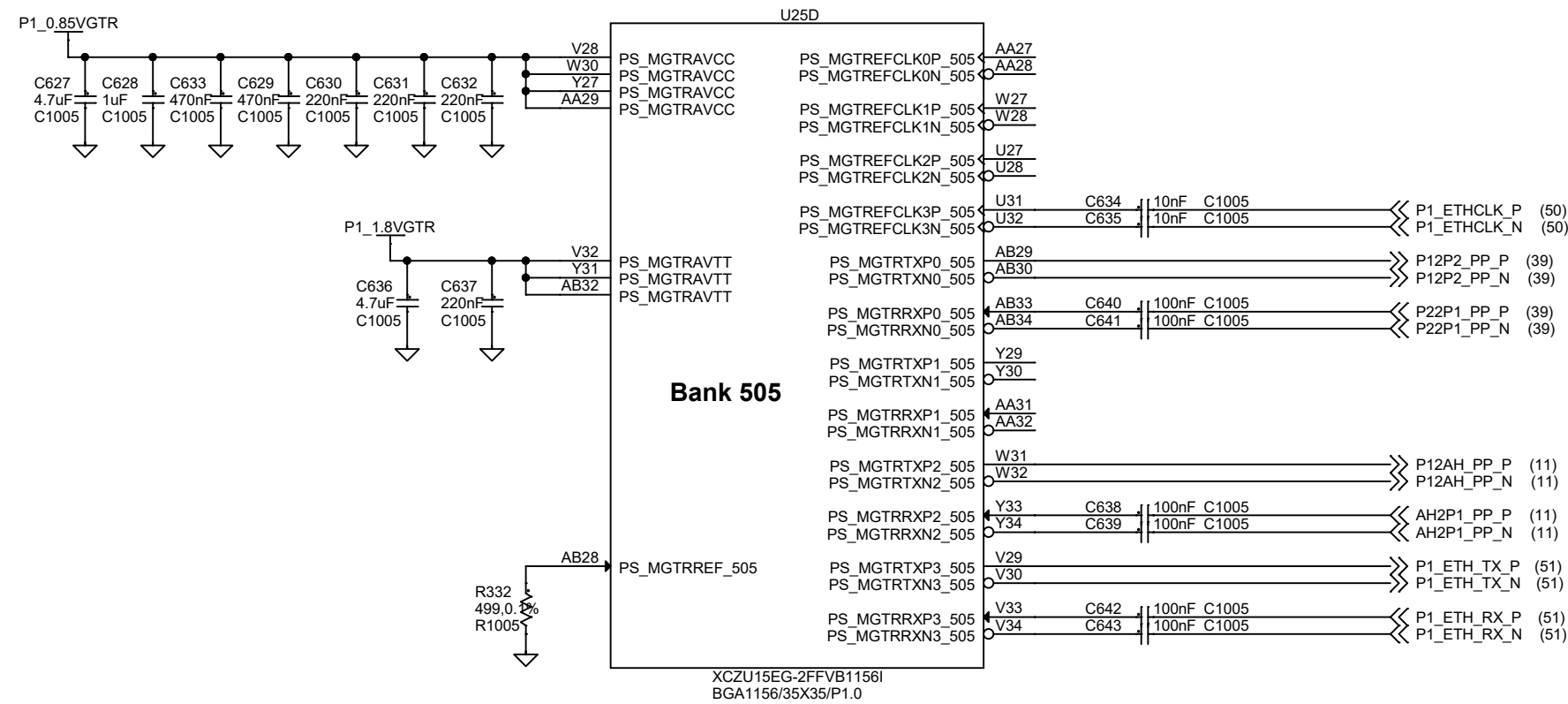
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Place at the end of the traces.
A 100nF per 4 resistors.

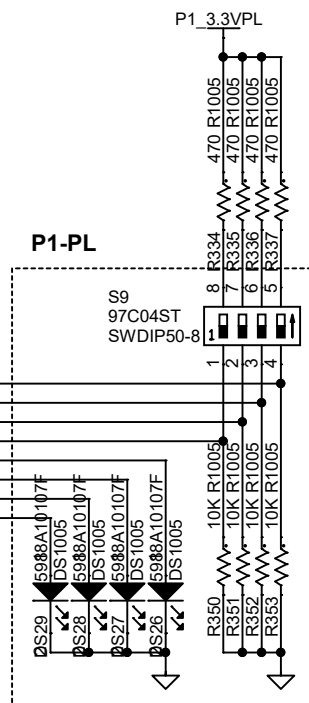
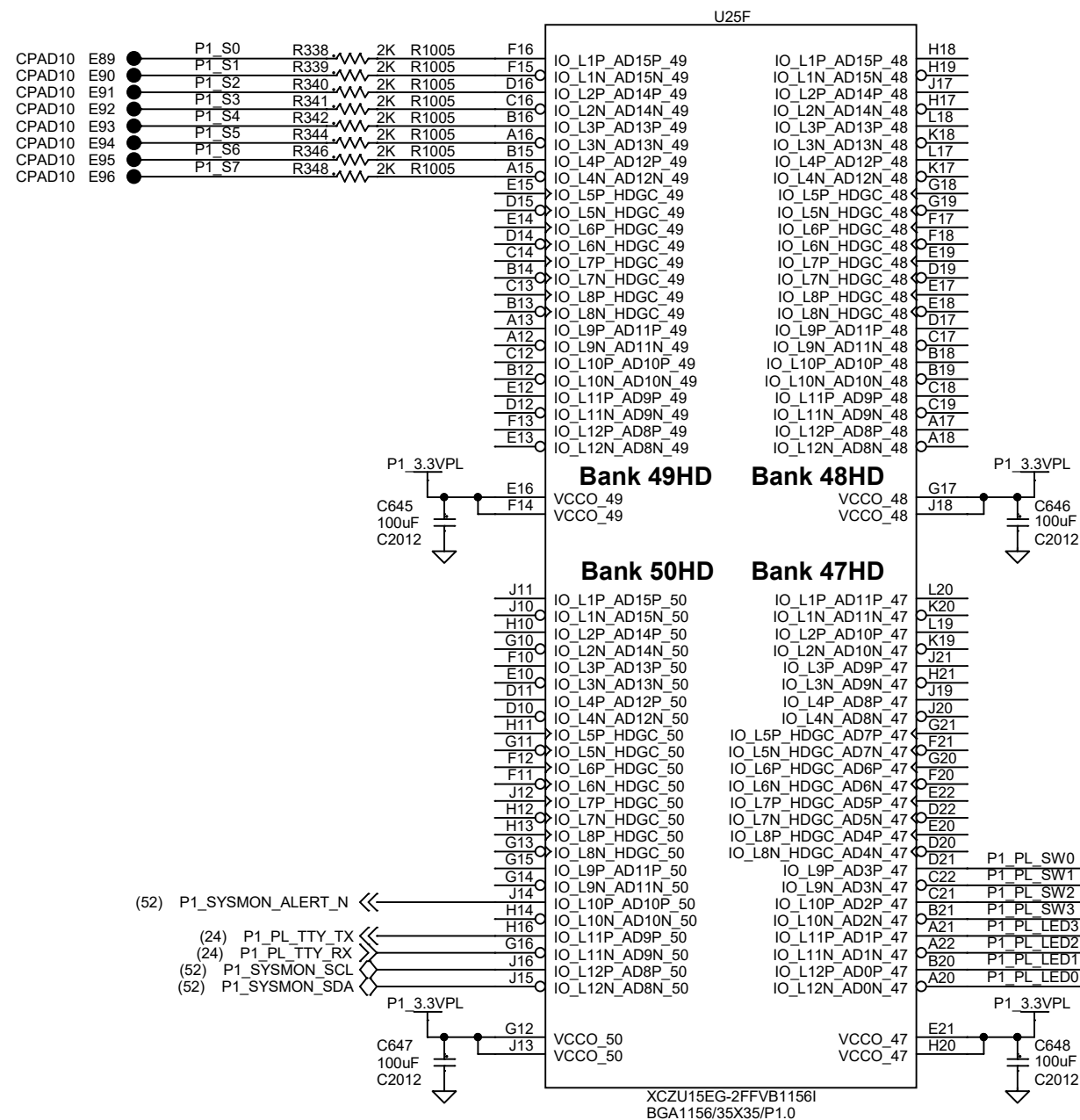
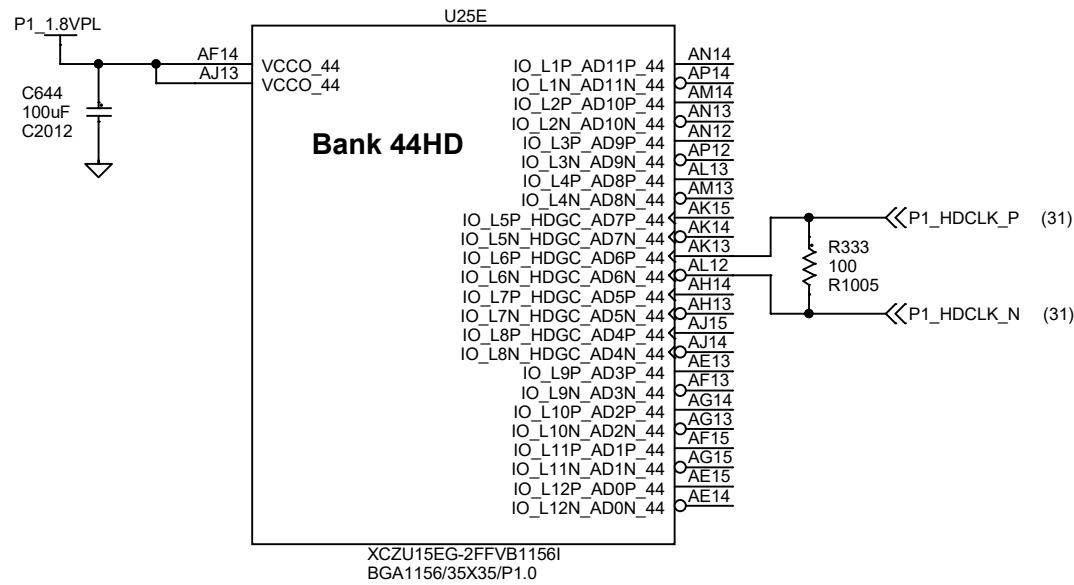


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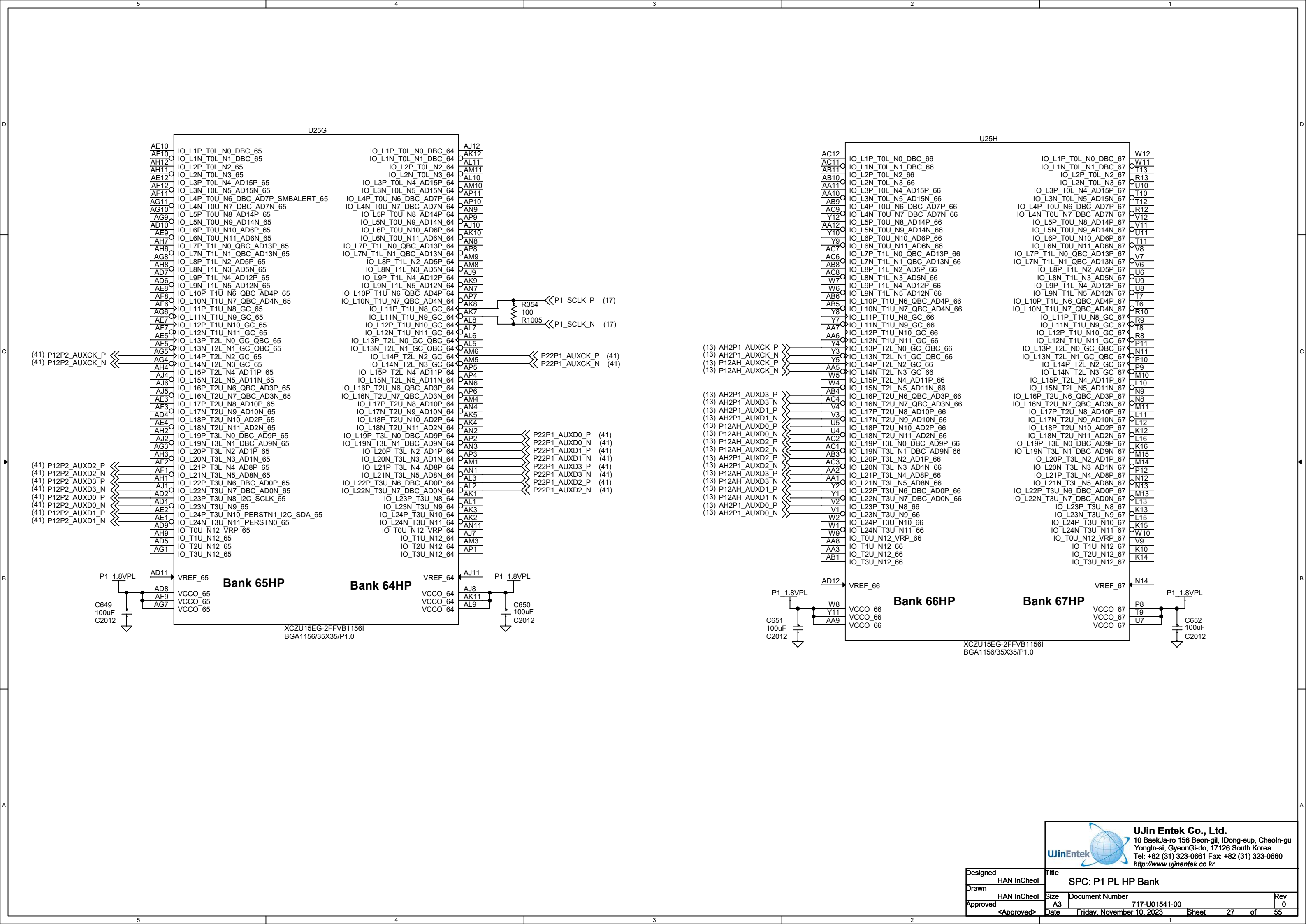
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Drawn	HAN InChool	Size	A3
Approved	<Approved>	Document Number	717-U01541-00
		Date	Thursday, November 16, 2023
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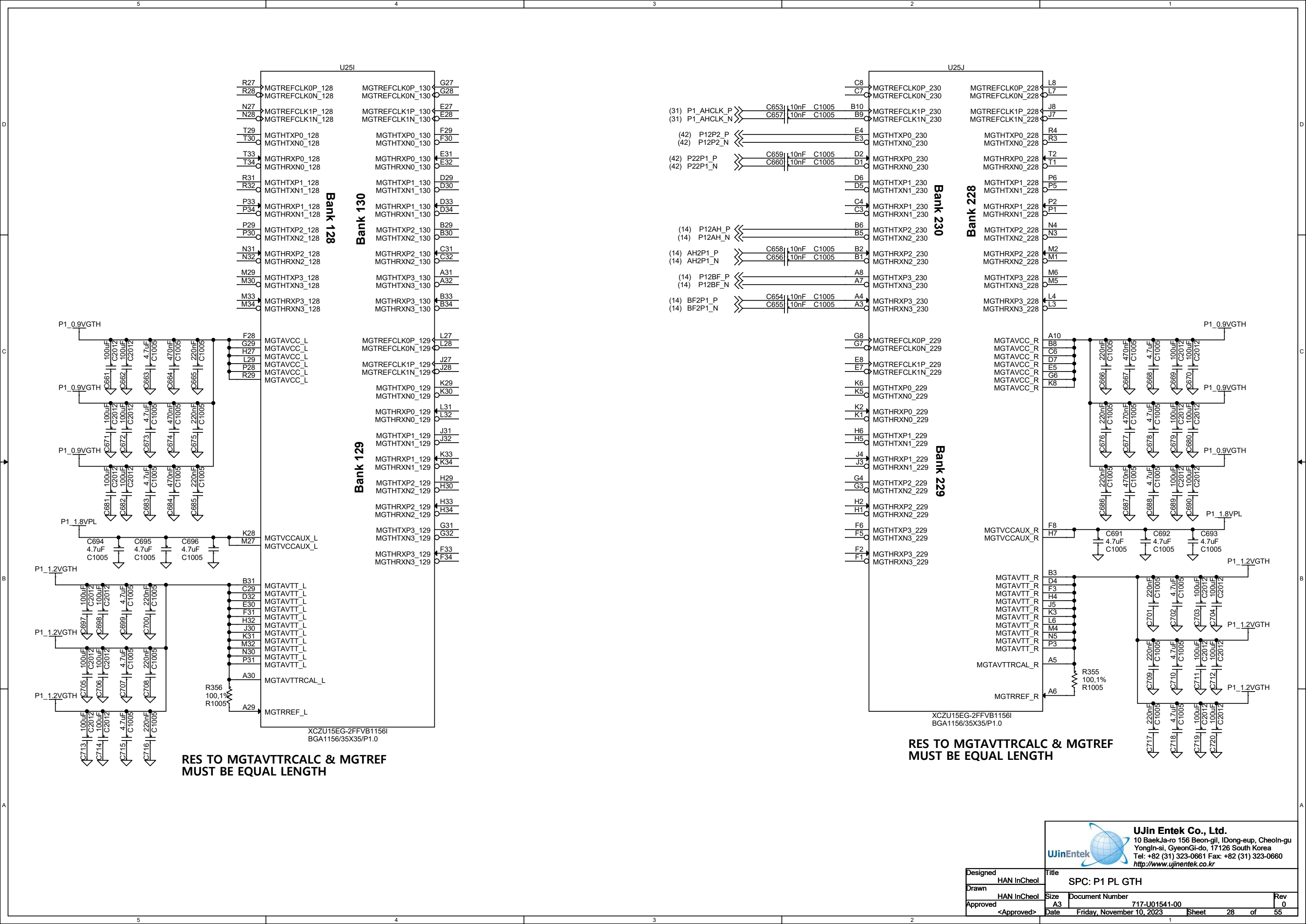


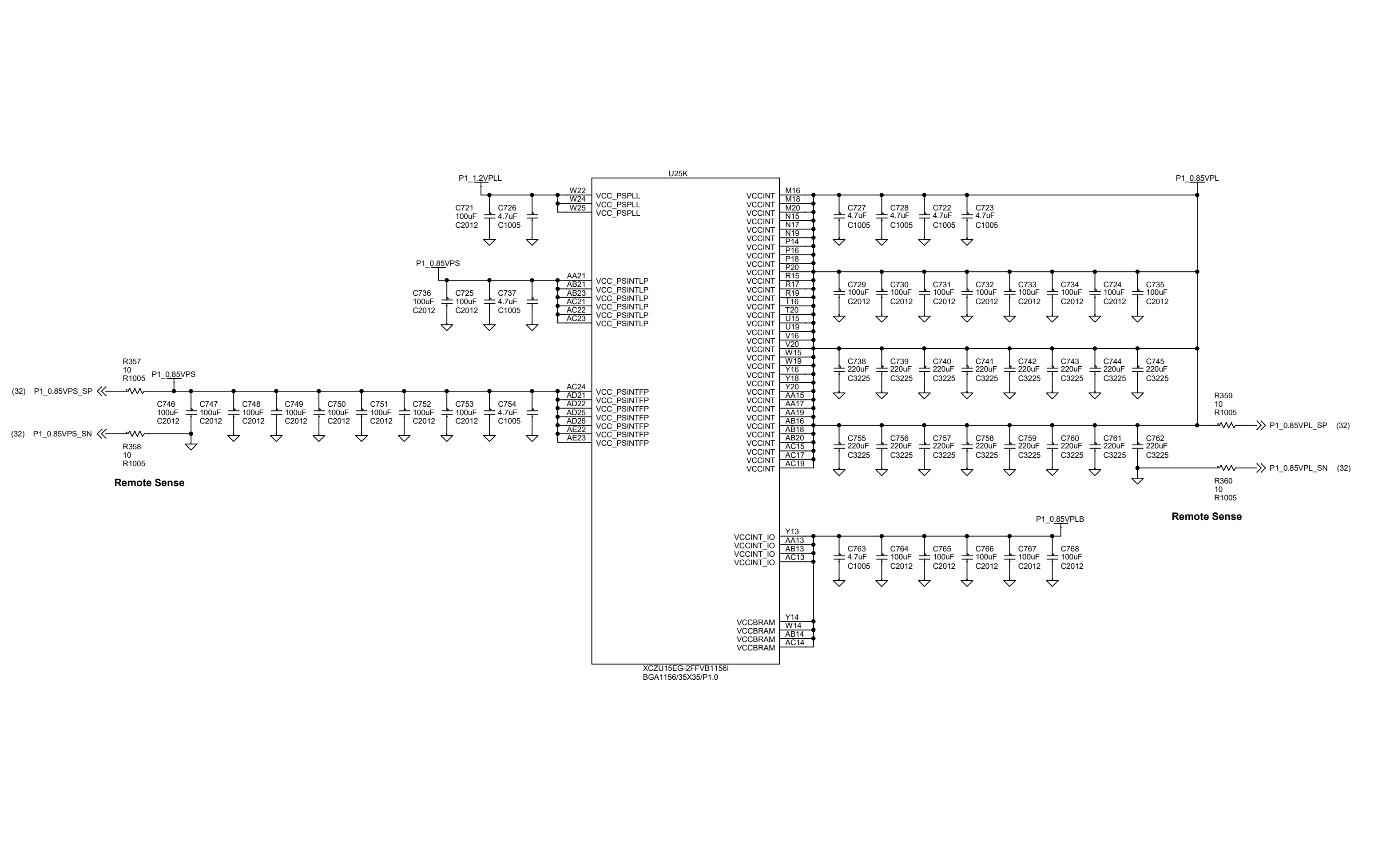
6Gbps max
Z = 50Ω single-ended / 100Ω differential
Trace match P/N < 2ps
Trace length < 254mm



Designed	HAN InCheol	Title	SPC: P1 PL HD Bank
Drawn	HAN InCheol	Size	A3
Approved	<Approved>	Document Number	717-U01541-00
		Date	Friday, November 10, 2023
		Sheet	26 of 55
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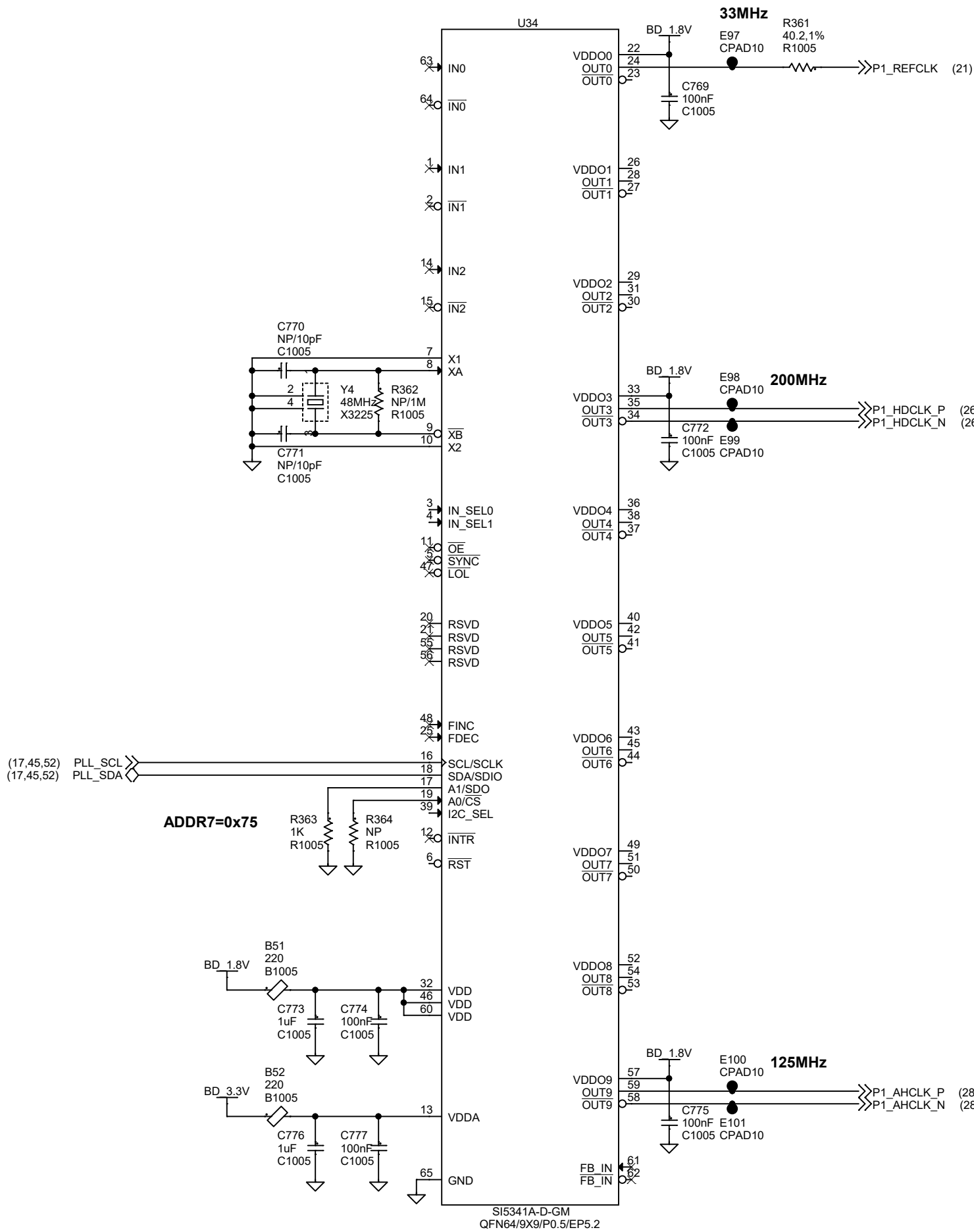







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Designed	HAN InCheol	Title			
Drawn	HAN InCheol	SPC: P1 SoC Power			
Approved	<Approved>	Size	Document Number	Rev	
		A3	717-U01541-00	0	
		Date	Friday, November 10, 2023	Sheet	29 of 55

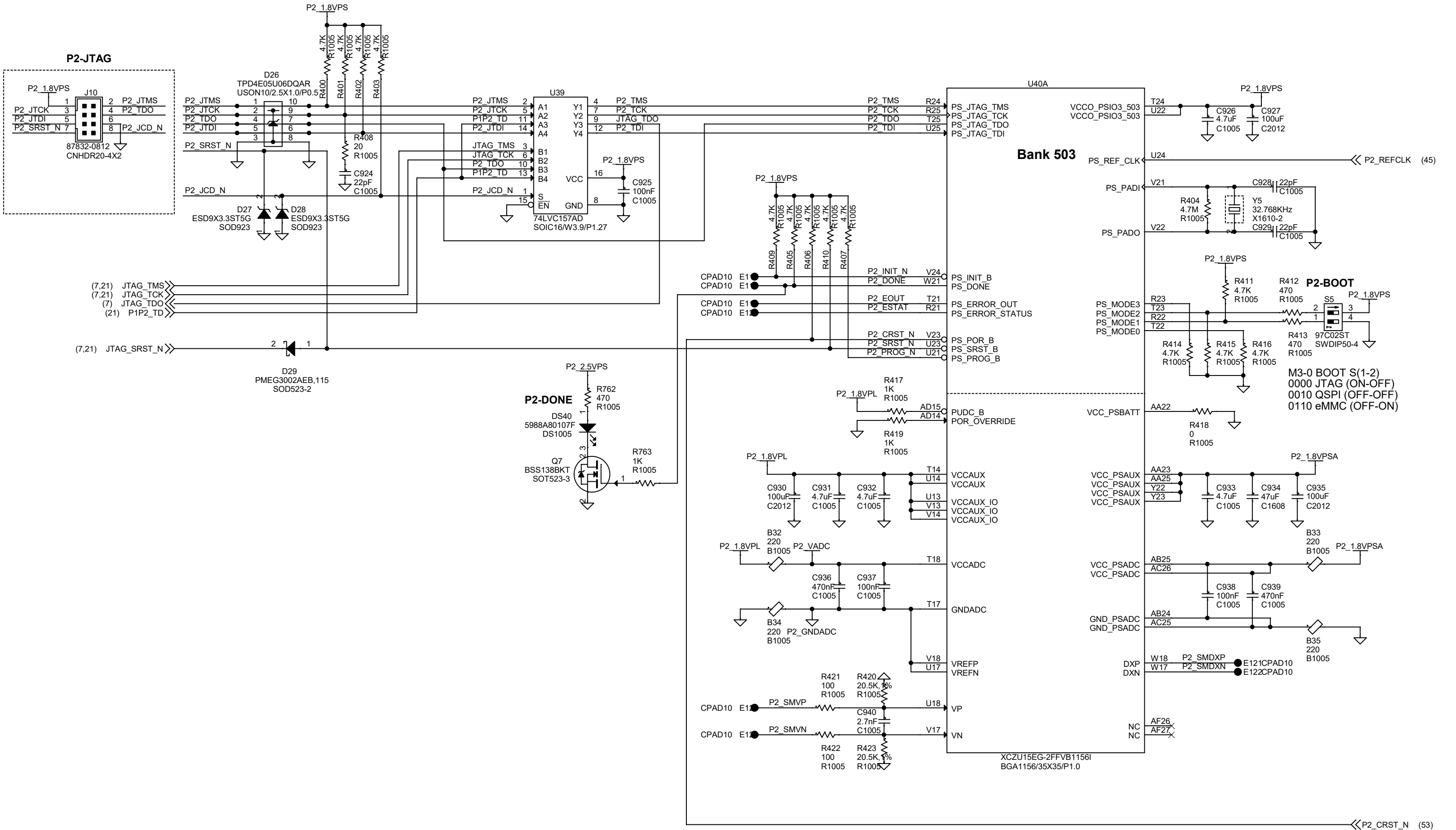


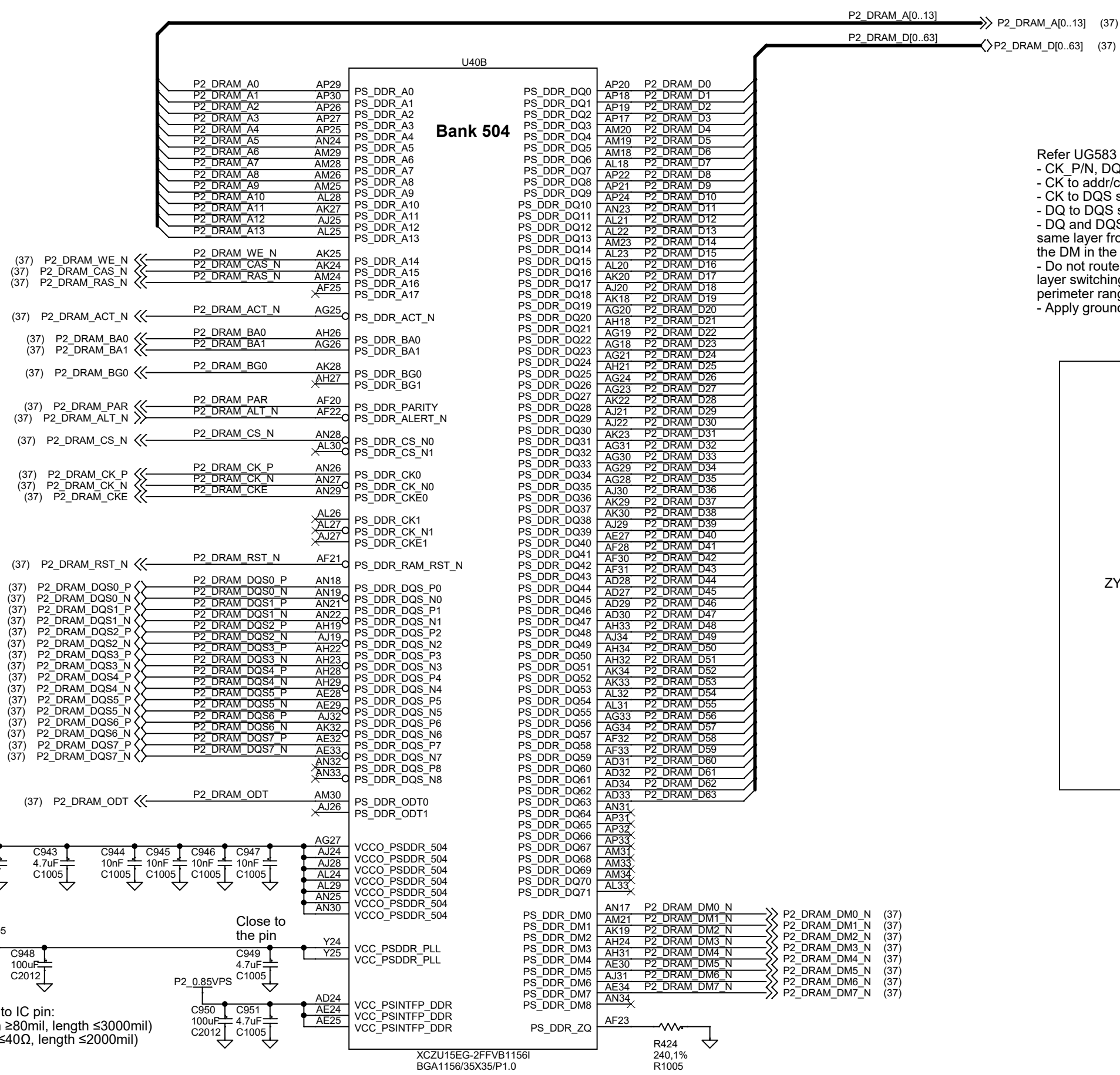
Programmer: ClockBuilder Field Programmer Kit (CBPROG-DONGLE)



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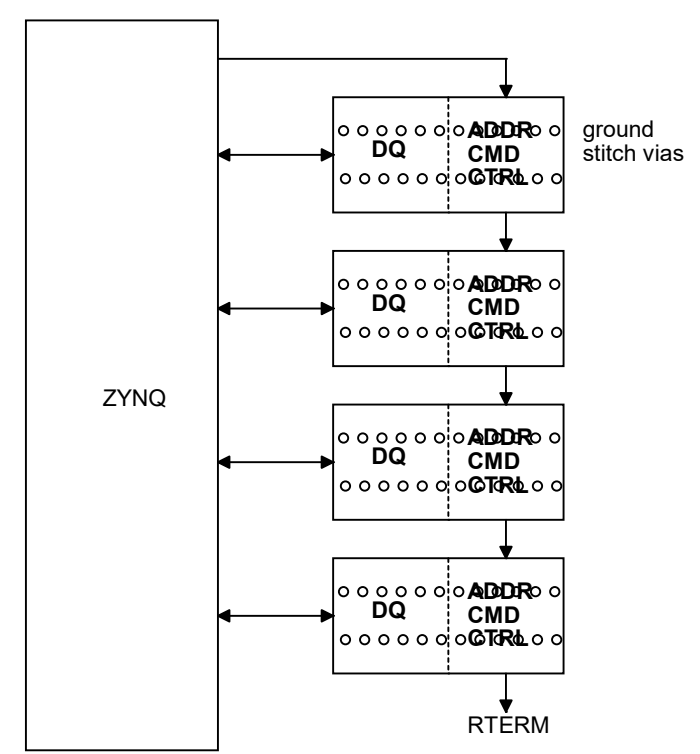
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Drawn	HAN InCheol	Size	Document Number	Rev
Approved	<Approved>	A3	717-U01541-00	0
		Date	Friday, November 10, 2023	Sheet 31 of 55





Refer UG583 p.34~64)

- CK_P/N, DQS_P/N skew < ±2ps, ±12mil
- CK to addr/cmd/ctrl skew < ±8ps, ±47mil
- CK to DQS skew < -149~+1796ps, -879~+10600mil
- DQ to DQS skew < ±5ps, ±29mil
- DQ and DQS signals in the same byte group should be routed in the same layer from Zynq to DRAM, except in the breakout areas. Include the DM in the byte group as applicable.
- Do not route any individual signal on more than two layers. Any signal layer switching via needs to have one ground via within a 50 mil perimeter range
- Apply ground stitch vias under DRAM

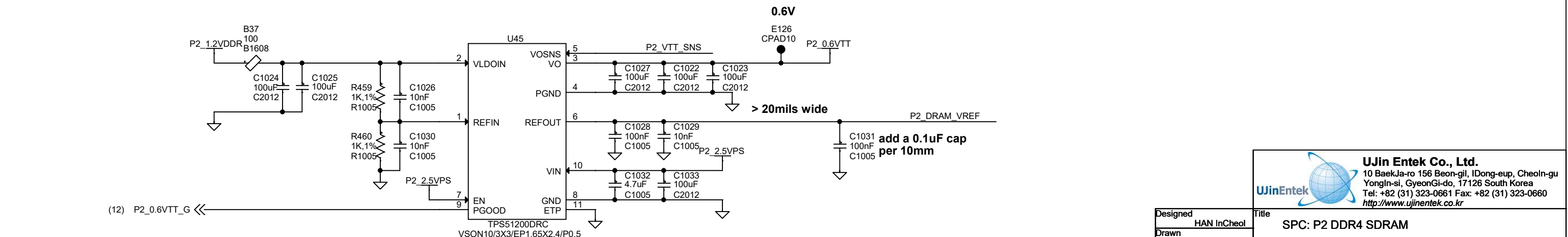
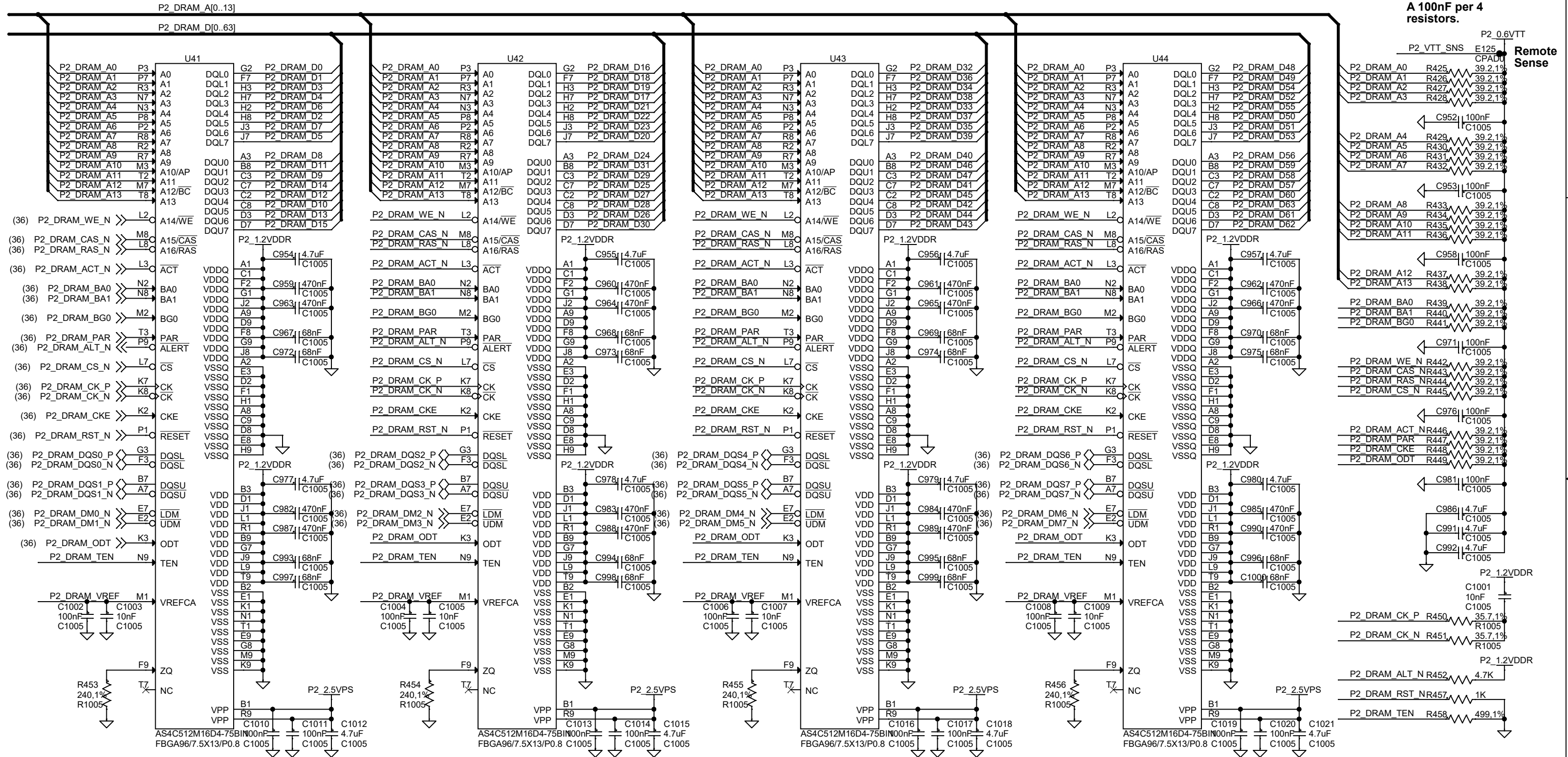


(36) P2_DRAM_A[0..13] >> P2_DRAM_A[0..13]
(36) P2_DRAM_D[0..63] << P2_DRAM_D[0..63]

Fly-by topology

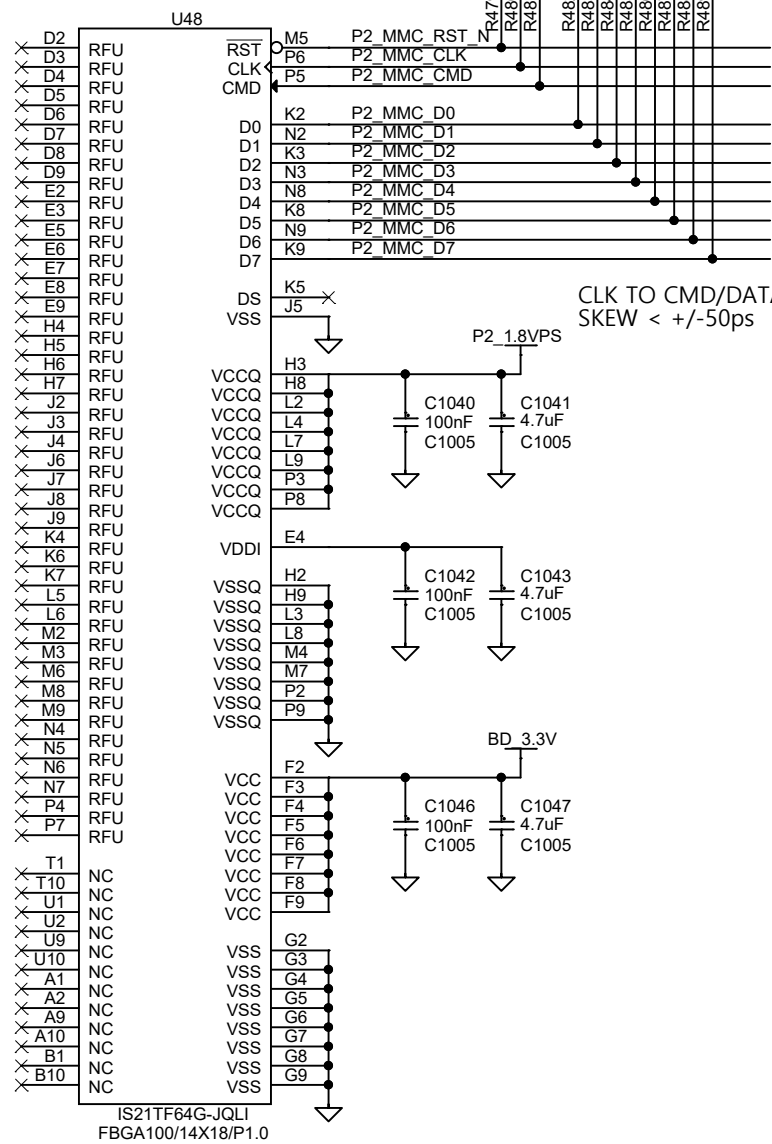
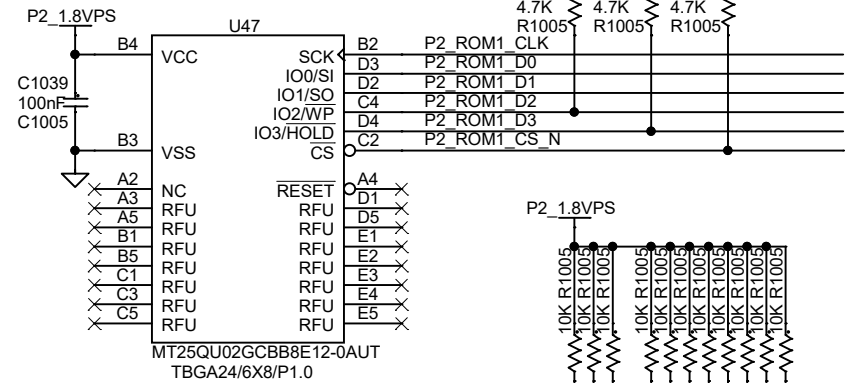
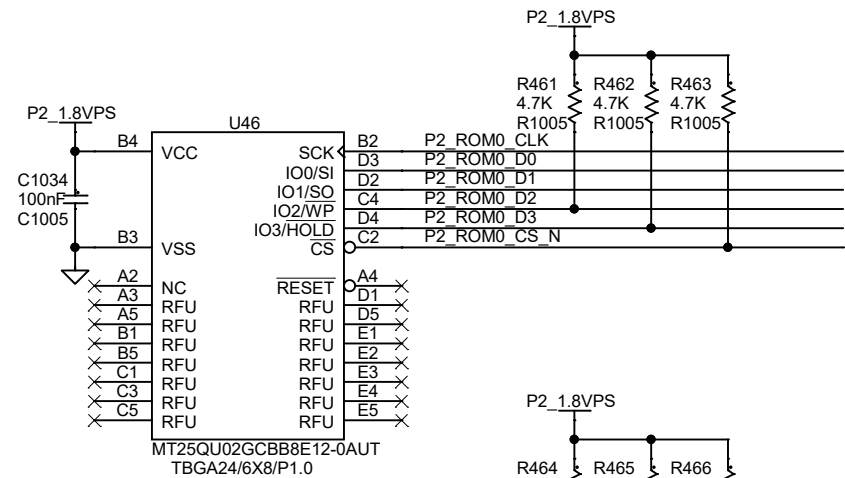
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Place at the end of the traces.
A 100nF per 4 resistors.

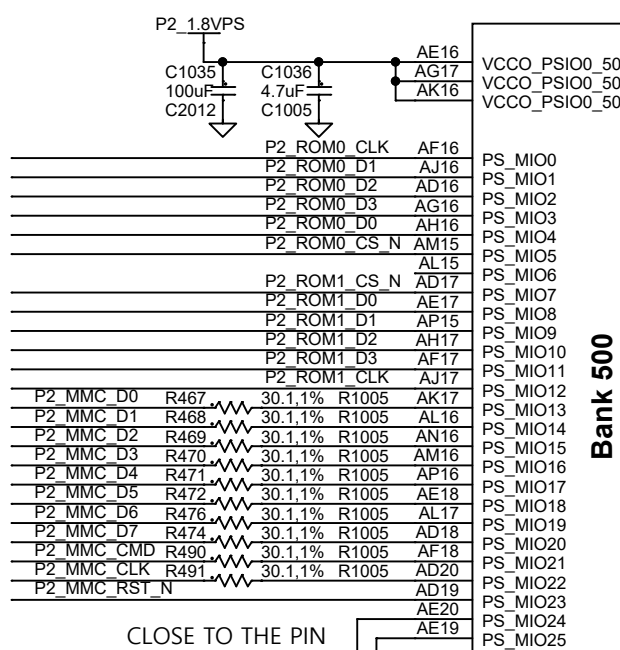


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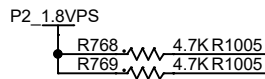
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Drawn	HAN InChol	Size	A3
Approved	<Approved>	Document Number	717-U01541-00
		Date	Thursday, November 16, 2023
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CLK TO CS/DATA
SKEW < +/-50ps
TRACE DELAY < 500ps



CLOSE TO THE PIN



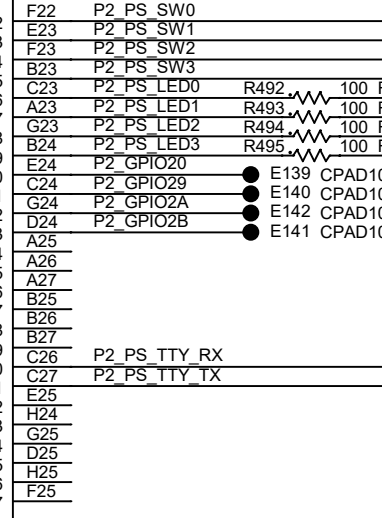
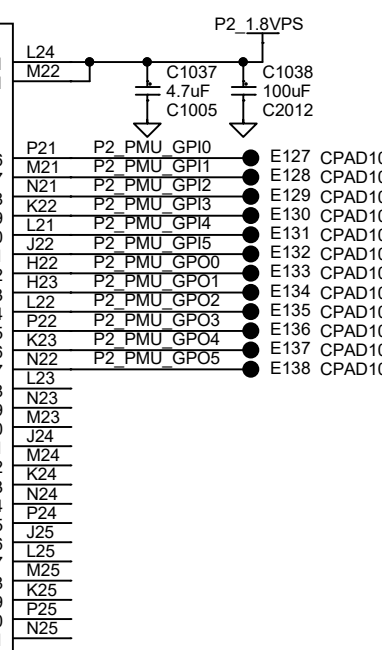
Bank 500

Bank 501

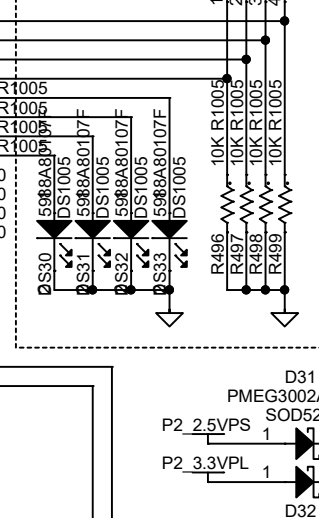
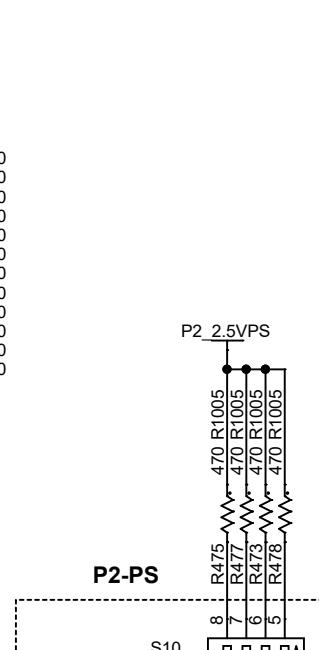
Bank 502

VCCO_PSIO2_502
VCCO_PSIO2_502
VCCO_PSIO2_502

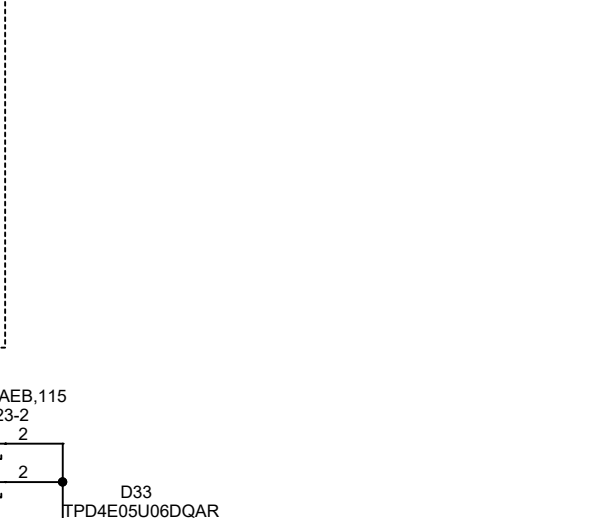
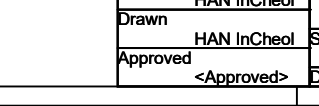
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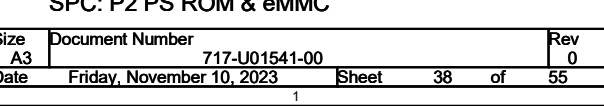
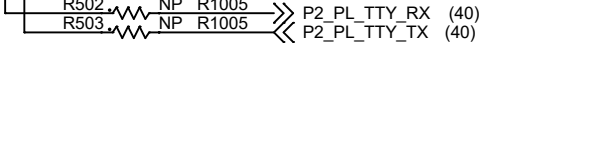
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VCCO_PSIO2_502



VCCO_PSIO2_502
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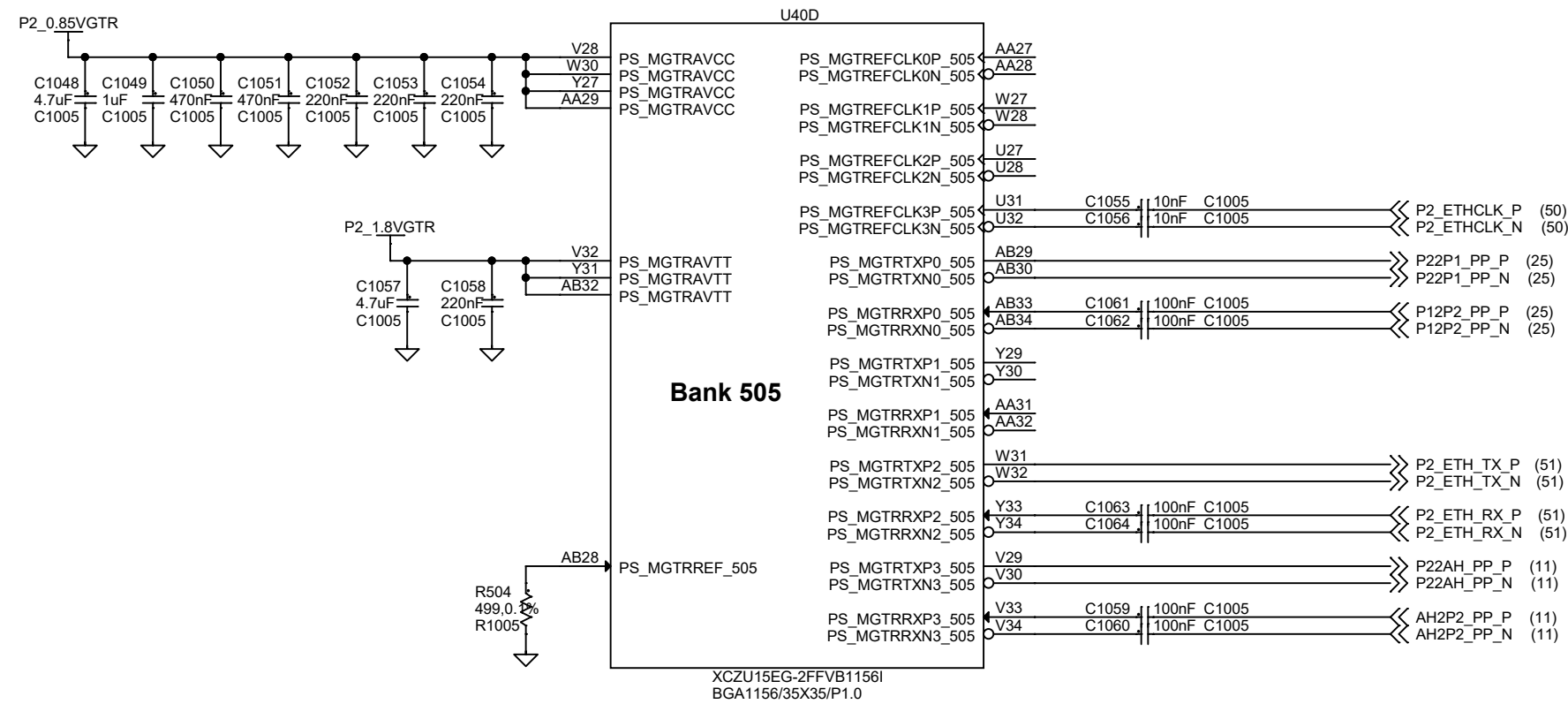


VCCO_PSIO2_502
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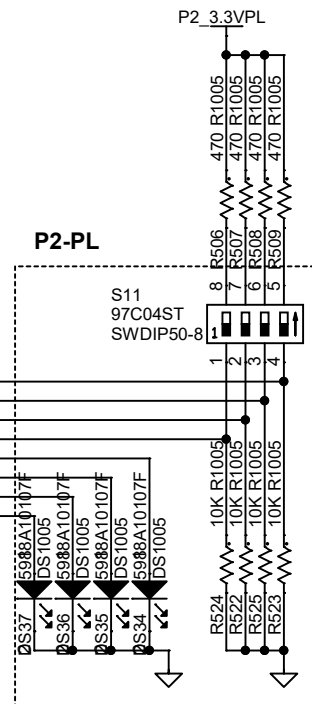
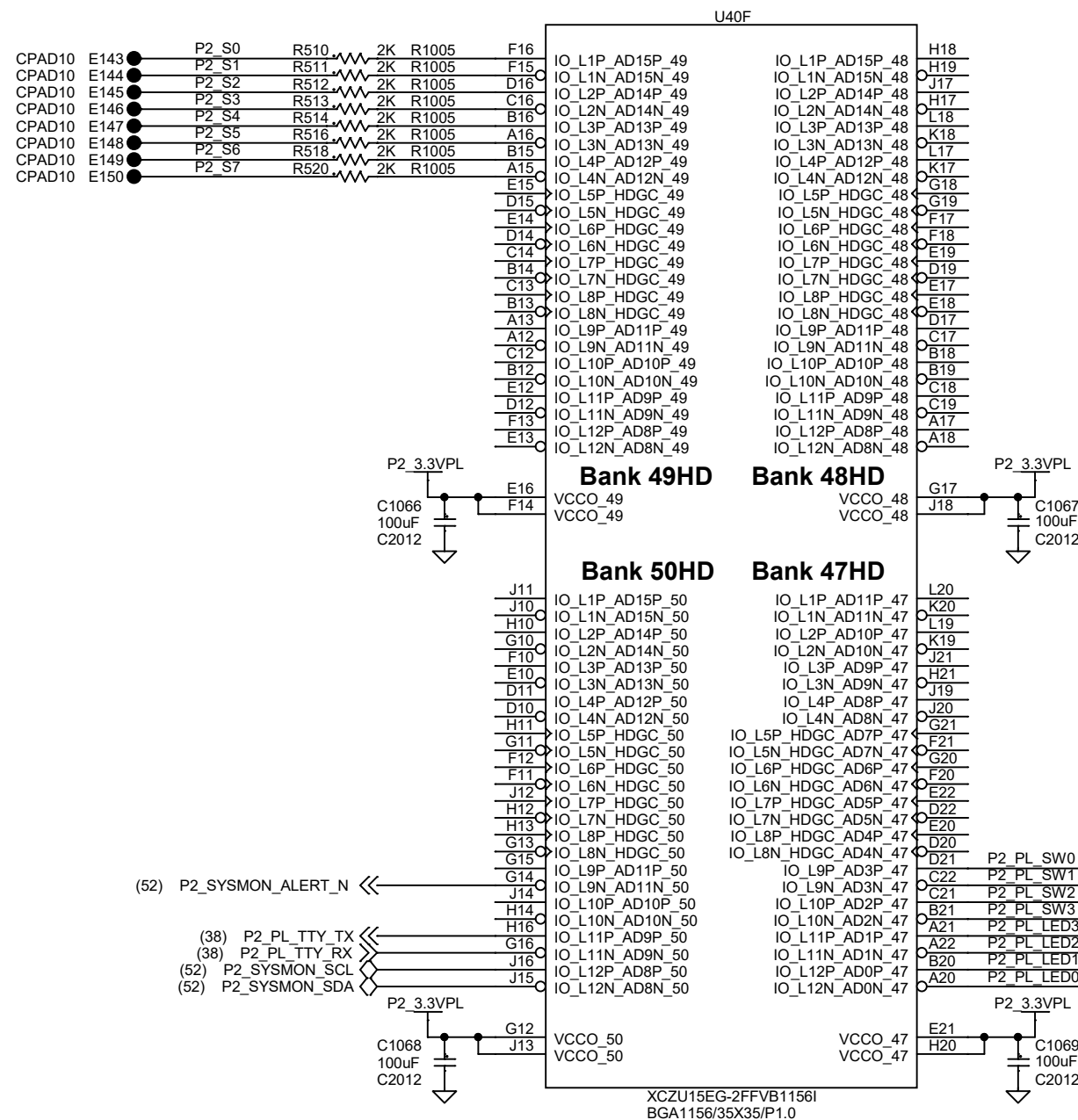
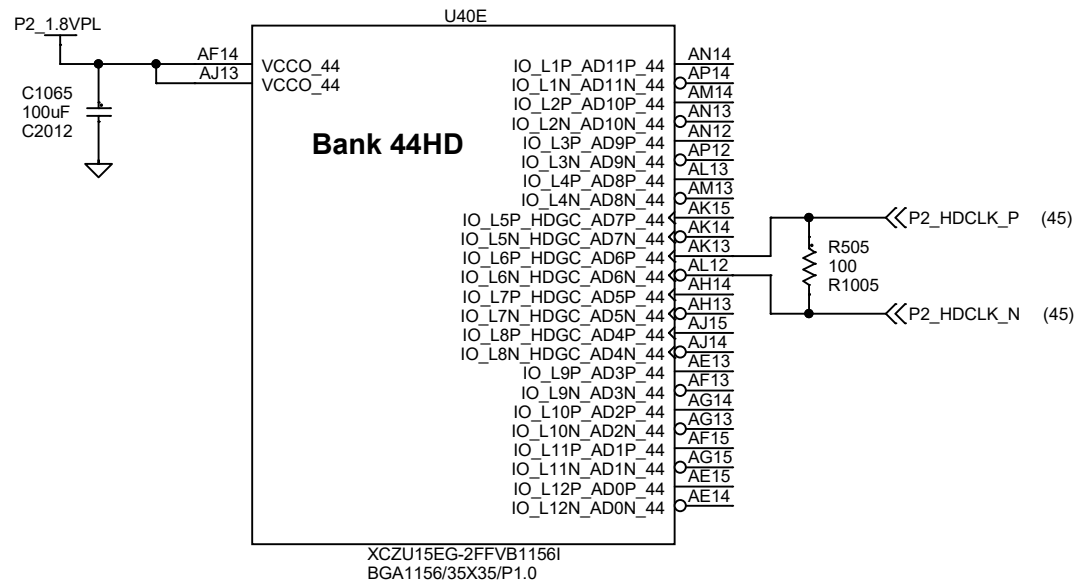


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Designed	HAN InCheol	Title	SPC: P2 PS ROM & eMMC
Drawn	HAN InCheol	Size	A3
Approved	<Approved>	Document Number	717-U01541-00
		Date	Friday, November 10, 2023
		Sheet	38 of 55
		Rev	0

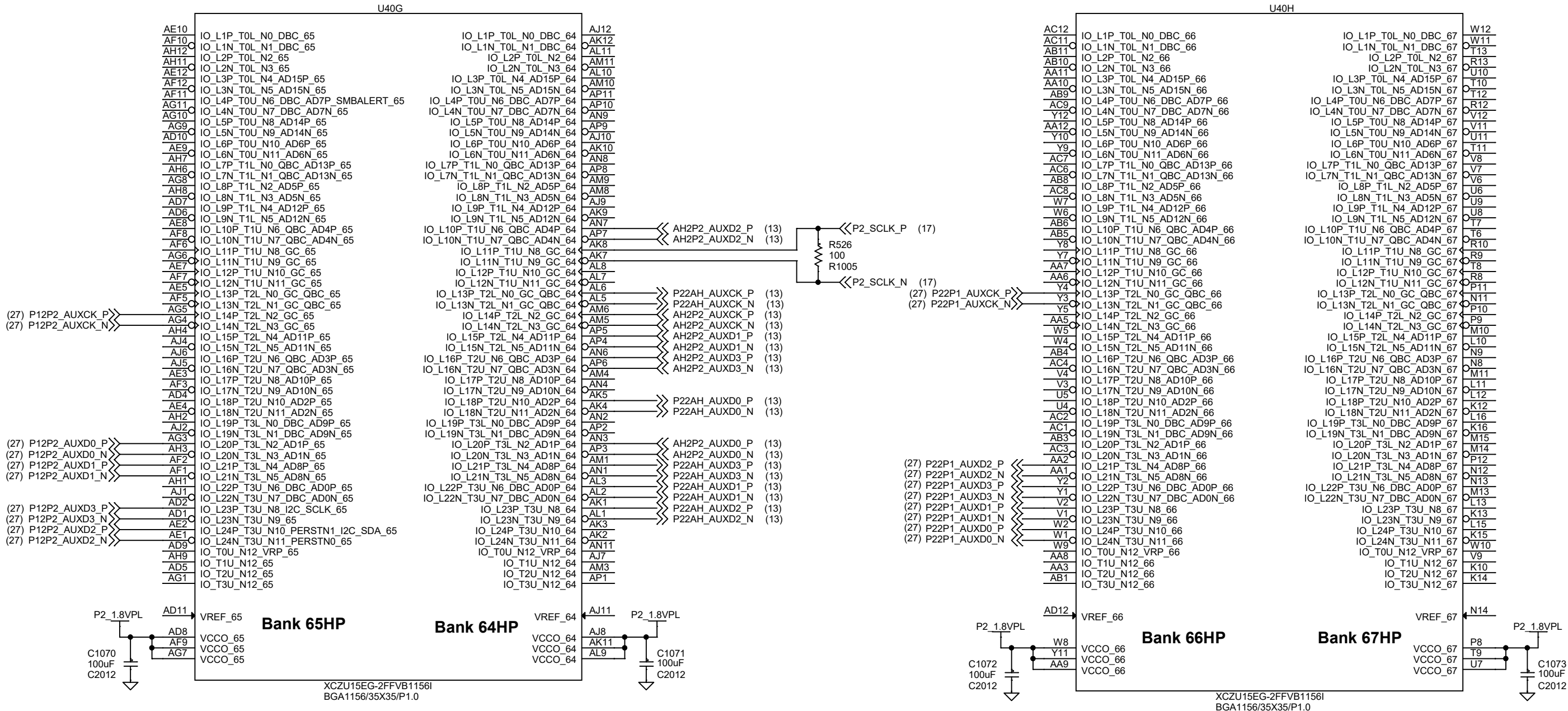


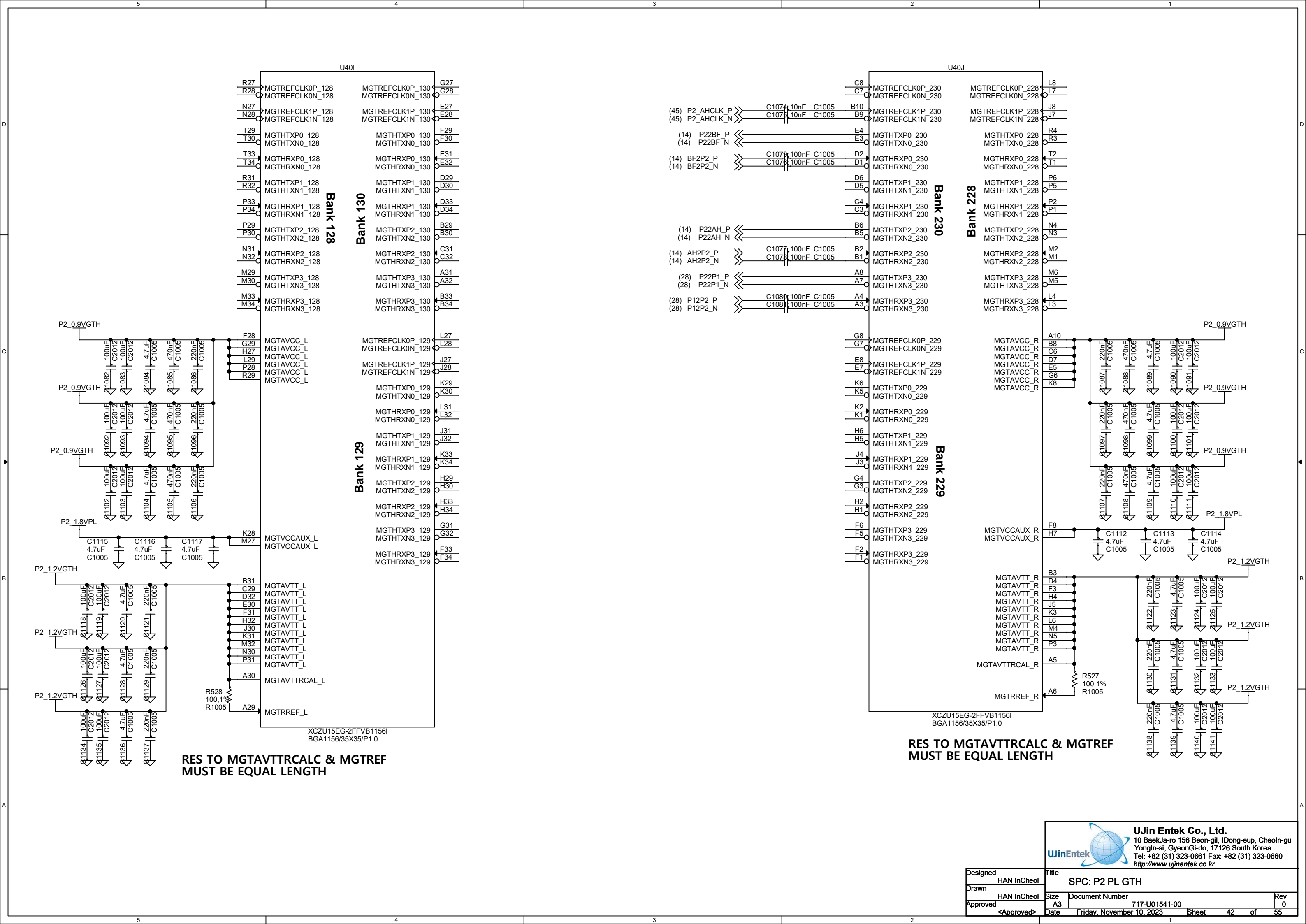
6Gbps max
Z = 50Ω single-ended / 100Ω diffenential
Trace match P/N < 2ps
Trace length < 254mm

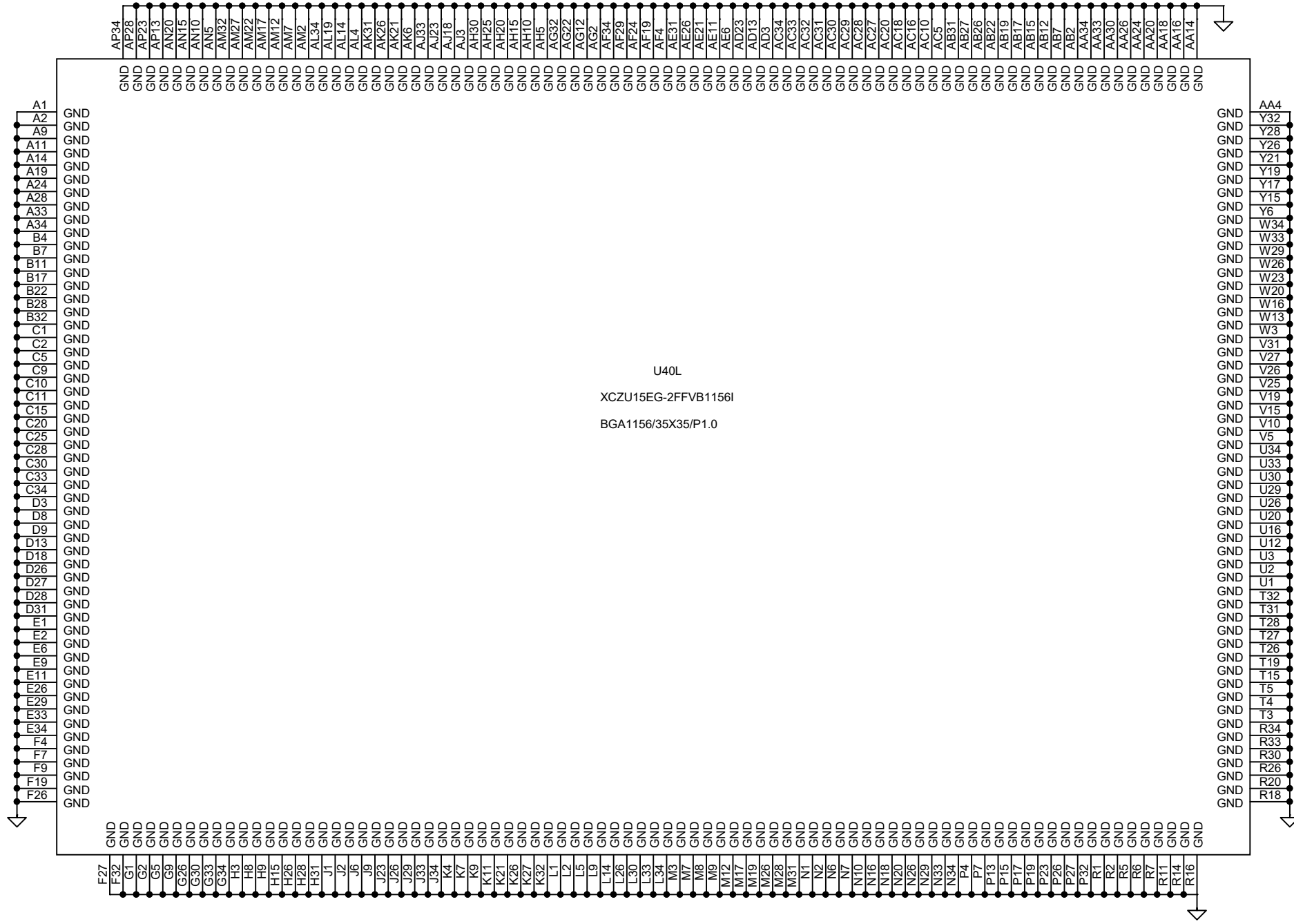


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Designed	HAN InCheol	Title	SPC: P2 PL HD Bank
Drawn	HAN InCheol	Size	A3
Approved	<Approved>	Document Number	717-U01541-00
		Date	Friday, November 10, 2023
		Sheet	40 of 55
		Rev	0



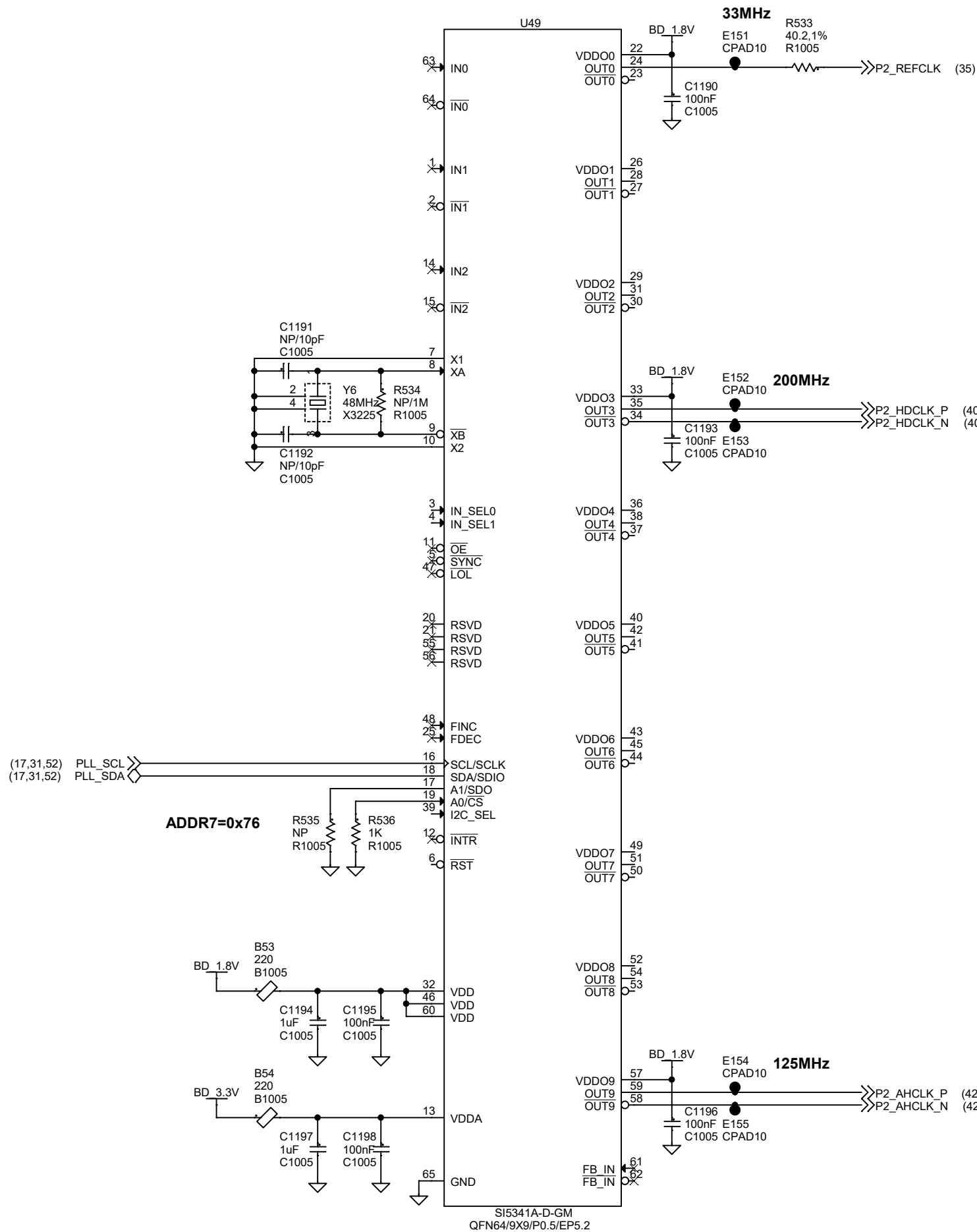







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Designed	HAN InCheol	Title		
Drawn	HAN InCheol	SPC: P1 SoC Ground		
Approved	<Approved>	Size	Document Number	Rev
		A3	717-U01541-00	0
		Date	Friday, November 10, 2023	Sheet 44 of 55

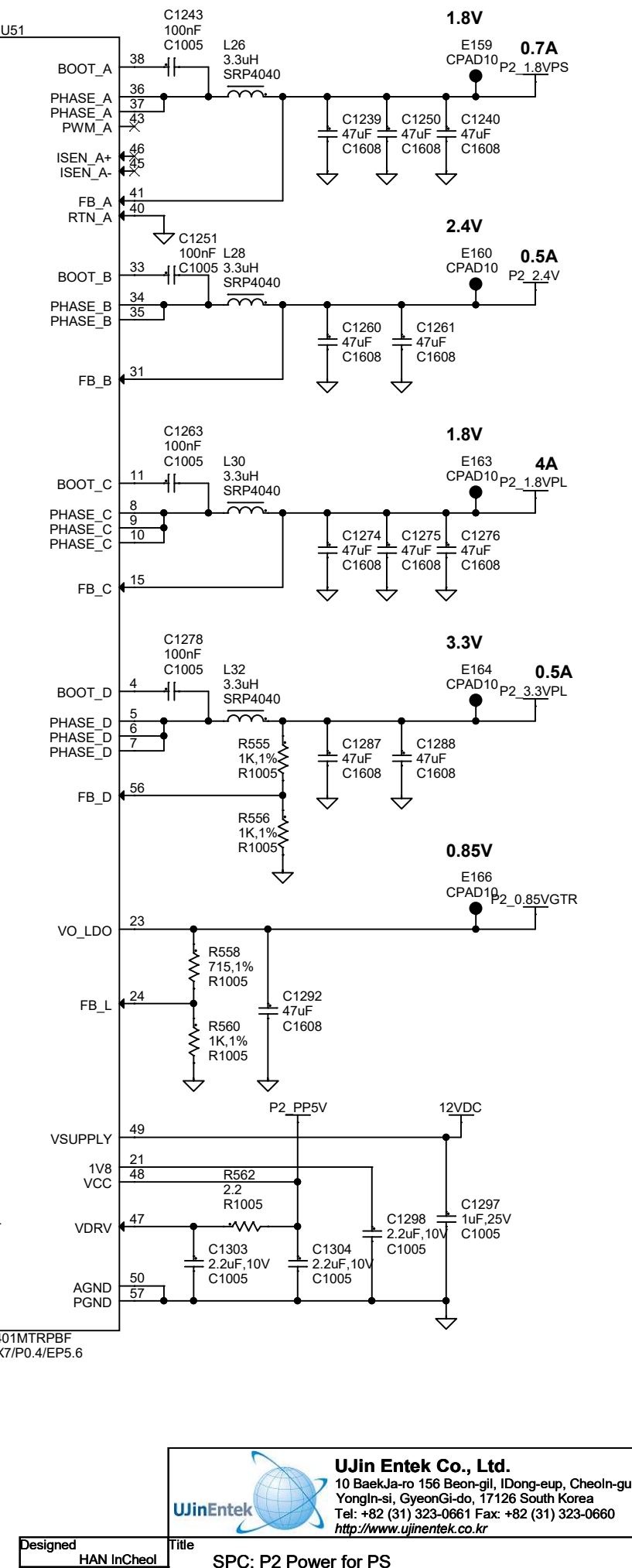
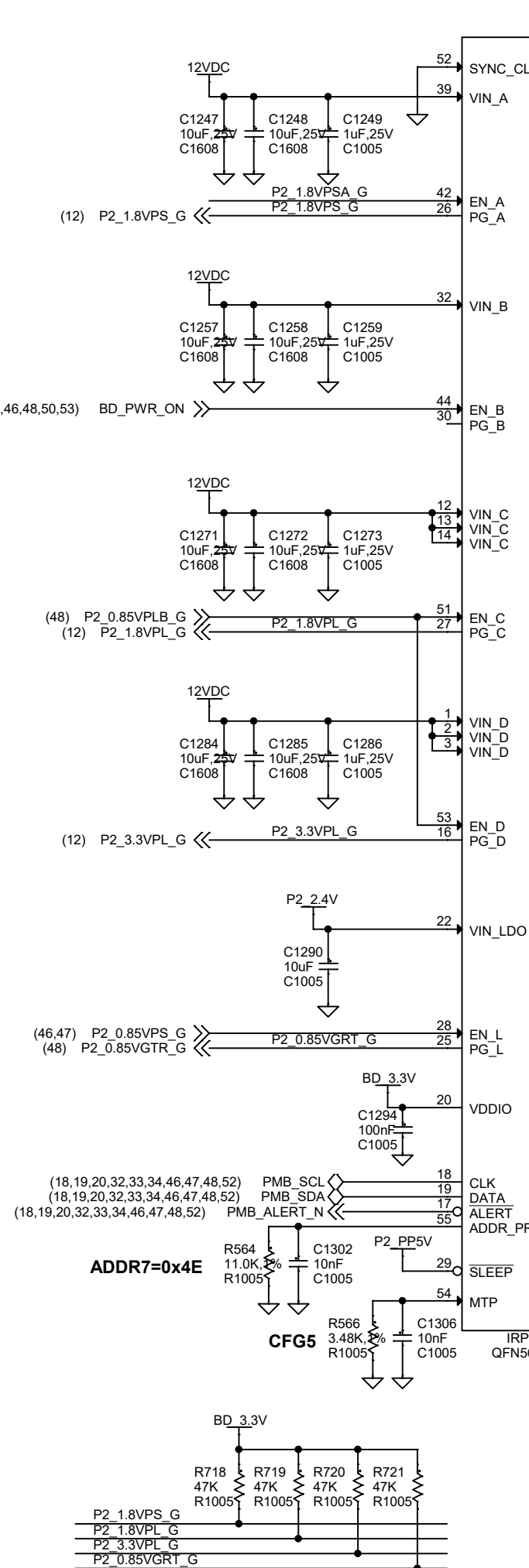
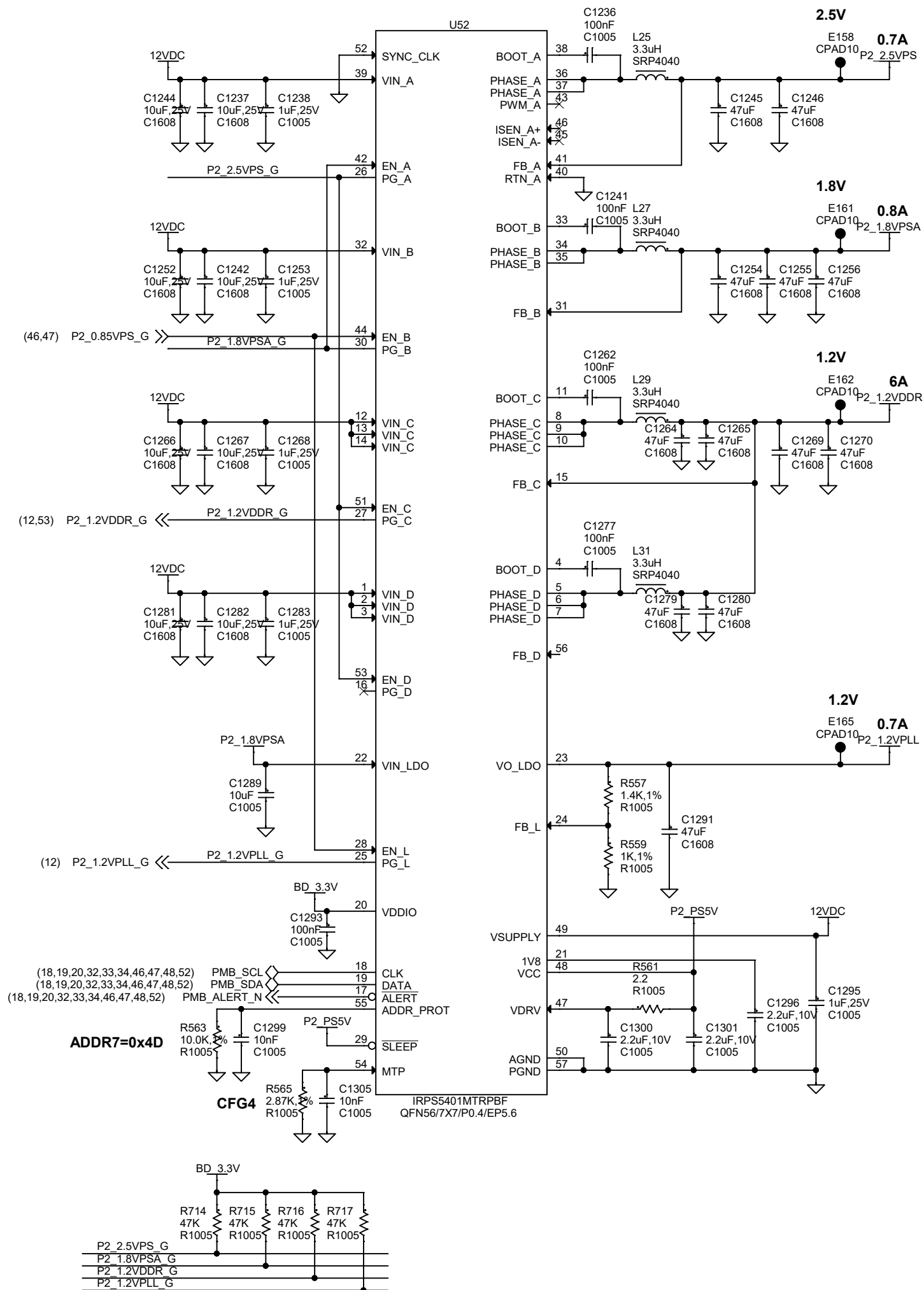


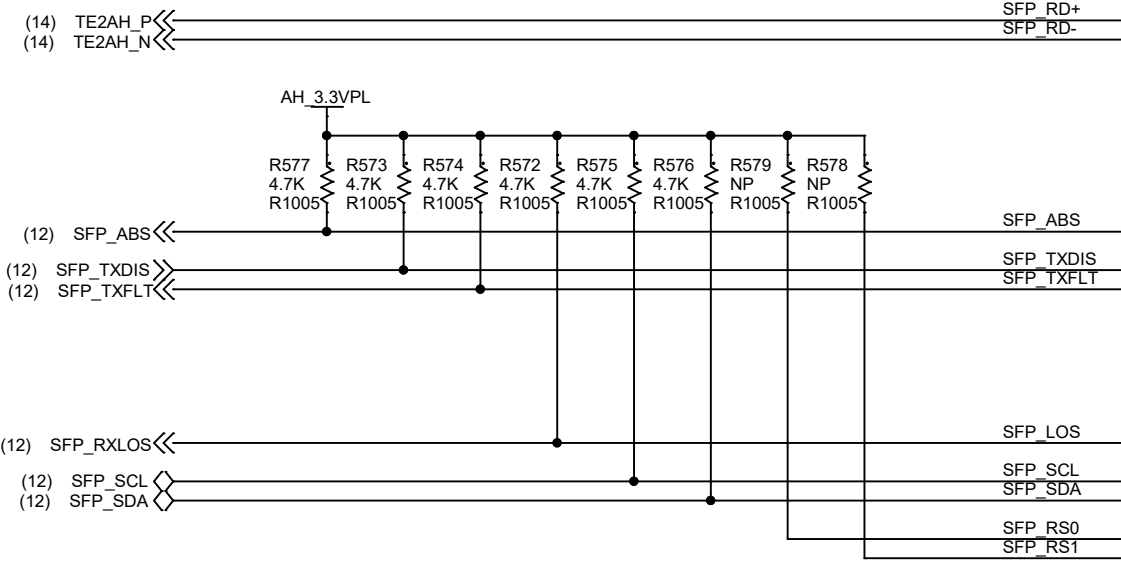
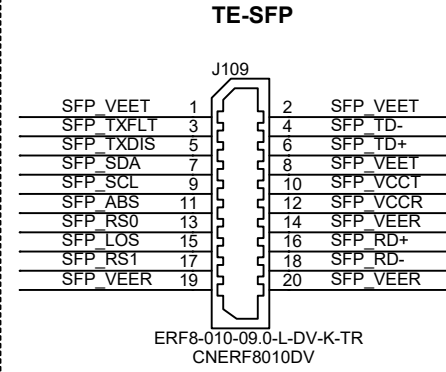
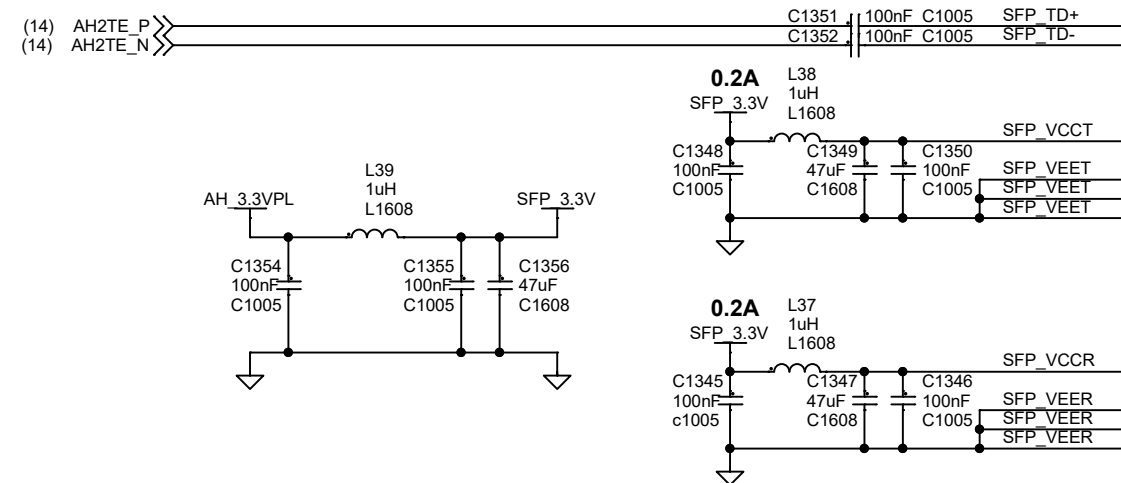
Programmer: ClockBuilder Field Programmer Kit (CBPROG-DONGLE)



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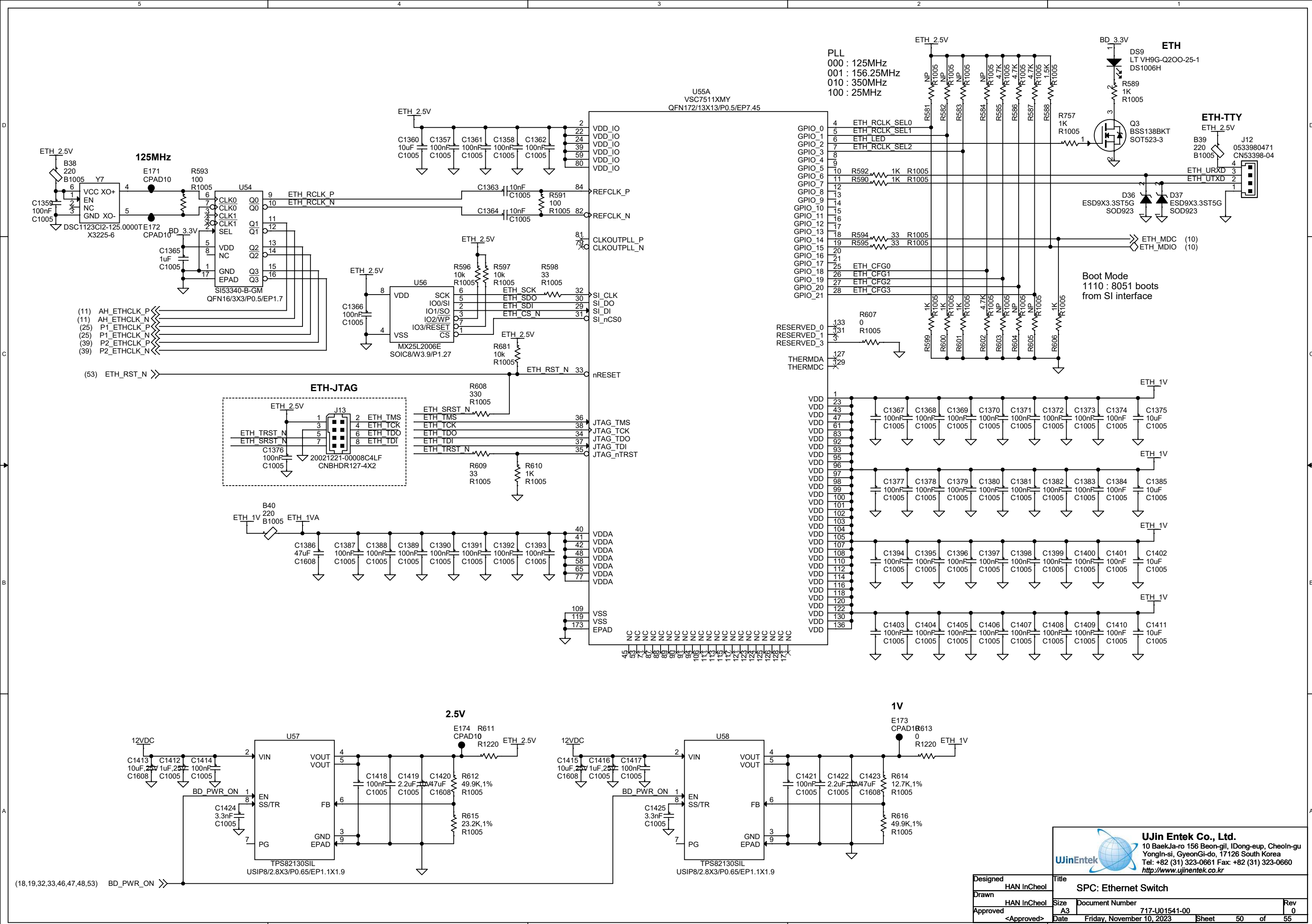
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Drawn	HAN InCheol	Size	Document Number	Rev
Approved	<Approved>	A3	717-U01541-00	0
		Date	Friday, November 10, 2023	Sheet 45 of 55

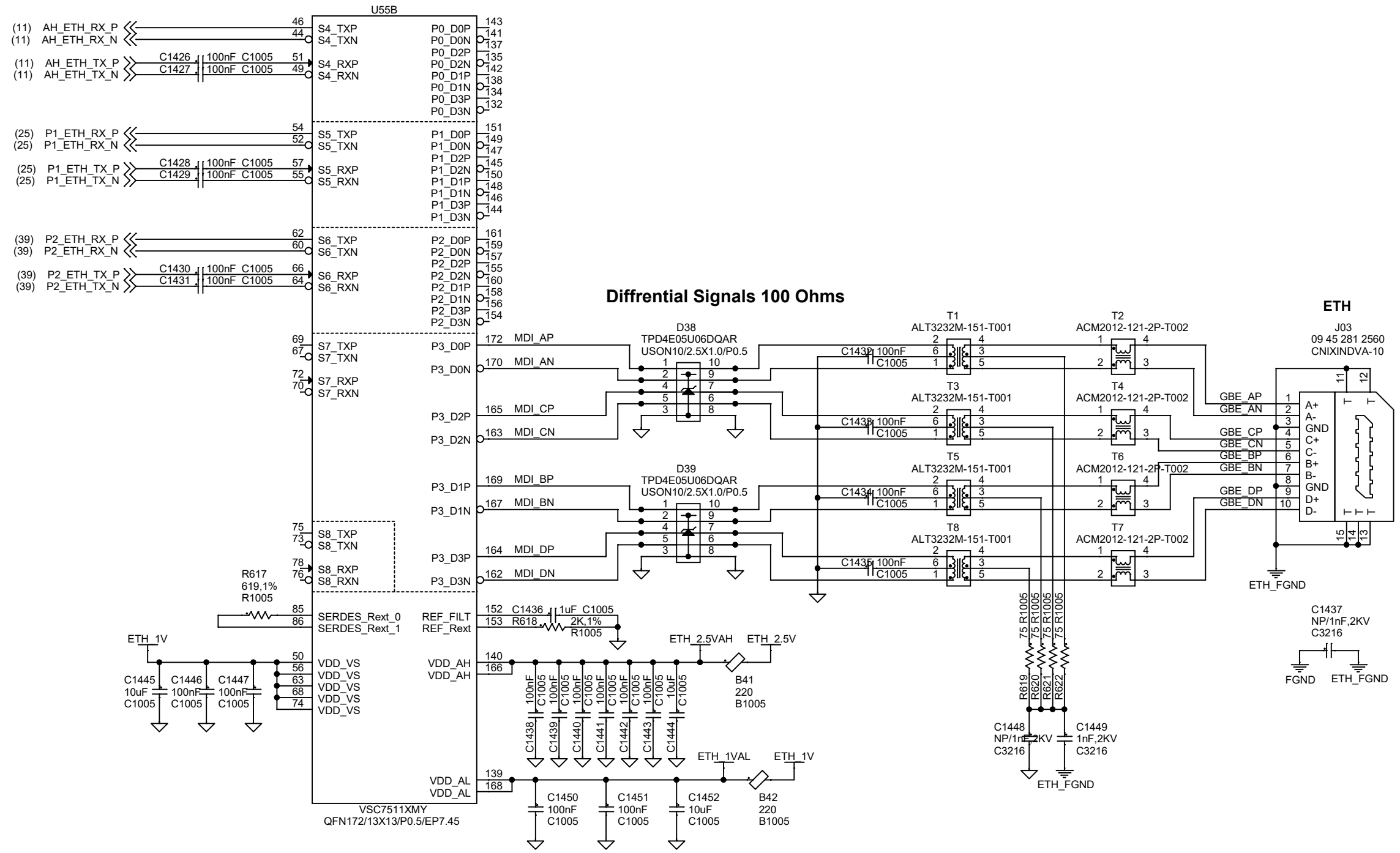


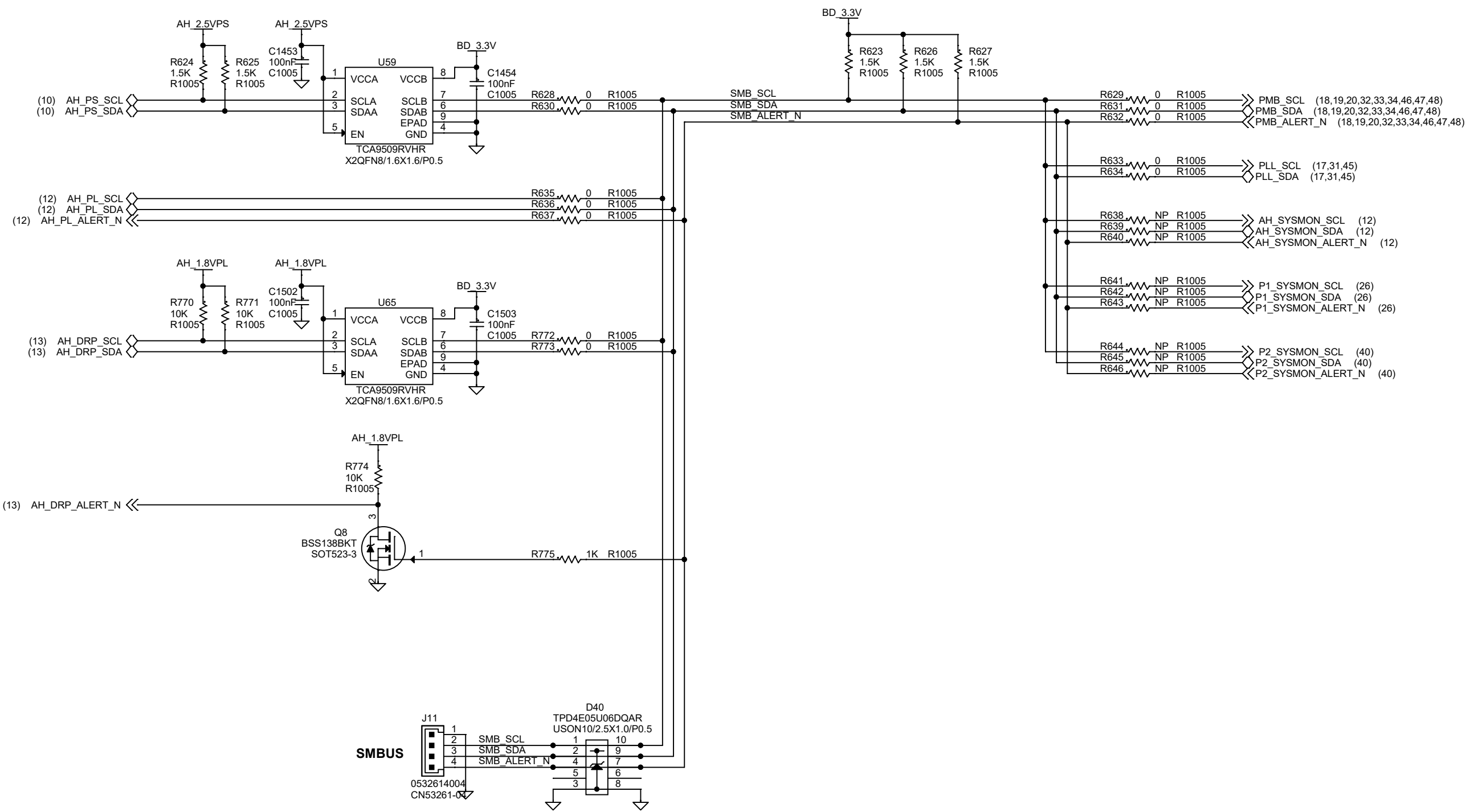


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Designed	HAN InCheol	Title	SPC: TE SFP Interface
Drawn	HAN InCheol	Size	A3
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		Date	Friday, November 10, 2023
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Drawn	HAN InCheol	Size	Document Number	Rev
Approved	<Approved>	A3	717-U01541-00	0
		Date	Friday, November 10, 2023	Sheet 52 of 55

