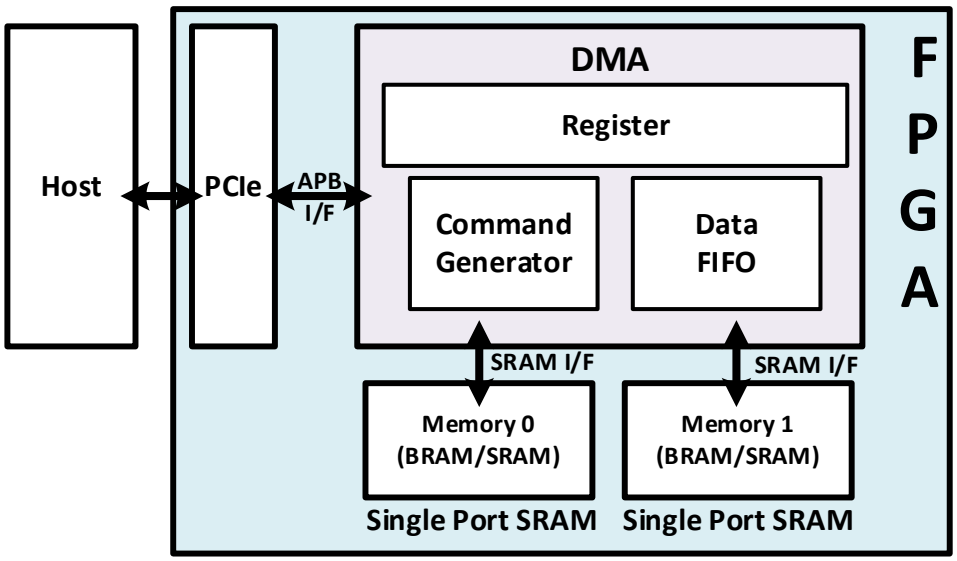
CastLab

LAB 2 (Simple DMA FPGA Test)

I. Objective

- Understand the basic Hardware Design flow by testing their design on FPGA.

II. Top Architecture



➢ **led signal is connected to LED on FPGA. (led0: Interrupt, led1, 2: Test Result)**

Table 3-29: **VCU118 GPIO Connections to FPGA U1**

FPGA (U1) Pin		Schematic Net Name	FPGA (U1) Direction	I/O Standard	Device
GPIO LEDs (Active-High) GPIO_LED signals are wired to FET LED drivers					
BANK 40	AT32	GPIO_LED_0	Output	LVCMOS12	DS7
BANK 40	AV34	GPIO_LED_1	Output	LVCMOS12	DS6
BANK 40	AY30	GPIO_LED_2	Output	LVCMOS12	DS8
BANK 40	BB32	GPIO_LED_3	Output	LVCMOS12	DS9
BANK 40	BF32	GPIO_LED_4	Output	LVCMOS12	DS10
BANK 42	AU37	GPIO_LED_5	Output	LVCMOS12	DS12
BANK 42	AV36	GPIO_LED_6	Output	LVCMOS12	DS13
BANK 42	BA37	GPIO_LED_7	Output	LVCMOS12	DS18

III. Supported Features

- Supported Feature in Lab 1
- **+ Test Mode**
  : When Mode Register(0x000C) is set to 2, the Design(DUT) should operate in Test Mode.
  : Please refer to the Ⅵ. Operation.

IV. Interface

- **Global**

Name	Bit	I/O	From/To	Clock	Description
CLK	1	I	Global	200MHz	Clock
RSTN	1	I	Global	200MHz	Reset Signal (Active Low)
INTR	1	O	SHELL	200MHz	Interrupt Signal (High Level Detection) (LED0)
LED	**2**	**O**	**Global**	**200MHz**	**Test Result (01: Fail, 10: Success) (LED1, 2)**

- **APB (Base Address : 0x0000_0000)**

Name	Bit	I/O	From/To	Clock	Description
PSEL	1	I	SHELL	200MHz	APB Select Signal
PENABLE	1	I	SHELL	200MHz	APB Enable Signal
PREADY	1	O	SHELL	200MHz	APB Ready Signal
PWRITE	1	I	SHELL	200MHz	APB Write Signal
PADDR	32	I	SHELL	200MHz	APB Address Signal
PWDATA	32	I	SHELL	200MHz	APB Write Data
PRDATA	32	O	SHELL	200MHz	APB Read Data

- **Memory 0 (Base Address : 0x0010_0000)**

Name	Bit	I/O	From/To	Clock	Description
mem0_en	1	O	Memory 0	200MHz	Memory Enable
mem0_we	4	O	Memory 0	200MHz	Memory Write Enable (byte enable)
mem0_addr	16	O	Memory 0	200MHz	Memory Address Signal
mem0_wdata	32	O	Memory 0	200MHz	Memory Write Data
mem0_rdata	32	I	Memory 0	200MHz	Memory Read Data

- **Memory 1 (Base Address : 0x0020_0000)**

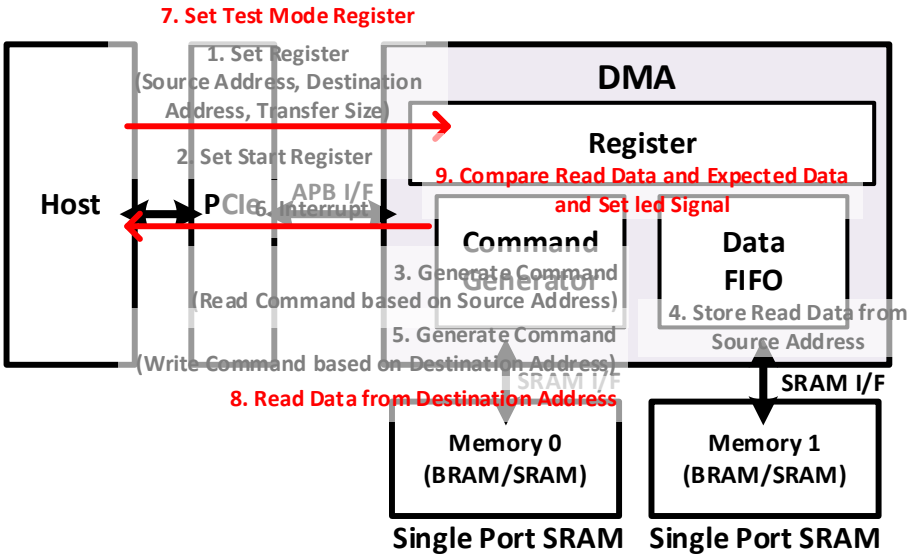
Name	Bit	I/O	From/To	Clock	Description
mem1_en	1	O	Memory 1	200MHz	Memory Enable
mem1_we	4	O	Memory 1	200MHz	Memory Write Enable (byte enable)
mem1_addr	16	O	Memory 1	200MHz	Memory Address Signal
mem1_wdata	32	O	Memory 1	200MHz	Memory Write Data
mem1_rdata	32	I	Memory 1	200MHz	Memory Read Data

V. Register Map

- **APB Register (Base Address : 0x0000_0000)**

Offset	Category	Name	Bit	Attribution	Description
0x0000	Config	Source Address	[31:0]	RW	Source Address
0x0004		Destination Address	[31:0]	RW	Destination Address
0x0008		Size	[31:0]	RW	Transfer size (in byte)
0x000C		Mode	[31:0]	RW	0: Idle, 1: Start Normal Transfer Operation, 2: Start Test
0x0010	Status	Interrupt	[31:0]	RW	Interrupt (Write : Clear Only)
0x0014 -0xFFFF	(RFU)	(RFU)	[31:0]	(RFU)	(RFU)

VI. Operation



<Overall Operation> - 1-6
- Same as Lab 1.

<Test Mode Operation> - 7-9

1) Set DMA Mode Register(0xC) to **2**(Test Mode Start).

2) DMA generate Command based on Register Value. (Read data from **Destination** Address.)

3) DMA compare Read Data and Expected Data(Given).

4) If Read Data and Expected Data are the same, the led signal is set to 2'b10, otherwise, set to 2'b01.