Power Electronics
Voltage Controller Design

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***Abstract* - Voltage control design allows many kinds of electronics to operate on a single power source. Among the various converters, the DC-DC Buck Converter allows us to lower the high voltage to the desired voltage and use it. In addition, the PI Controller can satisfy the system response conditions such as overshoot, rising time, and removal of steady state errors. In this experiment, when DC $12[V]$ is applied to Buck Converter, the output voltage is reduced to $5[V]$. In addition, the PI Controller is designed so that $5[V]$ is output even if $12[V]$ changes. For this purpose, obtain Buck Converter Modeling, PI Controller Modeling, and Feedback Gain. In case of Buck Converter, the output voltage varies with duty cycle. So it controls the reference voltage to control the duty cycle. If you insert the step input into the controlled Buck Converter, you can check that the overshoot, rising time and settling, etc are all controlled as desired. In addition, it can be seen that $5[V]$ is output even if the voltage changes between $8[V]$ and $16[V]$.**

I. Introduction

Many of the appliances and electronics we use have their own operating voltage range, depending on the internal IC, and the voltage precision requirements vary. So, we need a converter that gives voltage multiplication or pressure. Typical converters include Buck Converter, Boost Convert, Buck-Boost Converter and Flyback Converter. In this experiment, the 12V battery in a car is changed to 5V to make a converter that charges the product. The simplest way to lower the voltage is to use a linear regulator. However, the linear regulator disperses extra power into heat, so it is very energy-wasting. A simple converter is Buck Converter, which efficiently compresses voltage. In the case of Buck Converter, 95% more efficient than linear controls.when used IC. In this experiment, DC-DC Buck Converter is designed to reduce voltage. Then, after designing Buck Converter, satisfy the given conditions (overshooting, rising time, steady state error, setting time, Magnitude and phase margin) through the PI controller. Make sure the product is not destroyed.

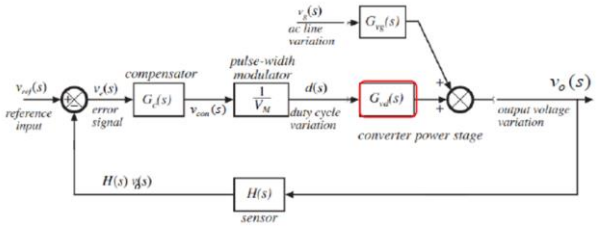


Figure 1. Overall Block Diagram

First, calculate the Capacitor, Inductor, and PI Controller gains for Buck Converter. Second, verify that the system operates safely using Matlab and PSIM. Third, implement Buck Converter and PI Controller and compare with simulation. Finally, check the difference between the experimental results and the simulation results, and explain our thoughts through discussion and analysis.

II. Preliminary

A. Buck Converter

DC-DC Buck Convert outputs DC output voltage by lowering the DC input voltage. Buck Converter consists of switch, diode, inductor, capacitor, load resistor. Buck Converter's switch uses the MOSFET Firing Circuit. We can control the duty cycle of the switch by adjusting the reference voltage of the MOSFET Firing Circuit.

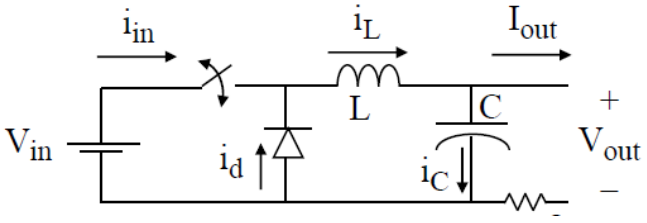


Figure 2. DC-DC Buck Converter

To analyze Buck Converter in an ideal state we must make four assumptions to maintain stable operation. First, the circuit is analyzed under the assumption of steady state. Second, Buck Converter operates in Continuous Conduction Mode(CCM). Third, the capacitance of the capacitor is large, therefore

output voltage is ripple-free. Fourth, input power and output power are the same.

The time when the switch is closed is called DT, and when the switch is open it is called $(1-D)T$.
When the switch is closed, the diode is open because it is reverse biased. In addition, the inductor voltage(v_L) and the inductor current(i_L) are as follows.

$$v_L = V_{in} - V_{out}$$

$$v_L = L\frac{di_L}{dt}$$

$$(\Delta i_L)_{closed} = \frac{V_{in} - V_{out}}{L} \times DT$$

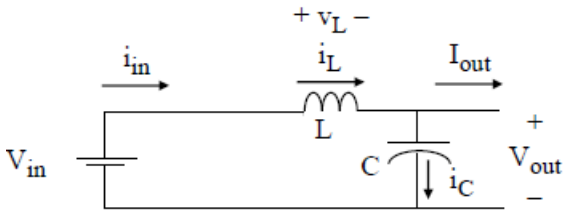


Figure 3. Switch Closed for DT Seconds

On the contrary, when the switch is open, the power supply is cut off and the diode become short. In addition, v_L and i_L will be as follows.

$$v_L = -V_{out}$$

$$v_L = L\frac{di_L}{dt}$$

$$(\Delta i_L)_{open} = \frac{-V_{out}}{L} \times (1-D)T$$

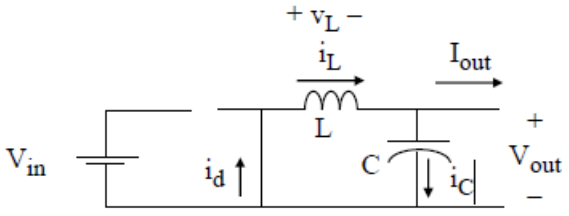


Figure 4. Switch Open for $(1-D)T$ Seconds

We analyze the circuit in the steady state. Therefore, the sum of $(\Delta i_L)_{closed}$ and $(\Delta i_L)_{open}$ is the same.

$$(\Delta i_L)_{closed} + (\Delta i_L)_{open} = 0$$

$$\frac{V_{in} - V_{out}}{L} \times DT - \frac{V_{out}}{L} \times (1-D)T = 0$$

As a result, output voltage and input voltage have the following relationship.

$$V_{out} = V_{in} \times D$$

When KCL is used, i_L is the sum of the capacitor current(i_c) and output current(I_{out}). Because the i_c for one cycle in the steady state is zero, the average inductor current(I_L) and I_{out} are the same.

$$I_L = I_{out} = \frac{V_{out}}{R_{Load}}$$

Maximum inductor current and minimum inductor current are as follows.

$$i_{L,max} = I_L + \frac{\Delta i_L}{2} = V_{out} \times (\frac{1}{R_{Load}} + \frac{1-D}{2Lf})$$

$$i_{L,min} = I_L - \frac{\Delta i_L}{2} = V_{out} \times (\frac{1}{R_{Load}} - \frac{1-D}{2Lf})$$

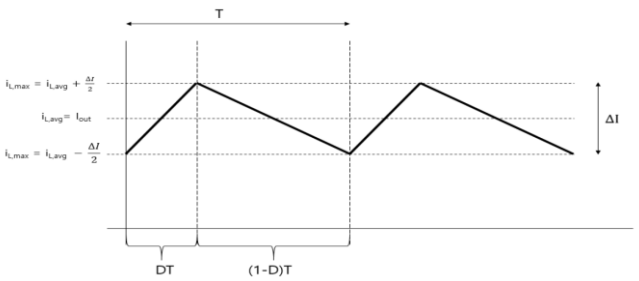


Figure 5. Inductor Current Waveform

Since the circuit operates in the CCM, the minimum inductor current must always be greater than zero. Therefore, the minimum inductance for CCM operation can be obtained as follows.

$$i_{L,min} \geq 0$$

$$i_{L,min} = V_{out} \times \left(\frac{1}{R_{Load}} - \frac{1-D}{2Lf}\right) = 0$$

$$L_{min} = \frac{(1-D)R_{Load}}{2f}$$

Four assumptions were made to ideally assume and analyze Buck Converter. But, in real world, even though the capacitance of the capacitor is very large, output voltage ripple exists. The output voltage ripple is as follows.

$$(\Delta Q: current\ charge\ amount\ of\ capacitor)$$

$$\Delta Q = C \times \Delta V_{out}$$

$$\Delta Q = \frac{1}{2} \times \frac{T}{2} \times \frac{\Delta i_L}{2} = \frac{\Delta i_L}{8f}$$

$$\Delta V_{out} = \frac{V_{out}(1-D)}{8LCf^2}$$

$$\frac{\Delta V_{out}}{V_{out}} = \frac{(1-D)}{8LCf^2}$$

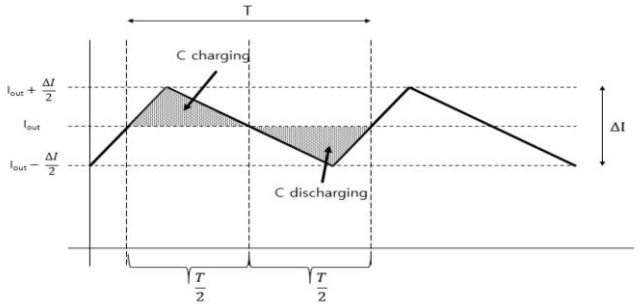


Figure 6. Current Charge Amount of Capacitor by Inductor Current Graph

B. PI Controller

The PI Controller basically has the form of a feedback controller. The PI Controller calculates the error by comparing the output value of the target with reference value. And it uses this error to calculate the control value.

The Proportional(P) Controller change the amount of control in proportion to the error value. An error is the difference between the desired control objective and the actual control state. The P Controller outputs the input value close to the target by multiplying the error by the protocol gain. The use of P Controller can speed up the system's response and cause overshoots. P Controller doesn't remove a steady state error.

Integral(I) Controller eliminates steady state errors by integrating and printing residual errors. But, I Controller could make the rising time of the system. The following expression is the Manipulated variable(MV) of the PI Controller.

$$MV(t) = K_p e(t) + K_i \int_0^t e(t)dt$$

In analogue circuits, the PI Controller is implemented using Op-amp. Figure 7. it is P Controller circuit and gain is as follows.

$$K_p = \frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1}$$

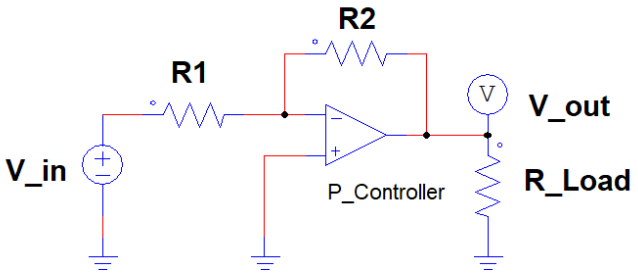


Figure 7. P Controller by PSIM

Figure 8. it is I Controller circuit, gain is as follows.

$$K_i = \frac{V_{out}}{V_{in}} = -\frac{Z_2}{Z_1} = -\frac{1}{R_1} \cdot \frac{1}{sC+1}$$

$$sC \gg 1 \rightarrow K_i = -\frac{1}{R_1} \cdot \frac{1}{sC}$$

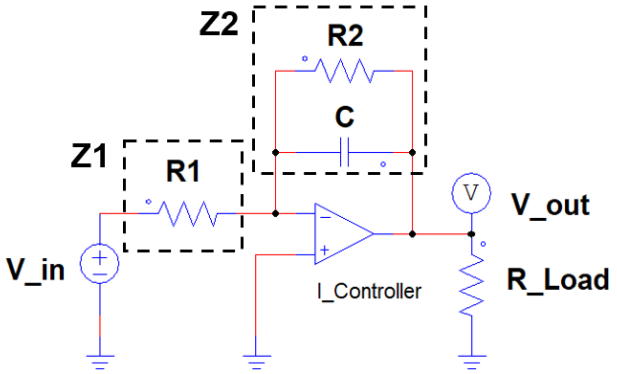


Figure 8. I Controller by PSIM

Figure 9. it is PI Controller circuit, gain is as follows.

$$\frac{V_{out}}{V_{in}} = \frac{Z_2}{Z_1} = -\left(\frac{R_2}{R_1} + \frac{1}{R_1 C} \cdot \frac{1}{s}\right)$$

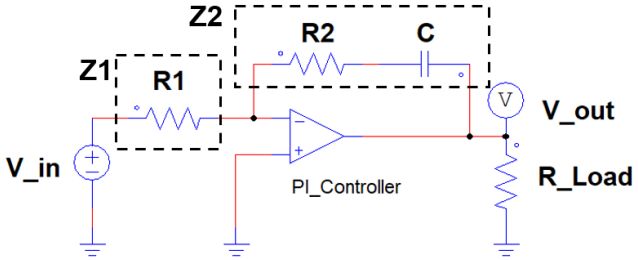


Figure 9. PI Controller by PSIM

III. Buck Convertor Modeling

A. Buck Converter Design

Determine the minimum inductance for the circuit to operate in CCM.

$$L_{min} = \frac{(1-D)R_{Load}}{2f}$$

$$L_{min} = \frac{\left(1-\frac{5}{12}\right)[-] \times 10[\Omega]}{2 \times 150[kHz]} = 19.44[\mu H]$$

To implement stable operating in CCM, determine the inductance of $40[\%]$ margin.

$$L = \frac{\left(1-\frac{5}{12}\right)[-] \times 10[\Omega]}{2 \times 150[kHz]} \times 1.4 = 27.22[\mu H]$$

When L and ΔV_{out} are as follows, determine capacitance.

$$L = 27.22[\mu H], \qquad \Delta V_{out} = 0.5[V]$$

$$C = \frac{(1-D)}{8Lf^2} \times \frac{V_{out}}{\Delta V_{out}}$$

$$C = \frac{\left(1-\frac{5}{12}\right)[-]}{8 \times 27.22[\mu H] \times 150[kHz]^2} \times \frac{5[V]}{0.5[V]} = 1.19[\mu F]$$

Therefore, use inductor and capacitor that meet the following conditions when designing Buck Converter.

$$L \geq 27.22[\mu H], \qquad C \geq 1.19[\mu F]$$

Inductor prevents over-currents and improves circuit stability. However, too large inductance causes disadvantageous to switching. The larger the capacitance, the more constant the output voltage is. However, when the capacitance is greater than $220[\mu F]$, the pole in the root locus goes to the right-half place. It causes unstable system. In consideration of this conditions, we have used the elements in designing Buck Converter.

Parameter		**Values**
Buck Converter	L	$220[\mu H]$
	C	$100[\mu F]$

Table 1. Buck Converter Specification

B. Buck Convertor Modeling

Set up a differential equation for modeling the Buck Converter.

$$\frac{dx}{dt} = \dot{x} = f(x(t), u(t), t)$$

$$x(t) : state\ vector$$

$$u(t): input\ vector$$

It is very difficult to analyze the dynamic system in real world. Because the system is not linear, the input changes over time. So, we can set up two options for model simulations. First, time invariant. Second, linearity. Most systems can be assumed to be linear in the small operating range. The following is a state-space model differential equation in the LTI system.

$$\frac{dx(t)}{dt} = Ax(t) + Bu(t)$$

$$y(t) = Cx(t) + Eu(t)$$

$\dot{x}(t): time\ derivative\ of\ the\ state\ vector$

$y(t): output\ vector$

$A: system\ matrix, \qquad B: input\ matrix$

$C: output\ matrix, \qquad E: feedforward\ matrix$

Buck Converter has two states depending on switch on/off. Therefore, there are two state equations.

Switch on:

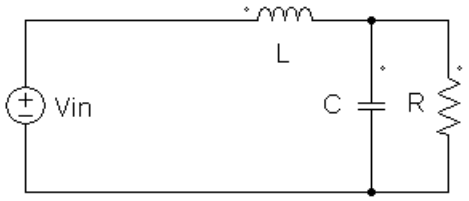


Figure 10. Buck Converter when Switch On

When switch on, determine a state equation using KVL, KCL.

$$v_g = L\frac{di_L}{dt} + v_o$$

$$i_L = C\frac{dv_c}{dt} + \frac{v_o}{R}$$

$$\begin{pmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{pmatrix} = \begin{pmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{pmatrix} \begin{pmatrix} i_L \\ v_o \end{pmatrix} + \begin{pmatrix} \frac{1}{L} \\ 0 \end{pmatrix} v_g = A_1 \begin{pmatrix} i_L \\ v_o \end{pmatrix} + B_1 \cdot v_g$$

Switch off:

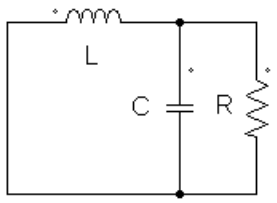


Figure 11. Buck Converter when Switch Off

When switch off, determine a state equation using KVL, KCL.

$$L\frac{di_L}{dt} + v_o = 0$$

$$i_L = C\frac{dv_c}{dt} + \frac{v_o}{R}$$

$$\begin{pmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{pmatrix} = \begin{pmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{pmatrix} \begin{pmatrix} i_L \\ v_o \end{pmatrix} + \begin{pmatrix} 0 \\ 0 \end{pmatrix} v_g = A_2 \begin{pmatrix} i_L \\ v_o \end{pmatrix} + B_2 \cdot v_g$$

Result of state-space averaging when switch on/off is the state equations of the equilibrium. If we can write the converter state equations during switch on/off, then the averaged DC model can be found. Determine each average of system matrix(A) and input matrix(B).

System matrix:

$$A_{avg} = \frac{(A_1 \cdot T_{ON} + A_2 \cdot T_{OFF})}{T_S}$$

$$A_{avg} = A_1 \cdot d + A_2 \cdot (1-d)$$

$$A_{avg} = \begin{pmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{pmatrix} d + \begin{pmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{pmatrix} (1-d)$$

$$A_{avg} = \begin{pmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{pmatrix}$$

Input matrix:

$$B_{avg} = \frac{(B_1 \cdot T_{ON} + B_2 \cdot T_{OFF})}{T_S}$$

$$B_{avg} = B_1 \cdot d + B_2 \cdot (1-d)$$

$$B_{avg} = \begin{pmatrix} \frac{1}{L} \\ 0 \end{pmatrix} d + \begin{pmatrix} 0 \\ 0 \end{pmatrix} (1-d)$$

$$B_{avg} = \begin{pmatrix} \frac{1}{L} \\ 0 \end{pmatrix} d$$

Find state equations about Buck Converter.

$$K\frac{dx(t)}{dt} = Ax(t) + Bu(t)$$

$$\begin{pmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{pmatrix} = \begin{pmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{pmatrix} \begin{pmatrix} i_L \\ v_o \end{pmatrix} + \begin{pmatrix} \frac{v_g}{L} \\ 0 \end{pmatrix} d$$

$$\dot{x} = \begin{pmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{pmatrix}, A = \begin{pmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{pmatrix}, B = \begin{pmatrix} \frac{v_g}{L} \\ 0 \end{pmatrix}, u = D$$

When the equilibrium condition is satisfied, the state estimate is as follows.

$$\dot{x} = 0 \rightarrow 0 = Ax + Bu$$

$$x = -A^{-1}\,Bu = \begin{pmatrix} i_L \\ v_o \end{pmatrix}$$

The transfer function of the system is obtained by switching from the time domain to the frequency domain. Buck Converter has two inputs which are duty cycle(d) and input voltage(v_g). Because it is an LTI system, the output voltage can be expressed using superposition.

$$V_o(s) = G_{vd}(s)D(s) + G_{vg}(s)V_g(s)$$

The transfer function of output voltage, which is output when input is duty cycle, is as follows.

$$G_{vd}(s) = \frac{V_o(s)}{D(s)}|_{V_g(s)=0}$$

The state equations of the time domain is converted to the frequency domain to obtain the transfer function of the system.

$$\dot{x} = Ax + Bu \rightarrow sX = AX + BU \rightarrow X = (sI - A)^{-1}BU$$

$$Y(s) = CX(s) + EU(s)$$

The transfer function is as follows because the duty cycle is input.

$$G_{vd}(s) = \frac{Y(s)}{U(s)} = \frac{V_o(s)}{D(s)} = C(sI - A)^{-1}B$$

$$(sI - A)^{-1} = \begin{pmatrix} s & \frac{1}{L} \\ -\frac{1}{C} & s + \frac{1}{RC} \end{pmatrix}^{-1}$$

$$(sI - A)^{-1} = \frac{1}{s^2 + \left(\frac{1}{RC}\right)s + \left(\frac{1}{LC}\right)} \begin{pmatrix} s + \frac{1}{RC} & -\frac{1}{L} \\ \frac{1}{C} & s \end{pmatrix}$$

$$G_{vd}(s) = \frac{\frac{v_g}{LC}}{s^2 + \left(\frac{1}{RC}\right)s + \left(\frac{1}{LC}\right)}$$

Calculate the transfer function by substituting the L, C values designed by A. Buck Converter Design above.

$$G_{vd}(s)$$

$$= \frac{\frac{12[V]}{220[\mu H] \times 100[\mu F]}}{s^2 + \left(\frac{1}{10[\Omega] \times 100[\mu F]}\right)s + \left(\frac{1}{220[\mu H] \times 100[\mu F]}\right)}$$

$$G_{vd}(s) = \frac{545454545.5}{s^2 + 1000s + 45454545.45}$$

Buck Converter when PI Controller is not designed. Check the magnitude margin and phase margin of the Buck Converter on the Bode plot.

$$(magnitude\ margin) = infinite$$

$$(phase\ margin) = 2.55[°]$$

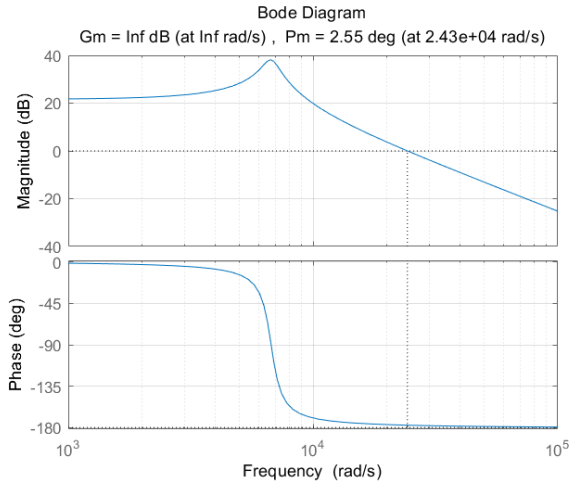


Figure 12. Buck Converter Margin without PI Controller

Check the pole in Figure 13. In the Root locus, the pole exists on the left half, and has a high natural frequency. This allows us to expect the system to respond quickly and a lot of oscillations.

$$\text{Pole} = -500 + 6.72(10^3)i[ds]$$

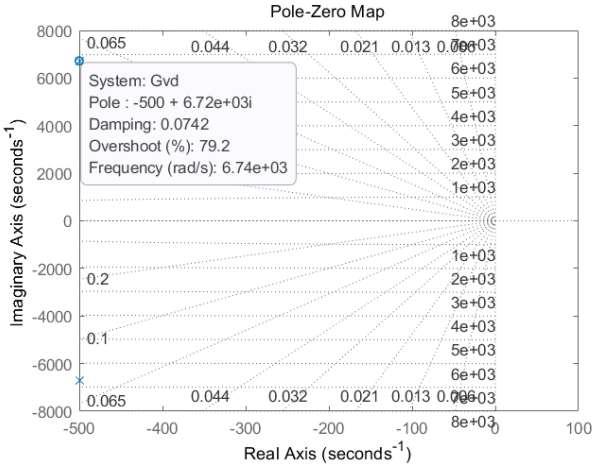


Figure 13. Buck Converter Pole in Root Locus

In Figure 14, 15. identified Buck Converter's response to step response with MATLAB and PSIM. Overshoot is approximated to $8.9[V]$, rising time to $0.2[ms]$. Therefore, we can confirm that Buck Converter modeling is correct.

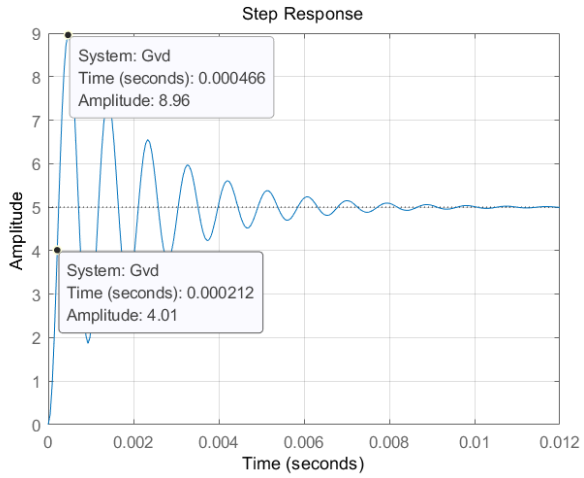
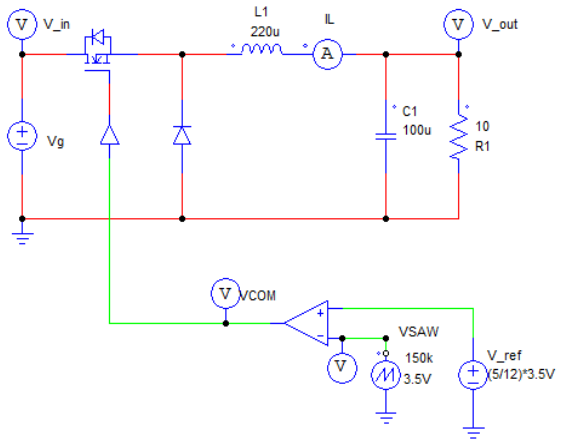
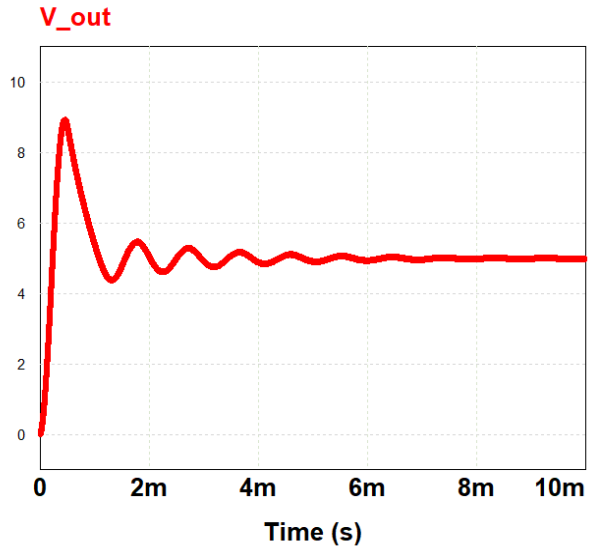


Figure 14. Buck Converter Output Voltage Graph by Matlab



(a) Buck Converter by PSIM



(b) Buck Converter Output Voltage Graph by PSIM

	x1	x2
Time	2.11149e-004	4.66694e-004
V_out	4.04829e+000	8.94661e+000

(c) Buck Converter Output Voltage Chart by PSIM

Figure 15. Buck Converter by PSIM

IV. PI Controller Design Method

A. Design Feedback Gain for Removing Disturbance

Before PI Controller Modeling, we must set the feedback for closed loops. At this time we changed the feedback gain to maintain the $5[V]$ output of Buck without being affected by changes in the input voltage. The Buck Converter we designed is a system with an input of $12[V]$ and an output of $5[V]$. Therefore, in order to maintain this input and output relationship, the maximum output voltage and max of PWM modulation should be adjusted through the feedback gain. The PWM modulation we used has a maximum voltage of $3.5[V]$ of the sawtooth wave.

$$V_{max} = 3.5[V], \qquad V_{out(max)} = 12[V]$$

Therefore, the feedback gain should be adjusted to $V_{\max}$ / $V_{out(max)}$ to match each other's maximum values.

$$H(s) = \frac{V_{max}}{V_{out(max)}} = \frac{5}{12}$$

B. PI Controller Design

The Buck Converter specification we are trying to obtain is as follows. Since the current system is not satisfied with this specification, we want to design a PI controller to satisfy the specification.

Parameter	Values
Gain Margin	>10 [dB]
Phase Margin	>20 [deg]
Rise Time	<15 [ms]
% Rise	80 %
Settling Time	<30 [ms]
% Settling	<5 %
% Overshoot	<10 %

Table 2. Voltage Control Specification

The delivery function of the PI Controller we designed is as follows.

$$G_c(s) = K_p + \frac{K_i}{s} = \frac{K_p s + K_i}{s} = \frac{K_p(s + K_i/K_p)}{s}$$

Therefore, if the ratio of K_i and K_p is Z, the transfer function of controller is organized as follows:

$$K = K_p, \qquad Z = \frac{K_i}{K_p}$$

$$G_c(s) = \frac{K(s+Z)}{s}$$

Z is determined first and K_p is determined to calculate and derive the K_i value. Root Locus was used to determine K_p and K_i.

- Finding Z Range $(Z = K_i/K_p)$

To determine the range of Z, K was assumed to be 1, then Z was changed to see the system characteristics according to the position of the pole when K went from zero to infinity, respectively. First, Z was set to $500[-]$, $1000[-]$, $1500[-]$, and $2000[-]$ respectively to identify rough stable sections.

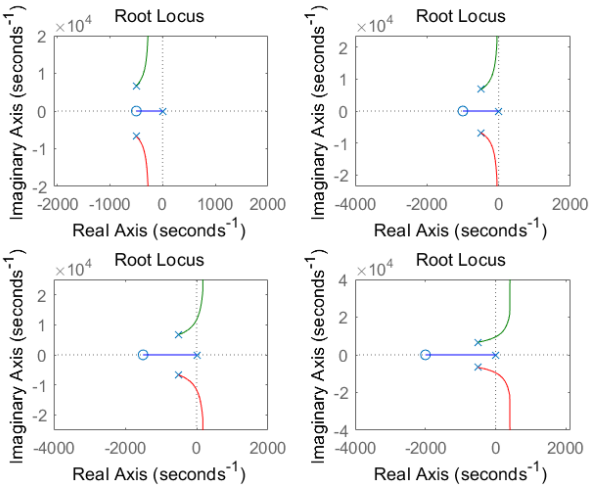


Figure 16. Root Locus at Different Z Values (1)

The above figure shows that if Z is over $1000[-]$, the position of the pole is positive, and the system is quickly unstable as K increases. In addition, if it is less than $500[-]$, it is difficult to design it smaller than $500[-]$ because it is easy to cause oscillations as K increases. Therefore, the range of K can be seen from $500[-]$ to $1000[-]$.

$$500[-] \leq K < 1000[-]$$

Next, Root Locus was identified by subdividing the values between them into $500[-]$, $700[-]$, $800[-]$, and $1000[-]$

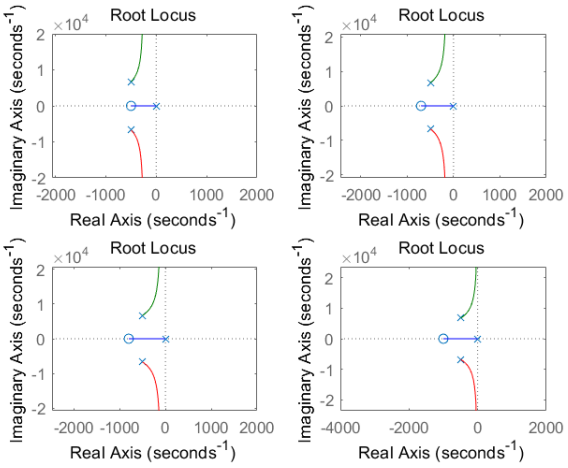


Figure 17. Root Locus at Different Z Values (2)

The results show that the ossification increases rapidly as the K value increases when Z is $500[-]$, except when Z is $1000[-]$, because the pole has to go to a stable section regardless of the value of K. Therefore, Z was specified as $800[-]$ to satisfy both stables and oscillations.

$$Z = \frac{K_i}{K_p} = 800[-]$$

- Finding K_p

We set the Z above as $800[-]$ to find the K_p value, which is the gain. The value was found using SISO TOOL in MATLAB to check the margin and step response of the system. Using SISO TOOL, you can check the system's bode plot and step response while changing the position of the system's pole. Therefore, we adjust the value of K to secure the margin we want and check the rising time and overshoot by looking at the step response to set the value that can come into the specification that we want. We set K to $0.3[-]$ because we satisfy all the specifications we want.

$$K = K_p = 0.3[-]$$

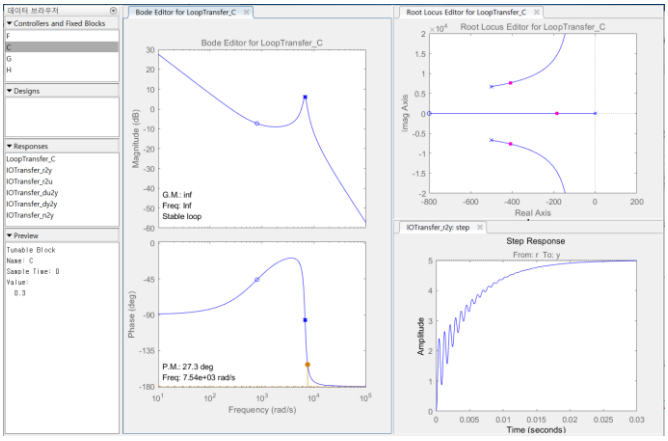


Figure 18. Finding K by SISO Tool in Matlab at K=0.3

Since the value of Z is set to $800[-]$, the value of K_i is calculated as K_p becomes 0.3 and K_i has a value of 240. Therefore, K_p and K_i have the following values:

$$K_p = 0.3[-], \qquad K_i = 240[-]$$

The margins found in the Bode Plot of SISO TOOL are as follows.

$$(Gain\ Margin) = \inf\,[dB]$$

$$(Phase\ Margin) = 27.3\ [deg]$$

$$(rising\ time) = 0.0075\ [sec]$$

$$(settling\ time) = 0.00159\ [sec]$$

Since the values satisfy all of the specifications we want, the transfer function of the controller using the current K_p and K_i values is as follows.

$$G_C(s) = \frac{0.3s + 240}{s}$$

V. Voltage Control System

We would like to see the transmission function of the previously modelled buck converter and PI controller when it is a closed loop of the whole system.

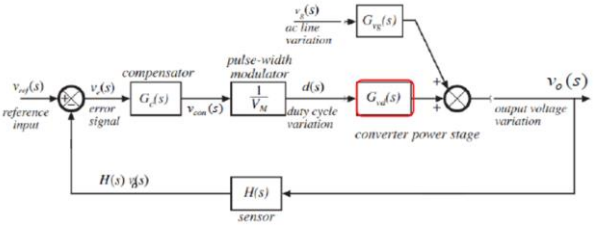


Figure 19. Overall Block Diagram

When the transfer function obtained earlier from the entire system is obtained, it is as follows.

$$G_C(s) = \frac{0.3s + 240}{s}$$

$$\frac{1}{V_M} = \frac{1}{3.5}$$

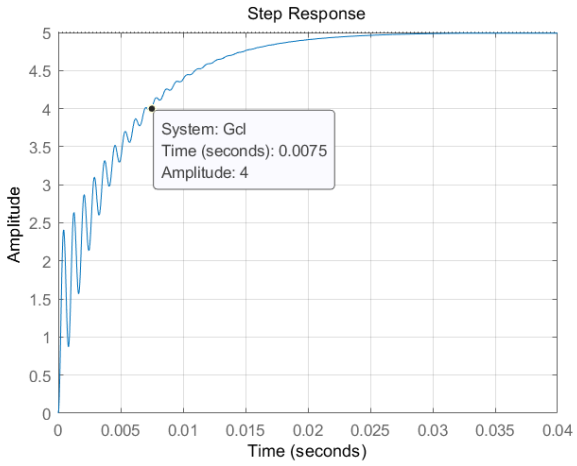
$$G_{vd}(s) = \frac{545454545.5}{s^2 + 1000s + 45454545.45}$$

$$H(s) = \frac{5}{12}$$

Thus, by calculating the close loop with each of these transfer functions, the transfer function of the whole system is derived as follows.

$$G_{cl}(s) = \frac{4.675 * 10^7 s + 3.74 * 10^{10}}{s^3 + 1000s^2 + 5.909 * 10^7 s + 1.091 * 10^{10}}$$

The following figure is the result of simulation with MATLAB script using the transfer function of the closed loop determined above. The characteristics of the system through Step response and stepinfo were consistent with SISO TOOL.



(a) Step Response with PI Controller

RiseTime: 0.0076
SettlingTime: 0.0159
SettlingMin: 2.7866
SettlingMax: 3.4219
Overshoot: 0
Undershoot: 0
Peak: 3.4219
PeakTime: 0.0323

(b) Step Information

Figure 20. Step Response with PI Controller

Therefore, the specifications of the system were rearranged into a table.

Parameter	Values
Gain Margin	inf [dB]
Phase Margin	27.3 [deg]
Rise Time	0.0076 [ms]
% Rise	80%
Settling Time	0.0159 [ms]
% Settling	<5 %
% Overshoot	0 %

Table 3. Closed Loop System specificatio

VI. IMPLEMENTATION OF AN ANALOG SYSTEM

A. Implementation of an Analog Controller in PSIM

To implement the designed system, we wanted to implement analog circuits through amplifiers, integrate, adder and subtractors using Op-amp. The figure below is a block diagram showing how the PI Controller is implemented in a circuit.

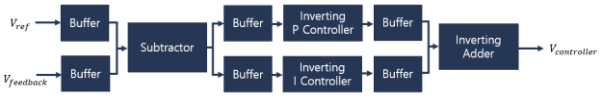


Figure 21. Analog PI Controller Block Diagram

In addition, the feedback was adjusted using the voltage divider to distribute the feedback gain by 5/12, as specified in 3.A.

Parameter		Values
Feedback Voltage Divider	R_{f1}	$8.50[k\Omega]$
	R_{f2}	$3.50[k\Omega]$
Subtractor	R_{s1}	$10.00[k\Omega]$
	R_{s2}	$10.00[k\Omega]$
	R_{s3}	$10.00[k\Omega]$
	R_{s4}	$10.00[k\Omega]$
P Controller	R_{p1}	$100.00[\Omega]$
	R_{pf}	$30.00[\Omega]$
I Controller	R_{i1}	$41.67[\Omega]$
	R_{if}	$200.00[k\Omega]$
	C_{if}	$100.00[\mu F]$
Adder	R_{a1}	$10.00[k\Omega]$
	R_{a2}	$10.00[k\Omega]$
	R_{a3}	$10.00[k\Omega]$

Table 4. Parameter Values in PSIM

In this way, it was implemented as an analog circuit using PSIM. Through PSIM simulation, we are trying to check the validity of the system we designed in the analog circuit.

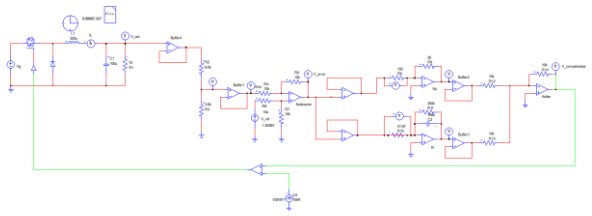
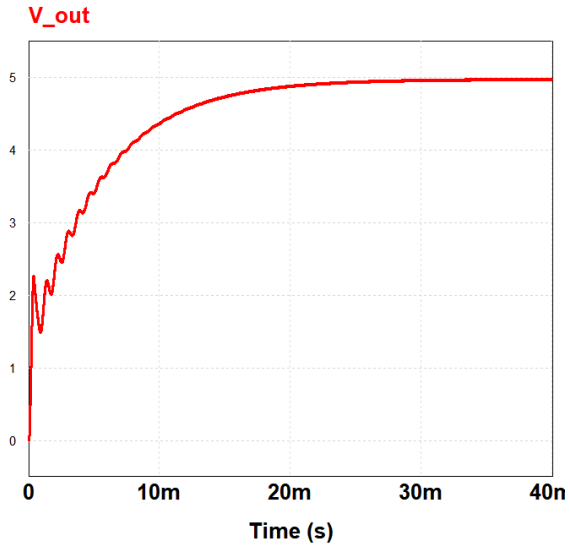


Figure 22. Buck Convertor Circuit in PSIM

- Simulated Step Response by V_{ref}



(a) V_{out} in PSIM

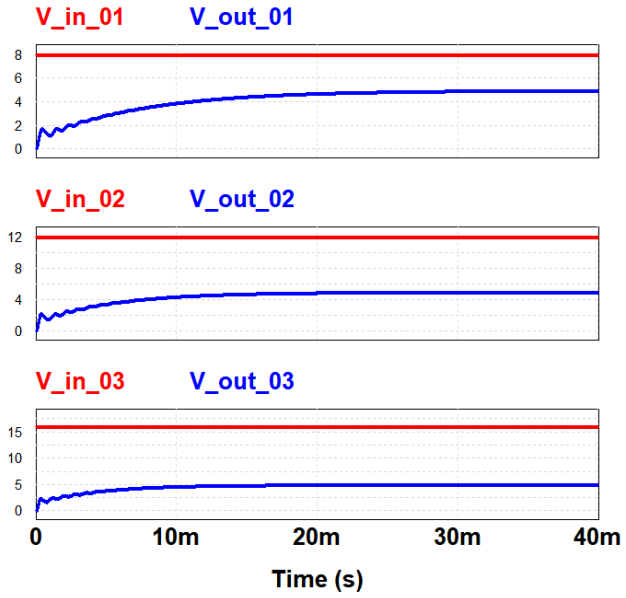
	x1	x2
Time	7.51520e-003	1.51516e-002
V_out	4.00854e+000	4.75111e+000

(b) Values of rising and settling time

Figure 23. Simulation of Theorical Values in PSIM

As a result of PSIM simulation, we determined that this model was valid due to the matching time, setting time, and overshoot.

- Simulated Step Response by V_g



(a) V_{in} and V_{out} in PSIM

	x1	x2
Time	1.50503e-002	3.00336e-002
V_in_01	8.00000e+000	8.00000e+000
V_out_01	4.42473e+000	4.90744e+000
V_in_02	1.20000e+001	1.20000e+001
V_out_02	4.74586e+000	4.96841e+000
V_in_03	1.60000e+001	1.60000e+001
V_out_03	4.87013e+000	4.97973e+000

(b) Values when time is 15[ms] and 30[ms]

Figure 24. Result of Disturbance Control

Each listening time and setting time is the result of the data cursor $15[ms]$ and $30[ms]$ of the specification given to us because it is difficult to capture the data cursor at once. At the rising time of 15[ms] first, it is greater than $4[V]$, which is 80% of the output, so it satisfies the given specifications. At setting time of $30\,[ms]$, this also satisfies the given specifications, with a difference of more than $4.75\,[V]$ with an error of 5% and within $5.25\,[V]$.

B. Actual Implementation of an Analog Controller

It is an analog circuit that is actually implemented.

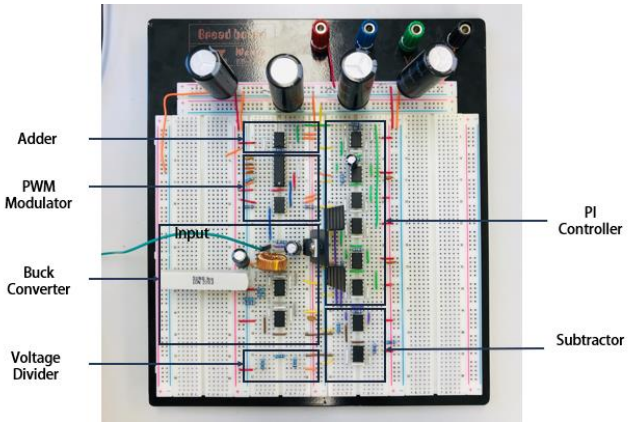


Figure 25. Analog Circuit Diagram

The elements were connected in series or in parallel to make the values used in the simulation as much as possible. The following table shows the values of the parameters used in the actual circuit.

Parameter		Values
Feedback Voltage Divider	R_{f1}	$8.55[k\Omega]$
	R_{f2}	$3.56[k\Omega]$
Subtractor	R_{s1}	$10.04[k\Omega]$
	R_{s2}	$9.98[k\Omega]$
	R_{s3}	$9.98[k\Omega]$
	R_{s4}	$9.98[k\Omega]$
P Controller	R_{p1}	$9.99[\Omega]$
	R_{pf}	$30.20[\Omega]$
I Controller	R_{i1}	$39.3[\Omega]$
	R_{if}	$199.3[k\Omega]$
	C_{if}	$104.60[\mu F]$
Adder	R_{a1}	$9.97[k\Omega]$
	R_{a2}	$9.97[k\Omega]$
	R_{a3}	$9.94[k\Omega]$

Table 5. Parameter Values in Actual Circuit

VII. RESULT

A. V_{out} Step Response as V_{ref}

A pulse waveform of $1.45[V]$ in magnitude and $1[Hz]$ in frequency was added to V_{ref} to confirm the step response of V_{out} according to V_{ref}. In the same experimental state, we tried to see the most common step response by averaging 10 steps. These 10 data are attached to the appendix.

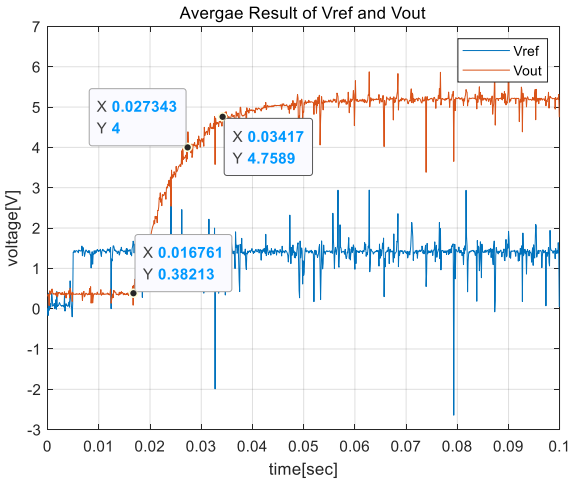


Figure 26. Analysis System Specification

Since the running time is up to 80% point, the data at $0[V]$ and $4[V]$ showed $0.01676[sec]$ and $0.02734[sec]$, respectively. Therefore, the rising time is calculated as follows. In addition, the setting point of $0.47[V]$ is $0.03417[sec]$, so it is possible to calculate the setting time and confirm that no overshooting occurs.

$$(rising\ time) = 0.02734 - 0.01676 = 0.01058\ [sec]$$

$$(settling\ time) = 0.03417 - 0.01676 = 0.01741\ [sec]$$

Therefore, the results of organizing these results into tables are as follows:

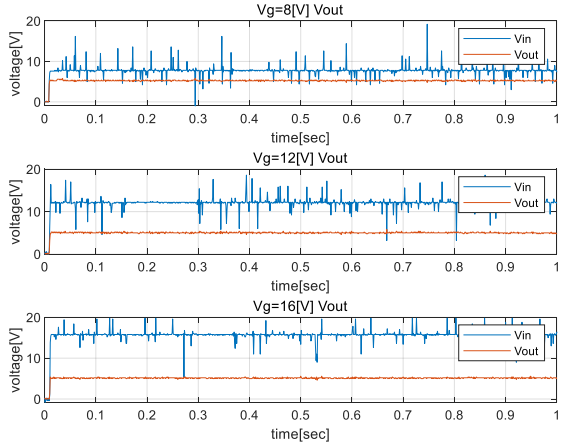
Specification	Simulated	Experimental
Rising Time	7.6[ms]	10.58[ms]
Settling Time	15.9[ms]	17.41[ms]
Overshoot	0%	0%

Table 6. Parameter Values in Actual Circuit

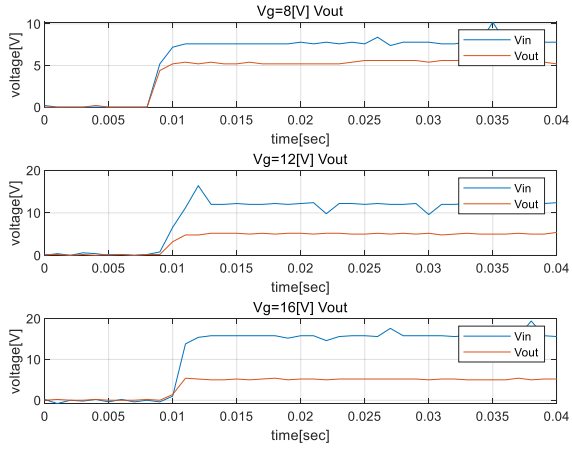
Errors occur in the elements of the hardware, resulting in errors, but results are similar to simulations.

B. V_{out} Step Response as V_g

The following figure illustrates the output when the voltages of V_g are $8[V]$, $12[V]$, $16[V]$, respectively.



(a) Step Response by V_g



(b) Transient Area

Figure 27. Analysis System Specification

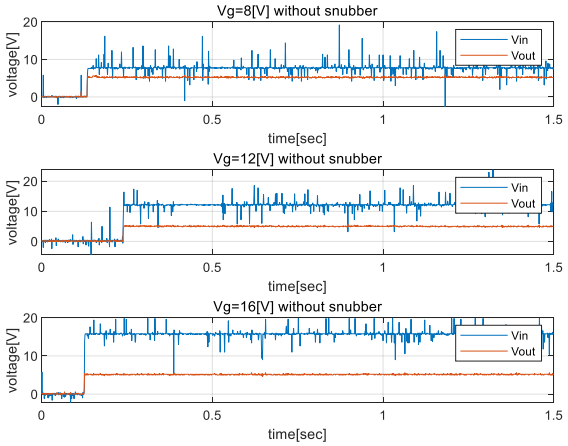
The output of $5[V]$ shall be maintained by the PI controller even if the Disturbance is entered at V_g. Figure 27. shows that the output remains at $5[V]$, although the outputs are $8[V]$, $12[V]$, and $16[V]$, respectively. In addition, we can see that both the listening time and setting time are satisfied as a result of magnifying the Transient. Therefore, the output remains constant even if the input voltage changes due to the disturbance in the input, preventing damage to the circuit.

VIII. OBSERVATION

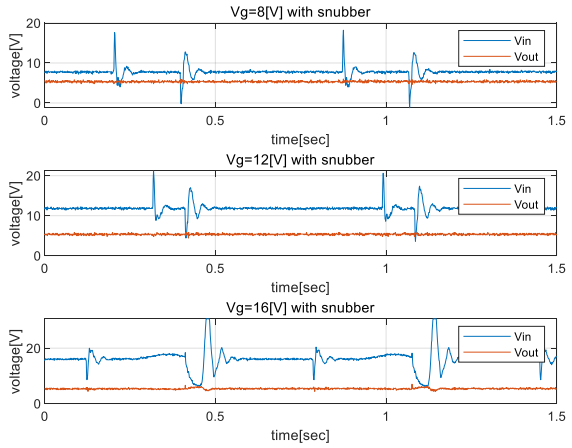
A. Snubber Capacitor

The Snubber Capacitor is a circuit used to suppress the transient voltage that occurs when the inductance load is switched on/off to the switching device.

The first case of using the snubber capacitor is when the voltage is suddenly applied or released at a very large rate during switching. If voltage is applied, the switch can be switched on without the need to apply a signal to the gate. If the voltage exits, high power may momentarily escape from the circuit, causing the circuit to lose power temporarily. Second, connect capacitor in parallel to switch to eliminate noise. However, the snubber capacitor charges when the switch is off. And when the switch is on, a large discharge current flows momentarily. This discharge current can cause great noise and affect the circuit. Thus, resistance limits the capacitor's charge current.
Figure 28. shows that the output voltage when the snubber capacitor was attached clearly reduces noise. This will confirm the noise removal effect of the snubber capacitor.



(a) Without Snubber



(b) With Snubber

Figure 28. Compare w/ and w/o Snubber Capacitor

Figure 29. shows the output voltage according to the presence or absence of snubber capacitor when reference voltage on/off.

In theory, the output voltage when connecting the snubber capacitor should be $0[V]$ when there is no reference voltage. However, the output voltage is $5[V]$ continues to be output. We think the reason for this result is that we did not connect the resistor with the snubber capacitor.

At switch off, the snubber capacitor is charged. Then it is discharged at switch on, when the voltage at both ends of the switch is increased by the snubber capacitor and a large discharge current is generated at the moment. Although no channel has been formed inside the MOSFET, the current flows from drain to source beyond n type. This is called pinch off. You can limit the current by attaching a resistance with a snubber capacitor.

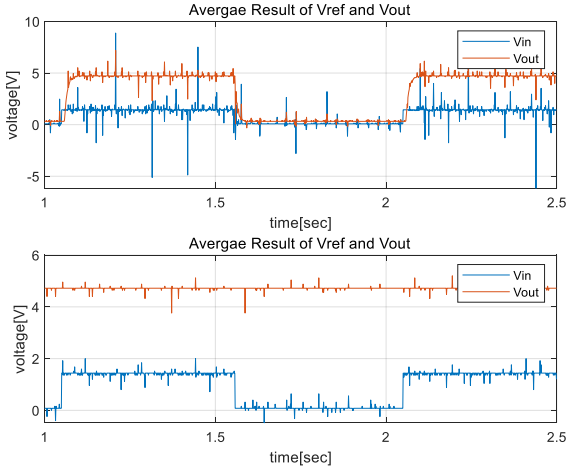


Figure 29. Compare w/ and w/o Snubber Capacitor

B. Bootstrap

Buck Converter determines the output according to the duty, but when the duty becomes larger than a certain value, it tends to fall rather than grow anymore. Therefore, you can attach bootstrap to guarantee the output.

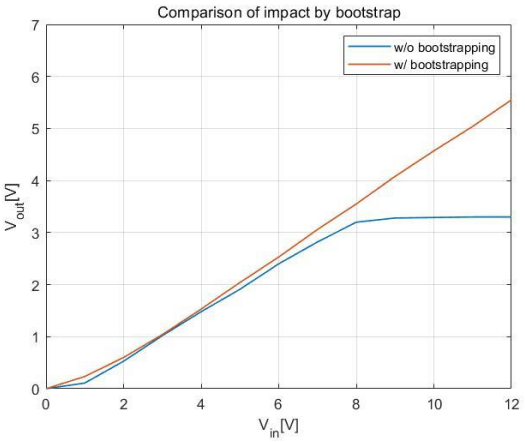


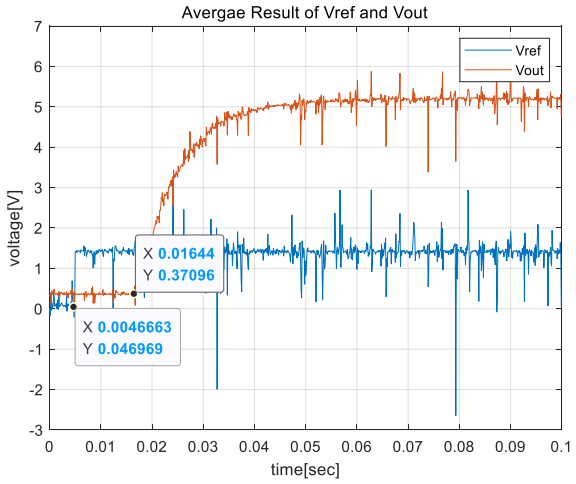
Figure 30. Comparison of Impact by Bootstrap

Bootstrap is used to flow voltage to produce the desired output compared to ground when the source end of the MOSFET is connected to ground. However, we didn't consider this flooding when modeling the system this time, and we don't know exactly how it will flow in the circuit because the source of the MOSFET is not ground. Therefore, when designing the voltage controller this time, it was not used because the degree of flooding of bootstrap cannot be considered.

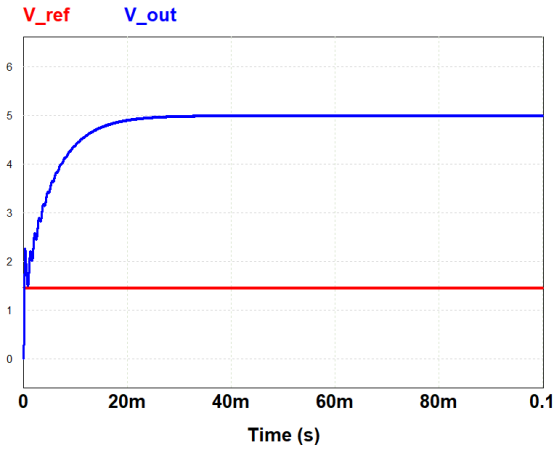
C. Time Delay

As a result of the experiment, the response of output voltage according to reference voltage was slow. Time delay issue seems to be caused by an analog circuit. In the actual circuit, the reference voltage must pass the subtractor, buffer, PI Controller, adder, PWM modulation, MOSFET driver chip and MOSFET to output the output voltage. Therefore, time delay cannot be completely removed. Also, because of the analogue uncertainty, the buffer was attached in the middle of the connection of the part. In addition, P Controller, I Controller were designed by disassembling and adder was designed to combine controlled signals. When to consider many elements, the optimal design will further reduce time delay.

The following is a time delay comparison graph of actual circuits and simulations.



(a) Experiment



(b) Simulation by PSIM

Figure 31. Time Delay in System Input and Output

D. Reason for Not Using D Controller

The controller being designed this time is a controller used to control voltage and current. The D controller is sensitive to momentary changes because it is differential. However, the rate at which the current changes is very fast, so using the D controller to control the current can instantly amplify to a very large value and damage the circuit. Therefore, the experiment was conducted without using the D controller.

IX. CONCLUSION

Through this Voltage Controller Design Project, the goal was to design and model the buck converter by understanding the operating characteristics of the converter and design and implement the PI controller that satisfies the given specification. The error of each element should be considered in implementing the two systems as analog circuits, and it is important to design them in consideration of the physical flow of the system, unlike digital control.

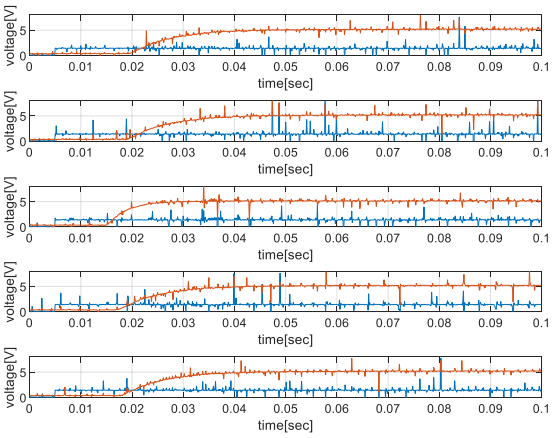
As a result, the rising time was slower than the driving time of the buck converter before designing the controller, but the resulting overshoot was removed. It satisfies the given specification, so the control is considered that the desired control has been achieved. It was also confirmed that the feedback gain produces a constant output of $5[V]$ even if an unexpected voltage enters V_g, the input of the buck converter.

X. WORK DISTRIBUTION

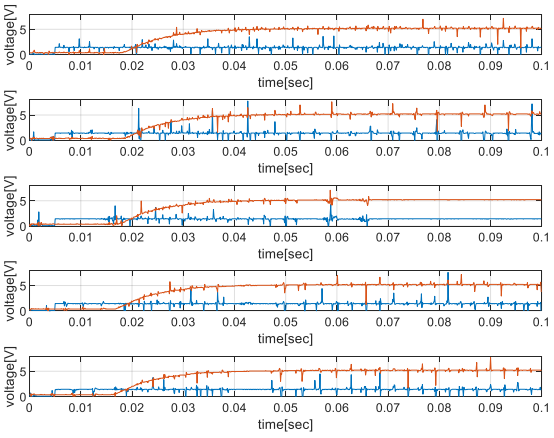
	Yoonkyoung Song	Byounghwan Jang
Circuit construction	50%	50%
Circuit Testing	50%	50%
Report	50%	50%

XI. APPENDIX

A. Step Response by V_{ref}



(a) Row Data 1~5



(b) Row Data 6~10

Figure 32. Row Data of Buck Converter by V_{ref}