IC Design
Homework # 2

Due on 11/02/2018, 13:20 in class

Plagiarism is not allowed. 10% penalty for each day of delay.

In this homework, you will learn the following:

- Hspice
- nWave

1. (70%)

Two of the following cells are assigned to each of you. Everyone must do cells （**10**）. Those whose student ID end with '*k*' must also do **cell *k***. (Ex. If your ID is Bxx901123, you need to do (3) EO3, (10) FA1)

(0) EN
(1) NR2
(2) OR2
(3) EO3
(4) AN3
(5) ND2
(6) AN2
(7) EO
(8) DRIVER
(9) IV
(10) FA1

For each cell,

a. Base on the layout view, draw **transistor-level** and **gate-level circuit** diagrams (using powerpoint, paint or 手畫)

b. Identify all **inputs** and **outputs**

c. List **truth table**

d. Revise the given netlist file to construct your cells. All PMOS transistors have width 0.5um and length 0.1um. All NMOS transistors have width 0.25um and length 0.1um. Parameters of 90nm model file (90nm_bulk.l) must be included during the simulation. The substrate of PMOS is connected to VDD and the substrate of NMOS is connected to VSS.

e. Run *Hspice* simulation on **all possible input** combinations. Assume

VDD=1.0V and VSS=0V. Use *nWave* to verify the truth table. Copy the **I/O waveform** to your report. State what you have observed.

f. Please discuss problems you have encountered.

Files that you will need (available on the class website)

HW2_2018.zip includes the following files

- HW2_2018.pdf (this document)
- HW2_tutorial_2018.pdf
- example.sp (CMOS inverter的範例程式)
- 90nm_bulk.l
- Pictures of layout (in "pic" folder)

Files that you need to submit

- Hard copy of your report (in class)

・List the names of the cells you did in homework in front of the report.

・Need to attach HSpice code and waveform results

References

[1] "SPICE," CIC handout, 2001

[2] "鳥哥的 Linux 私房菜," http://linux.vbird.org/

If there's any workstation account/password problem, please directly contact workstation administrator，邱茂菱，d01943010@ntu.edu.tw

2. **(20%)** In Chapter 3, we analyzed the rising and falling delays of a NAND3 gate with fanout *h* (slide 10 of Chapter 3) . Following similar approach, derive the falling and rising delays of a NOR3 gate.

3. **(10%)** You are considering lowering VDD to try to save switching power of a CMOS processor chip. You also want to change Vt proportionally to maintain clock speed. Will dynamic power consumption go up or down? Why? Will static power consumption go up or down? Why?

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HW2 Office hours: 10/30 19:00-21:00 @ 博理 **211**

11/01 19:00-21:00 @ 博理 **214**

If you have no time at office hours, you can email TA to discuss another time for appointment.