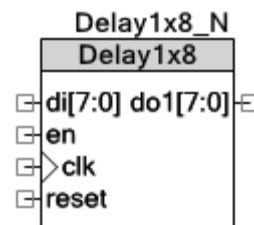


8-bit Delay by One Clock

1.0

Features

- 8-bit Flip-Flop
- Uses datapath resources
- Synchronous enable and reset



General Description

An 8-bit register using datapath resources without consuming macrocell resources.

When to use an 8-bit Delay by One Clock

The component is useful when wide registers are required and macrocell resources are not available.

Input/Output Connections

This section describes the various input and output connections for Delay1x8. An asterisk (*) in the list of I/Os indicates that the I/O may be hidden on the symbol under the conditions listed in the description of that I/O.

clk – Input

All data is captured on the rising edge of the **clk** input.

en – Input

The **en** signal enables the capture of the data input. This is a level sensitive enable signal. Data is captured on each clock when **en** is high.

reset – Input

The **reset** signal is a synchronous reset of the component. The reset function has priority over the enable signal (reset occurs even if **en** is low).

di[7:0] – Input

8-bits of data to capture.

do1[7:0] – Output

8-bit registered data output.

Application Programming Interface

This component does not use an Application Programming Interface (API). Operation of this component is controlled by hardware signals only.

When returning to an active mode from a low power state, the component starts from the reset state with the registered output set to 0.

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