CYPRESS SEMICONDUCTOR CORPORATION
Internal Correspondence

Date: Monday 12/17/2012 **WW: 1251**
To: **ROSS**
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Author File#: KEES#175
Subject: **HART RX filter**
Distribution: ROSS, DRSW, GDK, GRSM, PHR

Summary:

This memo summarizes the receive (RX) filter implementation required to meet the HART specifications. The filter requires 1 opamp in medium power mode and 11 passive components. The filter implements a 3 pole high pass filter with a cutoff of 600 Hz and a single pole low pass filter with a cutoff of 5 Khz. The filter was constructed on an -030 / -050 plug in module and tested to ensure it performed as needed.

Attached File Summary:

File # is the LTspice simulation file. Remove the .PDF extension to use the file.

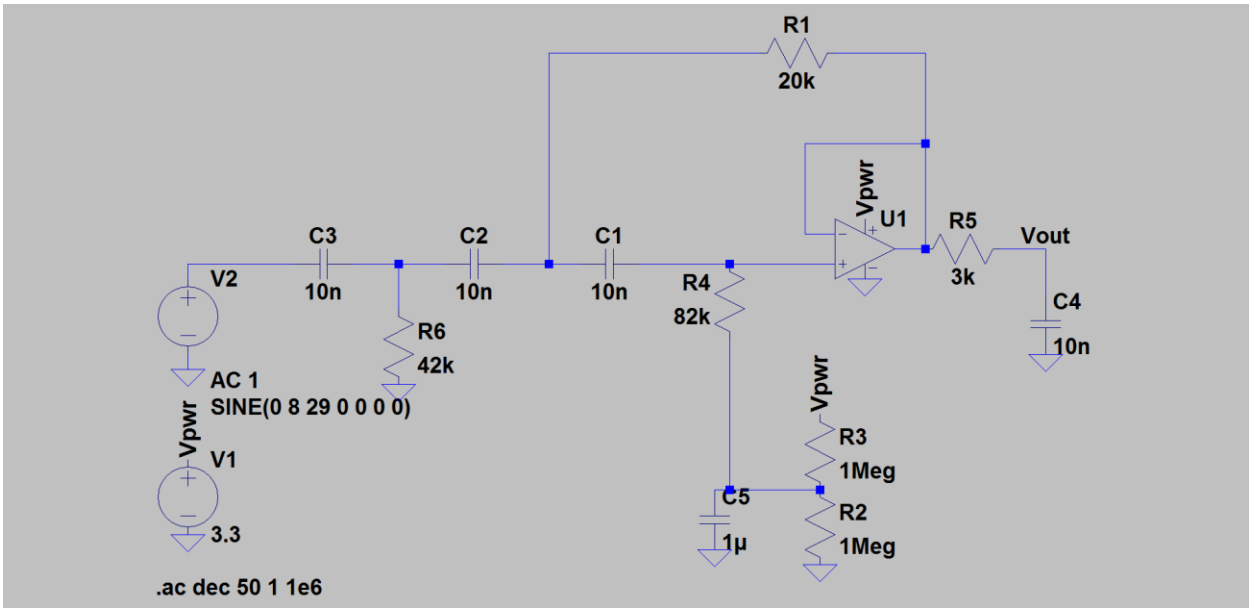
Details:

The RX filter was based on the filter implementation described in BIOL # 58 (HART Receive channel test results). My changes to the filter implementation include:

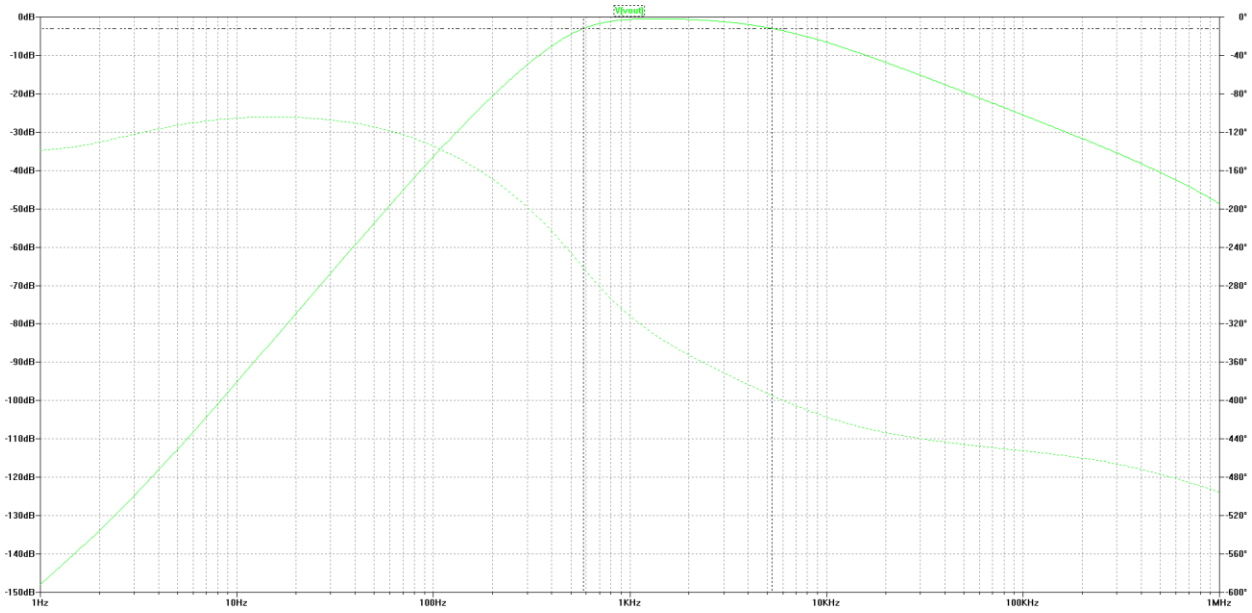
- Altering the values of the R and C by an order of magnitude to reduce sensitivity to contaminants like flux and oil. R was reduced, and C was increased
- Swapping the passive high pass and low pass filters on the output and input of the active filter. The large signal swings that must be accommodated at very low frequencies (16 volt peak to peak at 29 Hz) seemed to indicate that a high pass filter as the first stage would reduce the amount of signal swing seen by the 2nd order highpass filter.
- Moving the low pass filter to the end eliminated the need to DC bias the output around Vdda/2, since this was already accomplished by the biasing of the Sallen-Key high pass filter.

- Since power consumption is a major concern, the Vdda/2 bias network was made with resistors as large as possible to reduce energy wasted in generating the DC bias voltage.
- The first order input high pass filter was connected to ground (rather than Vdda/2) to prevent energy being coupled into the DC bias point, reducing the effectiveness of the next filter stages.

The following circuit was simulated in LT spice:

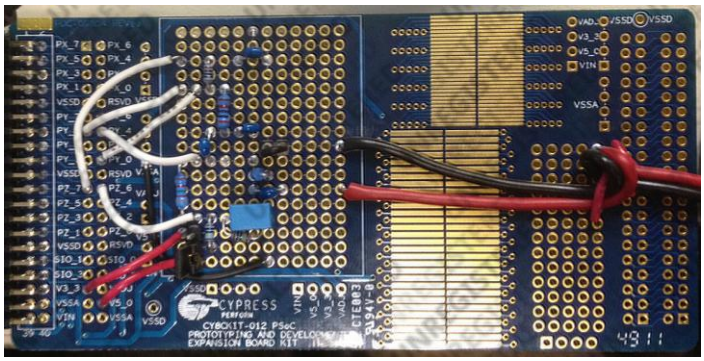


The opamps parameters were adjusted to match the performance limits of an opamp in medium power mode with a 3.3 volt rail. The gain bandwidth product was set to 1 Mhz, the slew rate was set to 0.9 v / us, the phase margin was set to 60 degrees and the open loop gain was set to 100,000. The frequency performance of the simulation is shown below:



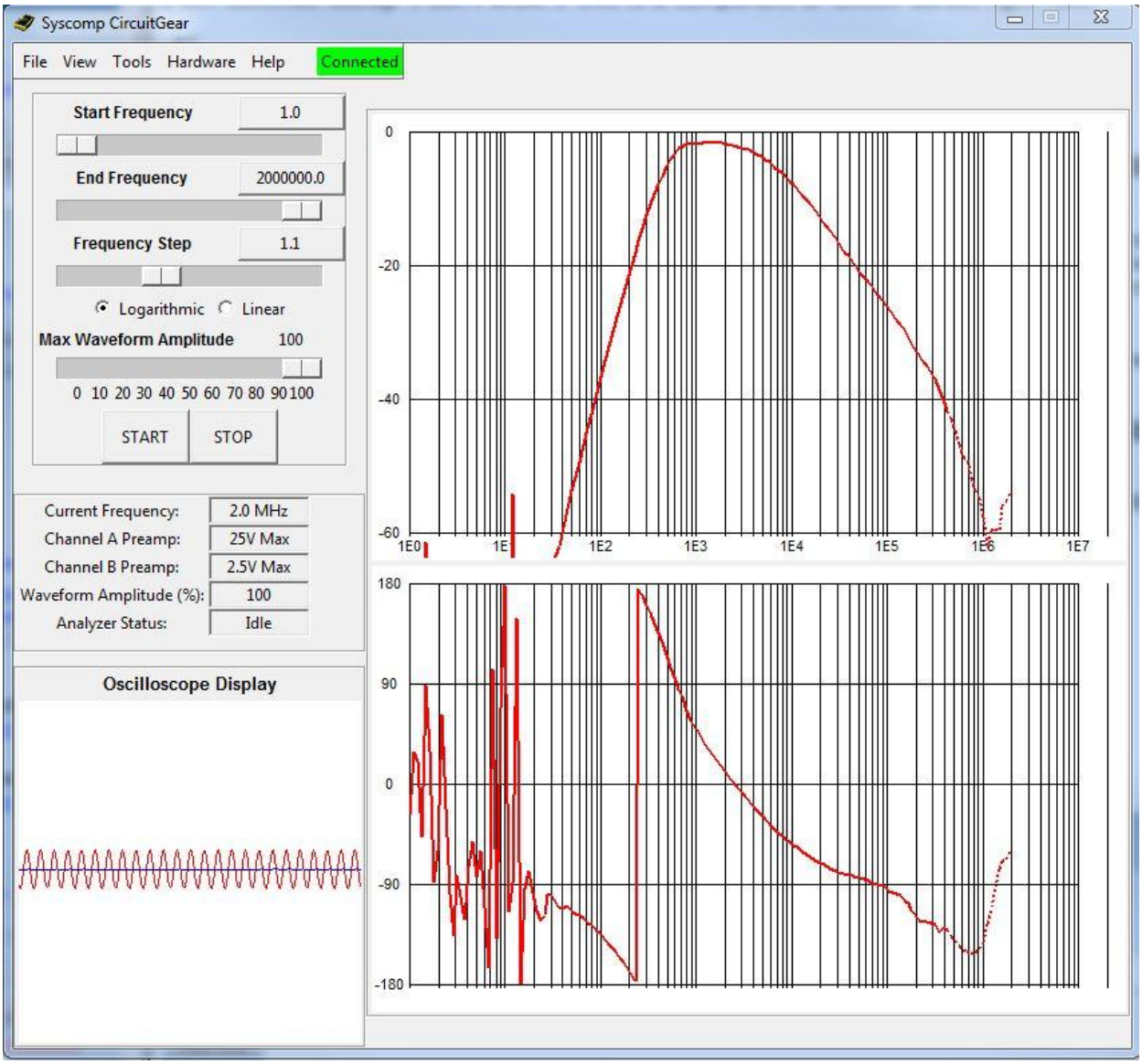
The – 3 dB points are 600 Hz and 5 Khz. The high pass filter has a slope of 60 dB per decade, and the low pass filter has a slop of 20 dB per decade. The pass band gain is from – 3 dB to 0 dB.

The filter was implemented on an expansion board. The board is intended to be used with an -030 / -050 kit.



The Frequency response of the RX filter was then tested with a SysComp CircuitGear to validate that its performance was close to the simulation. The following picture is a screenshot of the tool output.

Signal levels below 60 dB are beyond the capabilities of this device so ignore the spurious behavior at very low frequencies. The response was reasonably close to the desired behavior of the circuit.



Pin connections are as follows:

Opamp Negative Input : P0[5]
Opamp Positive Input: P0[4]
Opamp Output: P0[0]
SAR ADC Positive input: P4[7]
SAR ADC Negative input: P4[6]

The SAR ADC positive connects to the output of the low pass filter (Vout) in the LTspice schematic, and the SAR ADC negative terminal connects the junction of R2, R3 and C5 in the LTspice schematic (Vdda/2 DC bias point).