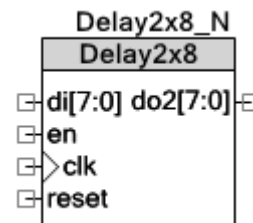


8-bit Delay by Two Clocks

1.0

Features

- Series connection of two 8-bit Flip-Flops (16-bits total storage)
- Uses datapath resources
- Synchronous enable and reset



General Description

A two deep chain of 8-bit registers using datapath resources while consuming just a single macrocell.

When to use an 8-bit Delay by Two Clocks

The component is useful when a delayed version of a register is needed. Multiple instances can be chained to create a register delay by any even number of clocks and a Delay1x8 component can be included in the chain to create a delay by any number of clocks.

A common application for a delay chain is a filtering operation such as an average filter.

Note: The output is created using a combinational mux of the two register values. That can result in glitches on the output at the clock edge.

Input/Output Connections

This section describes the various input and output connections for Delay2x8. An asterisk (*) in the list of I/Os indicates that the I/O may be hidden on the symbol under the conditions listed in the description of that I/O.

clk – Input

All data is captured on the rising edge of the **clk** input.

en – Input

The **en** signal enables the capture of the data input. This is a level sensitive enable signal. Data is captured on each clock when **en** is high.

reset – Input

The **reset** signal is a synchronous reset of the component. The reset function has priority over the enable signal (reset occurs even if **en** is low). Reset will clear the values stored in both storage registers.

di[7:0] – Input

8-bits of data to capture.

do2[7:0] – Output

8-bit delayed data output.

Application Programming Interface

This component does not use an Application Programming Interface (API). Operation of this component is controlled by hardware signals only.

When returning to an active mode from a low power state, the component starts from the reset state with both storage registers reset to 0.

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