CYPRESS SEMICONDUCTOR CORPORATION
Internal Correspondence

Date:	Thursday 1/31/2013	**WW: 1302**
To:	**PSoC Apps**	
Author:	Chris Keeser (KEES)	
Author File#:	KEES#181	
Subject:	**SC/CT DeltaSigma Modulator Component**	
Distribution:	PSoC_Apps	

Summary:

This memo is meant to distribute the first order DeltaSigma modulator component constructed from the SC/CT blocks. This component exposes the useful DeltaSigma modulator functionality of the SC/CT blocks in an easy to use way. Provide a clock (5 Khz to 4 Mhz), a reference (the 1.024 volt SC/CT block reference is the only suitable reference that does not require buffering) and an analog input in order to use the modulator. The component also exposes the integrator reset for incremental mode, as well as the analog output of the integrator for educational or creative purposes. There is currently no datasheet for the component, but all that is required is to call the _Start() API in order to use the modulator.

The modulator has 2 input ranges. Vref +/- 2*Vref and Vref +/- 0.5*Vref. When using the 1.024 reference, the modulator input ranges are 0 – 3.072 volts and 0.512 – 1.536 volts.

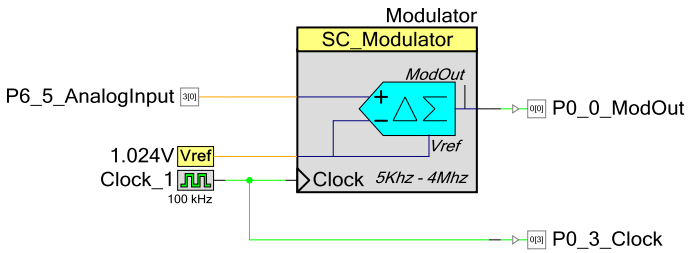
Rev *A: The component now correctly handles different clock sources and low voltage boost pump operation. Please use this version.

Attached File Summary:

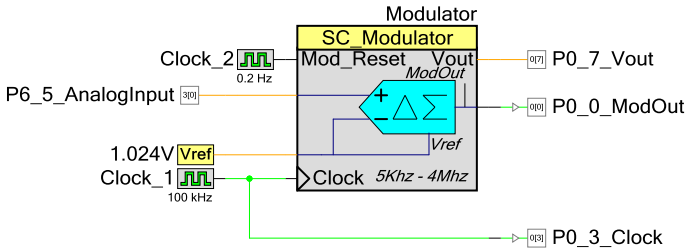
File # 2 is the archive of the component (using Creator 2.2 component export feature). To use the file, download it and replace the .PDF extension with .ZIP.

Details:

This is what the component looks like:



And this is what it looks like with all optional features enabled:



To use the modulator, you only need to call INSTANCE_NAME_Start(); In the examples shown above, it would be Modulator_Start();

The clock terminal controls the speed of the modulator output. The recommended clock rate is between 5 Khz and 4 Mhz. The upper limit is set by the BROS specs, and the lower limit by the droop of the integrator. To get the best performance across all conditions, you should probably use a clock of 10 Khz or faster. The output can change on the falling edge of this clock.

The Vref terminal sets the negative input and range of the modulator. The two ranges are:

1.) Vref +/- 2*Vref
2.) Vref +/- 0.5*Vref.

When using the 1.024 reference, the modulator input ranges are 0 – 3.072 volts and 0.512 – 1.536 volts. If you intend to use another reference besides the 1.024 volt, you need to buffer that reference before it is consumed by the modulator. The Vref input is low impedance and will load down any reference connected to it without proper buffering.

The analog input is the input to the modulator. This analog value will be converted into a modulated output depending on the voltage applied to the input compared to the reference. A voltage applied to the input that is equal to the reference voltage will result in a modulated output with a ~50% duty cycle. If the voltage is less than the reference, it will reduce the duty cycle. If the voltage applied is higher than the reference, it will increase the duty cycle.

The (optional) Mod Reset signal is used to reset the integrator inside the modulator. This is useful when using the modulator as a part of an incremental converter. The modulator should be reset at the end of every conversion in an incremental converter in preparation for the next conversion. When the mod reset signal is high, the integrator is shorted, discharging the integrating capacitor. While the reset signal is high, the modulator output is undetermined and should be ignored.

The Mod out signal is the digital modulator output. This output will change on the falling edge of the applied clock (if it is going to change).

The (optional) Vout terminal is the output of the integrator. This can be useful for educational or creative purposes and was added for the adventurous.

A datasheet may be added at some time in the future to capture this information.