Chapter 6
Combinational Circuit Design

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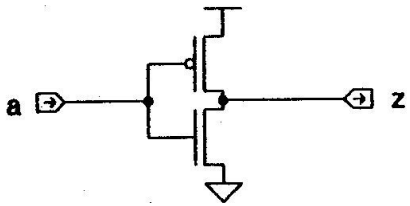
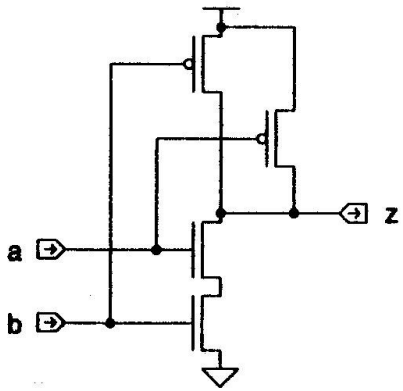
CMOS Logic Structures

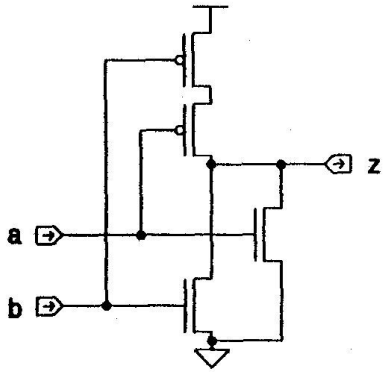
- Static CMOS logic is still the widely used and safest CMOS logic family.
- One drawback of the static logic is that it has both PMOS and NMOS inputs, making the input capacitance large.
- Also PMOS transistors are slow, making them the easiest target to eliminate.
- Another disadvantage is the full swing requirement (V_{DD} <-> GND), which makes switching slower.
- Many logic families introduced in this chapter are not practical and are introduced for “record-of-ideas” reason.

CMOS Static Logic

- Ratioless -- all transistors (NMOS and PMOS) can be of the same size.
- P-N matching -- requires the same number of PMOS and NMOS transistors.
- Static, restored logic -- clock not necessary; consumes power only during gate switching.

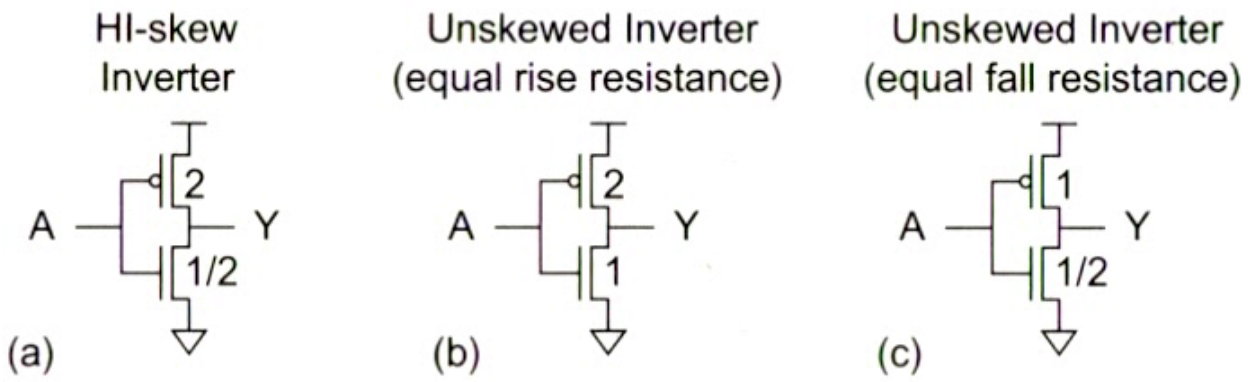






Static Logic (cont'd)

- Different supply voltage lower than 1.8 V down to even a few hundred mV can be used in complementary CMOS logic circuit for the purpose of increasing speed or lowering power consumption.
- Input ordering – inner input should be tied to slowest-arriving signal because it carried least delay.
- Transistor sizes in P/N blocks can be sized so as to favor certain transition and adjust the gate inversion voltage.



P/N Ratio

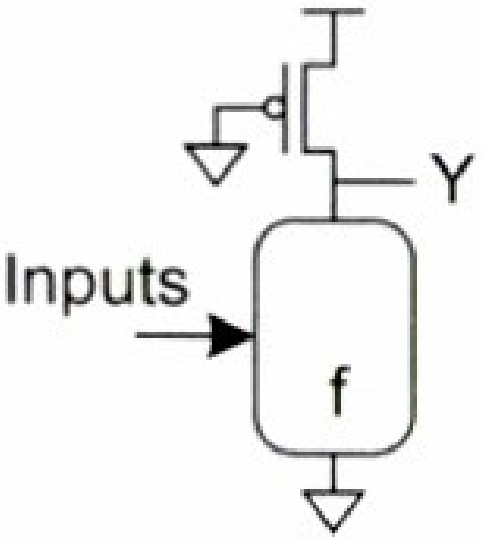
- The best ratio of the P/N is not 2 that makes equal rise/fall time, but rather 1.414, which makes the least average delay.
- This will significantly decrease the area and the power too. But the saving in delay is only 3% from the case of P/N ratio of 2.

Observations

- For speed:
  - NAND vs. NOR
  - Many simple stages vs. fewer high fan-in stages
  - Latest-arriving input
- For area and power:
  - Many simple stages vs. fewer high fan-in stages

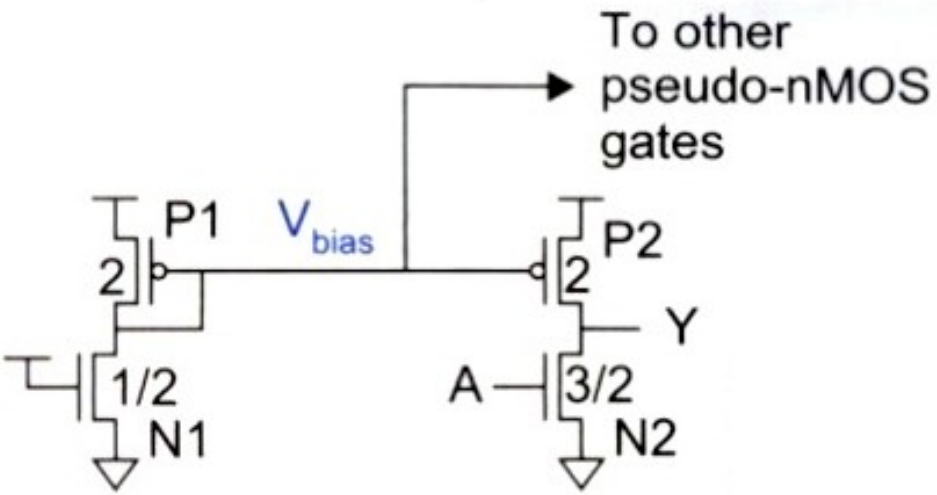
Ratioed Logic -- Pseudo-NMOS

- Replace the upper PMOS block by an always-on PMOS transistor. Same as NMOS Logic except for a PMOS transistor replacing a depletion-mode NMOS transistor.
- The ratio of the sizes of load and driver (β_p/β_n) needs careful tuning to set an acceptable gate threshold voltage, usually set to about 1/4 .
- High power consumption. Current flows whenever the N-block conducts. (approximately half of the time)



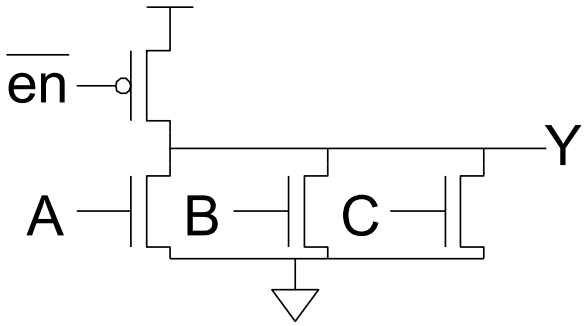
Pseudo-NMOS (cont'd)

- It is slower than static logic in NAND structure, but it is faster in NOR structure. Thus is most popular in NOR-structured ROM and PLA.
- This technique will automatically (regardless of process variation) generate the correct bias voltage for the PMOS with a current that is 1/3 of the current in an ON N-block.



Pseudo-nMOS Power

- Pseudo-nMOS draws power whenever Y = 0
  - Called static power $P = I_{DD}V_{DD}$
  - A few mA / gate * 1M gates would be a problem
  - Explains why nMOS went extinct
- Use pseudo-nMOS sparingly for wide NORs
- Turn off pMOS when not in use



Ratio Example

- A chip contains a 32 word x 48 bit ROM
  - Uses pseudo-nMOS decoder and bitline pullups
  - On average, one wordline and 24 bitlines are high
- Find static power drawn by the ROM
  - $I_{on\text{-}p}$ = 36 μA, V_{DD} = 1.0 V
- Answer:

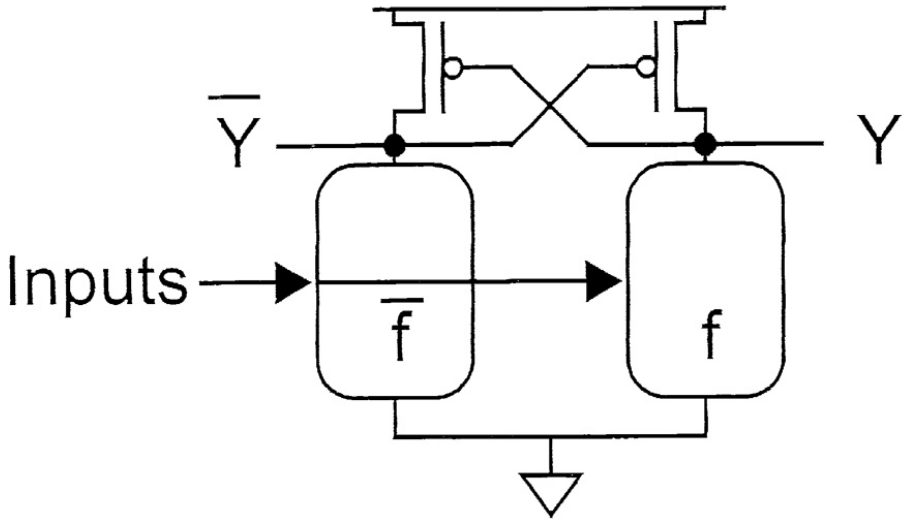
$$P_{\text{pull-up}} = V_{DD} I_{\text{pull-up}} = 36\ \mu\text{W}$$

$$P_{\text{static}} = (31+24) P_{\text{pull-up}} = 1.98\ \text{mW}$$

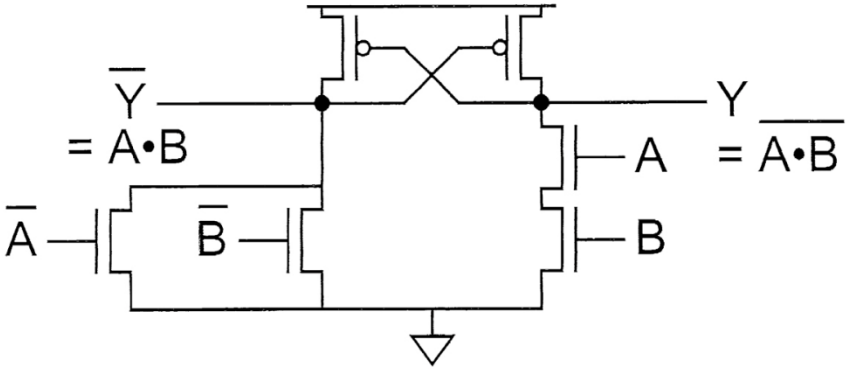
31 word lines low and 24 bit lines low

Cascode Voltage Switch Logic (CVSL)

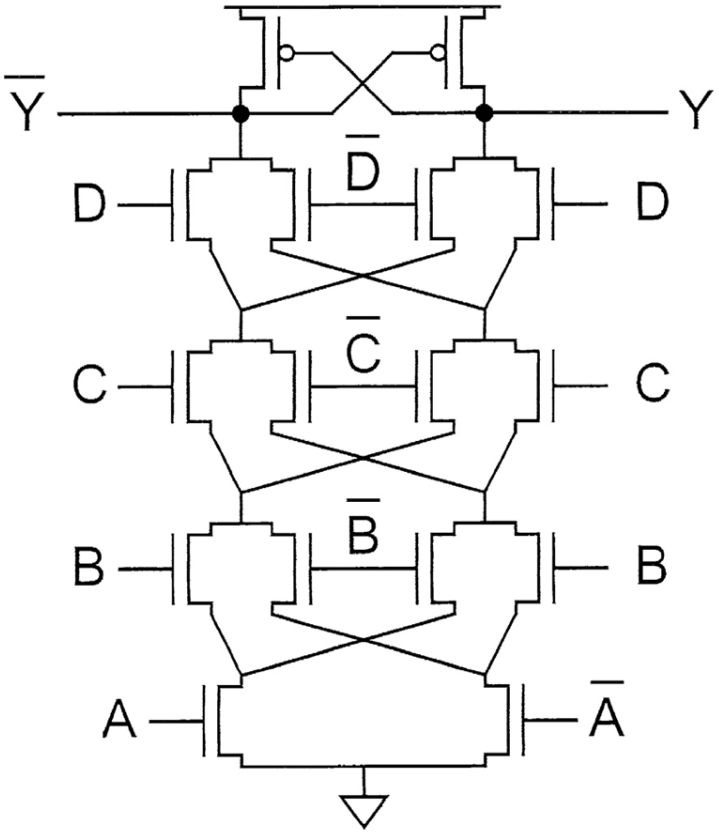
- Two complementary N-blocks and two PMOS load devices are needed. This version is called static CVSL and may be slower than the complementary logic because the load devices have to fight the N-blocks during switching.
- Not good for both NAND and NOR because one of the two must be NMOS in series; complementary inputs are needed.



CVSL Gates



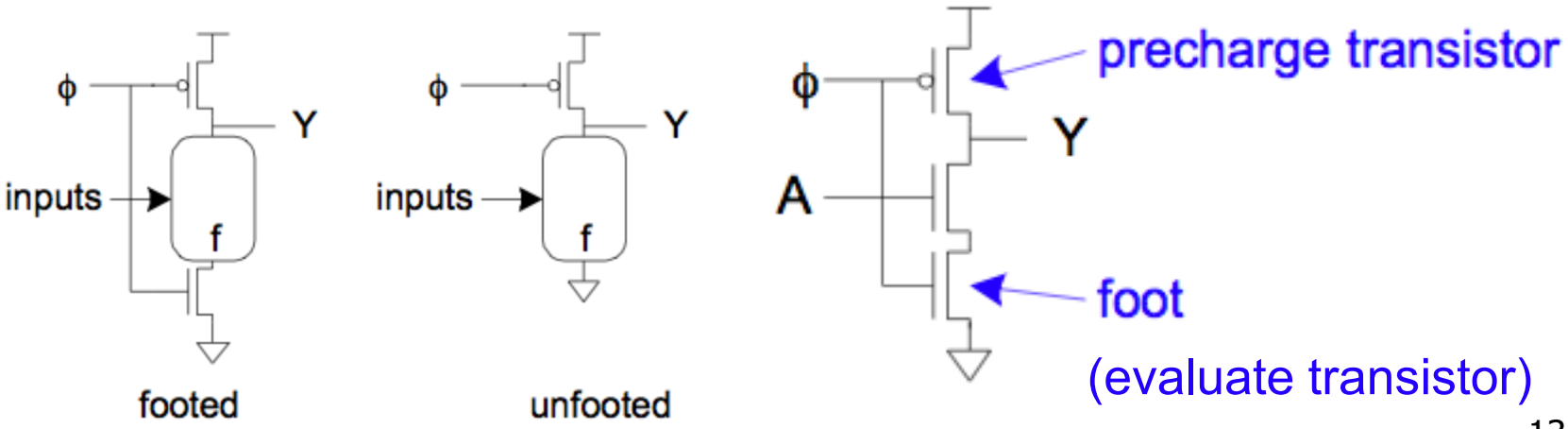
2-input AND/NAND gate



4-input XOR/XNOR gate

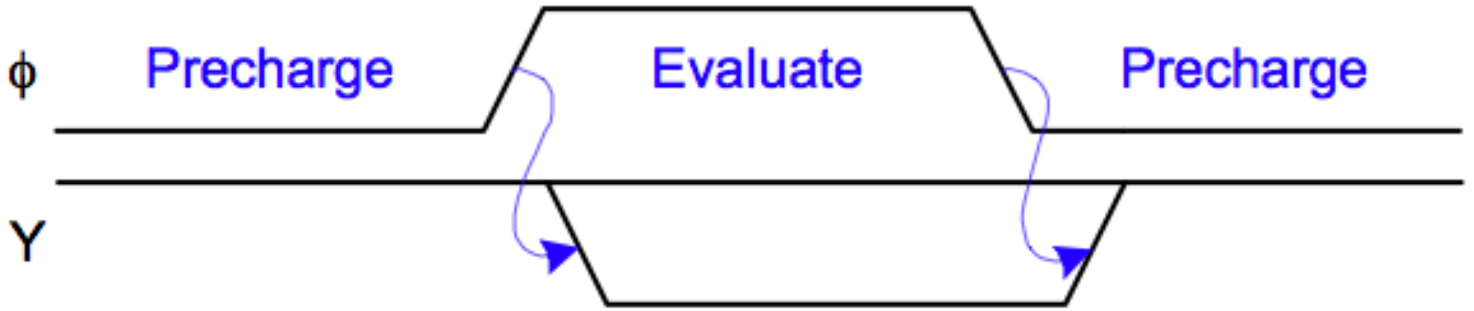
Dynamic CMOS Logic

- NMOS logic block + PMOS precharge transistor + NMOS evaluate transistor.
- Clk (ϕ) is a single phase clock. The pull-up time is improved while the pull-down time is increased due to series *foot* transistor.
- The load needs not be weaker since it is turned off during N-block conduction.



Dynamic Logic Operation

- Two modes of operation: precharge and evaluate: Y is precharged to V_{DD} when clk (ϕ) = 0 and is conditionally discharged when clk (ϕ) = 1 and the N-block conducts.

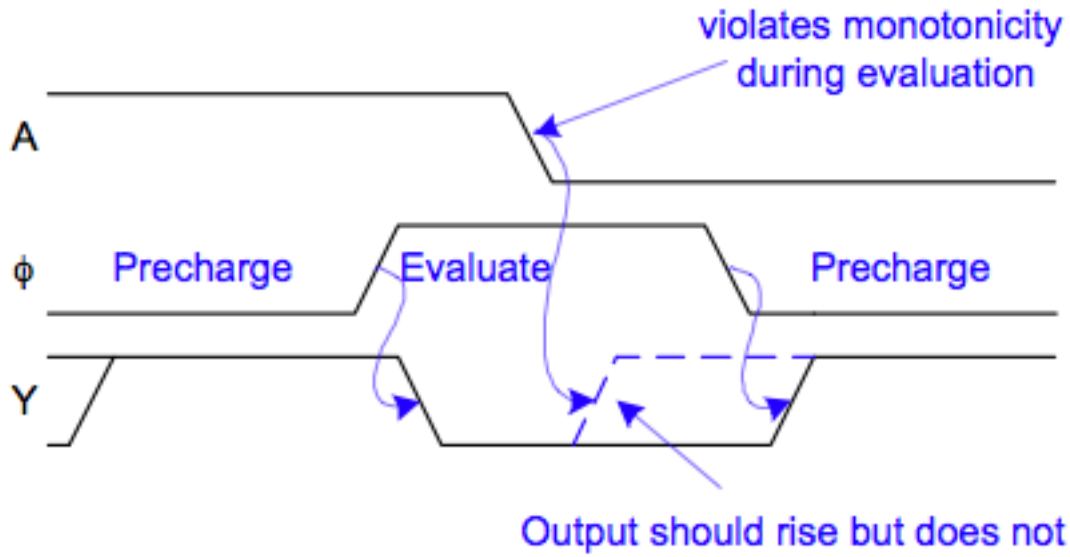


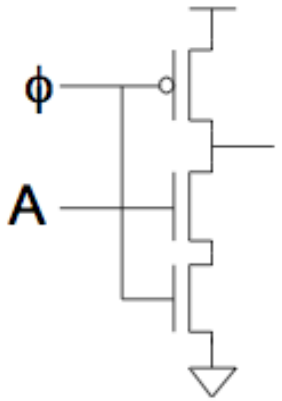
Noise Sensitivity

- Dynamic gates are very sensitive to noise
  - Inputs: $V_{IH} \sim V_{th}$
  - Outputs: floating output susceptible noise
- Noise sources
  - Capacitive crosstalk
  - Charge sharing
  - Power supply noise
  - Feedthrough noise
  - And more!

Monotonicity in Inputs

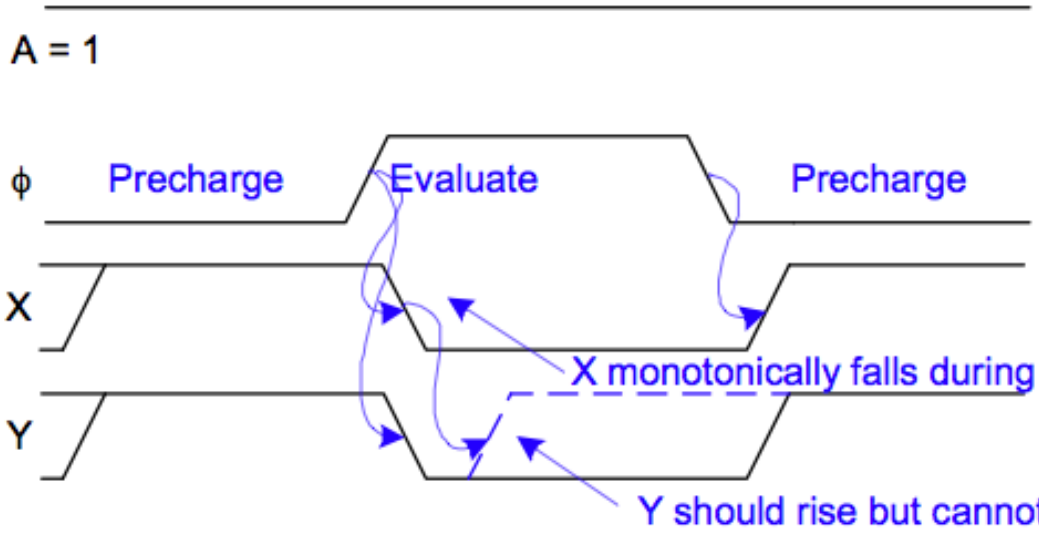
- Dynamic gates require monotonically rising inputs during evaluation
  - 0->0; 0->1; 1->1
  - but not 1->0

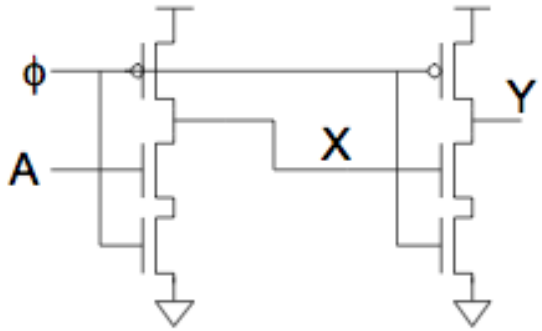




Failures in Dynamic Logic

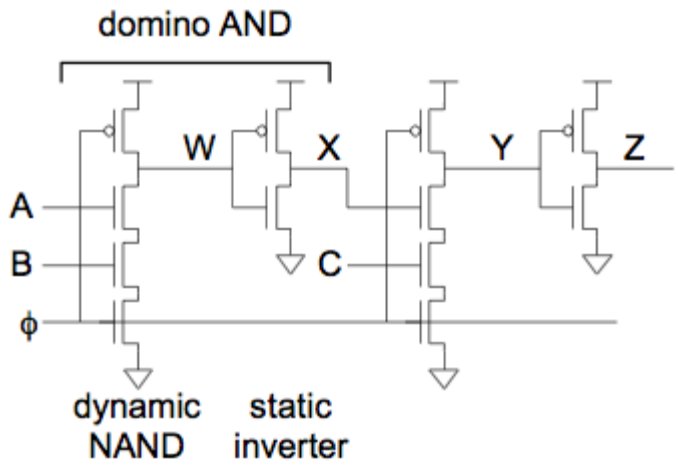
- Dynamic logic gates can not be cascaded because dynamic gates produce monotonically falling outputs during evaluation, which causes possible erroneous discharge in the next stage.
- One solution is Domino Logic.

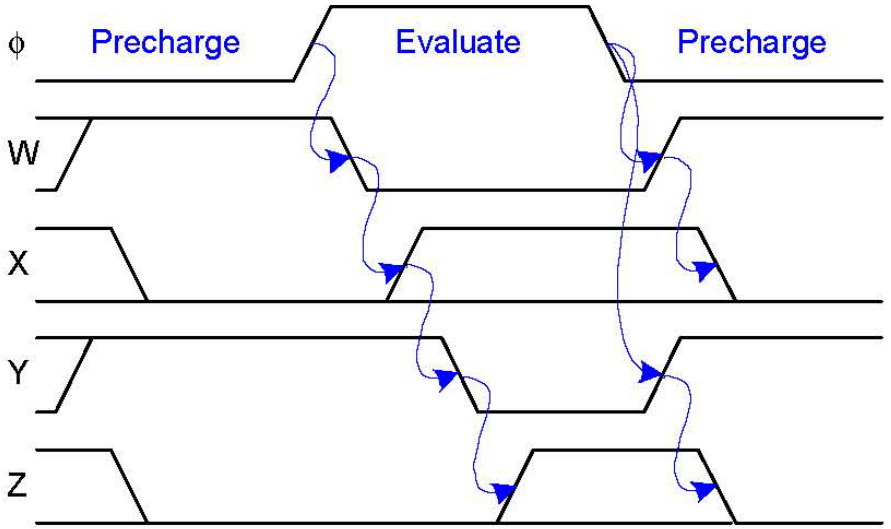




CMOS Domino Logic

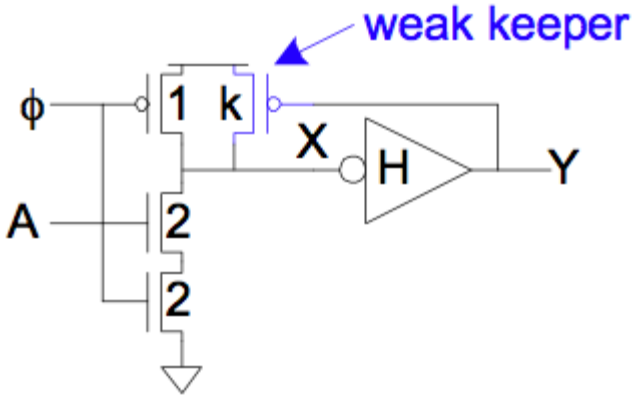
- An inverter is added at the output of a dynamic logic gate.
- When clk (ϕ) = 0, W = 1, X = 0, NMOS transistors in the N-block of succeeding gates are turned off and the succeeding gates precharge successfully.
- When clk (ϕ) = 1, W is conditionally discharged and X may become 1, affecting the output of the succeeding gates.





Domino Logic (cont'd)

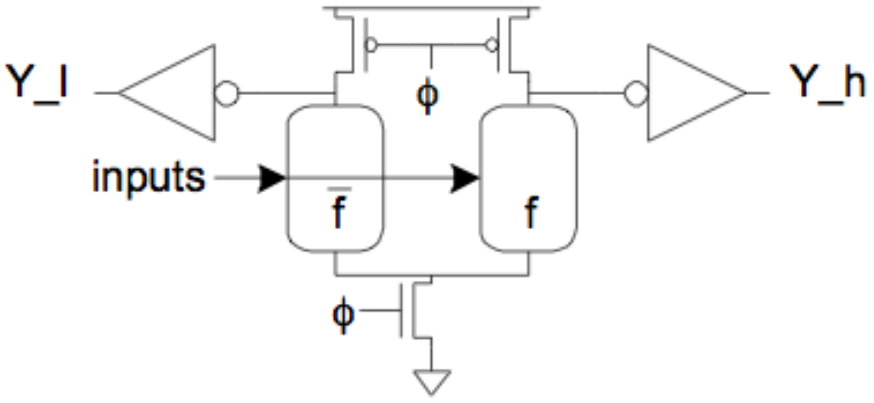
- Only one-way (0->1) change at nodes X and Z is allowed. The gates evaluate as dominoes fall.
- Precharging in parallel and evaluation in series.
- As many gates as possible can be cascaded as long as the clock period is long enough.
- Latching version is implemented by an extra PMOS controlled by the output and in parallel with the precharge transistor to replenish the leaked charge.



Dual-Rail Domino Logic

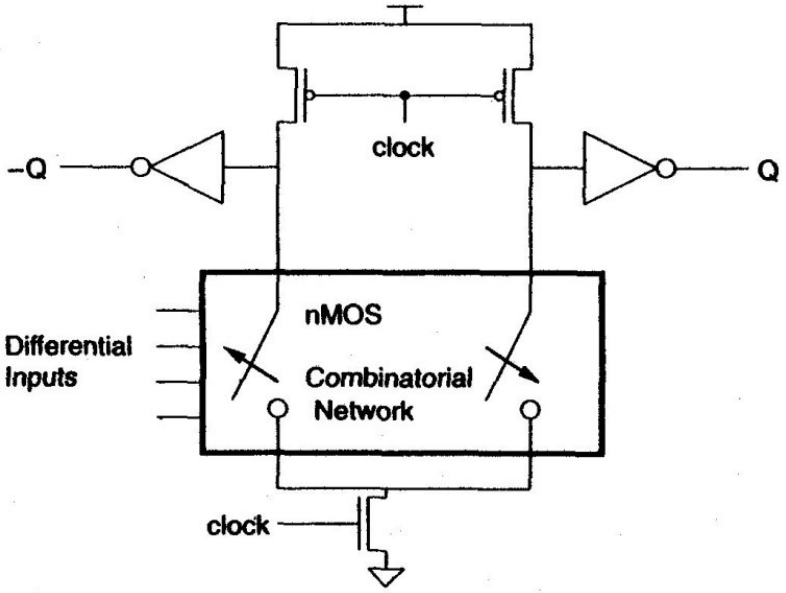
- Dual-rail domino can have inverting outputs
  - Takes true and complementary inputs
  - Produces true and complementary outputs
  - A completion signal can be added (used in asynchronous circuits)

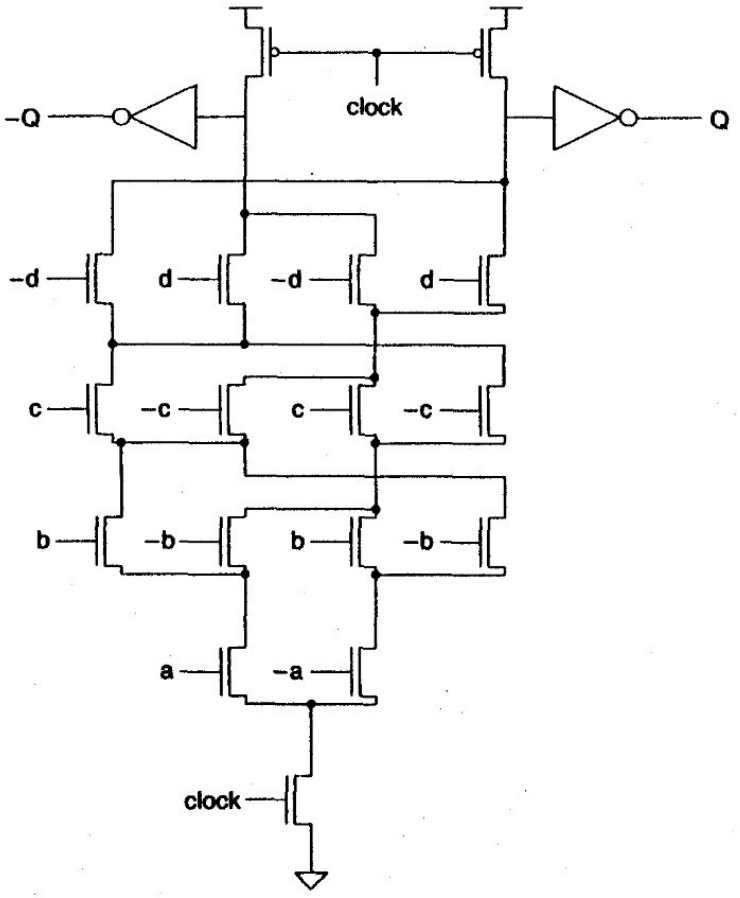
sig_h	sig_l	Meaning
0	0	Precharged
0	1	'0'
1	0	'1'
1	1	invalid



Clocked CVSL

- Another name for dual-rail domino logic.
- Two complementary domino logic gates (back to back), but with a merging NMOS block.



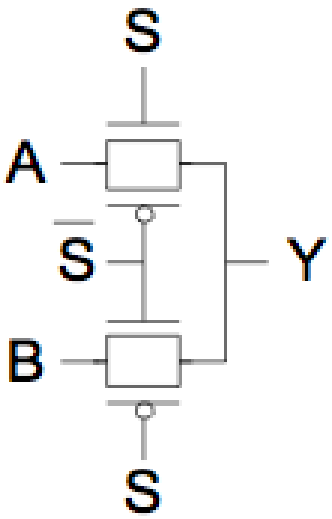


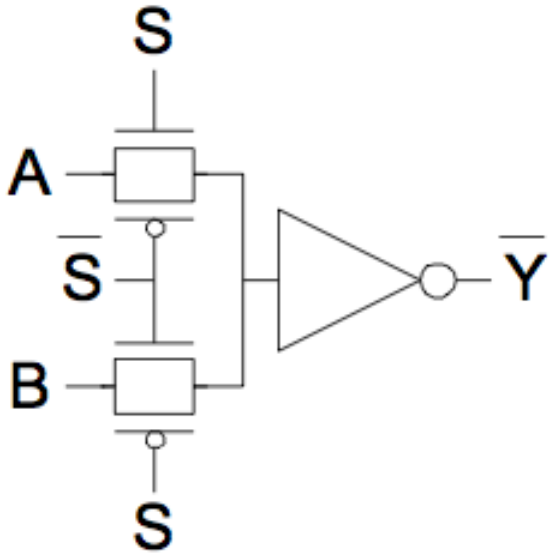
Domino Logic Summary

- Domino logic is attractive for high-speed circuits
  - 1.5-2 times faster than static CMOS
  - But many challenges:
    - Monotonicity
    - Leakage
    - Charge sharing
    - Noise
  - Widely used in high-performance microprocessors

Pass Transistor Circuits

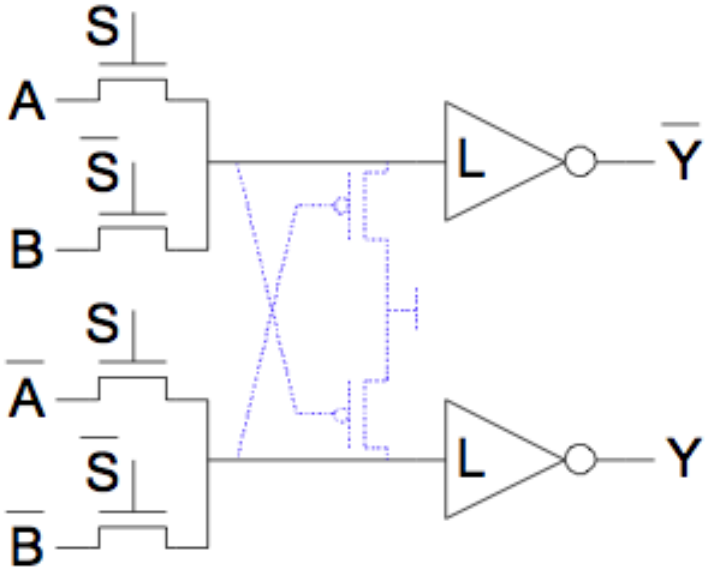
- Use pass transistors like switches to do logic
- Inputs drive diffusion terminals as well as gates
- CMOS + Transmission Gates (CMOSTG)
  - 2-input multiplexer example
  - Gates is restoring after adding the output inverter





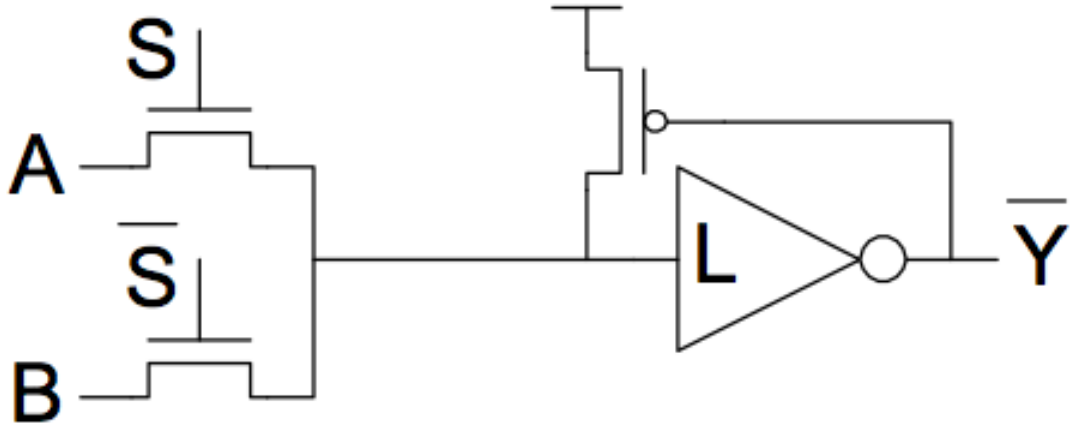
CPL

- Complementary Pass-transistor Logic
  - Dual-rail form of pass transistor logic
  - Optional cross-coupling for rail-to-rail swing



LEAP

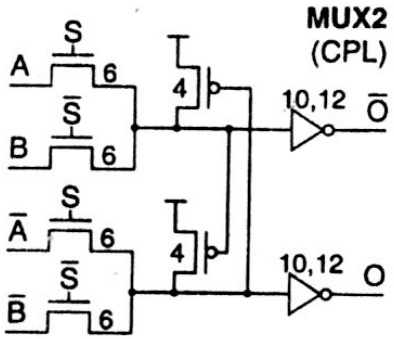
- LEAn Integration with Pass transistors
- Get rid of cross-coupled PMOS transistors
  - Use weak PMOS feedback to pull output high



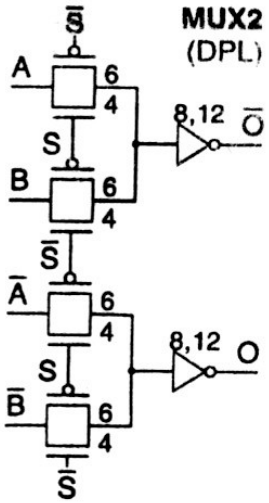
More Pass Transistor Logics

- Double Pass transistor Logic
- Swing Restored Pass transistor Logic

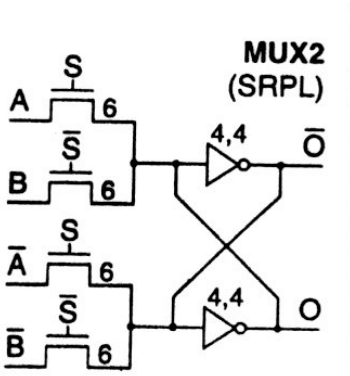
CPL



DPL



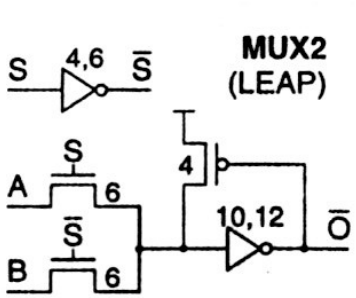
SRPL



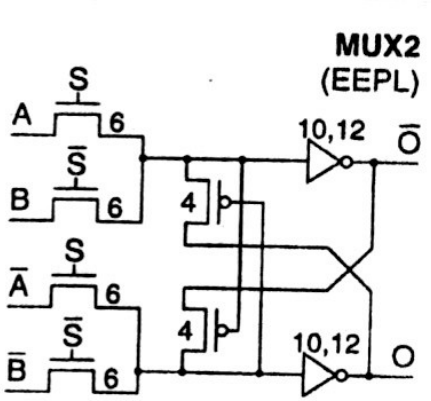
More Pass Transistor Logics

- Energy-Economized Pass transistor Logic
- Push-Pull Pass transistor Logic

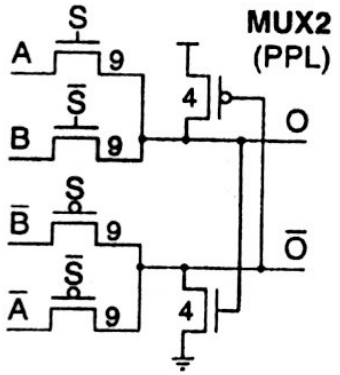
LEAP



EEPL

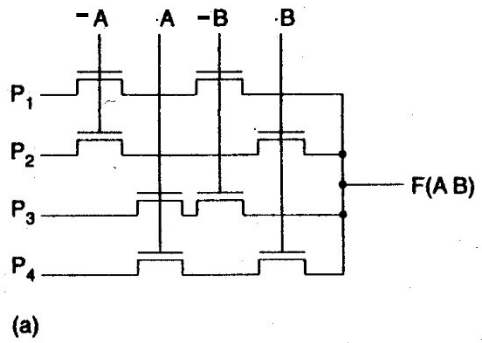


PPL



Boolean Function Unit

- Implement all *n*-input Boolean function (truth table)
- There are 2^{2^n} possible *n*-input Boolean functions.



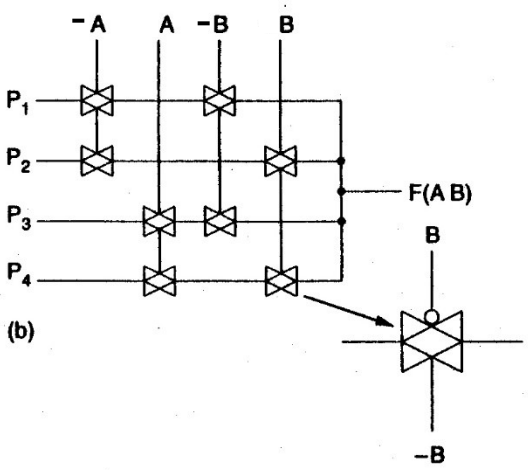
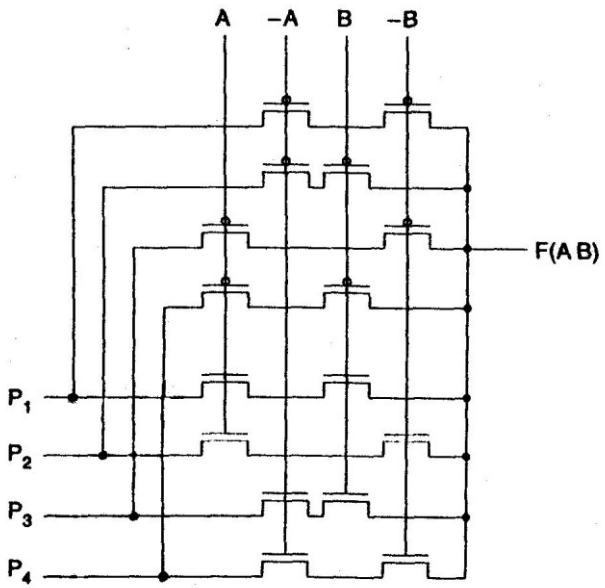


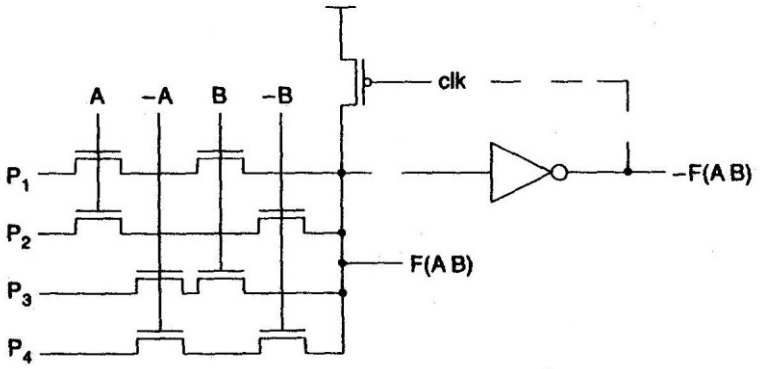
TABLE 5.9 Some Functions Implemented by the Boolean Function Unit

OPERATION	P1	P2	P3	P4
AND (A,B)	0	0	0	1
XOR (A,B)	0	1	1	0
OR (A,B)	0	1	1	1
NOR (A,B)	1	0	0	0
NAND (A,B)	1	1	1	0

Boolean Function Unit

- Better layout topology groups NMOS and PMOS transistors together separately.
- NMOS version has the fastest fall time while the dynamic version needs a precharge phase and thus extends the clock cycle. Adding an inverter at the output of the dynamic function unit makes it static.





Summary on Logic

- Static logic is the best choice since it is noise-immune, dissipates no DC power, and is quite fast.
- Pseudo-NMOS logic is largely for large fan-in circuits, e.g. PLA, ROM.
- Domino logic should be used with extreme care (poor noise margin, coupling, charge sharing, etc.) and are not suggested for inexperienced designers.
- Pass transistor logic can be simple for some function, e.g. XOR. CPL is the most promising.
- The more you can make a gate look like inverter, the faster it is. Small number of cascaded transmission gates can also be fast.