Chapter 10
Power/Clock Distribution, IO, and Packaging

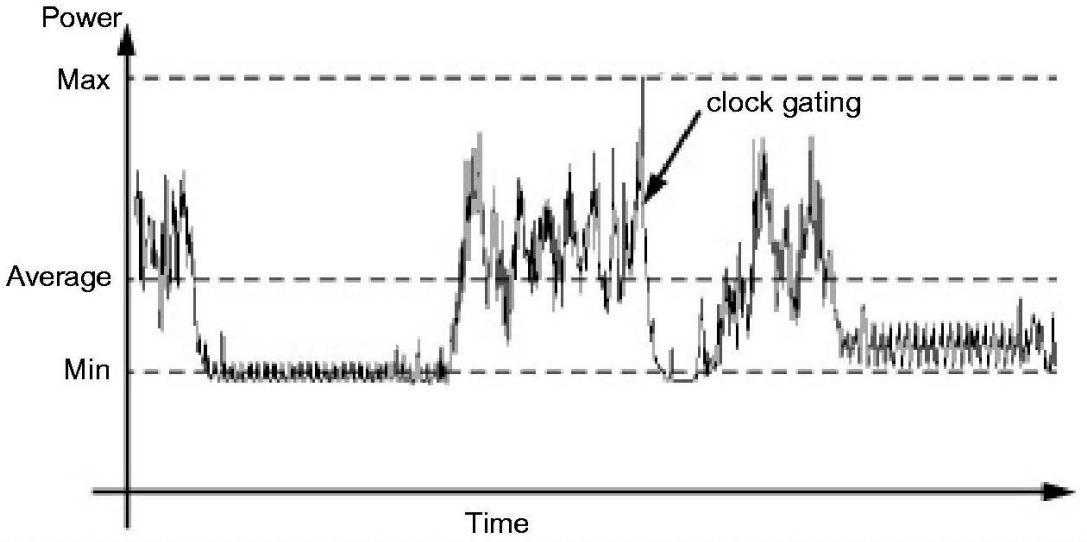
闕志達
台灣大學電機系

Power Distribution

- Power Distribution Network functions
  - Carry current from pads to transistors on chip
  - Maintain stable voltage with low noise
  - Provide average and peak power demands
  - Provide current return paths for signals
  - Avoid electromigration & self-heating wearout
  - Consume little chip area and wire
  - Easy to lay out

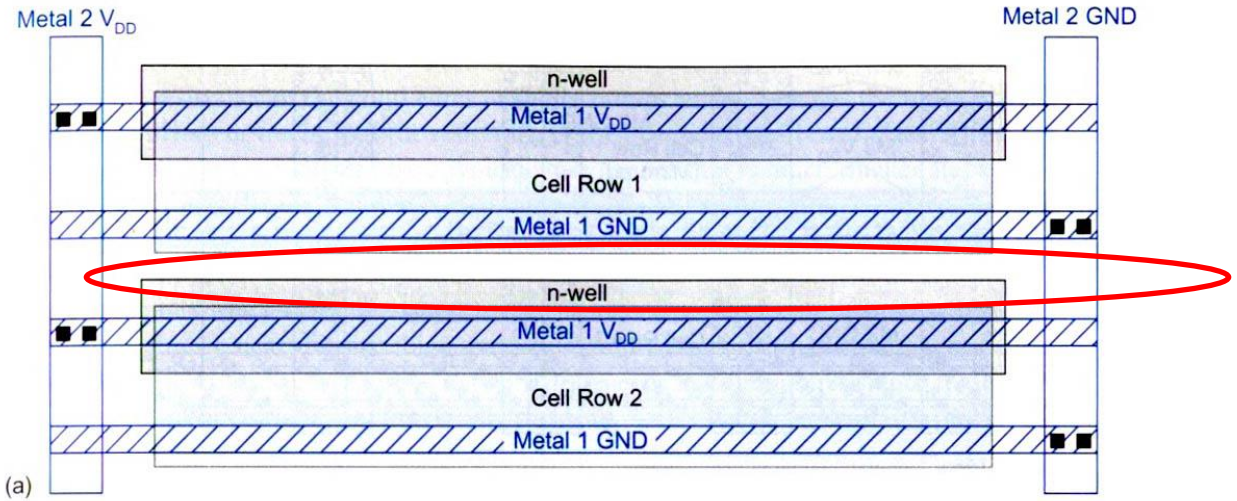
Power Requirements

- $V_{DD} = V_{DDnominal} - V_{droop}$
- Want V_{droop} < +/- 10% of V_{DD}
- Sources of V_{droop}
  - IR drops
  - di/dt noise
- I_{DD} changes drastically

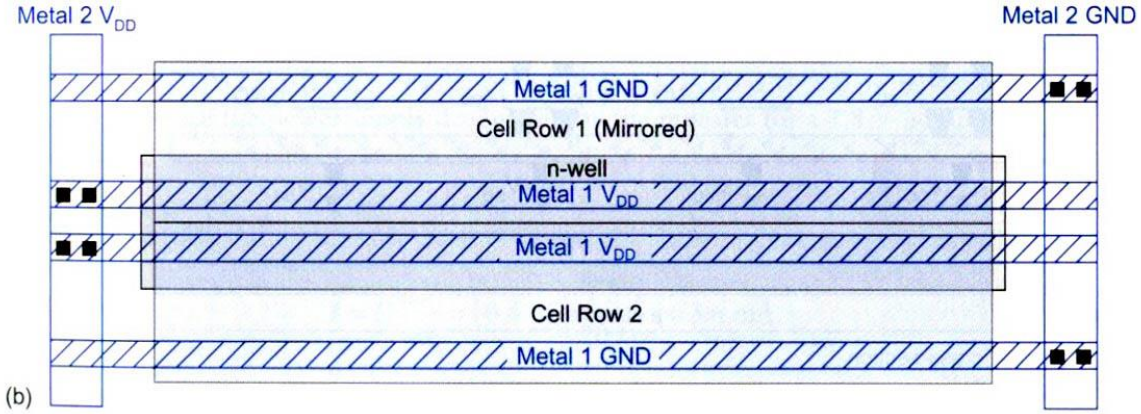


Power Distribution Network

- Network for standard-cell design



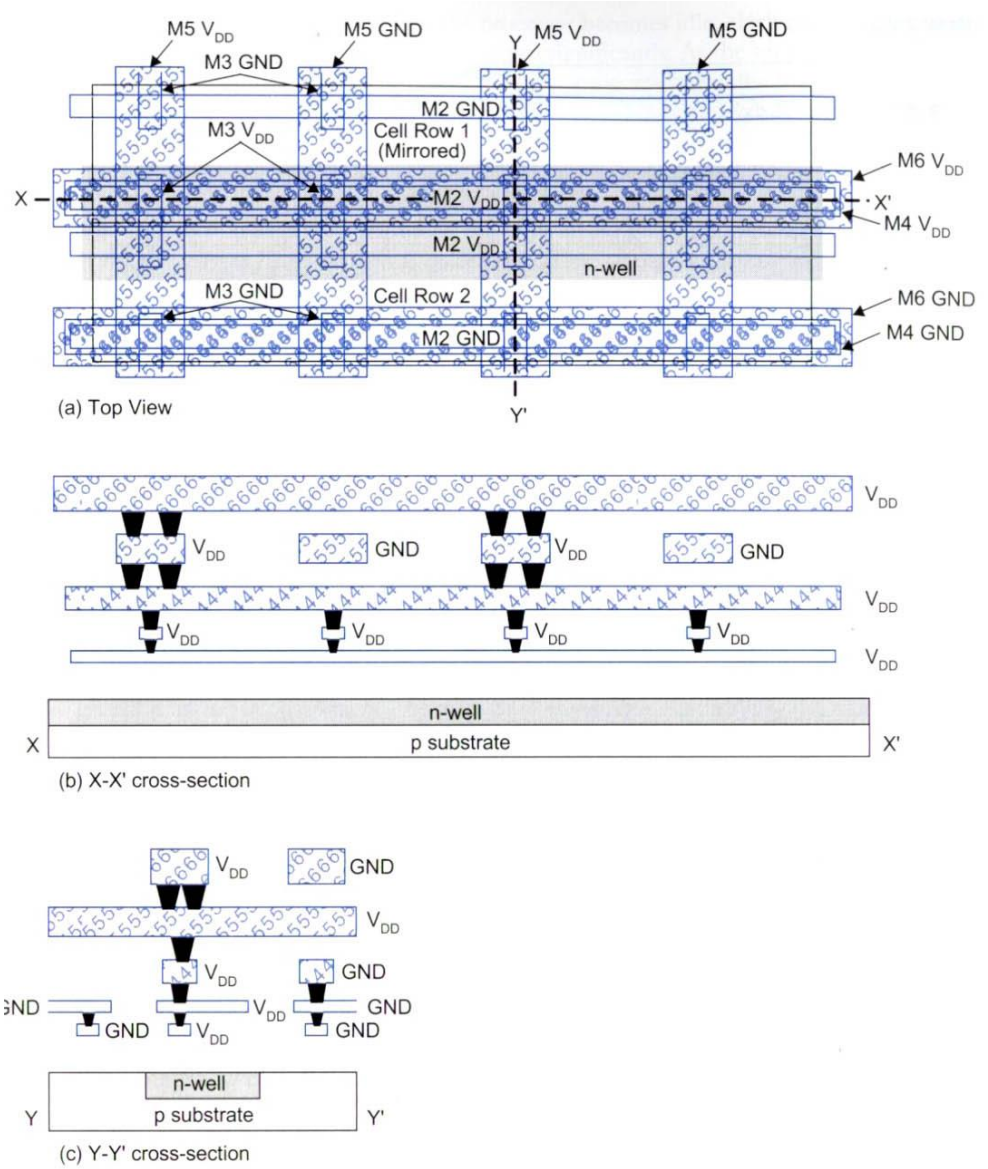
Routing channel



Over-the-cell routing

Power Distribution Network

- Network for high-power IC
  - Use grid of top-level metal to reduce resistance.
  - Plenty of vias to carry large current.

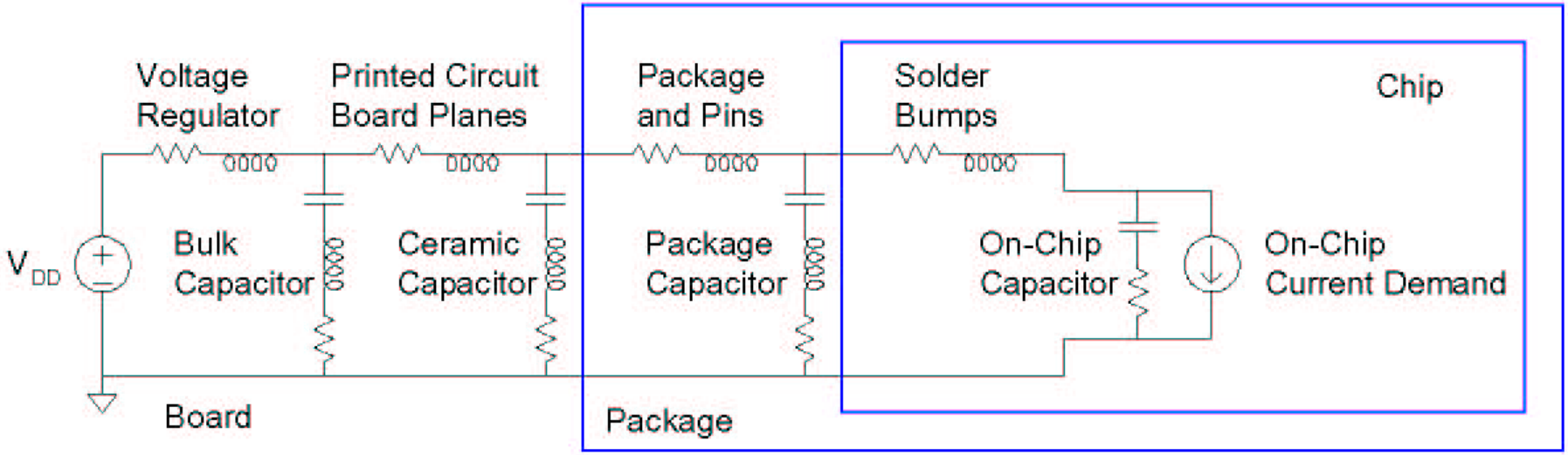


IR Drop and Ldi/dt

- IR Drop
  - When a large current flow through non-zero-resistance power/ground lines, there will be voltage drop due to Ohm's law.
- Ldi/dt noise
  - Wires (especially bonding wires) have inherent inductance and with change of current magnitude along the wires, there will be Ldi/dt voltage drop across the wires.
- Remedy
  - On-chip bypass capacitance can reduce the need to go through long wires for local current needs and thus reduces IR drop and Ldi/dt effects.

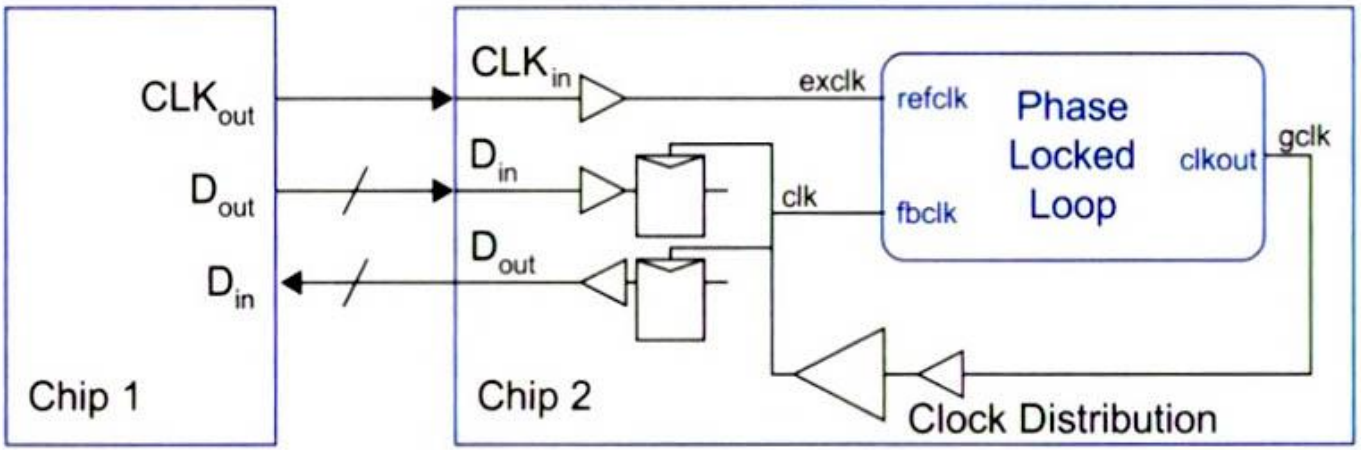
Power Network Model

- Power comes from regulator on system board
  - Board and package add parasitic R and L
  - Bypass capacitors help stabilize supply voltage
  - But capacitors also have parasitic R and L
- Simulate system for time and frequency responses



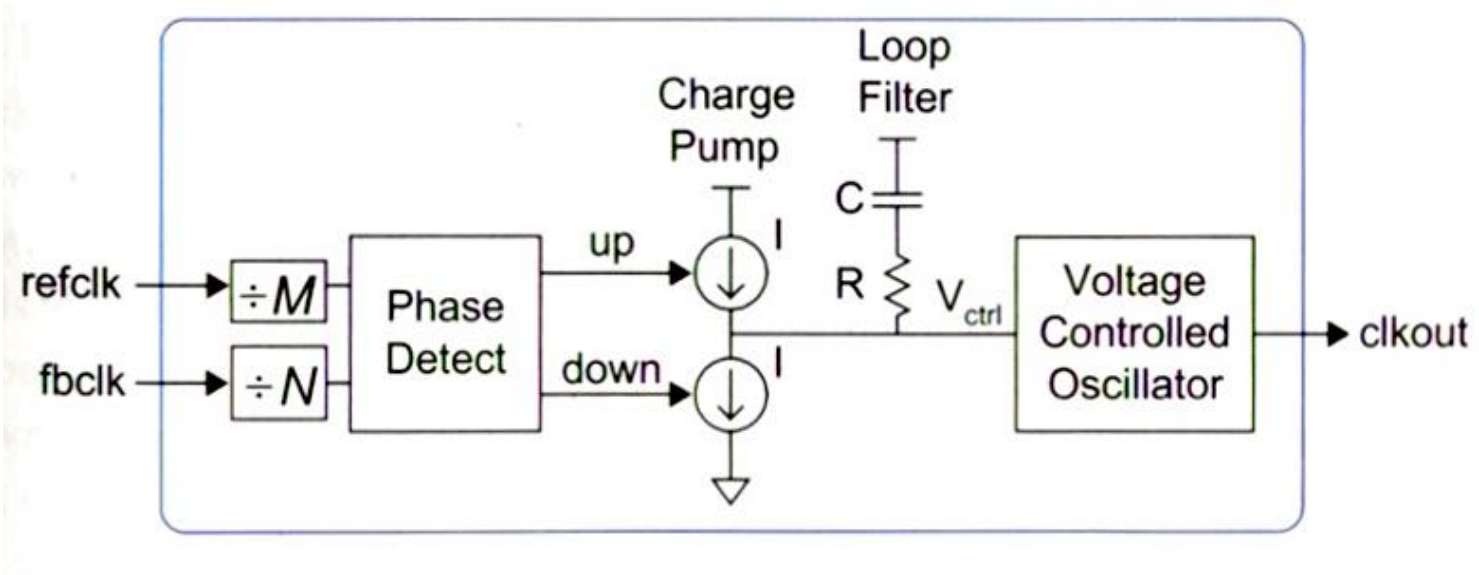
Clock Generation

- Receive an external clock signal and generate a global clock to be distributed to all sequencing elements and memory.
- Simplest design will be a big buffer.
- Nowadays, many different version/phase/frequency of clock signals are needed in a complicated IC.
- Use PLL to generate clock signals with different phase and frequency.



Phase-Locked Loop

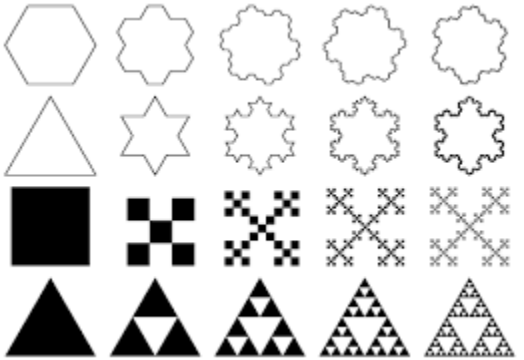
- A phase locked loop (PLL) can be used to synchronize the internal clock of a chip with an external clock. It can also be used to generate an internal clock with higher frequency, especially when the internal clock rate higher than GHz is now common.



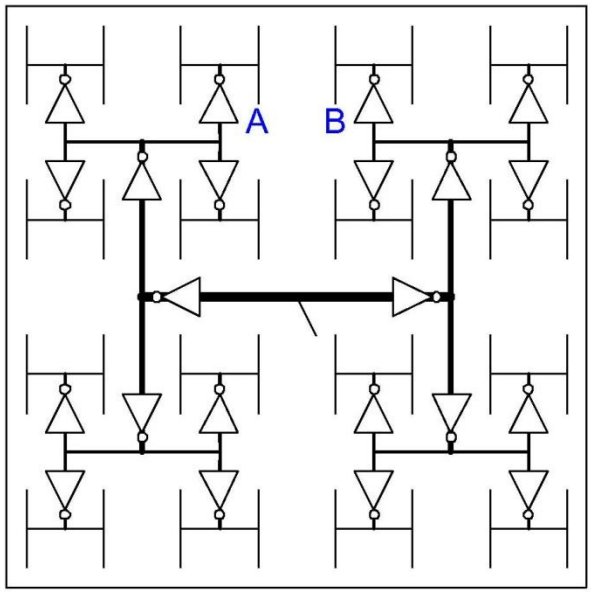
Clock Distribution -- Grid

- Use grid on two or more levels to carry clock (similar to power grid)
- Make wires wide to reduce RC delay
- Ensures low skew between nearby points
- But possibly large skew across die

Clock Distribution – H-Tree

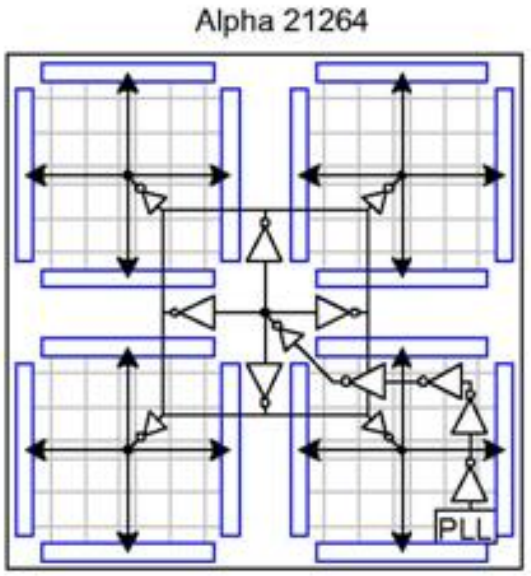


- Fractal structure
  - Gets clock arbitrarily close to any point
  - Matched delay along all paths
- Delay variations cause skew
- A and B might see big skew though they are very close. This is due to non-uniform clock loading.



Clock Distribution – Hybrid

- Use H-tree to distribute clock to many points
- Tie these points together with a grid
- Ex: IBM Power4, PowerPC, Alpha
  - H-tree drives 16-64 sector buffers
  - Buffers drive total of 1024 points
  - All points shorted together with grid



Summary on Clock Signal

- Clock is a very sensitive signal. It must be delivered to all registers without distortion in waveform or too much delay skew.
- Clock drivers are needed for driving large load. Actually, drivers are needed to drive all signals with large load, e.g. RESET signal.
- Gated clock is often used to reduce circuit activity and thus power consumption. Make sure that proper gated clock waveform is provided.
- Never use outputs of some complex combinational circuits as clock for some registers (hazard of glitches and spurious switching)

Chip Inputs/Outputs

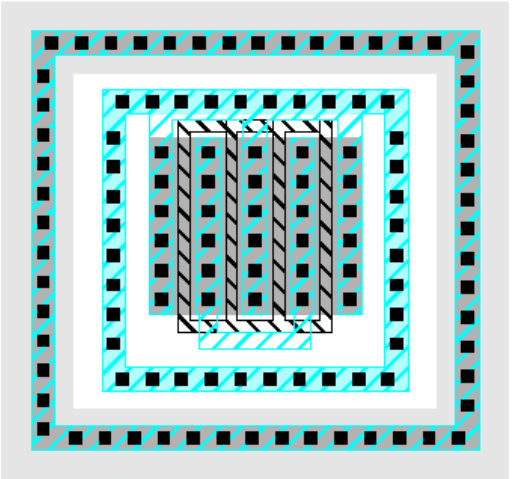
- Input/Output System functions
  - Communicate between chip and external world
  - Drive large capacitance off chip
  - Operate at compatible voltage levels
  - Provide adequate bandwidth
  - Limit slew rates to control di/dt noise
  - Protect chip against electrostatic discharge
  - Use small number of pins (low cost)

I/O Pad Design

- Pad types
  - V_{DD} / GND
  - Output
  - Input
  - Bidirectional
  - Analog

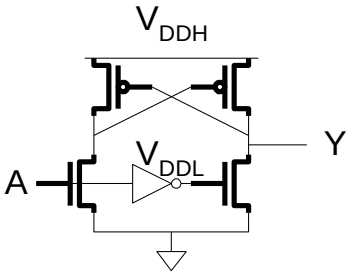
Output Pads

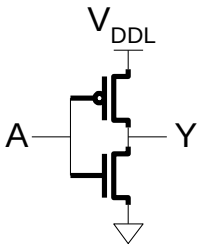
- Drive large off-chip loads (2 – 50 pF)
  - With suitable rise/fall times
  - Requires chain of successively larger buffers
- Guard rings to protect against latchup
  - Noise below GND injects charge into substrate
  - Large nMOS output transistor
  - p+ inner guard ring
  - n+ outer guard ring
    - In n-well



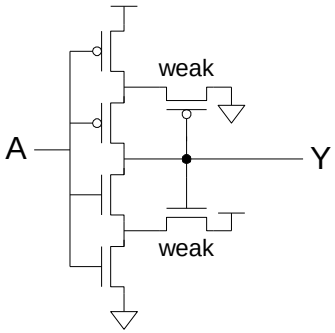
Input Pads

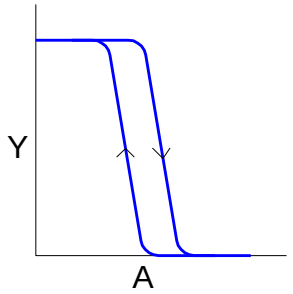
- Level conversion
  - Higher or lower off-chip V
  - May need thick oxide gates





- Noise filtering
  - Schmitt trigger
  - Hysteresis changes V_{IH}, V_{IL}

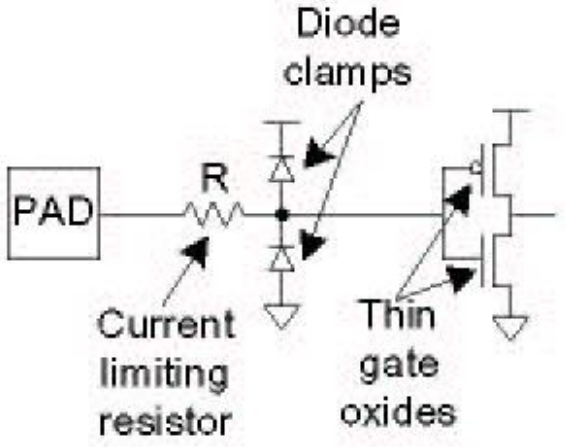


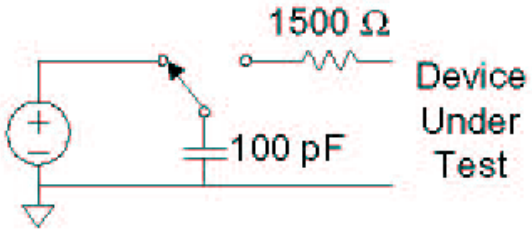


- Protection against electrostatic discharge (ESD, see next page)

ESD Protection

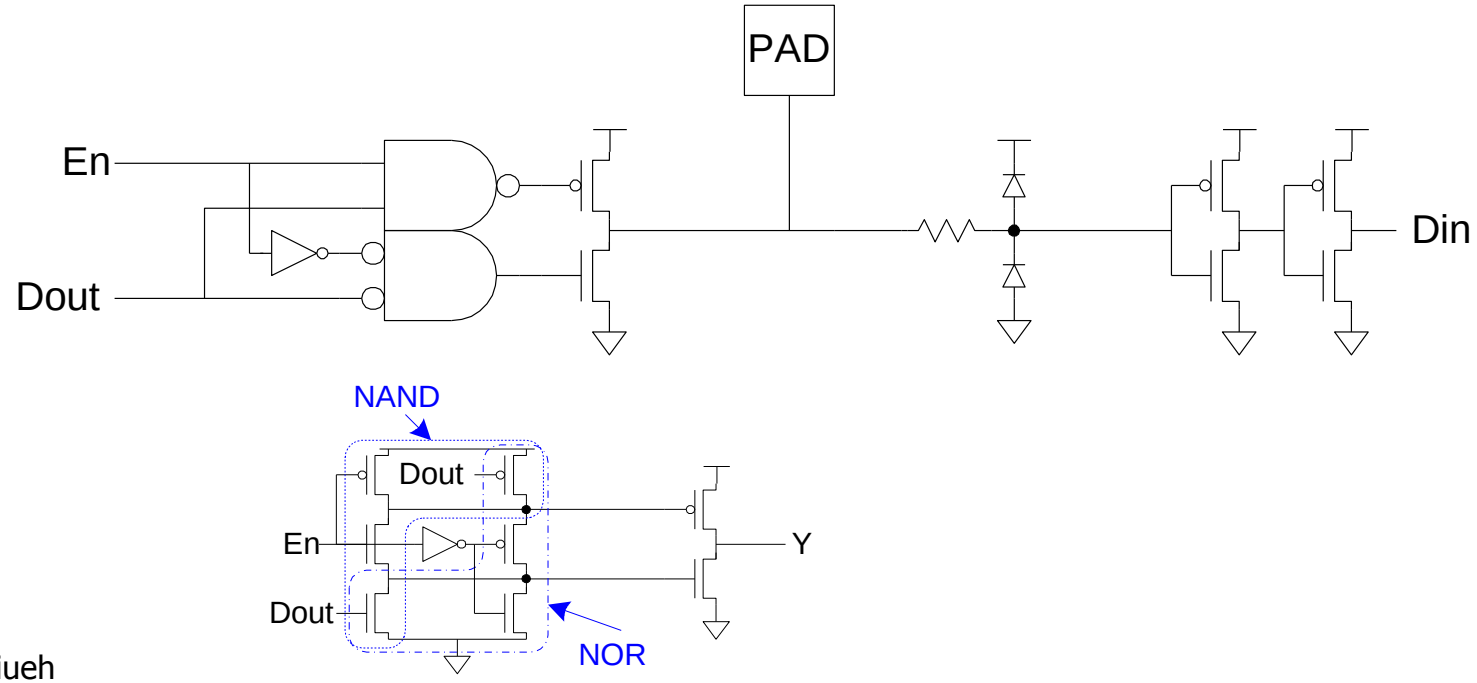
- Static electricity builds up on your body
  - Shock delivered to a chip can fry thin gates
  - Must dissipate this energy in protection circuits before it reaches the gates
- ESD protection circuits
  - Current limiting resistor
  - Diode clamps
- ESD testing
  - Human body model
  - Views human as charged capacitor
  - Voltage source can be 2-4KV or 15KV

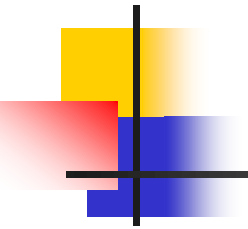




Bidirectional Pads

- Combine input and output pad
- Need tristate driver on output
  - Use enable signal to set direction
  - Optimized tristate avoids huge series transistors



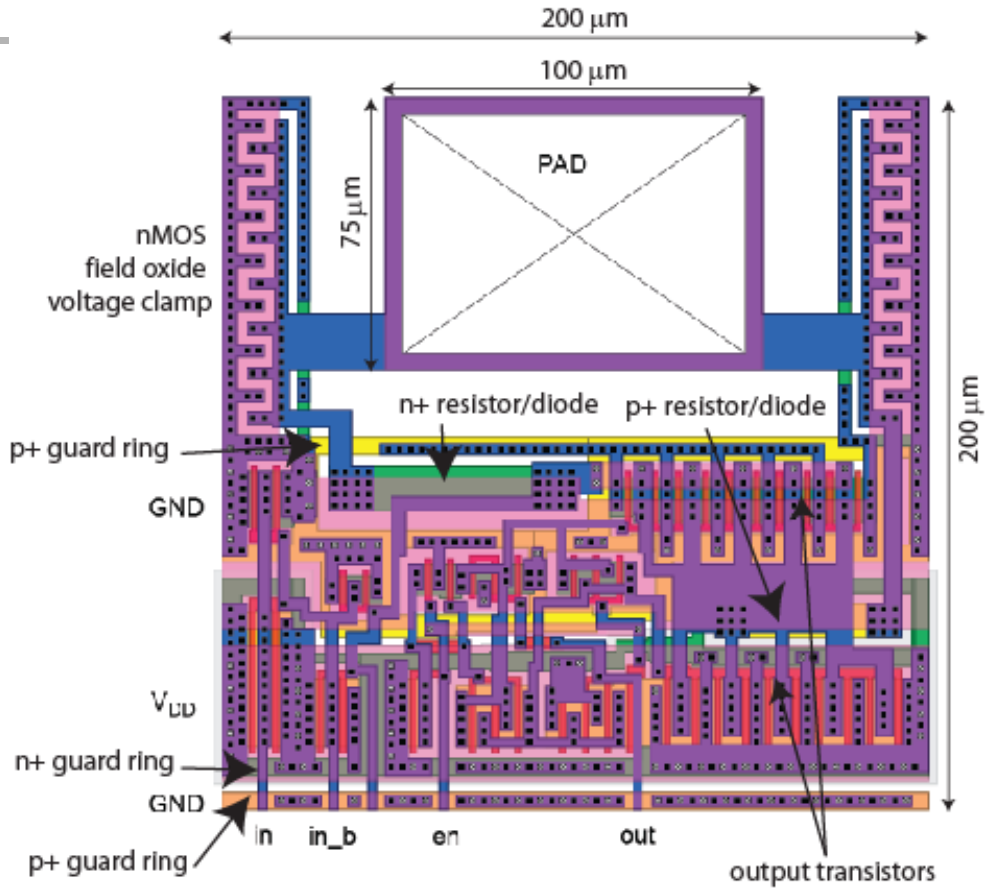


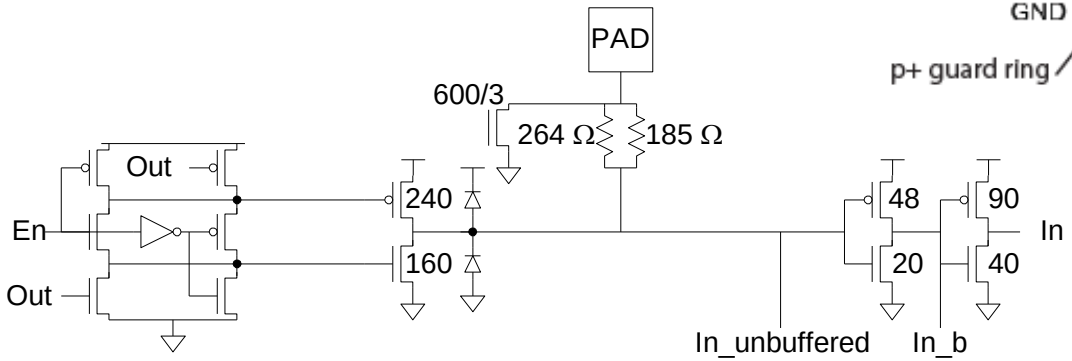
Analog Pads

- Pass analog voltages directly in or out of chip
  - No buffering
  - Protection circuits must not distort voltages

MOSIS I/O Pad

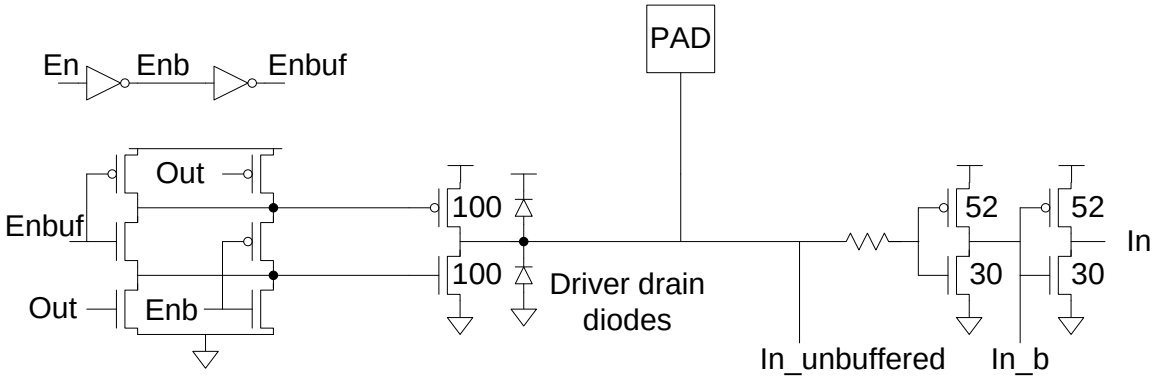
- 1.6 μm two-metal process
  - Protection resistors
  - Protection diodes
  - Guard rings
  - Field oxide clamps

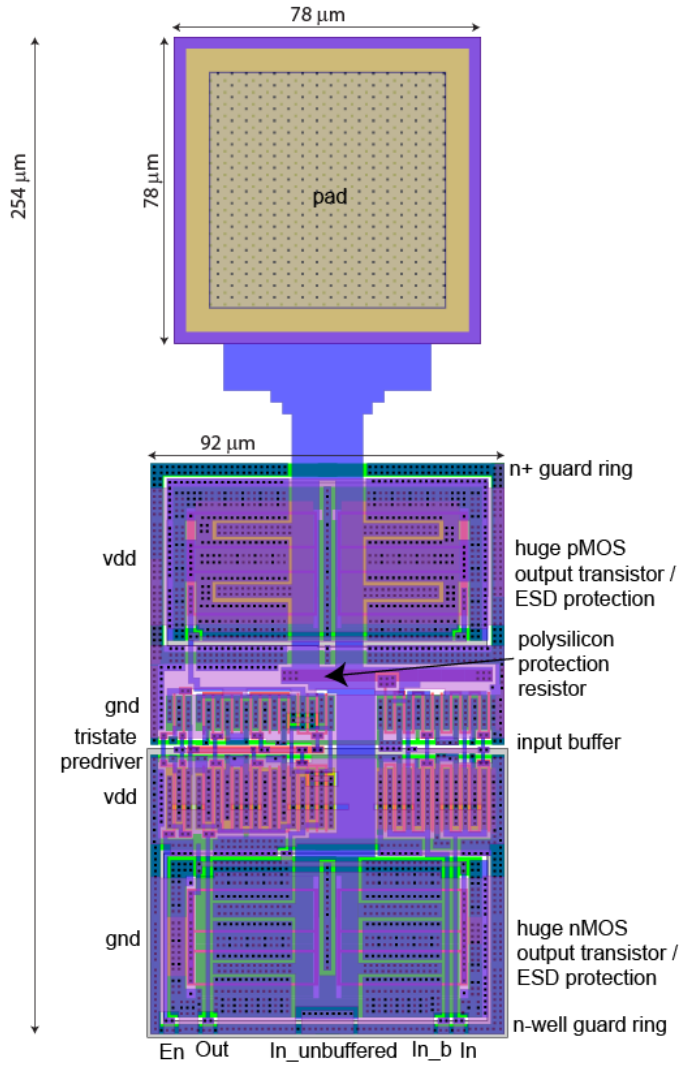




U. of Utah I/O Pad

- 0.6 μm three-metal process
  - Similar I/O drivers
  - Big driver transistors provide ESD protection
  - Guard rings around driver



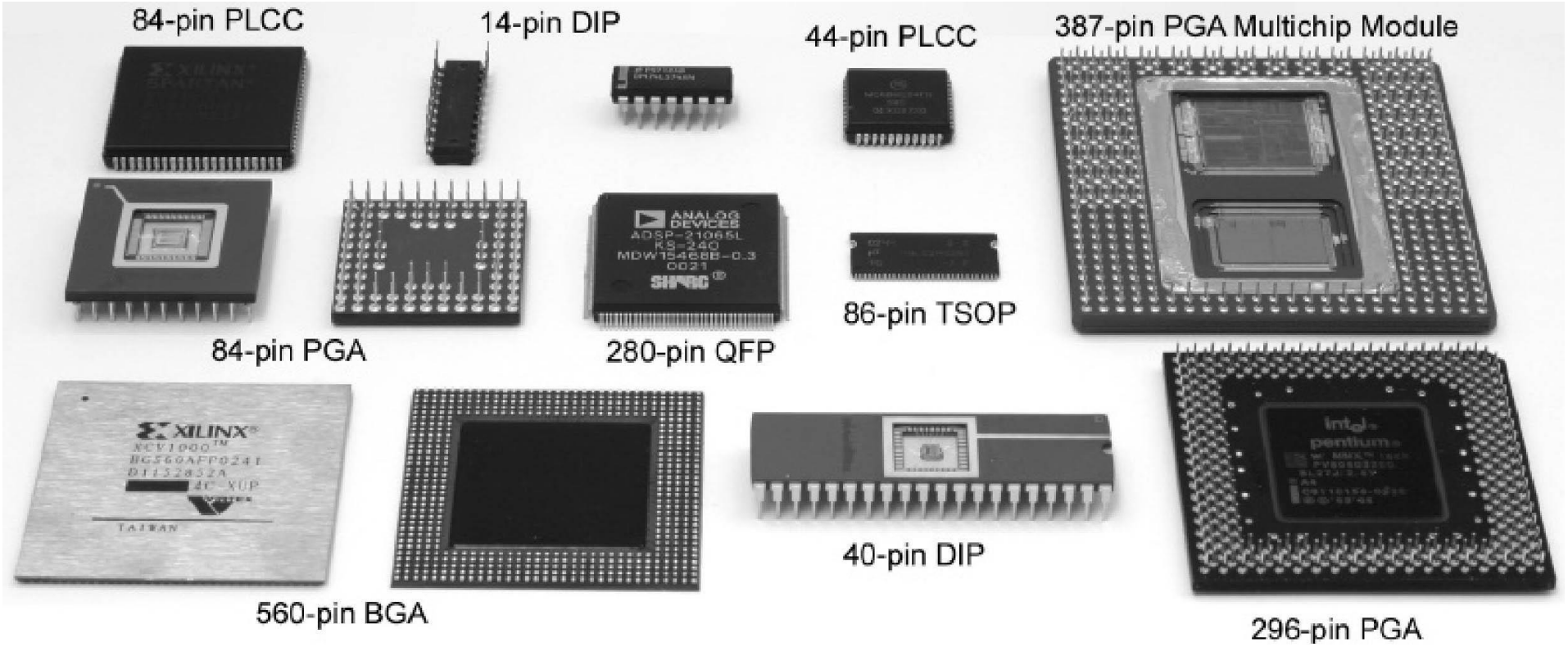


Packages

- Package functions
  - Electrical connection of signals and power from chip to board
  - Little delay or distortion
  - Mechanical connection of chip to board
  - Removes heat produced on chip
  - Protects chip from mechanical damage
  - Compatible with thermal expansion
  - Inexpensive to manufacture and test

Package Types

- Through-hole vs. surface mount



Multi-chip Modules (MCM)

- a. k. a. System in Package (SiP)
- Pentium Pro MCM
  - Fast connection of CPU to cache
  - Expensive, requires known good dice