IC Design

Homework # 4

(Due on 2017/01/06, 13:20, Verilog code upload to CEIBA, hardcopy report to class)

✧ Plagiarism is not allowed. 10% penalty for each day of delay.

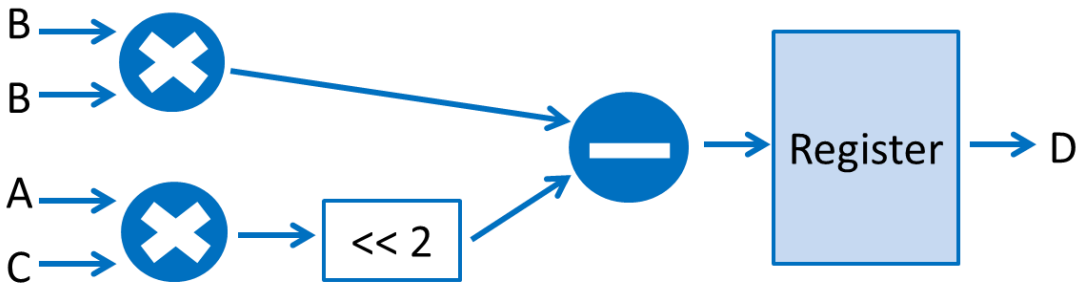
✧ Any further questions, you can leave messages on the board of the class website or send e-mail to the TA

Specifications

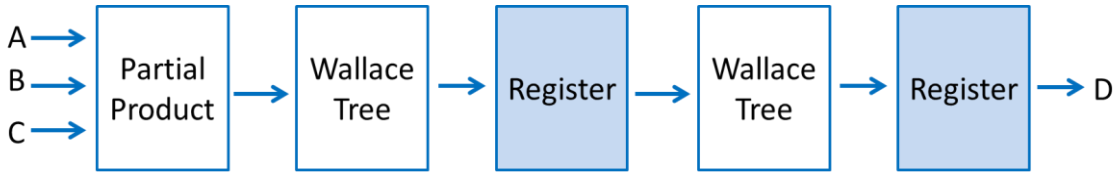
Design a calculator circuit with reset that computes the **Discriminant of Quadratic Equation**. There are three inputs, i.e., A with 4 bits, B with 7 bits, and C with 6 bits. And there is one output D with 15 bits. Note that all the inputs and output are signed integers and all the inputs and outputs are in the form of 2's complement. The relation between input and output is

$$D = B^2 - 4AC$$

The flow diagram is as follows.



You have to design your Wallace tree in two-stage pipeline (use module FD2 (positive edge) in lib.v), and the detailed flow diagram is as follows.



➢ Your design must support **2's complement** input and output such as $(-7)_{10}=(1001)_2$.

➢ There should be a **reset signal** for the register.

➢ Please add pipeline registers to your circuit to design a two-stage pipeline circuit. You can loosen your simulation timing first, (i.e., **`define HALF_CYCLE XXXX** in the testbench_ppl.v), then shorten the clock period to find your critical path.

➢ Your design should be based on the **standard cells in the lib.v**. All logic

operations in your design **MUST consist of the standard cells** instead of using the operands such as "+", "-", "&", "|", ">", and "<".

- Design your homework in the given "DOQE_ppl.v" file. **You are NOT ALLOWED to change the filename and the header of the top module (i.e. the module name and the I/O ports)**.
- If your design contains more than one module, don't create new file for them, just put those modules in "DOQE_ppl.v."
- The first stage of your design may be a partial product generator that generates partial product terms; the second is the Wallace tree structure with pipeline register; the third is a 15-bit output register.
- The provided test-bench *testbench_ppl.v* will reset your register first and then feed inputs and check the output results.
- The output waveform will be dumped to file "DOQE*_ppl.fsdb*", you can use nWave to examine it.

Grading Policy

1. Gate-level design using Verilog (70%)

Your score will depend on both the correctness and performance of your design.

(a) Correctness (50%)

We provide a test bench with 100 patterns which automatically grades your design. Your score in this part will be 50* (1 – error numbers / 100)

(b) Ranking (20%)

We will rank all students who have passed (a) in terms of the product of the half-cycle time and the number of transistors. The score will be given as follows.

Percentage of passing students	Score
If your ranking > 85 %	20
65%~84%	16
35%~64%	12
15%~34%	8
0%~14%	4
Using operands, not standard cell logic	0
Correctness failed	0
Plagiarism	0

2. Report (30%)

(a) Circuit diagram (10%)

Plot the gate-level circuit diagram of your design. You are encouraged to plot it hierarchically so that readers can understand your design easily.

(b) Simulation (10%)

(5%) Record your **minimum half-cycle time** according to your simulation and **plot critical path** on the diagram in (a).

You have to write down your minimum half-cycle time according to your simulation. This minimum half-cycle time would be verified by TAs.

(5%) Find the number of transistors in your design **by hand.**

Compute the product of the minimum half-cycle time and the number of transistors.

The numbers of transistors from each cells are specified in the lib.v

(c) Discussion (10%)

Discuss about your design. For example, introduce your design, how do you cut your pipeline? What is your Wallace structure? How do you improve your critical path and the number of transistors? How do you trade-off between area and speed?

Notification

- Following are the files you will need (available on the class website)
  HW4.rar includes
  - **HW4_2016.pdf** : this document.
  - **HW4_tutorial** Tutorial in class
  - **DOQE_ppl.v**:
    Dummy design file. Program the design in this file.
    The header of the top module and the declaration of the I/O ports are predefined in this file and you are not allowed to change them.
  - **lib.v**: standard cells.
  - **testbench_ppl.v**:
    Test bench for your design.
  - **A.dat, B.dat , C.dat**:
    Input patterns for test bench. Please put these files in the folder that contains testbench_ppl.v when doing simulation.
  - **answer.dat**:
    Output patterns of correct answers for test bench. Please put the file in the folder that contains testbench_ppl.v when doing simulation.

- You should submit the **Report** (hardcopy) in class.
- Your Verilog codes written in **only one file** should be uploaded to CEIBA by due time (Don't use e-mail).

- **Electronic version of Verilog codes should be uploaded to CEIBA by due time.**
  - Rename your DOQE_ppl.v as **HW4_Student ID.v**, Ex. HW4_b03901001.v
  - Do **NOT** change any **module name** and **port name** in Verilog file.
  - Upload your Verilog file (single file) to **CEIBA**

TA email: r04943028@ntu.edu.tw , EE2-329
HW4 Office hours: 2017/01/03 (二) 19:00~21:00 博理 211
2017/01/05 (四) 19:00~21:00 博理 211
If you have no time at office hours, you can email TA to discuss another time for appointment.