IC Design

Homework # 3

(Due on 2016/12/16, 13:20. Verilog code and Report upload to CEIBA)

- ✧ Plagiarism is not allowed. 10% penalty for each day of delay.
- ✧ Any further questions, you can send e-mail to the TA or leave messages on the board of the class website.
- ✧ TA email: r04943028@ ntu.edu.tw, EE2-329

Specifications

In this homework, you are asked to design a gate-level combinational circuit that finds the median among five given numbers. The inputs of this circuit are **five distinct 6-bit unsigned** digital values, denoted as *i0, i1, i2, i3, i4*. The output of the circuit, denoted as *median*, is a **3-bit number** that indicates which one is the median. The relationship between input and output is listed as follows:

- ➢ If *i0* is the median, *median* will be 3'b000.
- ➢ If *i1* is the median, *median* will be 3'b001.
- ➢ If *i2* is the median, *median* will be 3'b010.
- ➢ If *i3* is the median, *median* will be 3'b011.
- ➢ If *i4* is the median, *median* will be 3'b100.

Following are some examples of the I/O:

Input					Output
i0	*i1*	*i2*	*i3*	*i4*	*median*
101101	010010	000011	111100	101111	000
000111	001010	011100	111011	00000	001
000011	111111	010101	101010	111000	011

There are some important things that you should notice:

- ➢ Your design should base on the **standard cells in the lib.v**. All logic operations in your design **MUST consist of the standard cells** instead of using the operands such as "+", "-", "&", "|", ">", and "<".
- ➢ Design your homework in the given "Comparator_51.v" file. **You are NOT ALLOWED to change the filename and the header of the top module (i.e. the module name and the I/O ports)**
- ➢ If your design contains more than one module, do not create new file for them,

just put those modules in “Comparator_51.v”

- You don’t need to consider the situation of two or more identical numbers. The five given numbers are always different.
- Run simulation : ***ncverilog +access+r tb_Comparator_51.v Comparator_51.v lib.v***
- The output waveform will be dumped to file “**Comparator_51.fsdb**”. You can use nWave to check it.

Grading

1. Gate-level design using Verilog (70%)

Your score will depend on both the correctness and performance of your design. We provide a testbench which automatically grades your design.

Correctness & Performance	Score
Fail to pass the test bench.	40 * (1-err #/1000)
Functionally correct	40
Critical path < 10ns	45
Critical path < 7ns	50
Critical path < 6ns	55
Critical path < 5ns	60
Critical path < 4ns	65
Critical path < 3ns	70
Using operands, not standard cell logic	0
Plagiarism	0

2. Report (30%)

You should also introduce and discuss about your design. Following are some requirements of your report.

- Circuit diagram (15%)

  Plot the circuit diagram of your design. You are encouraged to plot it hierarchically so that the reader can understand your design easily.
- Discussion (15%)

  Discuss about your design. For example, introduce you design, how do you do the comparison, which technique is adopted in your design, how do you improve your critical path.

- You have to put the simulation result in your report. Ex:

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Congratulations! Your score is 70!
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Notification

- Following are the files you will need (available on the class website)

  HW3.rar includes

  - **HW3_2016.pdf** : this document.
  - **HW3_tutorial** Verilog introduction
  - **Comparator_51.v**:
    Dummy design file. Program the design in this file.
    The header of the top module and the declaration of the I/O ports are predefined in this file and you are not allowed to change them.
  - **lib.v**: standard cells.
  - **tb_Comparator_51.v**:
    Testbench for your design.
  - **in0.dat, in1.dat, in2.dat, in3.dat, in4.dat**:
    Input patterns for test bench. Please put these files in the folder that contains tb_Comparator_51.v when doing simulation.
  - **answer.dat**:
    Output patterns of correct answers for test bench. Please put the file in the folder that contains tb_Comparator_51.v when doing simulation.

- The following files should be compressed and uploaded to CEIBA by due time.
  - Report (PDF format)
  - Comparator_51.v
- File name rule : *HW3_(student id)_v#*

  Ex. HW3_b03901301_v1.rar

  Ex. HW3_b03901311_v2.rar