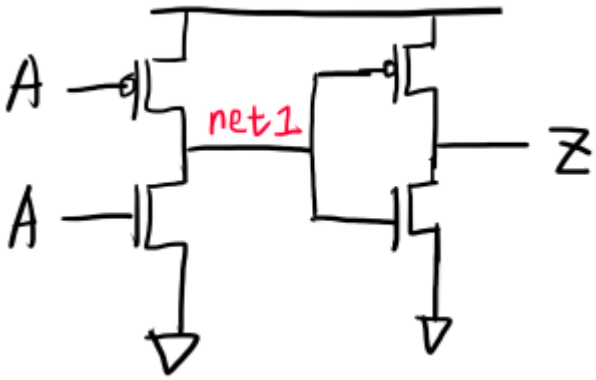
積體電路設計 hw2　　b02502108 陶昇永

Layout 8: Driver

a. Transistor-level circuit:



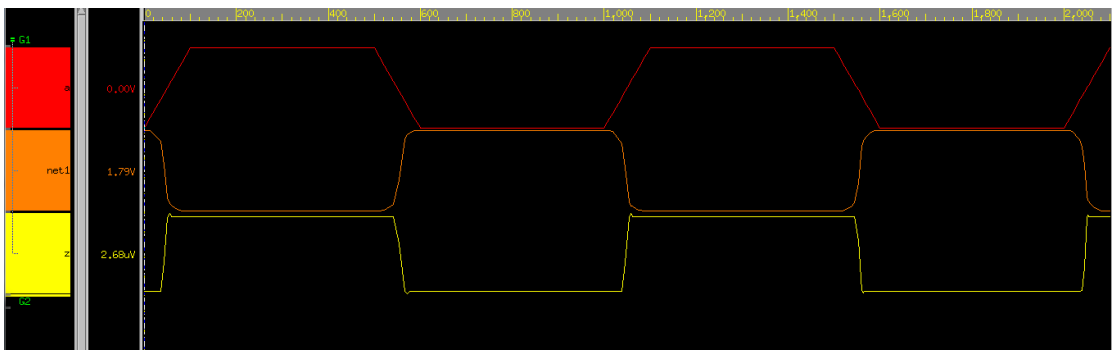
b. Gate-level circuit:

c. Inputs and outputs:
Input: A
Output: Z

d. Truth table:

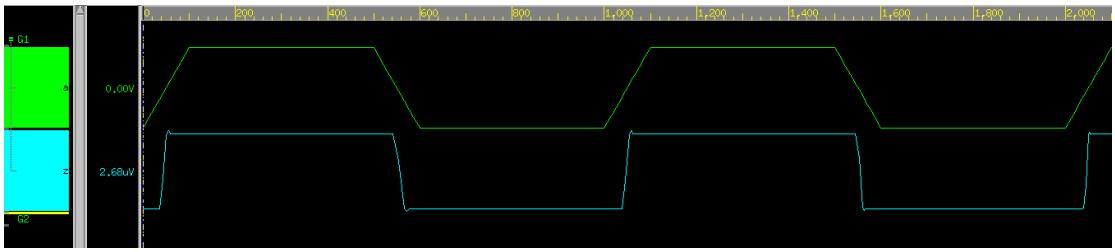
A	Z
0	0
1	1

e. Hspice/ nWave simulation:



由上圖可知，Vin 經過一級 inverter 後，信號因此 0、1 互換。之後再經過一

級類似 inverter 的電路，讓 0、1 再次換回與 input 相同，因此可以當 driver 來使用。下圖為 input 與 output 直接比較:

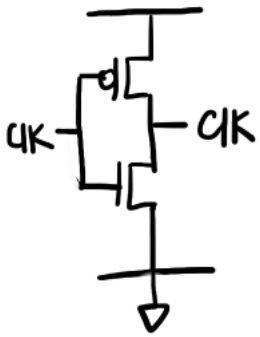


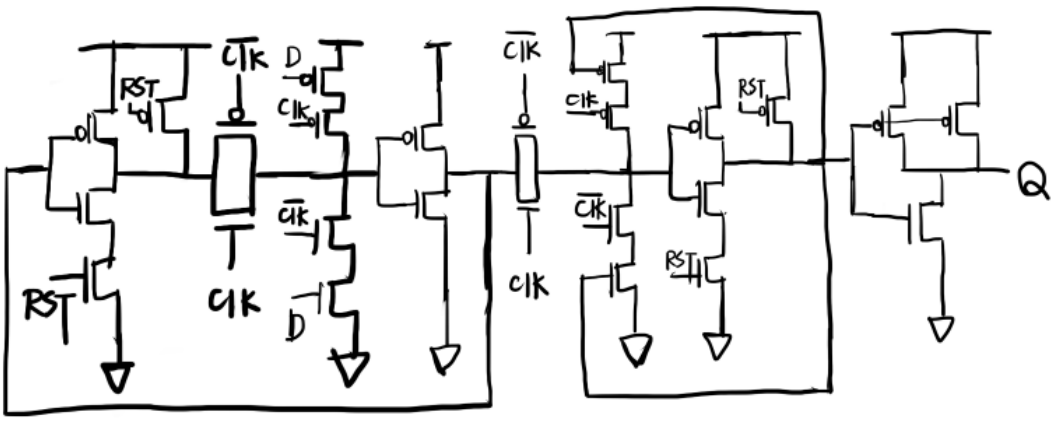
f. Hspice code:

```
*********************************************
.inc '90nm_bulk.l'
.SUBCKT Inv DVDD GND In Out
*.PININFO DVDD:I GND:I In:I Out:O
MN1 Out In GND GND NMOS l=0.1u w=0.25u m=1
MP1 Out In DVDD DVDD PMOS l=0.1u w=0.5u m=1
.ENDS
*********************************************

Vdd DVDD    0   1.8
Vss GND     0   0

Vin A      0   pulse (0 1.8 0 100n 100n 0.4u 1u)

x1 DVDD     GND A  net1     Inv
X2 DVDD     GND net1 Z   Inv

.tran 10n 2.1u
.op
.option post
.end
```

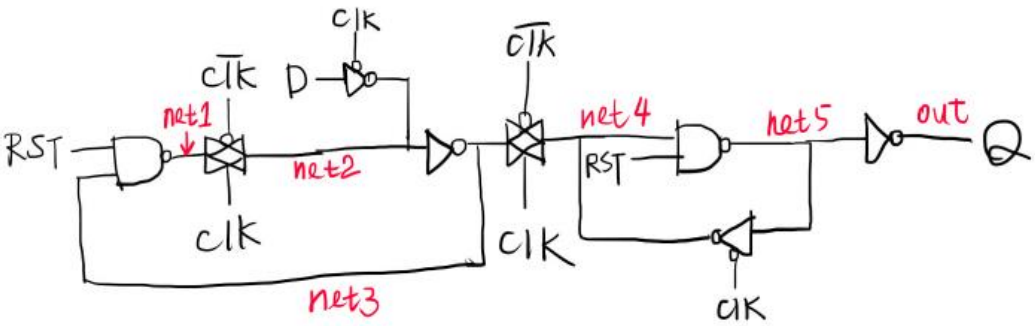
Layout 10: FD2

a. Transistor-level circuit:



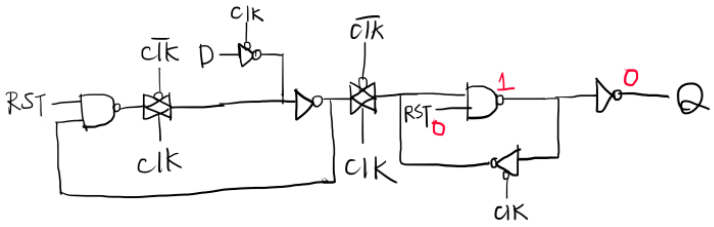


b. Gate-level circuit:



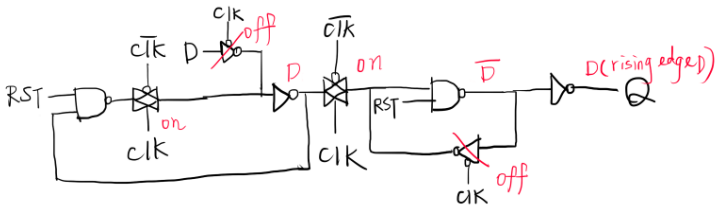
c. Inputs and outputs:
Inputs: RST, CLK, D
Output: Q

d. Truth table:
RST = 0: Q = 0

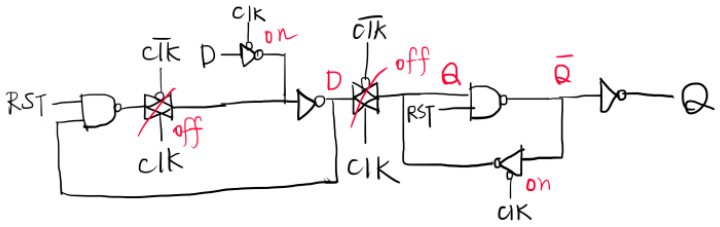


RST	D	Q
0	0	0
0	1	0

RST = 1:
CLK on: Q = D(rising edge)

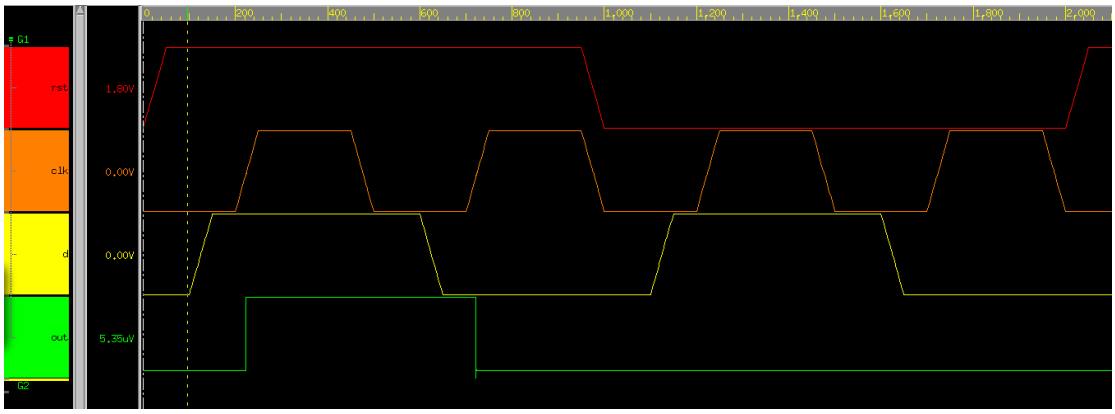


CLK off: PTL(transmission gate) off, Q keep



RST	CLK	D	Q
1	↑	X	D
1	除了↑以外	X	Q0(keep value)

e. Hspice/ nWave simulation:



如圖所示，當 RST 為 0 時，output Q 被強制歸零，RST=1 時，則看 CLK，若 CLK 為 rising edge，則 output Q = D，其他時候 output Q keep 原本的 Q 值，直到下次 rising edge 或 RST = 0 將 Q 歸零。此為 D flip/flop。

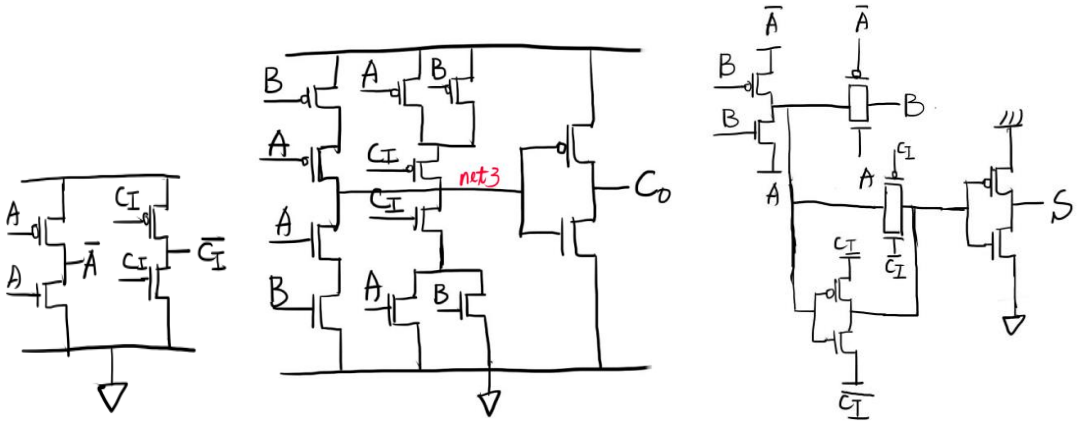
f. Hspice code:

```
*********************************************
.inc '90nm_bulk.l'
.SUBCKT Inv DVDD GND In Out
*.PININFO DVDD:I GND:I In:I Out:O
MN1 Out In GND GND NMOS l=0.1u w=0.25u m=1
MP1 Out In DVDD DVDD PMOS l=0.1u w=0.5u m=1
.ENDS
*********************************************
.SUBCKT Nand DVDD GND In1 In2 Out
*.PININFO DVDD:I GND:I In1:I In2:I Out:O
MN1 X   In1 GND GND NMOS l=0.1u w=0.25u m=1
MN2 Out In2 X   GND NMOS l=0.1u w=0.25u m=1
MP1 Out In1 DVDD DVDD PMOS l=0.1u w=0.5u m=1
MP2 Out In2 DVDD DVDD PMOS l=0.1u w=0.5u m=1
.ENDS
*********************************************
.SUBCKT Invv DVDD GND In Out
*.PININFO DVDD:I GND:I In:I Out:O
MN1 Out In GND GND NMOS l=0.1u w=0.25u m=1
MP1 Out In DVDD DVDD PMOS l=0.1u w=0.5u m=1
MP2 Out In DVDD DVDD PMOS l=0.1u w=0.5u m=1
.ENDS
*********************************************
.SUBCKT PTL DVDD GND In In1 In2 Out
*.PININFO DVDD:I GND:I In In1:I In2:I Out:O
MN1 Out In1 In GND NMOS l=0.1u w=0.25u m=1
MP1 Out In2 In DVDD PMOS l=0.1u w=0.5u m=1
.ENDS
*********************************************
.SUBCKT CLKInv DVDD GND In1 In2 In3 Out
*.PININFO DVDD:I GND:I In1:I In2:I In3 Out:O
MN1 x   In1 GND GND NMOS l=0.1u w=0.25u m=1
MN2 Out In2 x    GND NMOS l=0.1u w=0.25u m=1
MP1 y   In1 DVDD DVDD PMOS l=0.1u w=0.5u m=1
MP2 Out In3 y    DVDD PMOS l=0.1u w=0.5u m=1
.ENDS
*********************************************
```

```
Vdd DVDD    0   1.8
Vss GND     0   0

Vin D      0   pulse (0 1.8 100n 50n 50n 0.45u 1u)
V1 CLK     0   pulse (0 1.8 0.2u 50n 50n 0.2u 0.5u)
V2 RST    0   pulse (0 1.8 0 50n 50n 0.9u 2u)

x0 DVDD     GND CLK  invclk     Inv
x1 DVDD     GND RST net3  net1     Nand
x2 DVDD     GND net1 CLK invclk  net2     PTL
x3 DVDD     GND D invclk CLK net2     CLKInv
x4 DVDD     GND net2  net3     Inv
x5 DVDD     GND net3 CLK invclk net4    PTL
x6 DVDD     GND net4  RST net5     Nand
x7 DVDD     GND net5  invclk CLK net4     CLKInv
x8 DVDD     GND net5  out     Invv

.tran 10n 2.1u
.op
.option post
.end
```

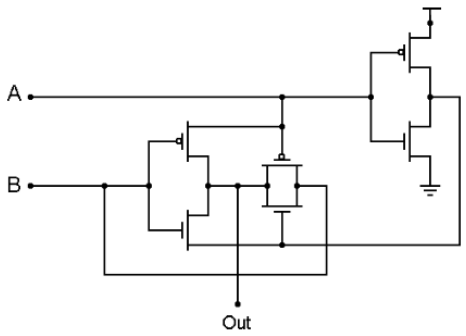
Layout 11: FA1

a. Transistor-level circuit:

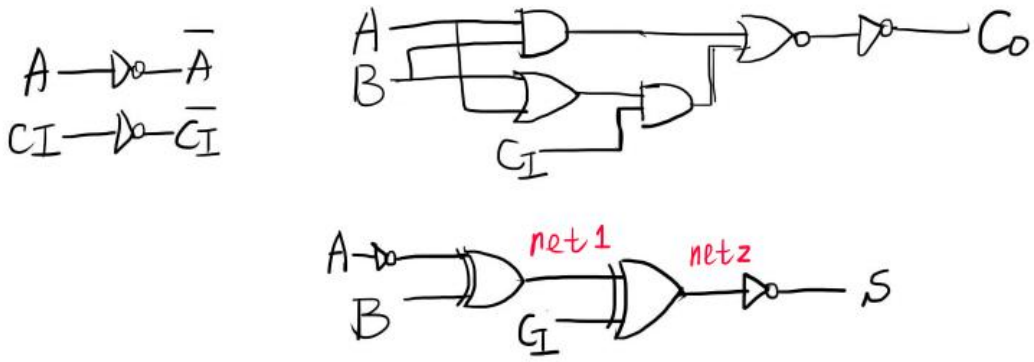


b. Gate-level circuit:

這是 A xor B:



因此 Gate-level circuit 如下:



c. Inputs and outputs:

Inputs: A, B, Ci

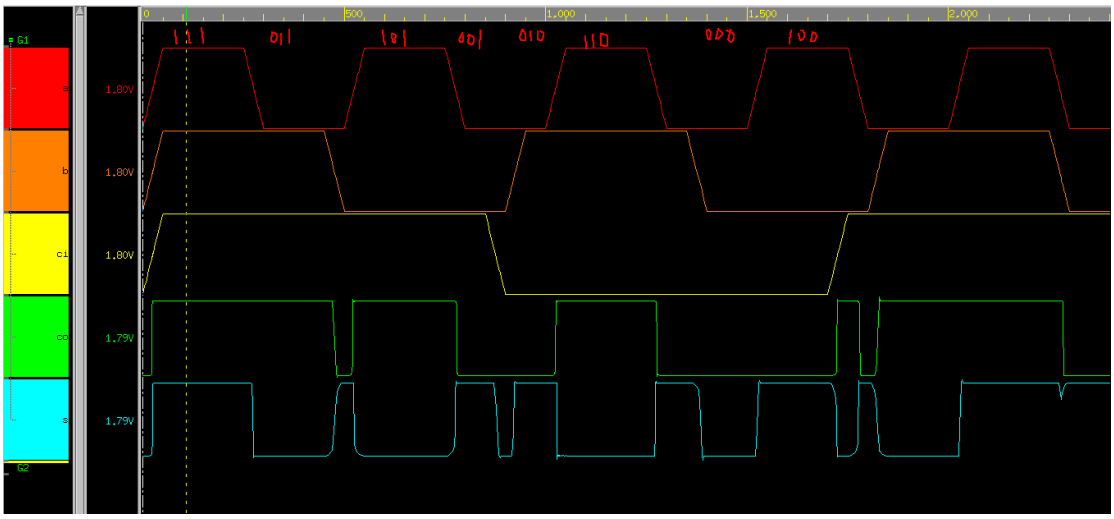
Outputs: Co, S

d. Truth table:

A	B	Ci	Co	S

0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

e. Hspice/ nWave simulation:



可以看出 8 種 input 組合，得出和 truth table 相同，此為 Full-Adder。

f. Hspice code:

```
**********************************************
.inc '90nm_bulk.l'
**********************************************
.SUBCKT Inv DVDD GND In Out
*.PININFO DVDD:I GND:I In:I Out:O
MN1 Out In GND GND NMOS l=0.1u w=0.25u m=1
MP1 Out In DVDD DVDD PMOS l=0.1u w=0.5u m=1
.ENDS
**********************************************
.SUBCKT Xor DVDD GND In In1 In2 Out
*.PININFO DVDD:I GND:I In:I In1:I In2:I Out:O
MN1 Out In1 In GND NMOS l=0.1u w=0.25u m=1
MN2 Out In  In1 GND NMOS l=0.1u w=0.25u m=1
MP1 Out In2 In DVDD PMOS l=0.1u w=0.5u m=1
MP2 Out In  In2 DVDD PMOS l=0.1u w=0.5u m=1
.ENDS
**********************************************
.SUBCKT Strange DVDD GND In1 In2 In3 Out
*.PININFO DVDD:I GND:I In1:I In2:I In3:I Out:O
MN1 X   In2 GND  GND NMOS l=0.1u w=0.25u m=1
MN2 Out In1 X    GND NMOS l=0.1u w=0.25u m=1
MN3 Y   In1 GND  GND NMOS l=0.1u w=0.25u m=1
MN4 Y   In2 GND  GND NMOS l=0.1u w=0.25u m=1
MN5 Out In3 Y    GND NMOS l=0.1u w=0.25u m=1
MP1 Z   In2 DVDD DVDD PMOS l=0.1u w=0.5u m=1
MP2 Out In1 Z    DVDD PMOS l=0.1u w=0.5u m=1
MP3 W   In1 DVDD DVDD PMOS l=0.1u w=0.5u m=1
MP4 W   In2 DVDD DVDD PMOS l=0.1u w=0.5u m=1
MP5 Out In3 W    DVDD PMOS l=0.1u w=0.5u m=1
.ENDS
**********************************************
Vdd DVDD    0   1.8
Vss GND     0   0

Vin A    0   pulse (0 1.8 0 50n 50n 0.2u 0.5u)
V1  B      0   pulse (0 1.8 0 50n 50n 0.4u 0.9u)
V2  CI   0   pulse (0 1.8 0 50n 50n 0.8u 1.7u)


x0 DVDD     GND A  invA     Inv
x1 DVDD     GND CI  invCI     Inv
x2 DVDD     GND B  invA  A  net1     Xor
x3 DVDD     GND net1  CI  invCI  net2     Xor
x4 DVDD     GND net2  S     Inv
x5 DVDD     GND A B CI  net3     Strange
x6 DVDD     GND net3  CO     Inv



.tran 10n 2.4u
.op
.option post
.end
```