

# Chapter 1

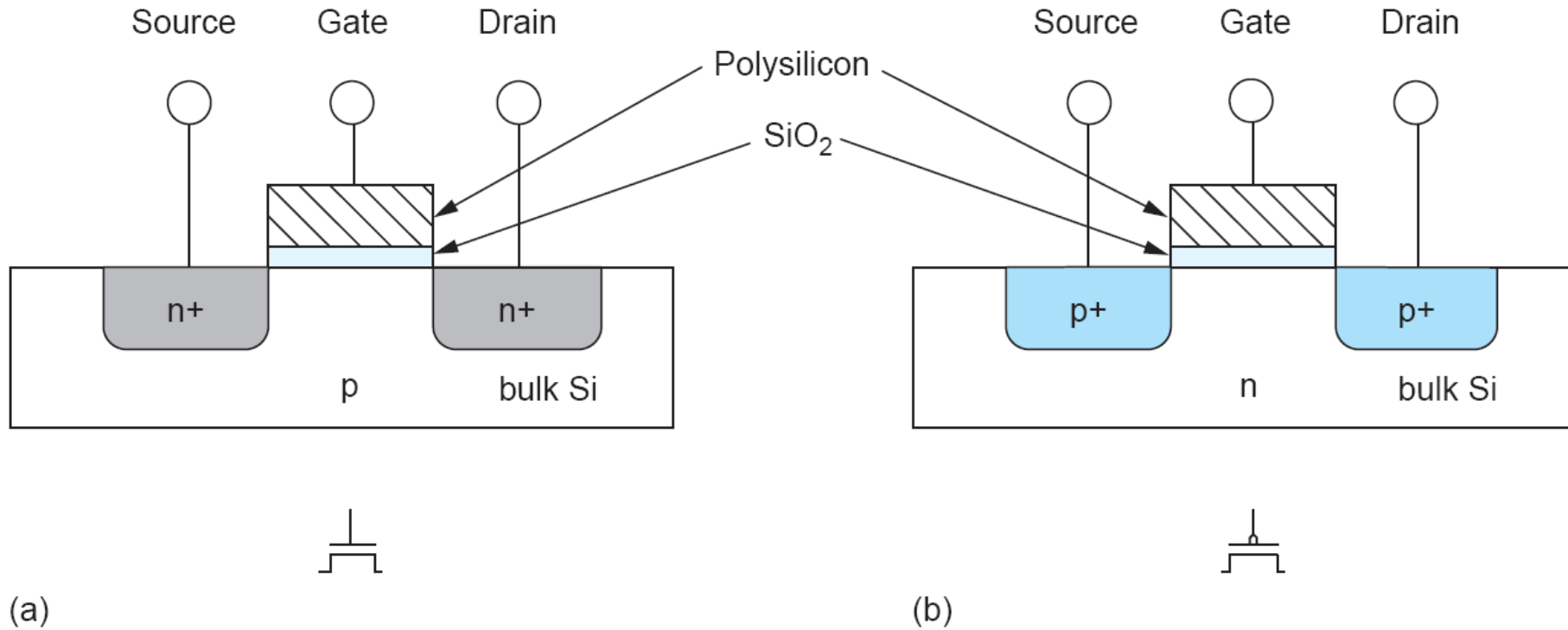
## Introduction to CMOS Circuits



闕志達

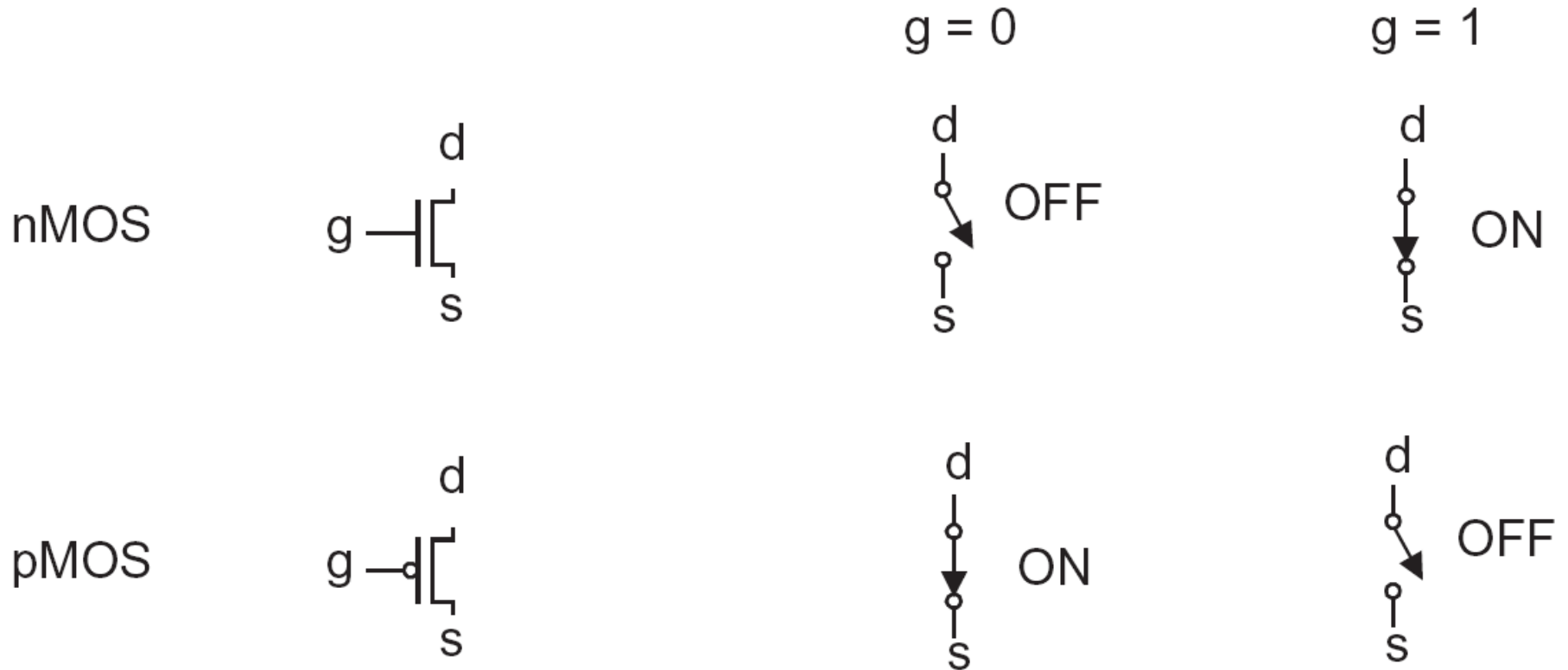
台灣大學電機系

# MOS Transistor



**FIGURE 1.9** nMOS transistor (a) and pMOS transistor (b)

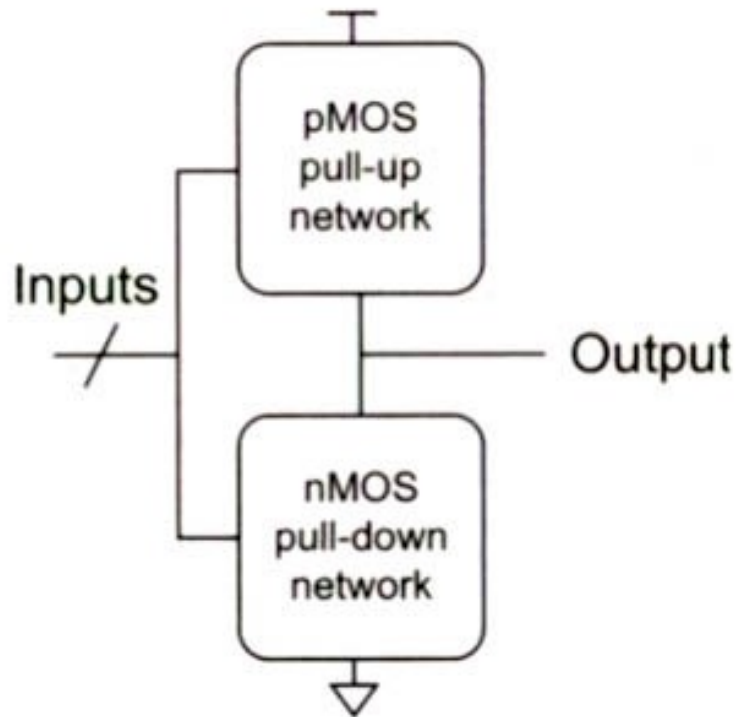
# MOS Switches



**FIGURE 1.10** Transistor symbols and switch-level models

# CMOS Static Logic

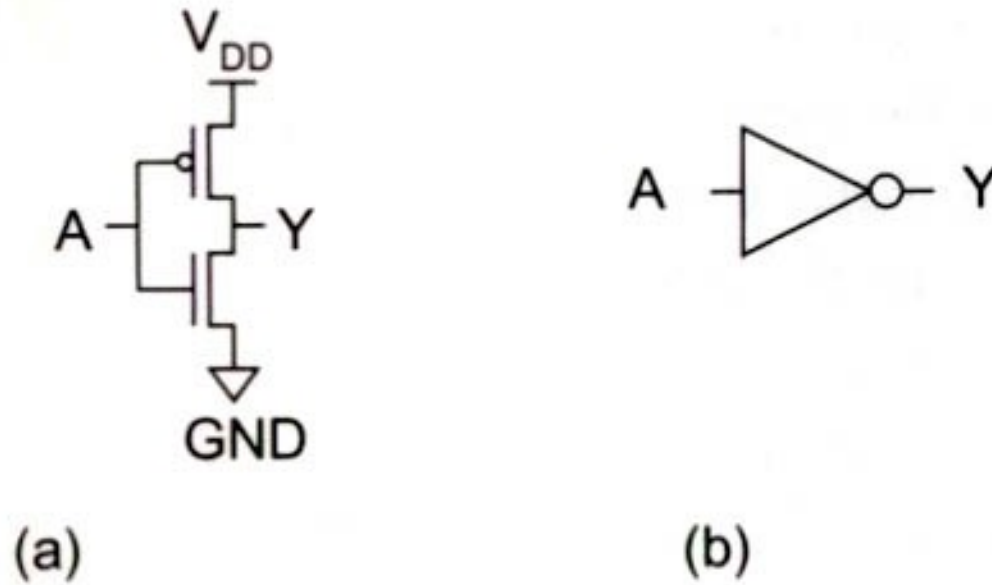
- Restored logic



**Table 1.3** Output states of CMOS logic gate

	pull-up OFF	pull-up ON
pull-down OFF	Z	1
pull-down ON	0	crowbarred (X)

# CMOS Inverter



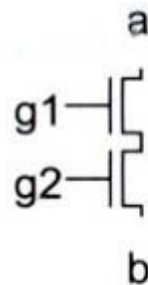
**FIGURE 1.11**

Inverter schematic

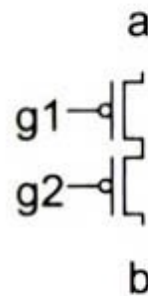
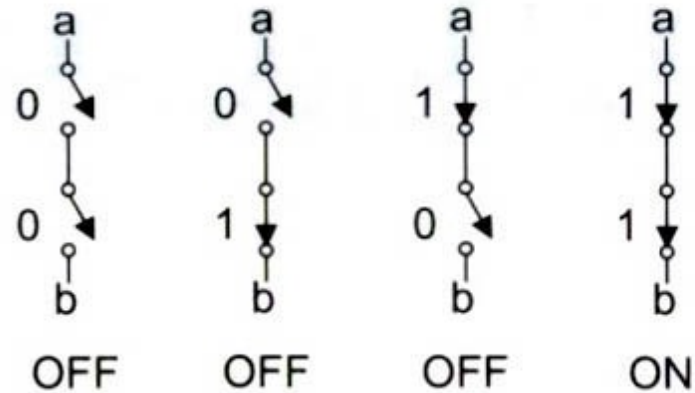
(a) and symbol

(b)  $Y = \overline{A}$

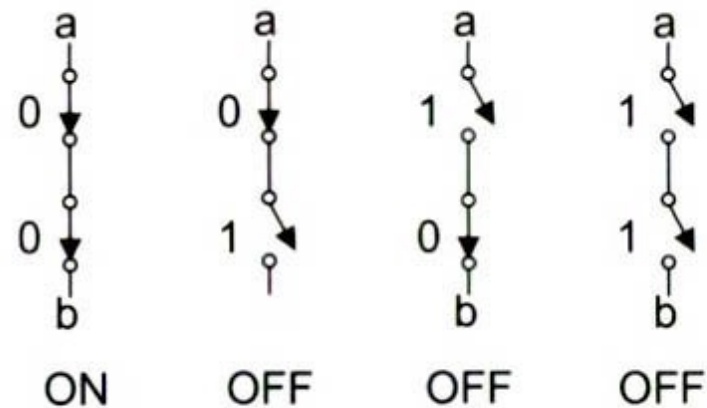
# Series Connection of Switches



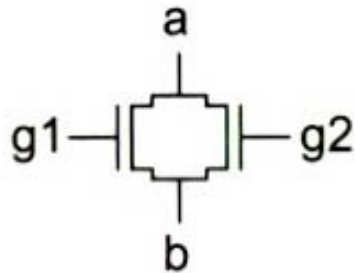
(a)



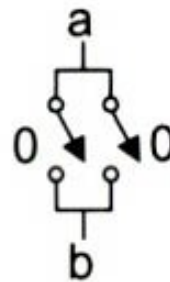
(b)



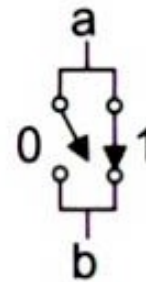
# Parallel Connection of Switches



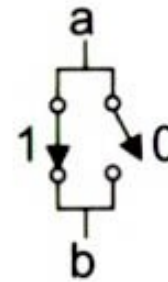
(c)



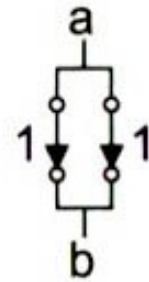
OFF



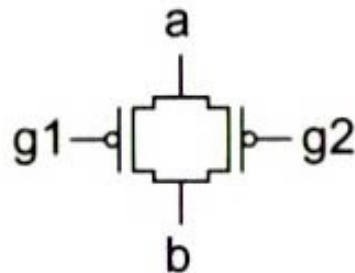
ON



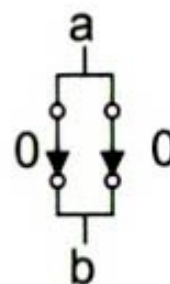
ON



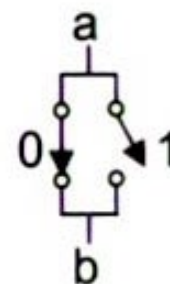
ON



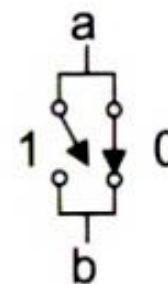
(d)



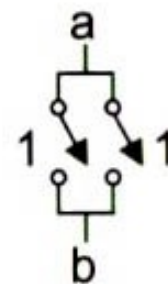
ON



ON

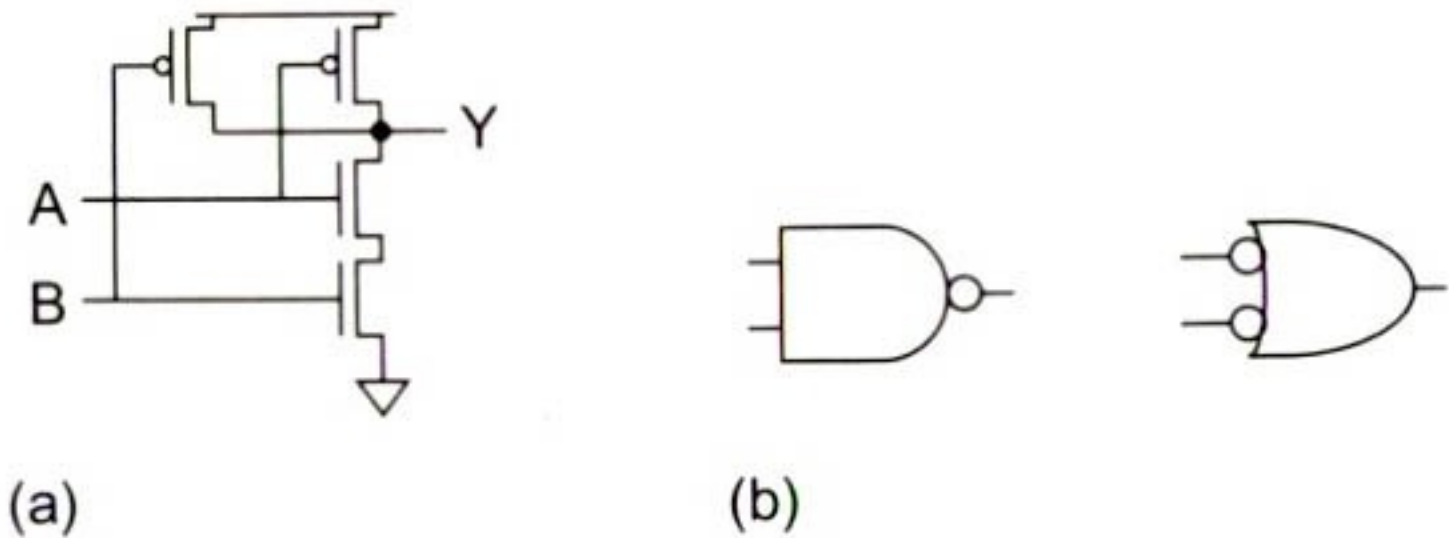


ON



OFF

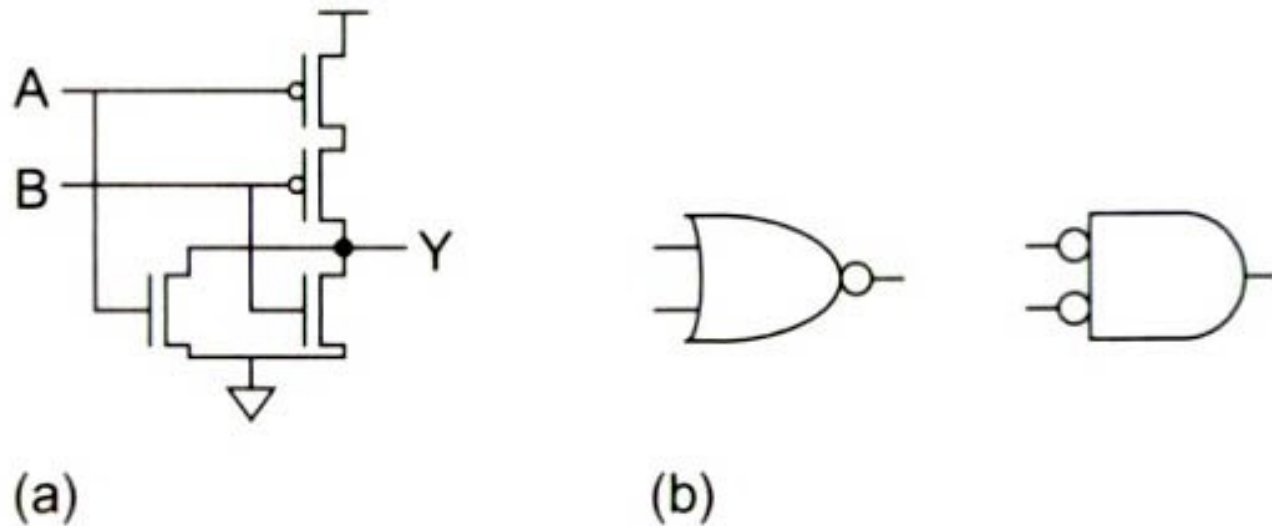
# NAND Gate



**FIGURE 1.12** 2-input NAND gate schematic (a) and symbol (b)  $Y = \overline{A \cdot B}$



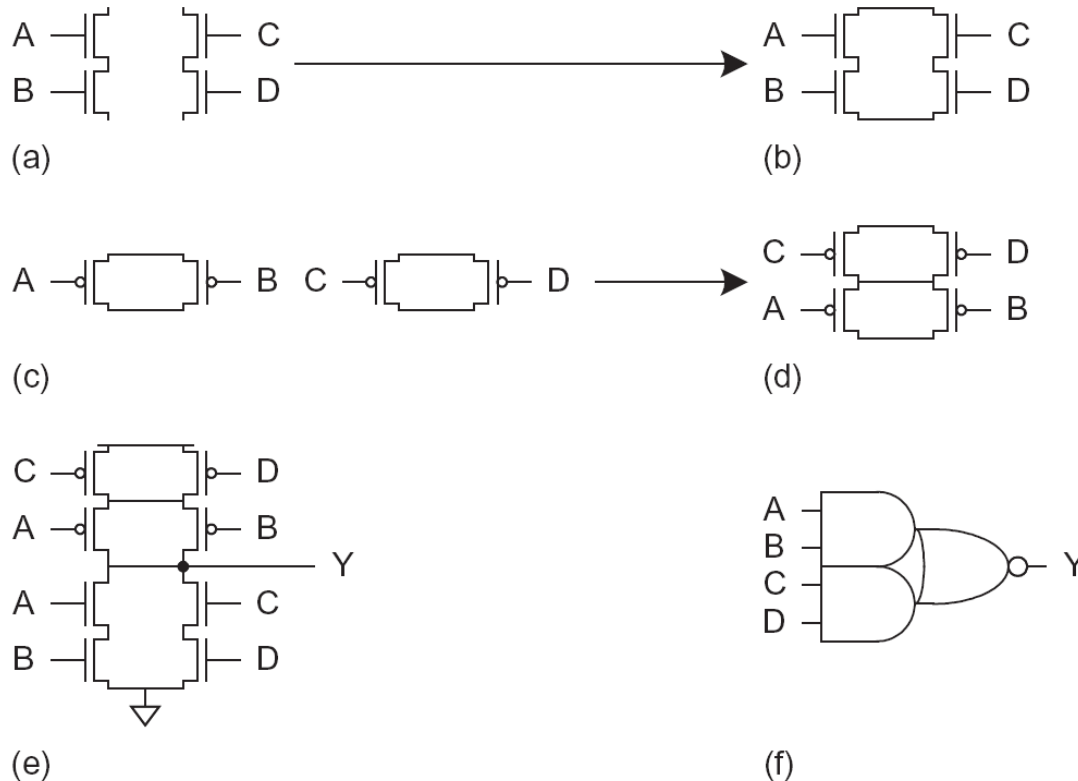
# NOR Gate



**FIGURE 1.16** 2-input NOR gate schematic (a) and symbol (b)  $Y = \overline{A + B}$

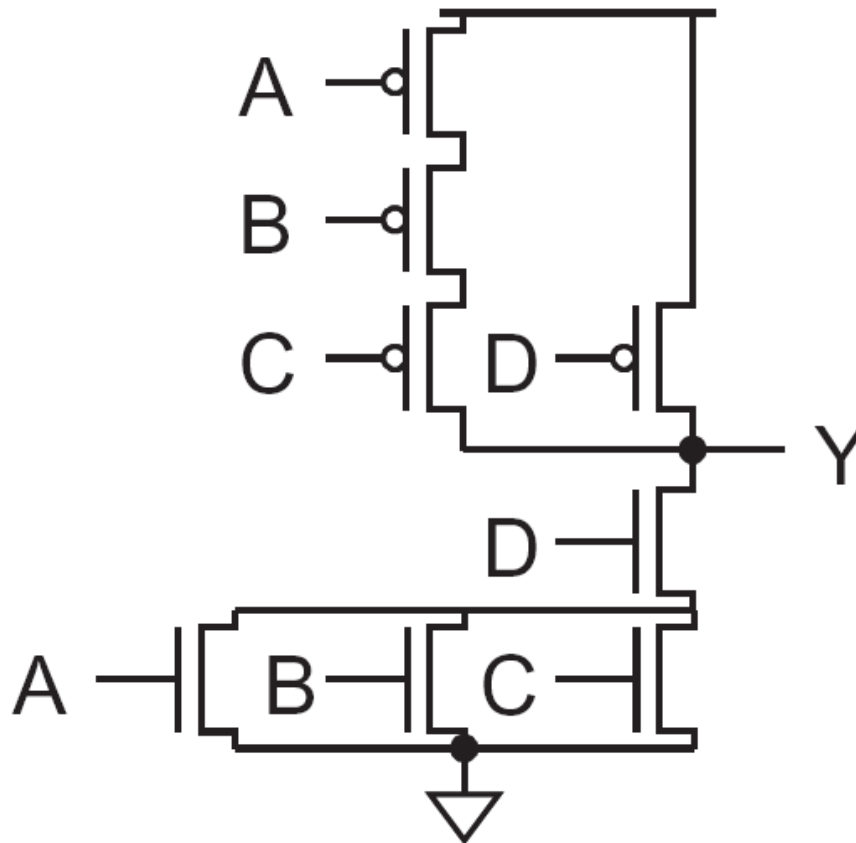
# Compound Gates

- NMOS first, AND => serial connection, OR => parallel connection
- PMOS is the dual of NMOS.
- Note that the gate has an inverting output.



**FIGURE 1.18** CMOS compound gate for function  $Y = (A \cdot B) + (C \cdot D)$

# Another Example

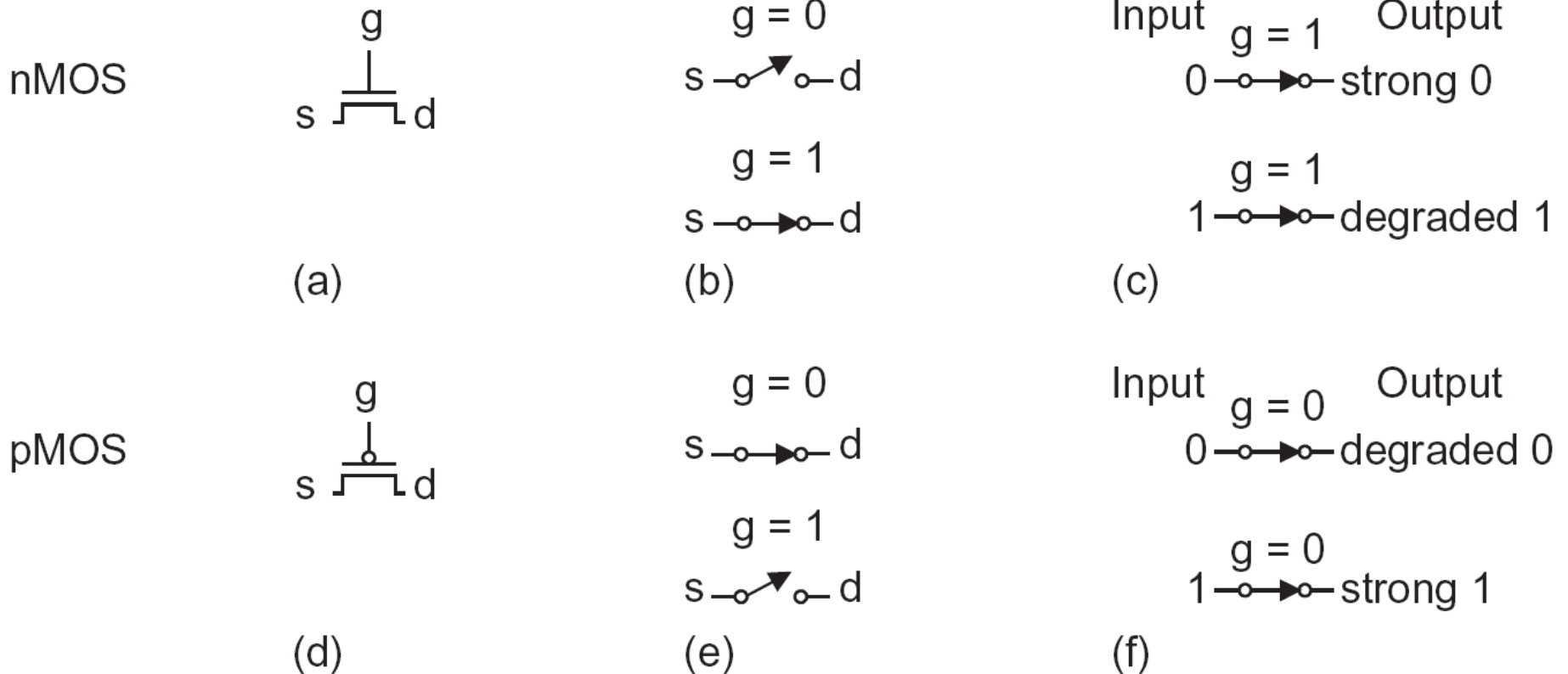


**FIGURE 1.19**

CMOS compound gate  
for function

$$Y = \overline{(A + B + C)} \cdot D$$

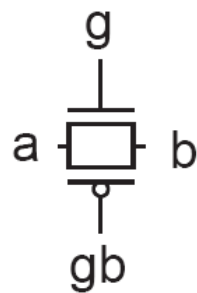
# Pass Transistors



**FIGURE 1.20** Pass transistor strong and degraded outputs

# CMOS Switch

## ■ Transmission Gate



(a)

$g = 0, gb = 1$   
 $a \rightarrow \nearrow \rightarrow b$

$g = 1, gb = 0$   
 $a \rightarrow \searrow \rightarrow b$

(b)

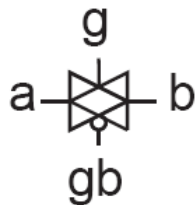
Input

Output

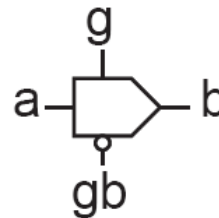
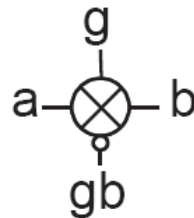
$g = 1, gb = 0$   
 $0 \rightarrow \rightarrow \text{strong } 0$

$g = 1, gb = 0$   
 $1 \rightarrow \rightarrow \text{strong } 1$

(c)



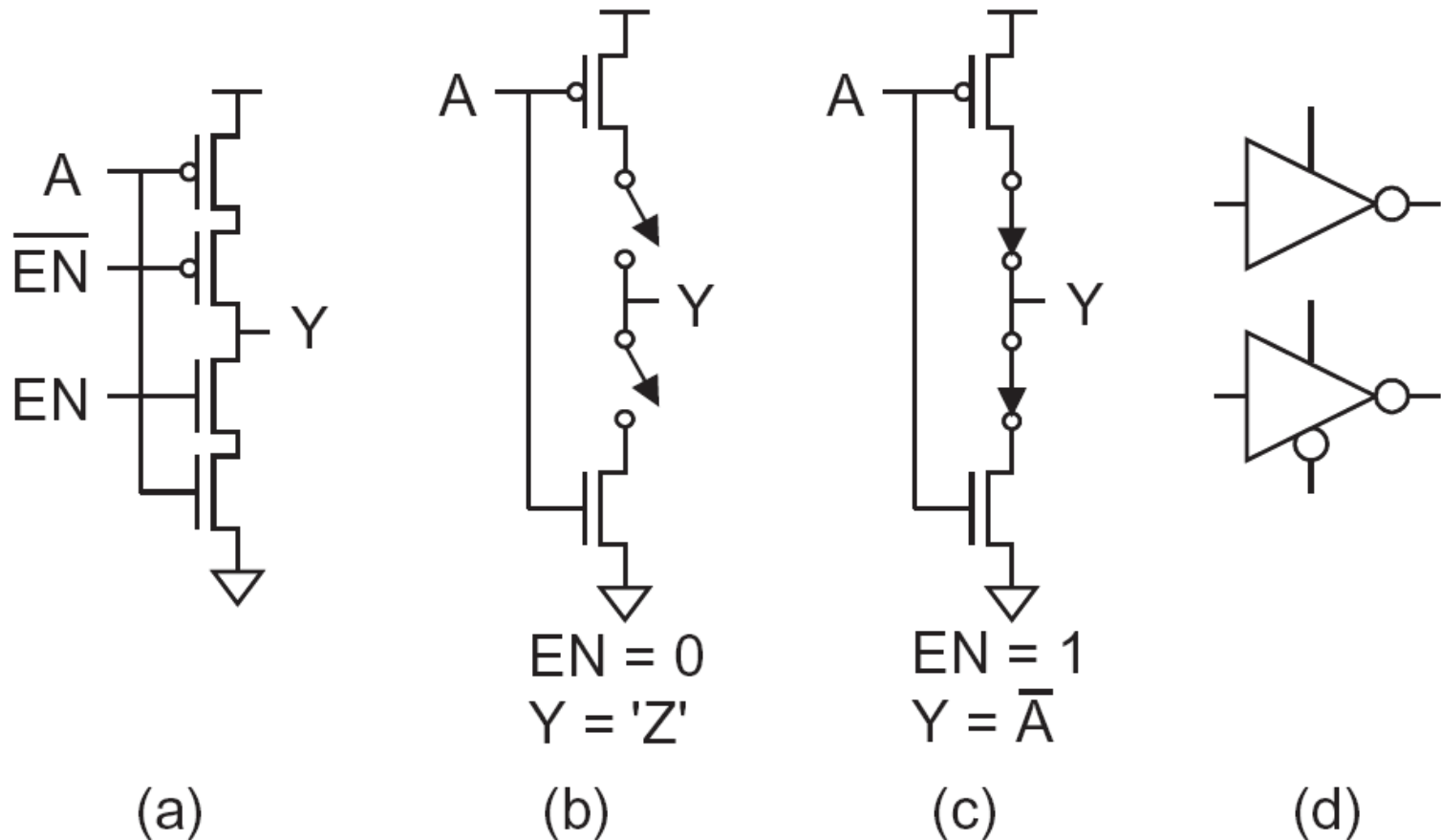
(d)



**FIGURE 1.21** Transmission gate

# Tri-state Inverter

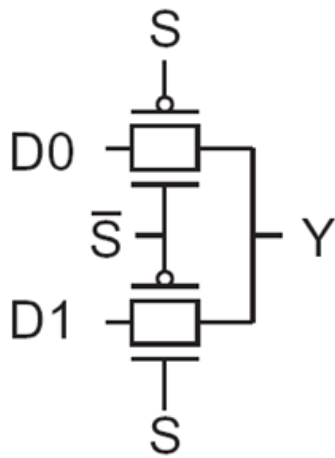
- Bus driver



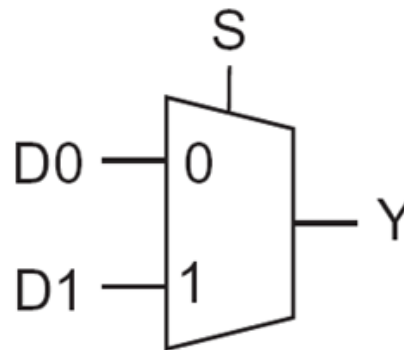
**FIGURE 1.27** Tristate Inverter

# Multiplexer

- Use transmission gates to build a 2-to-1 multiplexer.
- Note that transmission gates are "bilateral" devices, hence this multiplexer can also be looked upon as a 1-to-2 demultiplexer depending on which end is the driving (more forceful) end.



(a)

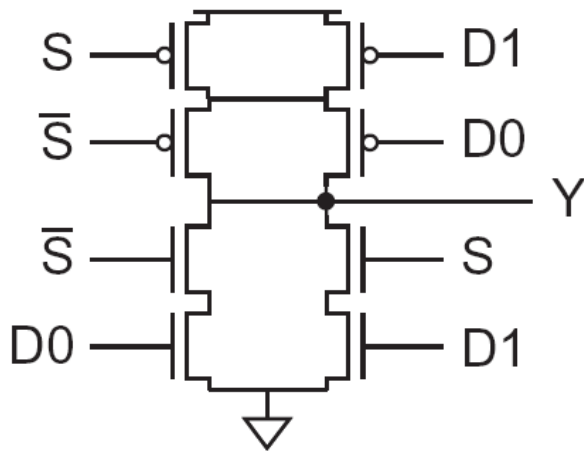


(b)

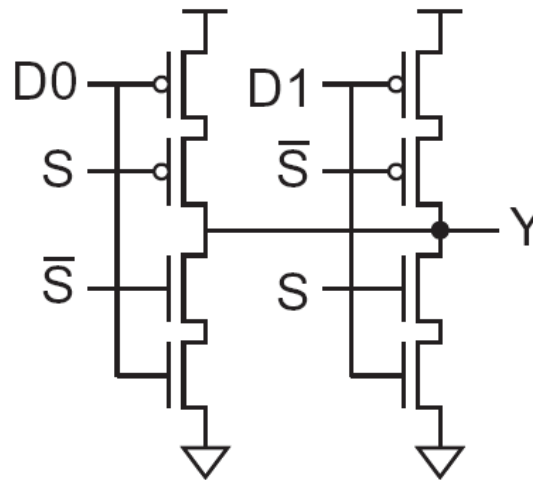
**FIGURE 1.28** Transmission gate multiplexer

# Static Inverting Multiplexer

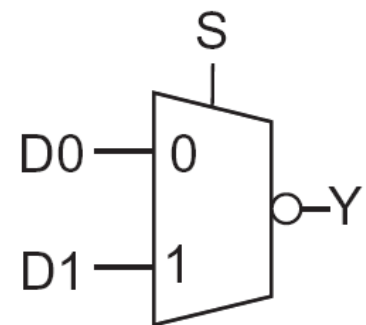
- $Y = \overline{(D0 \bullet S' + D1 \bullet S)}$



(a)



(b)



(c)

**FIGURE 1.29** Inverting multiplexer



# 4:1 Multiplexer

**FIGURE 1.30** 4:1 multiplexer

