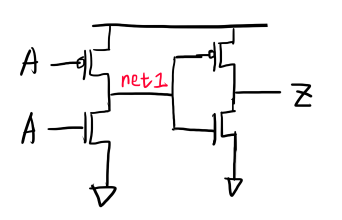
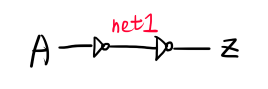
積體電路設計 hw2 b02502108 陶昇永

**Layout 8: Driver**

1. Transistor-level circuit:



1. Gate-level circuit:



1. Inputs and outputs:

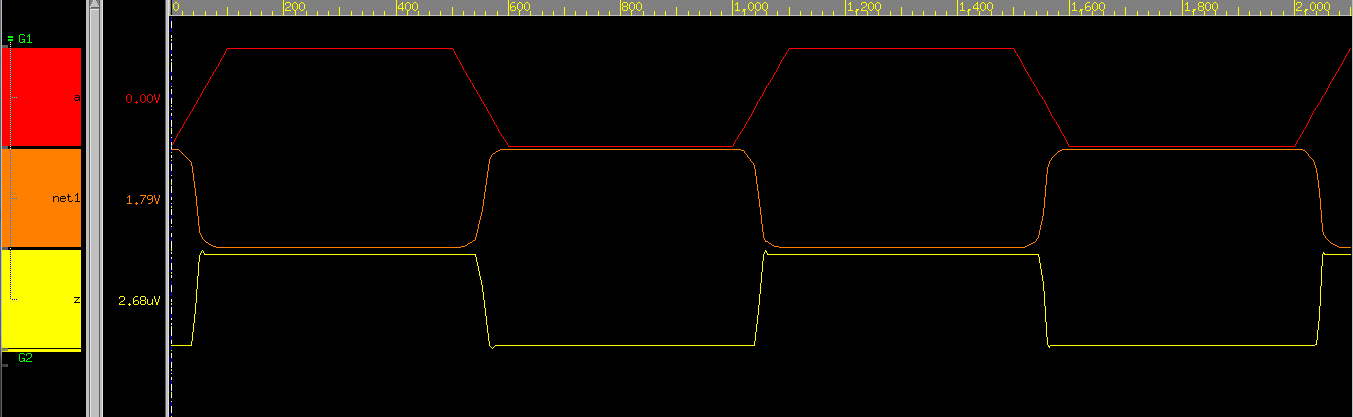
Input: A

Output: Z

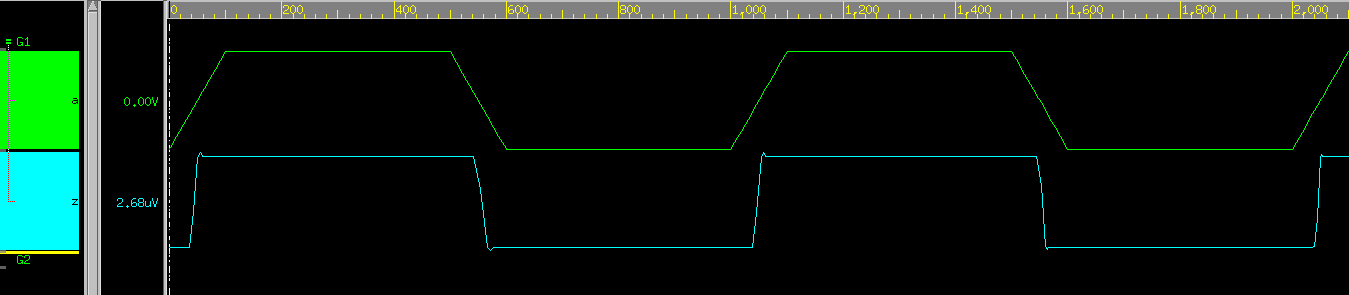
1. Truth table:

|  |  |
| --- | --- |
| A | Z |
| 0 | 0 |
| 1 | 1 |

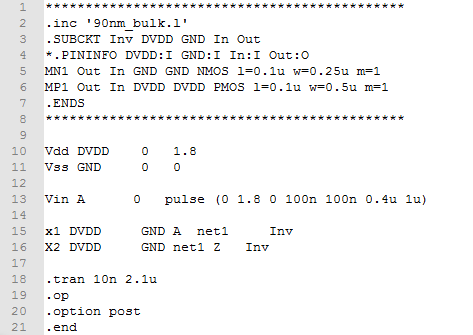
1. Hspice/ nWave simulation:



由上圖可知，Vin經過一級inverter後，信號因此0、1互換。之後再經過一級類似inverter的電路，讓0、1再次換回與input相同，因此可以當driver來使用。下圖為input與output直接比較:

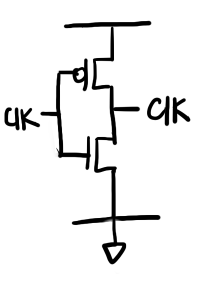


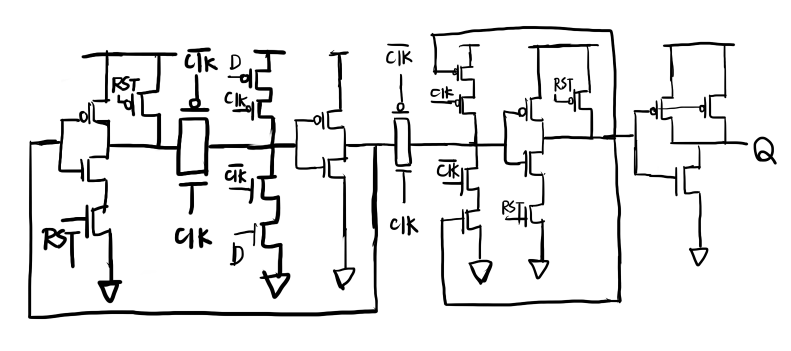
1. Hspice code:



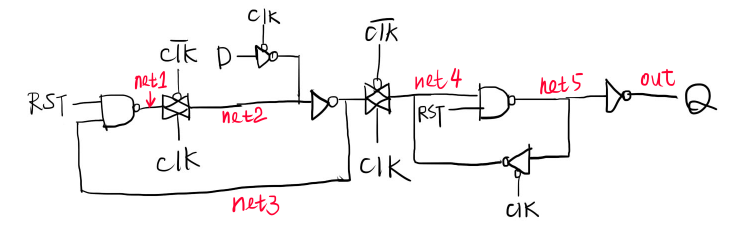
**Layout 10: FD2**

1. Transistor-level circuit:





1. Gate-level circuit:



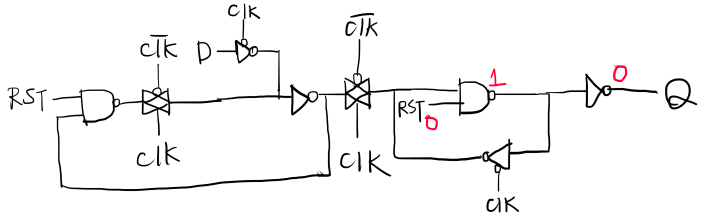
1. Inputs and outputs:

Inputs: RST, CLK, D

Output: Q

1. Truth table:

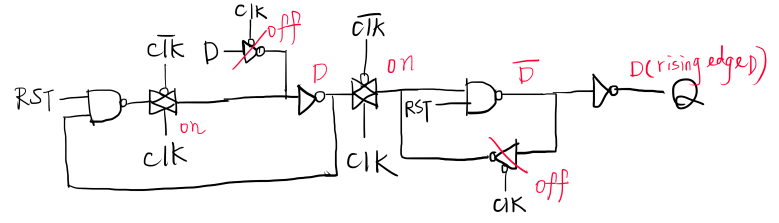
RST = 0: Q = 0



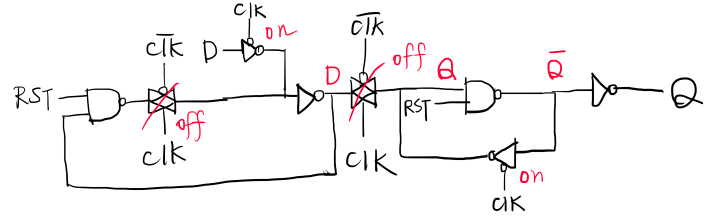
|  |  |  |
| --- | --- | --- |
| RST | D | Q |
| 0 | 0 | 0 |
| 0 | 1 | 0 |

RST = 1:

CLK on: Q = D(rising edge)

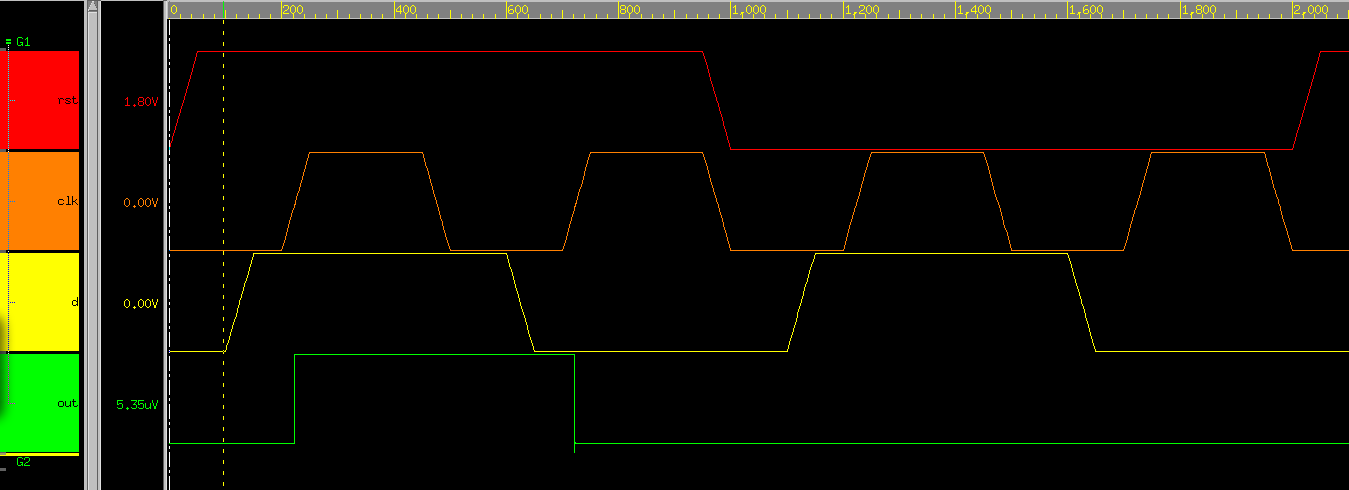


CLK off: PTL(transmission gate) off, Q keep



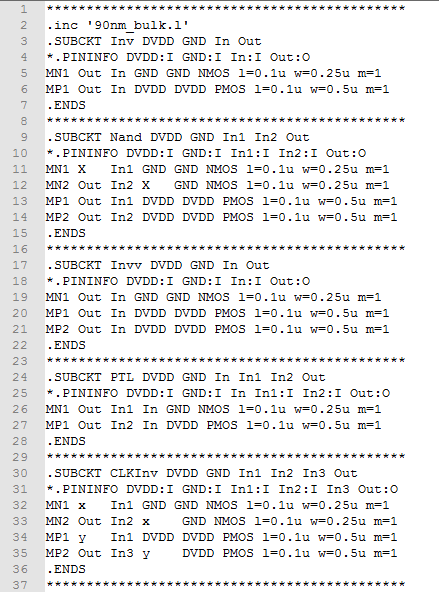
|  |  |  |  |
| --- | --- | --- | --- |
| RST | CLK | D | Q |
| 1 | ↑ | X | D |
| 1 | 除了↑以外 | X | Q0(keep value) |

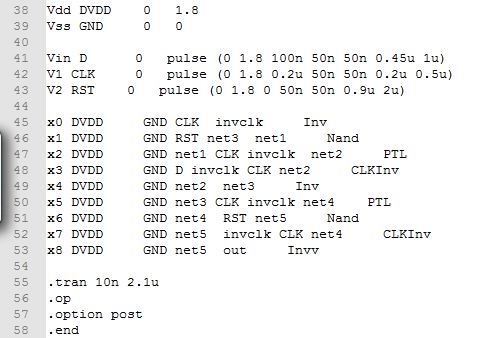
1. Hspice/ nWave simulation:



如圖所示，當RST為0時，output Q 被強制歸零，RST=1時，則看CLK，若CLK為rising edge，則output Q = D，其他時候output Q keep 原本的Q值，直到下次rising edge或RST = 0將Q歸零。此為D flip/flop。

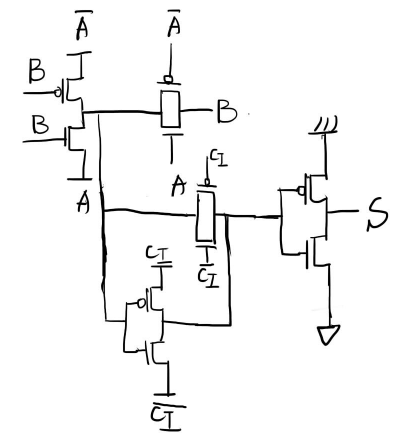
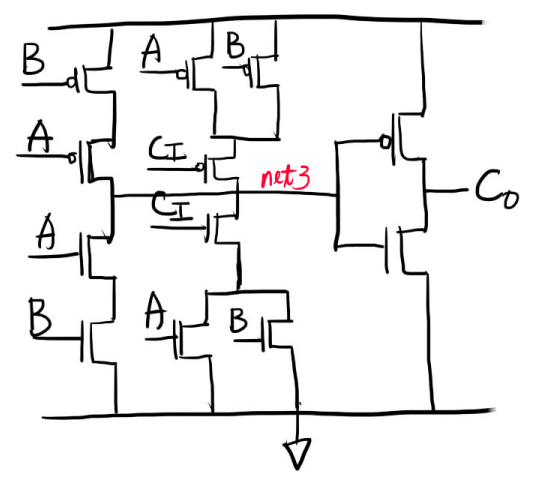
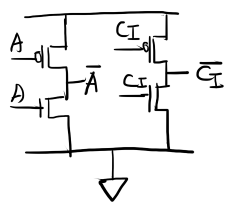
1. Hspice code:





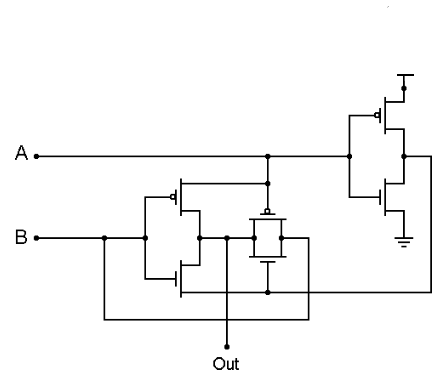
**Layout 11: FA1**

1. Transistor-level circuit:

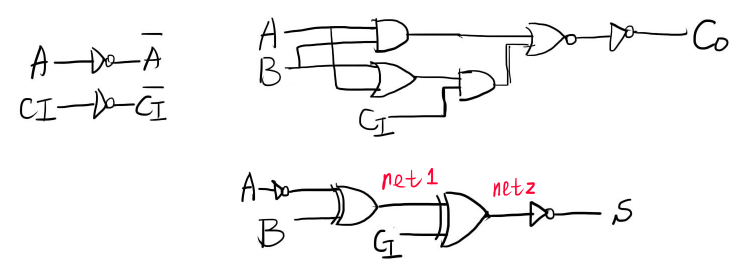


1. Gate-level circuit:

這是A xor B:



因此Gate-level circuit如下:



1. Inputs and outputs:

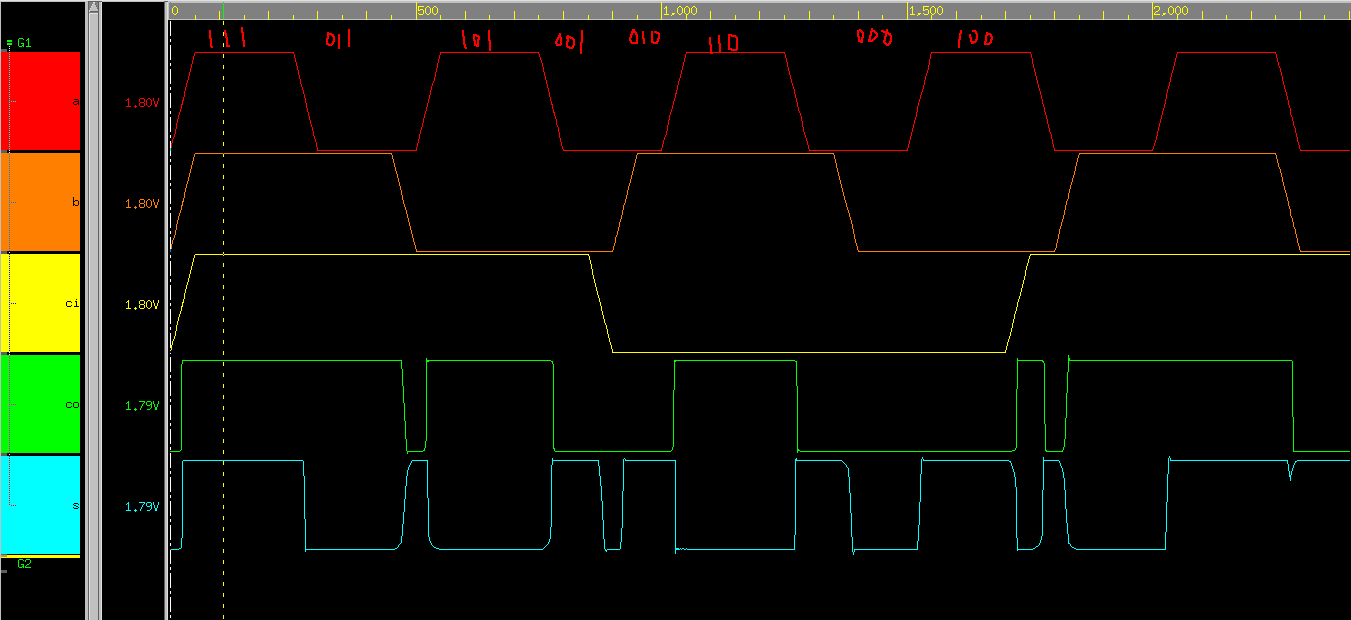
Inputs: A, B, Ci

Outputs: Co, S

1. Truth table:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | Ci | Co | S |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |

1. Hspice/ nWave simulation:



可以看出8種input組合，得出和truth table相同，此為Full-Adder。

1. Hspice code:

