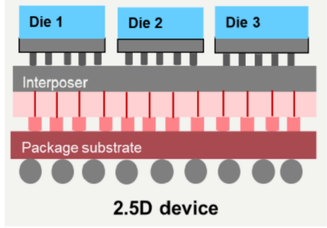
Methods for securing commercial dies in silicon substrates for heterogenous integration

ChengYu Chiu (chiu120@purdue.edu), PinChen Su(su363@purdue.edu), Takeuchi Yoshiki(ytakeuch@purdue.edu), Qiming Chai(chaiq@purdue.edu),
Co-author: Mary Vaughan, Dr. Bermel, Dr. Mohammadi
Birck Nanotechnology Center, Elmore Family School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN, USA

SCALE
SCalable Asymmetric Lifecycle Engagement
Developing the U.S. Defense Microelectronics Workforce

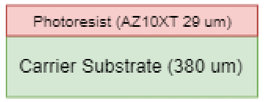
Background

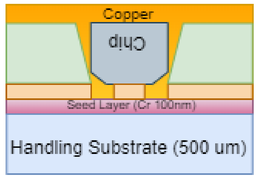
- **Heterogeneous Integration** combines diverse components and technologies into a single system for enhanced performance and functionality.
- **2.5D Heterogeneous Integration** uses an interposer (silicon, glass, or organic) to connect multiple chips side-by-side
- **Objects:** Embedding chipsets into silicon as a unified structure, covered with copper (Cu) for electromagnetic shielding, and interconnecting each unit using aluminum (Al).
- **Goal:** Enabling high-density, high-performance integration with improved interconnectivity compared to traditional planar designs.



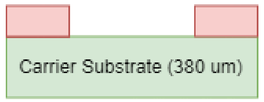
General Heterogeneous Integration [1]

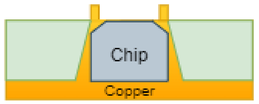
Process



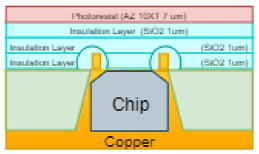


Electroplating:
- The metal seed layer serves as a cathode, enabling the vertical growth of copper, which fills the gap and secures the chiplets in place.

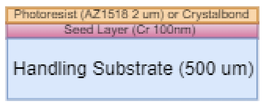




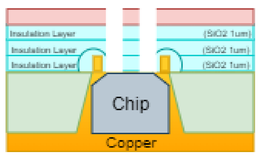
Carrier Wafer:
- 380um Silicon through-etched wafer patterned with 30um of AZ10XT.



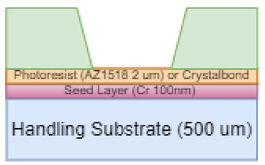
SiO2 Deposition:
- After the handling wafer has been removed, an insulating layer is added to prevent shorting,

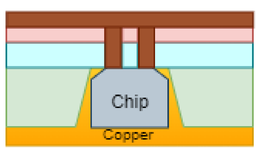


Handling Wafer:
- 500um Silicon wafer plated with 100um Chromium and 200um Au.

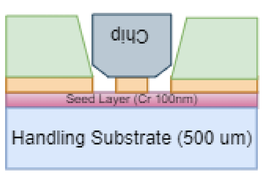


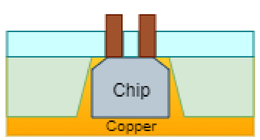
SiO2 Etch:
- Patterning and etching through the insulator to expose contacts.



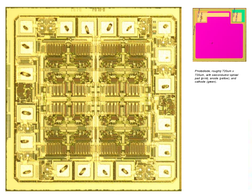


Metallization
- interconnects are created between the dies with aluminum.





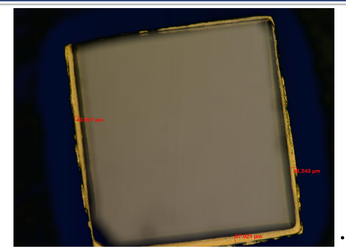
Embedded Dies:
- A photodiode is a photovoltaic device that generates a current when its optical component encounters light.
- The D-latch serves as a logic memory-bank to store the value captured by the photodiode



Results

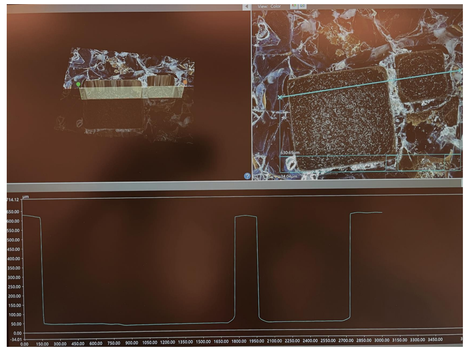
Lithography:

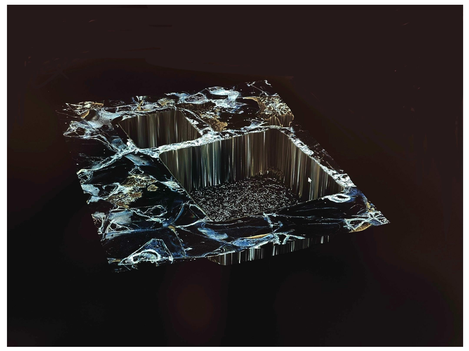
Etching:
- Utilized Tergeo plasma cleaning process to remove photoresist residue, resulting in an improved etch profile on the edges.
- Using DSE etcher successfully etched through a 380 μm thick substrate in Trial 2 and 4 with two different recipes, achieving sidewalls with less than 8° and 4° deviation from vertical, respectively.



Handling wafer
- We utilized physical vapor deposition (PVD) CHA E-beam Evaporator to deposit a 100 nm chromium (Cr) and a 200 nm gold (Au) layer on the silicon substrate.
- Compared to Trail 1 just 100 nm Cr seed layer, the Cr layer on Trail 4 promotes adhesion between the Au and the substrate, while the Au layer prevents the formation of an oxidation layer on top.

- Trial 4 with 100nm of Cr and 200nm of Au handling wafer





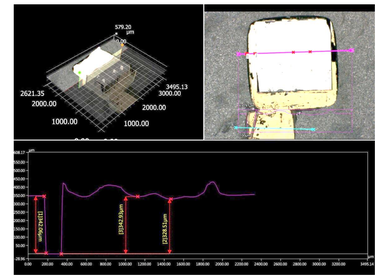
- Trial 1: Cr seed layer – Top layer of Cr oxidized, and very little Cu deposited.

Step	Time(s)	Pressure	C4F8(sccm)	SF6(sccm)	Ar(sccm)	RF2(w)	RF3
Gas Stabilization	20	20		75	30	0	0 - Auto
Ignite	5	20		75	30	100	1500W-4000
Ignite 2	5	25		75	30	100	1500W-Hold
Dep	2	25	150		30	5	2000W-Hold
Etch A	1.9	40		150	30	50	2000W-Hold
Etch B	2	60		150	30	5	2500W-Hold

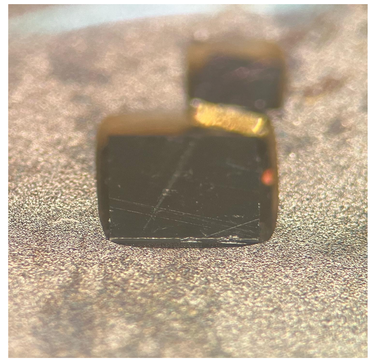
- This Bosch-process-based recipe alternates C4F8 deposition and SF6 etching, using precise RF power and pressure control to achieve high-aspect-ratio, anisotropic silicon etching with smooth vertical sidewalls.

- Etch recipe with 10um/min etch rate

Adhesive improvement:
- AZ1518 -> AZ10xt
  More time to attach the chiplets
- Crystal bond 555 (water soluble) -> Crystal bond 595
  Preventing chiplets from detaching in the electroplating bath
- Place the chiplets first then attach the handling wafer

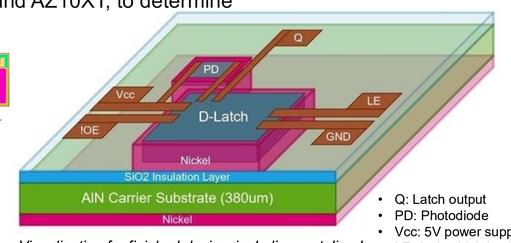


- Trial 1 electroplating result



- Copper deposited in the carrier substrate

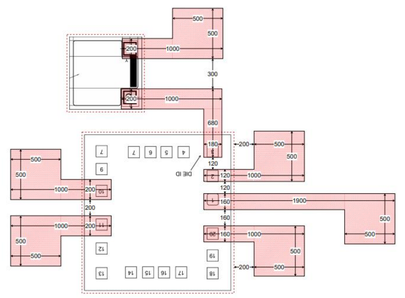
Electroplating:
- Using the Iko Jr. Electroplater, the applied current setting is critical for balancing speed and quality.
- Trial 1: Cr seed layer – Top layer of Cr oxidized, and very little Cu deposited.
- Trial 2: Cr seed layer – Slightly improved deposition rate, PD chiplet detached during plating.
- Trial 3: 15nm Cr and 200nm Au – Chiplets detached from handling wafer, but an improvement was seen in deposition rate.



Visualization for finished device, including metalized interconnects and pads.

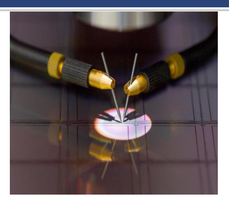
- Q: Latch output
- PD: Photodiode
- Vcc: 5V power supple
- LE: Active high latch enable
- !OE: Active low output enable

Metallization:
- After handling wafer has been removed, insulating layer is added to prevent shorting.
- Patterning and etching expose contacts and interconnects created between the dies with aluminum.
- Created with KLayout



Future Goals

- Enhance corner profile and consistency in etching process for improved outcomes.
- Investigate various backfilling techniques while maintaining a primary focus on electroplating.
- Evaluate the adhesion properties of different materials, specifically comparing Crystal Bond and AZ10XT, to determine the optimal choice.`



[2] Wafer probing system

Acknowledgements

Thank you to Dr. Bermel, Dr. Mohammadi, Dr. Chen, and Birck staff for the continual support of this project. We appreciate the opportunity to use the Birck Nanotechnology Center facilities, including the cleanroom. Also, thank you to Vertically Integrated Projects for providing undergraduates the opportunity to dive deeper into the concepts we learn in class.

[1] Shenzhen QYC CO, LTD
[2] Thermo Fisher Scientific 2023

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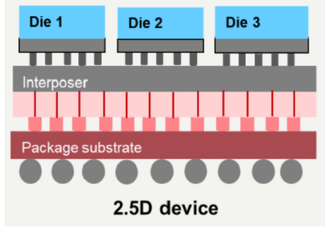
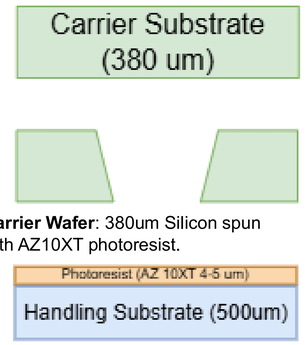
Background

- **Heterogeneous Integration** allows for separately manufactured chips and passive components to be packaged together into a single device, improving performance and scalability.
- **2.5D Heterogeneous Integration** uses a single interposer to combine chips side-by-side.
- **Objects:** Chips are embedded into our silicon interposer and electrically interconnected with aluminum. Copper covers the chips for electromagnetic shielding.
- **Goal:** Implementing improved density, performance, and interconnectivity for applications in low-orbit satellites.



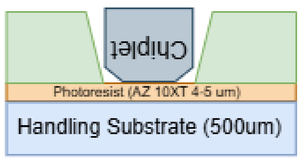
General Heterogeneous Integration [1]

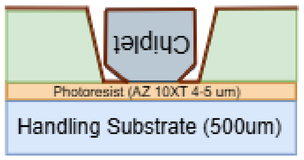
Process

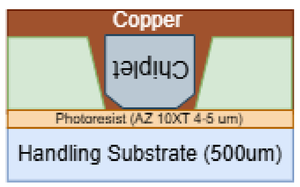


Carrier Wafer: 380um Silicon spun with AZ10XT photoresist.

Deposition:
Deposit a 100nm seed layer of Cu







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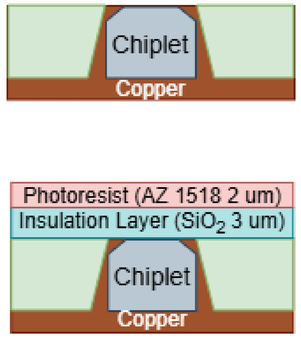

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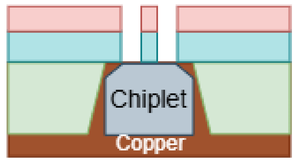

SiO2 Etch:
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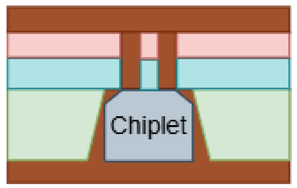

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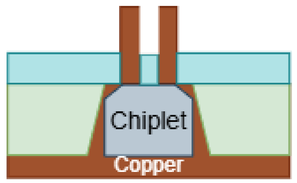

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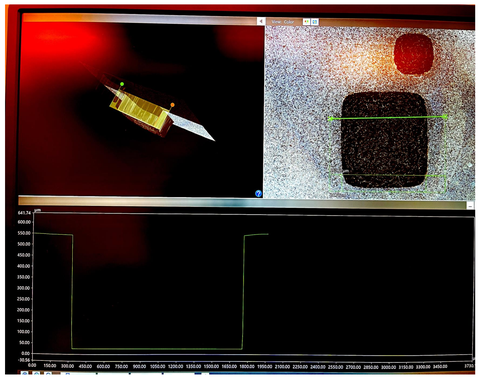

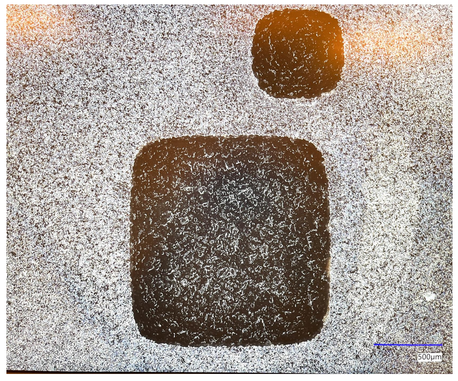

- Trial 2: surface of carrier wafer - no cracking due to high temperature

Step	Time(s)	Pressure	C4F8(sccm)	SF6(sccm)	Ar(sccm)	RF2(w)	RF3
Gas Stabilization	20	20		75	30	0	0 - Auto
Ignite	5	20		75	30	100	1500W-4000
Ignite 2	5	25		75	30	100	1500W-Hold
Dep	2	25	150		30	5	2000W-Hold
Etch A	1.9	40		150	30	50	2000W-Hold
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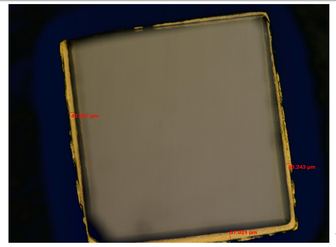
- This Bosch-process-based recipe alternates C4F8 deposition and SF6 etching, using precise RF power and pressure control to achieve high-aspect-ratio, anisotropic silicon etching with smooth vertical sidewalls.
- Etch recipe with 10um/min etch rate



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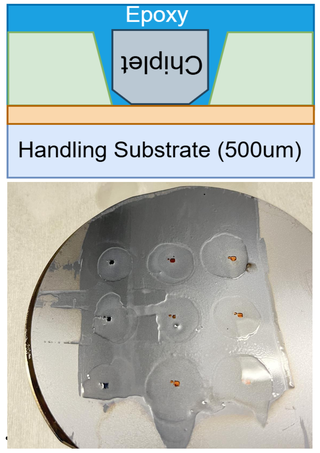
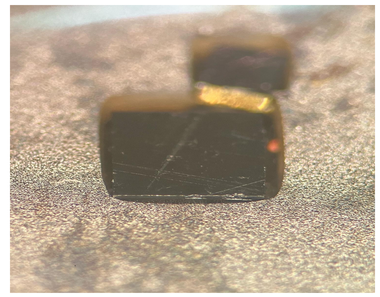
- Compared to Trail 1 just 100 nm Cr seed layer, the Cr layer on Trail 4 promotes adhesion between the Au and the substrate, while the Au layer prevents the formation of an oxidation layer on top.
- Trial 4 with 100nm of Cr and 200nm of Au handling wafer

Etching Recipe improvement:
- AZ1518 -> AZ10XT
- Crystal bond 555 -> 595
- Etching improvement: 10min to 5min cycles, preventing photoresist from cracking.
- Used crystal bond leaks from etched hole.



Epoxy Backfilling:
- Spread the epoxy on the wafer as adhesive.
- Removes the need for PVD + electroplating, due to high failure rates of such.



- Trial 1 electroplating result

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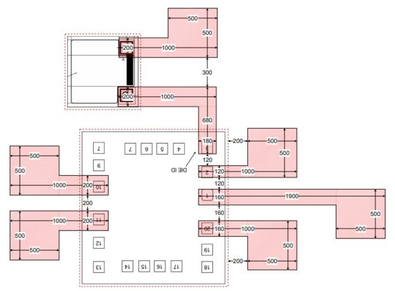
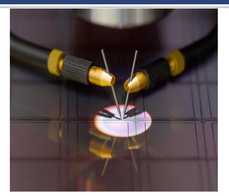


Future Goals

- Experiment with backfilling methods and disussing multi-purposing potentials of material around chiplets.
- Analyze the adhesion characteristics of various materials to identify the most effective option.
- Complete the construction of a course website that accelerates the pre-experiment trainings of new students, and allow faculty and external personnels to understand the course better.



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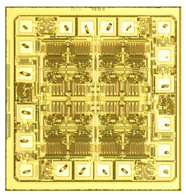

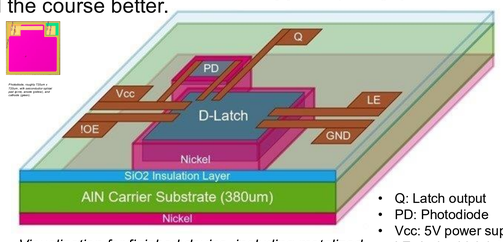

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- !OE: Active low output enable

Acknowledgements

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[1] Shenzhen QYC CO, LTD
[2] Thermo Fisher Scientific 2023