

# Multichannel EEG-Based Brain-Computer Interface for Real-Time Mouse Control

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## Design Document



Figure 0.0.1: Picture of EEG and BCI

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## Revision Log

Date	Revision	Changes
02/02/2025	v0.1	Covered Design Document 1 Assignment Requirements
03/16/2025	v0.2	Covered Design Document 2 Assignment Requirements
04/20/2025	v0.3	Covered Design Document 3 Assignment Requirements Glossary Page, Section 3.1, 3.4, 3.5, and 6 were updated.
05/03/2025	v1.0	The Final Design Document Most paragraphs were reviewed and/ or revised for the final submission.

Table 1: Revision Log

## Glossary

- **ADC** Analog-to-Digital Converter, a device that converts analog EEG signals into digital data for processing by a microcontroller.
- **BCI** Brain-Computer Interface, a system that enables direct communication between the brain and an external device by translating neural signals into commands.
- **BLE** Bluetooth Low Energy, a wireless communication protocol used for transmitting EEG data with low power consumption.
- **Channels (EEG)** Parallel pathways in the EEG circuit, each processing signals from a specific electrode pair, enabling multi-point brain activity measurement (e.g., four channels for capturing distinct scalp regions).
- **CMRR** Common-Mode Rejection Ratio, a measure of an amplifier's ability to reject noise common to both input signals, critical for EEG signal clarity.
- **EEG** Electroencephalography, a non-invasive method to record electrical activity of the brain using electrodes placed on the scalp.
- **FFT** Fast Fourier Transform, an algorithm used to convert time-domain EEG signals into frequency-domain representations for analysis.
- **ICA** Independent Component Analysis, a computational method to separate mixed EEG signals into independent sources, isolating artifacts like blinks.
- **Microcontroller Subsection** The area of the PCB dedicated to the STM32H723ZG microcontroller, handling EEG signal digitization and communication with the PC via UART and Bluetooth.
- **PCB** Printed Circuit Board, a physical board that connects electronic components using conductive tracks, used to integrate the EEG circuit, power supply, and microcontroller subsystems.
- **PCB Layout** The physical arrangement of components, traces, and connections on a printed circuit board, designed to implement the electrical schematics while optimizing space, signal integrity, and manufacturability.
- **Power Supply (EEG System)** The circuit that converts a 14.4V battery input into dual  $\pm 5V$  outputs to power the EEG circuit and instrumentation amplifier, ensuring stable operation for signal acquisition.
- **SSVEP** Steady-State Visually Evoked Potential, a brain response elicited by visual stimuli flickering at specific frequencies, measurable via EEG.

- **Traces** Conductive pathways on a PCB that connect components, forming the electrical circuits defined by the schematic, critical for signal transmission and power distribution.
- **UART** Universal Asynchronous Receiver/Transmitter, a serial communication protocol for data exchange between the microcontroller and a PC.

# 1 Introduction

## 1.1 Executive Description

We are designing and developing a brain-computer interface (BCI) using EEG technology to assist individuals with physical disabilities in interacting with computers more easily. The system works by placing electrodes on the user's head to measure brain activity, specifically detecting voltage fluctuations associated with sensory-motor functions. These signals are then processed by a microcontroller, which runs advanced algorithms to interpret 2D mouse movements and button clicks based on the user's intent.

By seamlessly translating brain activity into real-time computer commands, our BCI system eliminates the need for traditional input devices, allowing users to navigate, click, and interact hands-free. This technology not only enhances accessibility for individuals with limited mobility but also restores independence and control, enabling them to work, communicate, and engage with digital environments effortlessly. Through this innovation, we aim to bridge the gap between human cognition and technology, making computer interaction more inclusive and intuitive.

## 1.2 User Story

Tom has always been passionate about technology, but after a quadriplegia, everything changed. Without the ability to use a keyboard or mouse, tasks he once loved coding, browsing, and staying connected and it became frustrating and impossible. He felt stuck, dependent on others, and disconnected from the digital world.

Sam, on the other hand, has no physical limitations, but he's always looking for new ways to interact with technology. Gaming with a keyboard and mouse started to feel repetitive so he wanted something more immersive and intuitive.

Thanks to our brain-computer interface (BCI) system, both Tom and Sam have discovered a new way to use their computers—with their minds. EEG technology reads brain signals and translates them into real-time commands. Tom is now coding and communicating freely, while Sam experiences gaming like never before. Whether for accessibility or entertainment, our project is redefining how people interact with technology, making it more inclusive, engaging, and futuristic.

## 2 Design Requirements

### 2.1 Requirements

1. **Wearable System** The system must be utilizing a **comfortable sports headband** to securely position four active wet electrodes (Fp1, Fp2, O1, O2, per 10-20 system) with conductive paste and a reference electrode (earlobe), ease of use, and consistent scalp contact for stable signal acquisition.
2. **EEG Signal Acquisition and Amplification** The system must include **four EEG channels** (Fp1, Fp2 for blink detection; O1, O2 for SSVEP-based cursor movement), each using an AD620AN instrumentation amplifier with a **minimum gain of 20** and a potentiometer adjustable between 10 and 10k  $\Omega$  to amplify differential signals (active vs. reference). A potentiometer must control the gain of the two AD620AN instrumentation amplifiers at once to ensure the gain consistency for two channels.
3. **System Performance** The system must achieve:
  - **Response Time:**  $<1$  second for blink detection and XY cursor movements, providing a seamless real-time experience.
  - **Blink Detection Accuracy:**  $\geq 90\%$  for reliable selection.
  - **XY Cursor Movement Accuracy:**  $\geq 80\%$  for smooth navigation, noting optimization is ongoing due to electrode contact and noise issues.
4. **Power Supply** The system must be **battery-powered**, delivering  $\pm 5V$  (via LM7805 and LM7905 regulators) with a battery voltage  $>5V$  under load and  $>60\%$  efficiency, supporting dual-supply op-amps and portability.
5. **Signal Processing and Filtering** The system must include:
  - A **60-Hz notch filter** (center at 60 Hz,  $\pm 10$  Hz) to reject power line noise.
  - **25-Hz and 50-Hz low-pass filters** (3rd-order Bessel, -3 dB at 25 Hz and 50 Hz) to pass low-frequency EEG signals (5–10 Hz).
6. **Data Transmission** The system must **wirelessly transmit four EEG channels** to a computer via a USART interface, ensuring reliable real-time data transfer for processing and control.
7. **User Functionality** The system must enable **real-time blink detection** and **mouse movement** to assist individuals with physical disabilities (e.g., paralysis, limited hand mobility) in communicating and interacting with a computer, enhancing accessibility and independence.

## **2.2 Factors influencing requirements**

### **2.2.1 Public Health, Safety, and Welfare**

1. The system must be **non-invasive, comfortable, and safe** for long-term use, ensuring that EEG electrodes and wearable components do not cause discomfort or health risks.
2. By enabling **hands-free computer interaction**, the system enhances **accessibility and independence** for individuals with physical disabilities.

### **2.2.2 Global Factors**

1. The system should be **adaptable for users worldwide**, addressing diverse disabilities and preferences to maximize accessibility.
2. It must comply with **international safety and medical standards** to ensure legal and safe global distribution.

### **2.2.3 Cultural Factors**

1. Different cultures have varying levels of **acceptance of assistive technology**, requiring awareness campaigns to encourage adoption.
2. The system should support **multiple languages and customizable interfaces**, making it user-friendly for people from different cultural backgrounds.

### **2.2.4 Social Factors**

1. The project aims to **bridge the digital accessibility gap**, allowing individuals with disabilities to **work, communicate, and engage with technology independently**.
2. **User training and support materials** (such as tutorials and customer assistance) should be provided to help users integrate the system into their daily lives.

### **2.2.5 Environmental Factors**

1. The hardware should use **sustainable and recyclable materials** to minimize environmental impact.
2. The system should be **energy-efficient**, optimizing power consumption to reduce electronic waste and extend battery life.

## 2.2.6 Economical Factors

1. The system must be **affordable** to ensure accessibility for users with disabilities, who may have limited financial resources.
2. A balance between **cost-effectiveness and innovation** is crucial to ensure competitiveness in the **growing BCI market**.

### 3 System Overview

#### 3.1 System Block Diagram

[DD1+]

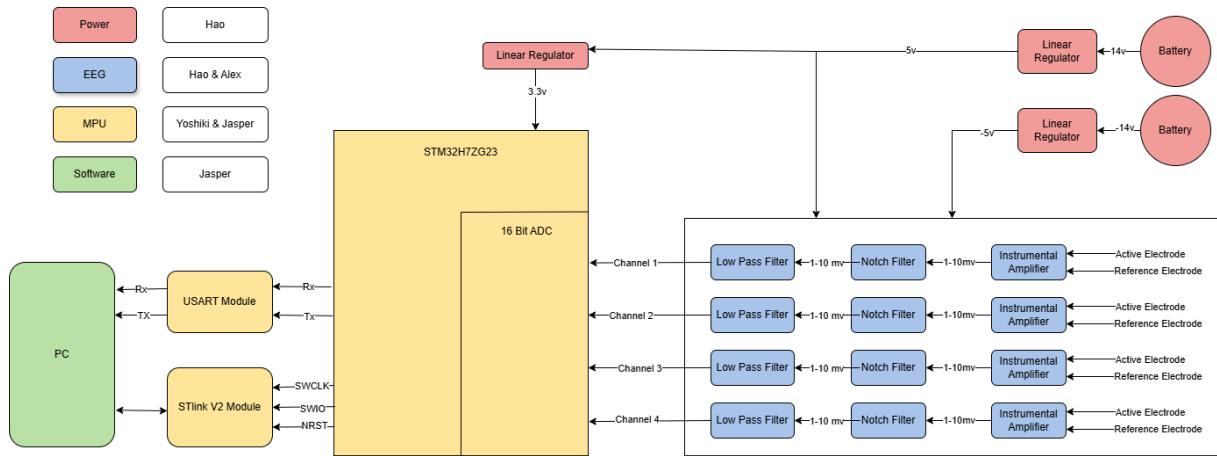


Figure 3.1.1: System Block Diagram

## 3.2 System Activity Diagram

[DD1+]

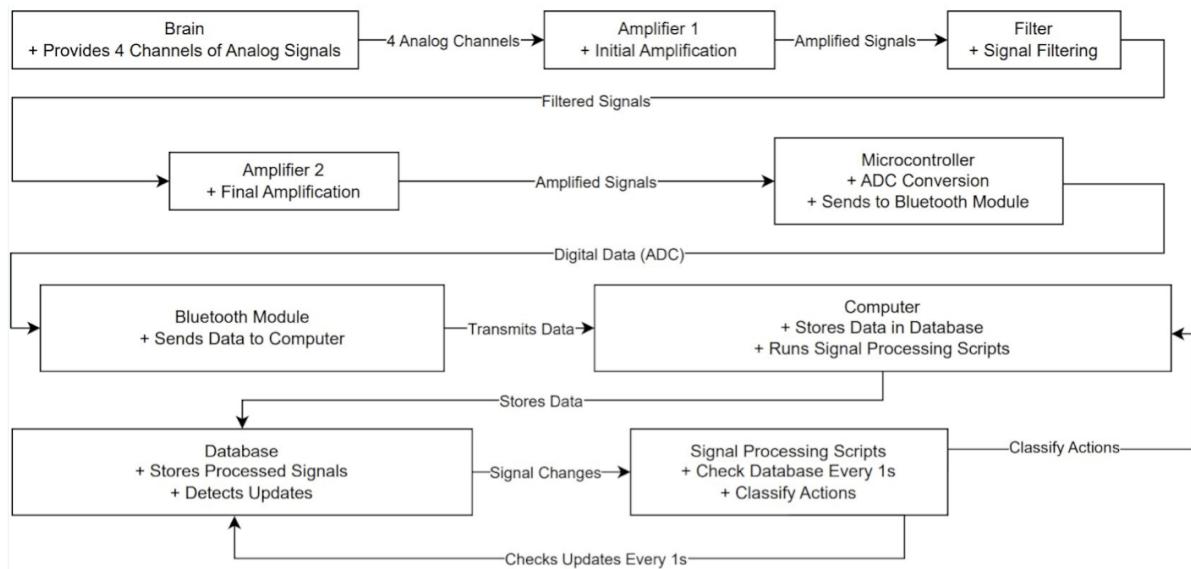


Figure 3.2.1: System Activity Diagram

### 3.3 System Mechanical Design (Extra Credit)

[DD3+]



Figure 3.3.1: System Mechanical Design

### 3.4 Integration Approach

[DD3+]

The Active Electrodes and Reference Electrode capture raw EEG signals from the brain. These electrodes are designed to detect the four channels of analog signals, which are then passed to the Instrumental Amplifiers. Each channel is connected to an amplifier with a gain of 10-100, amplifying the weak EEG signals to a detectable level. Following amplification, the signals are filtered through a series of Notch Filters and Low Pass Filters and to remove noise and unwanted frequencies, such as power line interference. This integration of electrodes, amplifiers, and filters ensures that the raw EEG signals are conditioned and cleaned for accurate digitization in the subsequent stages.

The filtered and amplified signals from each channel are then fed into the STM32H72023 microcontroller, which houses a 16-bit Analog-to-Digital Converter (ADC). The ADC converts the analog signals into digital data, preparing them for further processing. The microcontroller interfaces with the USART Module, which facilitates serial communication to transmit the digitized data to the PC. Additionally, the microcontroller is connected to an STLINK V2 Module for debugging and programming, ensuring reliable operation. This integration between the microcontroller, ADC, and communication modules ensures seamless conversion and transfer of EEG data to the computational platform.

The PC receives the digital data via the USART Module through Rx/Tx lines. The PC runs software components, including Jasper for signal processing and action classification. The software processes the incoming data, stores it, and applies algorithms to detect signal changes and classify actions. The PC also interfaces with the STLINK V2 Module for debugging purposes, ensuring system reliability. Power is supplied to the system via Linear Regulators (3.3V and 1.8V), which are connected to Batteries (5V and 1.8V), providing stable voltage to the microcontroller and other components.

The Database checks for updates every second, ensuring that the system remains up-to-date with the latest data, while the Signal Processing Scripts detect signal changes and classify actions based on predefined criteria. This integration enables real-time data processing and storage, allowing the system to dynamically respond to new data and provide actionable insights. The modular and sequential nature of this design ensures scalability and ease of maintenance, as each subsystem can be independently optimized while maintaining interoperability within the overall system.

### 3.5 System Photographs

**EEG circuit:** The EEG circuit includes the input of four channel Electrodes, an instrumentation amplifier and filters with the input of the user's signal and serve as the first stage of the signal processing for the whole system.

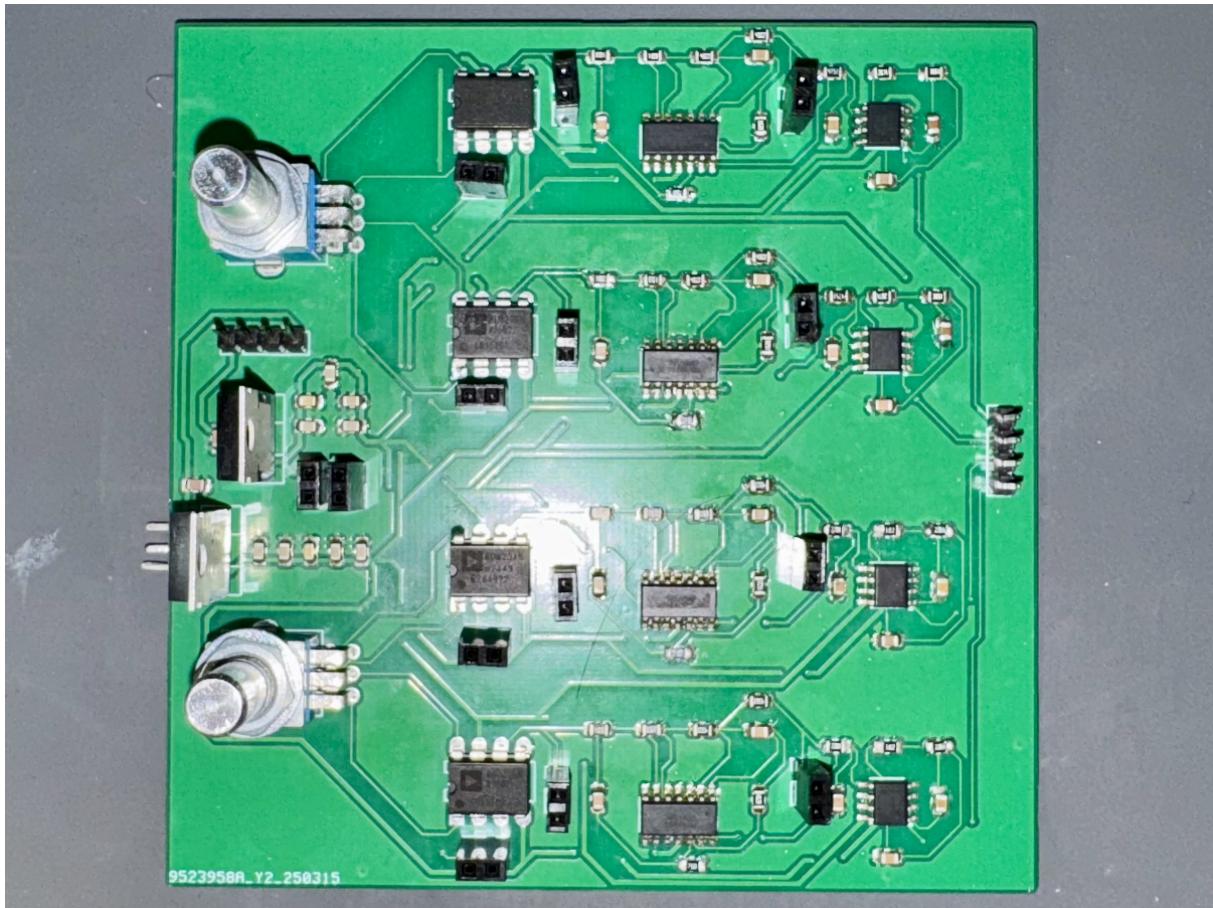


Figure 3.5.1: [PCB of EEG circuit]

**Microprocessor:** The microprocessor control unit receives the analog signals conditioned by the EEG front-end and converts them to digital form using the onboard ADC of the STM32 microcontroller. Running custom firmware, the MCU performs real-time signal processing which include digital filtering.

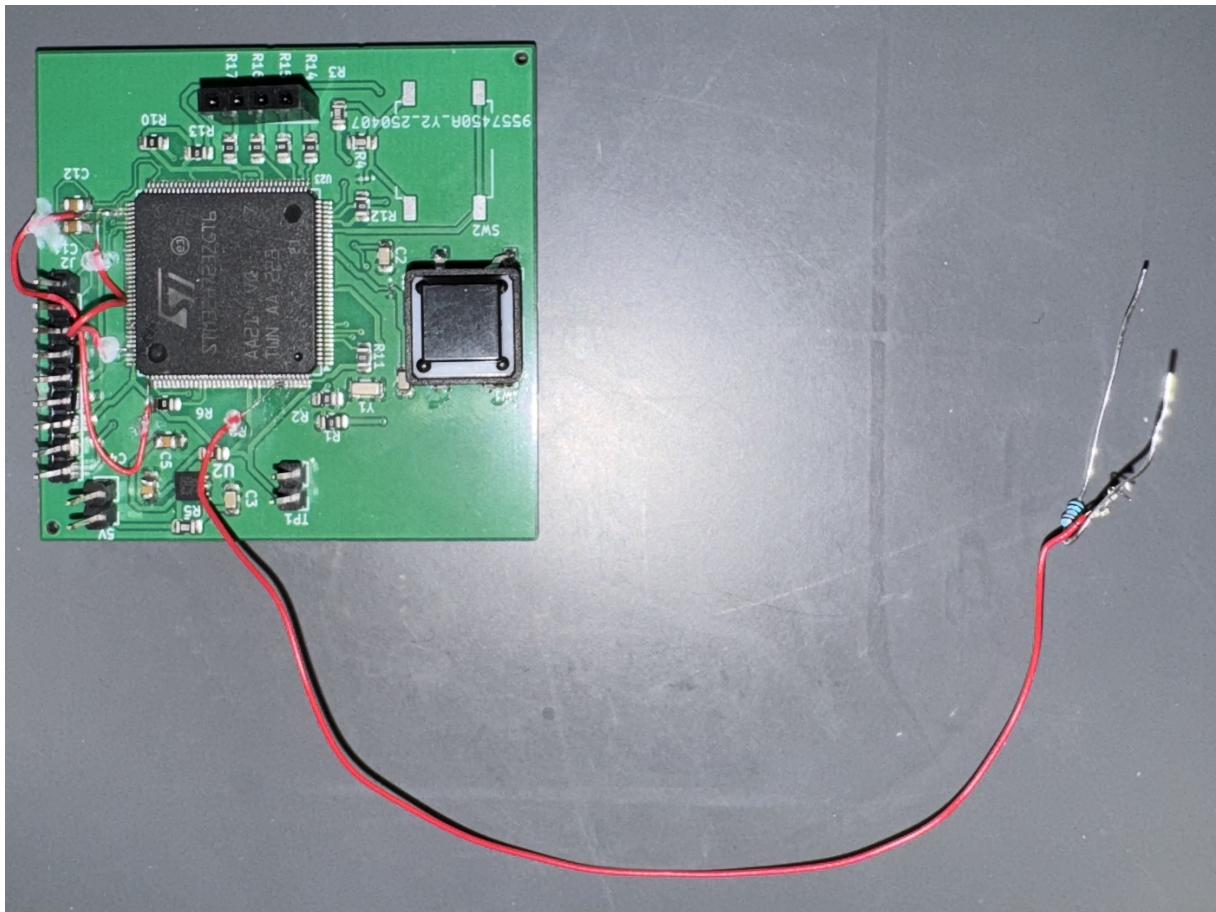


Figure 3.5.2: [PCB of the Microprocessor Unit]

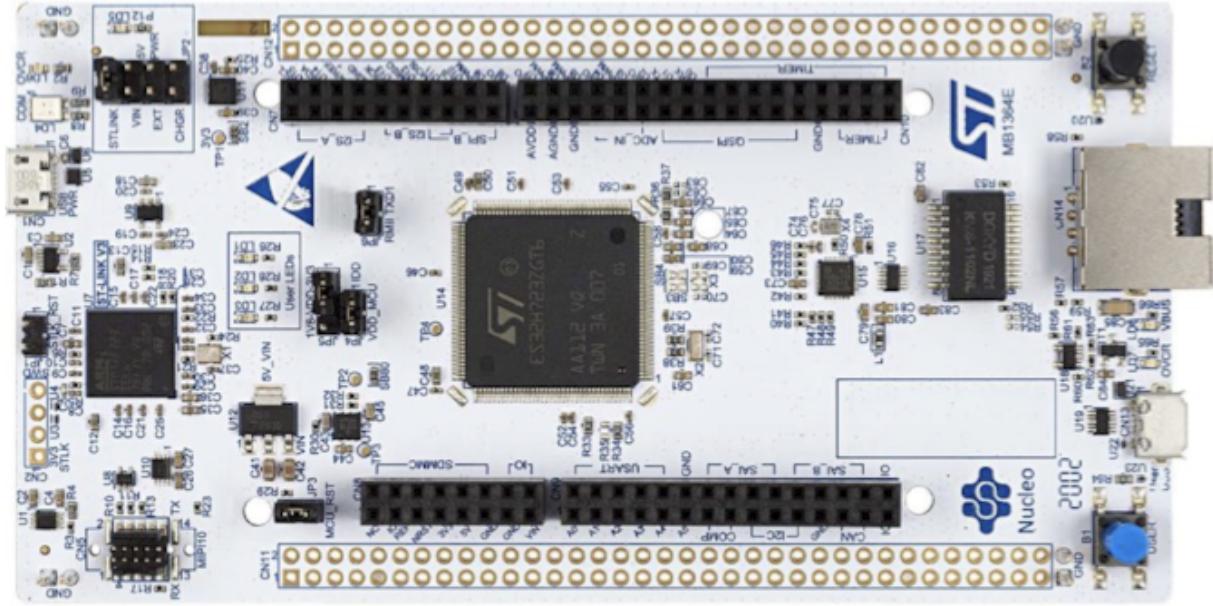


Figure 3.5.3: STM32H723ZG Microprocessor

## 4 Subsystems

### 4.1 Subsystem 1: Mouse Action Classification

#### 4.1.1 Subsystem Diagrams

[DD1+]

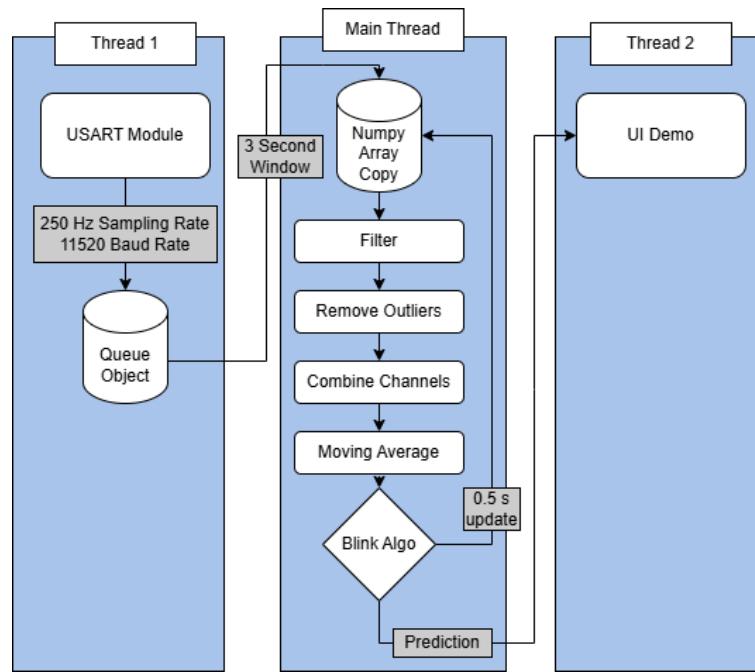


Figure 4.1.1: Subsystem Block Diagram

#### 4.1.2 Specifications

#### 4.1.3 Input Requirements

- **EEG Data:** 4 channels, 250 Hz sampling rate received via USART and stored in a dequeue object of length  $3 * \text{sampling rate}$ .
- **Data Packet Structure:** One sample from each of the 4 channels.
- **Error Handling:** Mechanisms to detect and manage data inconsistencies include try-except blocks.

#### 4.1.4 Processing Requirements

- **Noise Reduction Techniques:**
  - Digital bandpass filtering for eliminating DC offset and high-frequency noise.
  - Digital notch filter to eliminate power line noise
  - Z-score-based outlier detection to remove noise in data
  - Moving average with window of 80 samples to smooth data
- **Blink Classification Method:** Threshold-based detection, discrete derivative.

#### 4.1.5 Demo Specifications

- **Jumping Game:** Working Google Dinosaur clone where jumps are triggered by blinks.
- **Keyboard:** Functional keyboard where letters are selected by blinks.
- **Assistant:** Proof-of-concept assistant that allows a disabled individual to perform actions such as toggling a light, opening a door, and alerting a caregiver.

#### 4.1.6 Performance Metrics

- **Accuracy of Blink Detection:** 90%.
- **Latency Targets:** Less than 800 ms from blink to action trigger

#### 4.1.7 Subsystem Interactions

The **local machine** will receive EEG data through the USART Rx and Tx pins that are sent via USB from the development board. i. Each data packet will contain 1 sample from each of the four channels, sampled at **250 Hz**.

A python method will handle incoming signals by reading from a serial port (COM11) and storing the incoming samples in a deque object that can be accessed in real time by processing scripts on the main thread.

#### 4.1.8 Core ECE Design Tasks

- **ECE 20875 and ECE 47300:** Python code, data science algorithms, and experiment design.
- **ECE 36200:** Communication protocols and words from Bluetooth module.
- **ECE 39595:** Object-oriented programming, class and repo structure.

- **ECE 30100:** Signal processing techniques like Fourier transforms.
- **ECE 36800:** General coding ability and custom algorithm design and implementation.

#### 4.1.9 Schematics

No Schematics for software.

#### 4.1.10 Parts

- Local Windows machine

#### 4.1.11 Algorithm

The blink detection algorithm follows a threshold-based method based on the standard deviation of the data. It finds a peak of the data and then takes the derivative of the signal to determine when the blink peak flattens out. Once the peak is detected, it must pass specific rules to make sure that it is the correct width and has not already been counted.

```

# copy queue objecy as numpy array and proccess data
channel_one_array = copy(queue_ch1)
clean_ch1 = proccessing_pipeline()

channel_two_array = copy(queue_ch2_copy)
clean_ch2 = proccessing_pipeline()

combined_signal = ave_signals(clean_ch1, clean_ch2)

peak_height = 1.5 * std(combined_signal)
peak_width = 0.3 * sampling_rate

# find peaks with scipy
peaks = find_peak(combined_signal, peak_height, peak_width)

#determine blink periods
blink_periods = []
for peak in peaks:
    # takes average difference over 10 samples
    derivative = take_different(combined_signal)

    for idx in range(peak + 15, len(combined_signal)):
        if derivadive[idx] < derivative_threshold:
            blink_periods.append((peak, idx))

# check for length of classified period and make sure
# blink hasn't been counted already
for period in blink_periods:
    if len(blink_period) <= min_blink_period
        return False
    if len(blink_period) >= max_blink_period
        return False
    if period_counted(period)
        return False

return True

```

Figure 4.1.2: Blink Algorithm Pseudoscope

#### **4.1.12 Theory of Operation**

The Brain-Computer Interface (BCI) software component processes and classifies EEG signals in real-time for blink detection and Steady-State Visual Evoked Potential (SSVEP) recognition. The system implements threshold-based classification algorithms extract neural responses while using a multi-threaded architecture to ensure efficient data acquisition, signal processing, and user interface updates.

This implementation aligns with the guidelines and best practices established in the field of brain-computer interfaces, as outlined in ISO 9241-971:2020 (Guidelines for BCI accessibility) and IEEE 802.15.6 (Wireless communication standard for body area networks).

##### **Blink Detection**

Blink detection is implemented using a threshold-based classification method on the time vs. amplitude trace of an EEG signal. The methodology follows principles outlined in Del R. Millán et al. (2004), which discusses the efficacy of simple thresholding for eye-blink classification in EEG-based BCI systems.

The steps include:

- Pre-processing: EEG signals are band-pass filtered (0.5 – 25 Hz) to remove DC drift and high-frequency noise, as suggested in Fatourechi et al. (2007) for artifact-based classification.
- Amplitude Thresholding: Peaks in the EEG waveform are detected using an empirically determined threshold based on the standard deviation of the sample as reported in He et al. (2017).
- Time Constraint Filtering: A detected blink is validated if it occurs within 100–400 ms, ensuring rejection of slow signal variations.
- Event Registration: If the blink satisfies the conditions, it is classified and stored in an event queue for downstream processing.
- This threshold-based method aligns with ISO 80601-2-26 (Standard for EEG devices), which specifies signal processing constraints and artifact rejection methods.

##### **Multi-threading Architecture**

To ensure real-time performance, the system employs a multi-threaded design that aligns with the real-time constraints specified in IEEE 11073-10406 (Standard for Wearable and Monitoring Devices).

Data Acquisition Thread:

- Reads EEG data from the external device (PCB).
- Stores the latest samples in a shared buffer (queue object).

Processing Thread:

- Runs the blink detection and SSVEP classification algorithms.
- Accesses the shared buffer to fetch EEG data and process it independently.

User Interface (UI) Thread:

- Displays real-time EEG waveforms, classification results, and user feedback.
- Ensures smooth UI updates without blocking signal processing.

This design follows best practices from POSIX real-time threading (IEEE 1003.1b-1993), ensuring that time-critical operations such as EEG signal classification and UI updates run concurrently without performance degradation

#### 4.1.13 Specifications Measurement

[DD3+ Every specification here should match the above specification. ]

1. **Input Requirements:** 4 channels at 250 hz must be read by Python scripts and be ready for real-time processing.

```
PS C:\Users\jaspe\BCI_Senior_Design> python .\src\data_input\test_in.py
Testing sampling rate over 1 seconds
Duration of Measurment: 1.0018200874328613 seconds
Number of samples recorded: 250
Sampling rate 250 / 1.0018200874328613 = 249.5458048167298

Testing sampling rate over 2 seconds
Duration of Measurment: 2.0007100105285645 seconds
Number of samples recorded: 502
Sampling rate 502 / 2.0007100105285645 = 250.91092530065234

Testing sampling rate over 3 seconds
Duration of Measurment: 3.003199815750122 seconds
Number of samples recorded: 753
Sampling rate 753 / 3.003199815750122 = 250.73256732733248
```

Figure 4.1.3: Sampling rate by PC

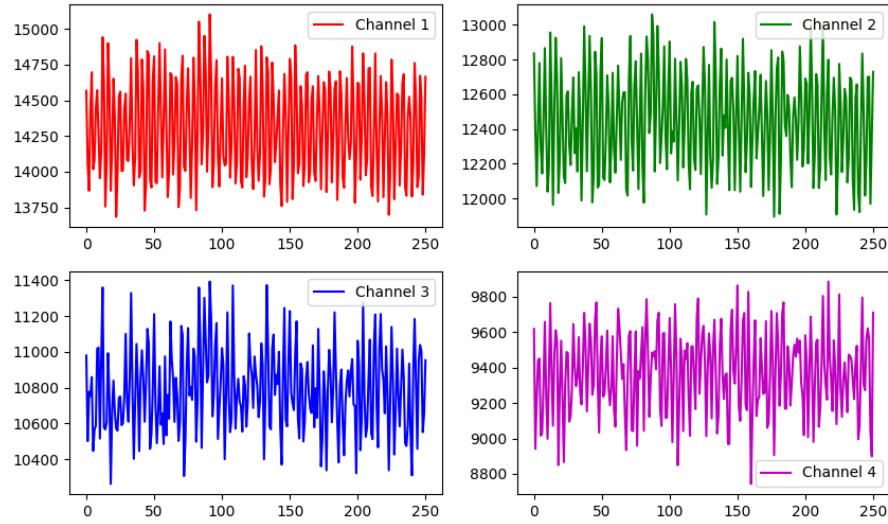


Figure 4.1.4: 4 channels of data

Three experiments were performed, sampling for one, two and three seconds. The sampling rate falls close to the expected 250 Hz sent by the MCU. All four channels can be read for processing.

2. Processing Requirements: Apply digital filters on the data, including 60 Hz notch filter, and a band pass filter, getting rid of DC offset and high frequencies that the analog filters did not get.

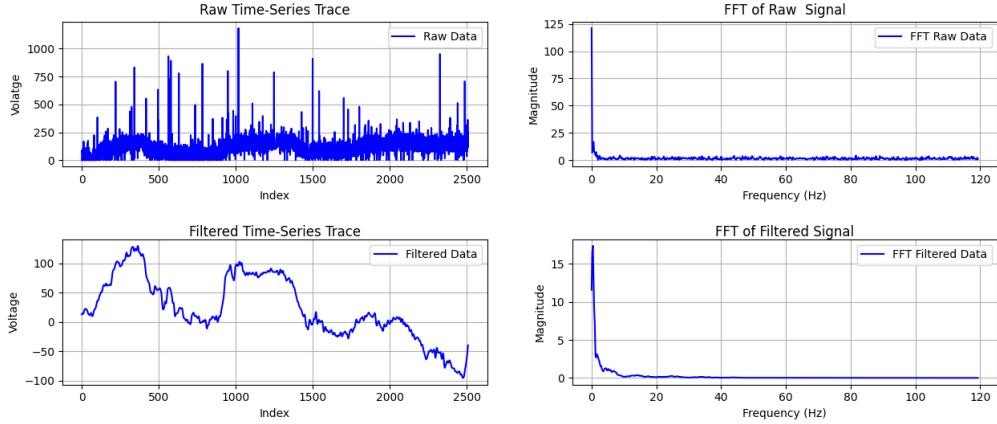


Figure 4.1.5: Processing of raw data

The digital band pass filter cleans up high frequencies and DC offset as shown in the FFT. 3. Latency requirement: An experiment was run to determine the average latency from blink to classification as outlined below:

- 60 seconds of data
- Log blink time with keyboard
- Log blink detected time

The results are shown below: Mean Latency: 0.72 s Var of Latency: 0.1 s<sup>2</sup> Median Latency: 0.73 s The metrics show that the latency target was met. The reasons for variance of the results are defined below:

- Threading
- Background local processes
- Windowing of data
- Inconsistent ground truth

**4. Performance Metrics:** A blink experiment was designed to determine accuracy, precision, and recall. The experiment design is described below.

- 2 full minutes of real time blink detection
- Number of samples = (total\_secs - window) / (update\_cycle\_time)
- $117 = (120 - 3) / (1)$

- Logged predictions for each window
- Metrics computed after experiment

A confusion matrix, a common evaluation method for binary classification problems is shown below:

	Predicted Positive	Predicted Negative
Actual Positive	TP = 17	FP = 0
Actual Negative	FN = 11	TN = 89

Figure 4.1.6: Blink Confusion Matrix

The metrics are shown below. High precision means that the algorithm is good at classifying a blink when it occurs. The low recall means that it predicts non blink as blink more than it should, meaning this is a room for improvement.

- **Precision:** 1.0000  
Formula: Precision =  $\frac{TP}{TP+FP}$
- **Recall:** 0.6071  
Formula: Recall =  $\frac{TP}{TP+FN}$

- **Accuracy:** 0.9060

**Demo:** All three demos were successful. Screenshots of the demos are provided below.

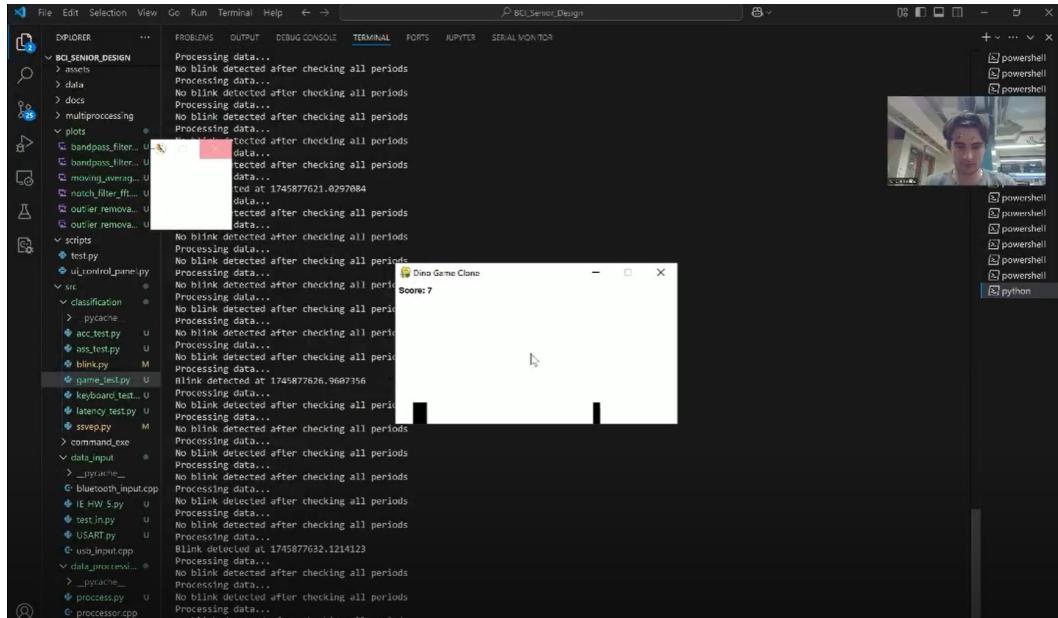


Figure 4.1.7: Dinosaur Game Demo

As you can see by the screenshot a score of 7 has been achieved showing that the demo works.

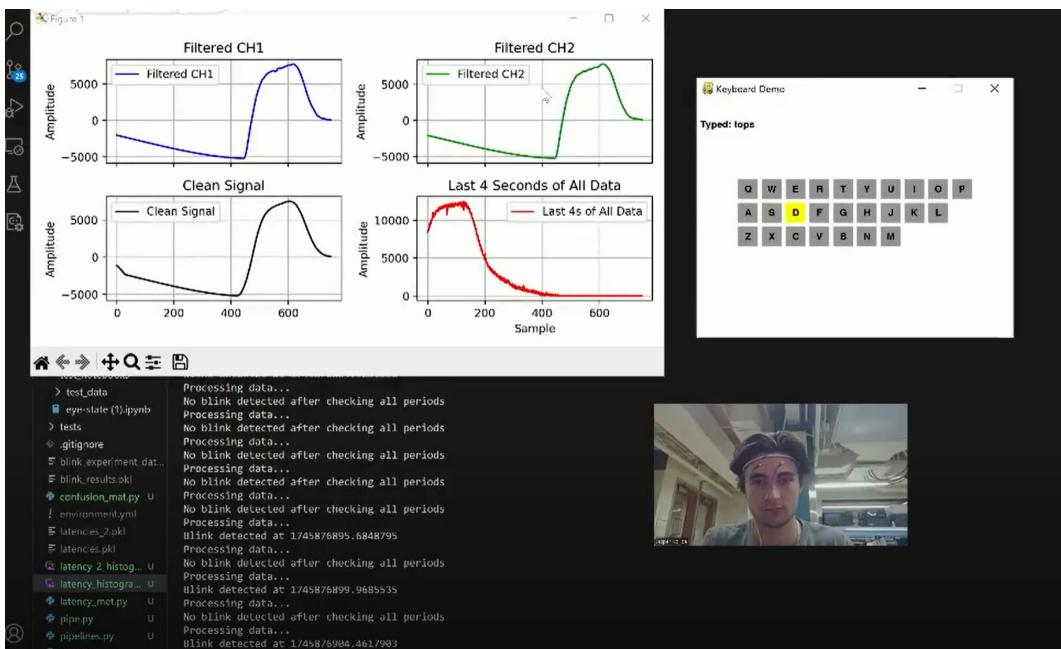


Figure 4.1.8: Keyboard Demo

The word "tops" has been spelled, indicating a working demo.

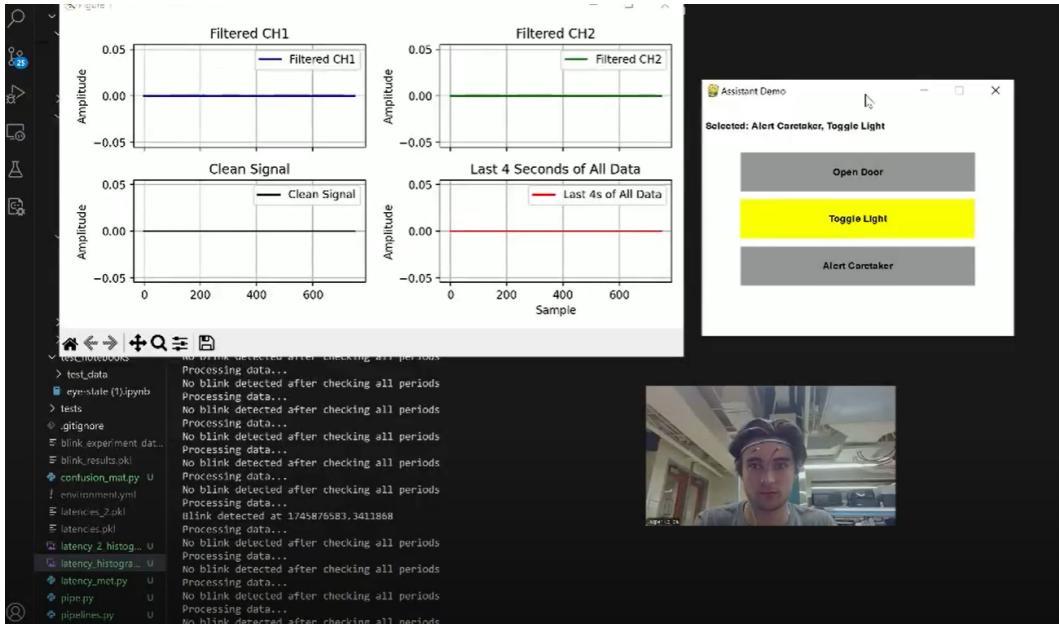


Figure 4.1.9: Assistant Demo

Toggle light and alert caretaker have been chosen, indicating a working assistant.

#### 4.1.14 Standards

[DD1+]

- Object Oriented Programming standards.
- Naming and documentation standards: docstrings, variable and method names.
- USART communication protocols

## 4.2 Subsystem 2: [EEG Circuit Filters]

### 4.2.1 Subsystem Diagrams

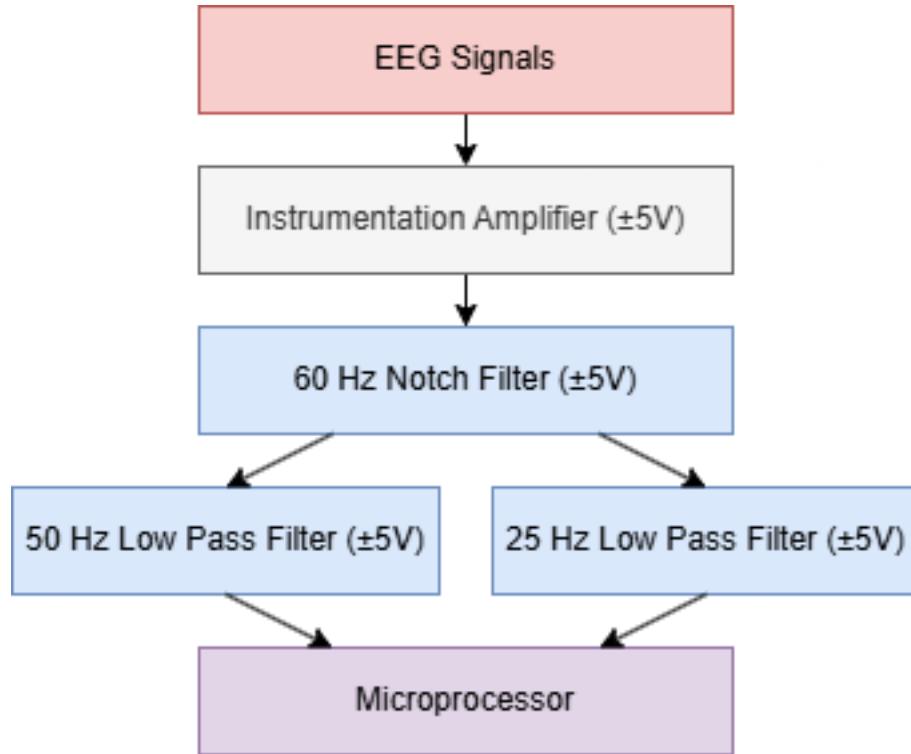


Figure 4.2.1: EEG Circuit Subsystem Block Diagram

### 4.2.2 Specifications

1. **60 Hz Notch Filter** A 60 Hz notch filter must be implemented after the instrumentation amplifier to remove powerline interference while preserving EEG signal integrity. The filter must achieve  $\geq 30\text{--}40$  dB attenuation at 60 Hz with a narrow bandwidth (59–61 Hz) to minimize distortion of EEG signals. It should use low-tolerance components to ensure accurate frequency targeting.

**Justification:** Powerline interference at 60 Hz can obscure EEG signals (0.5–50 Hz). A notch filter with high attenuation and narrow bandwidth removes this noise without affecting critical EEG bands, ensuring clear signals for amplification and digitization.

**Requirements:**

- **Center Frequency:** Precisely tuned to 60 Hz.
  - **Attenuation:**  $\geq 30\text{--}40$  dB at 60 Hz.
  - **Bandwidth:** 59–61 Hz to preserve EEG signals.
  - **Minimal Phase Distortion:** Low phase shifts to maintain EEG waveform timing.
2. **25 Hz Low-Pass Filter** A 25 Hz low-pass filter must be implemented to suppress high-frequency noise while preserving Delta (0.5–4 Hz), Theta (4–8 Hz), and Alpha (8–13 Hz) EEG bands. The filter must have a cutoff frequency of  $\approx 25$  Hz, a roll-off of  $\geq -40$  dB/decade (second-order or higher), and minimal phase distortion for signal integrity.

**Justification:** Low-frequency EEG bands are critical for applications like sleep or neurological studies. A 25 Hz low-pass filter attenuates high-frequency noise (e.g., Beta, Gamma, artifacts) while preserving lower bands, ensuring clear signals with minimal distortion.

**Requirements:**

- **Cutoff Frequency:**  $\approx 25$  Hz.
  - **Filter Order:** Second-order or higher,  $\geq -40$  dB/decade roll-off.
  - **Minimal Phase Distortion:** Low phase distortion to preserve EEG waveforms.
  - **Flat Passband:** Consistent gain below 25 Hz for Delta, Theta, and Alpha bands.
3. **50 Hz Low-Pass Filter** A 50 Hz low-pass filter must be implemented after the non-inverting amplifier to remove high-frequency noise while preserving EEG bands (0.5–50 Hz). The filter must have a cutoff frequency of  $\approx 50$  Hz, a roll-off of  $\geq -40$  dB/decade (second-order or higher), and minimal phase distortion for signal integrity.

**Justification:** EEG signals (Delta to Beta) are susceptible to high-frequency noise from muscle activity or electronics. A 50 Hz low-pass filter eliminates noise above 50 Hz, ensuring clear EEG signals for accurate analysis.

**Requirements:**

- **Cutoff Frequency:**  $\approx 50$  Hz.
- **Filter Order:** Second-order or higher,  $\geq -40$  dB/decade roll-off.
- **Minimal Phase Distortion:** Low phase distortion to preserve EEG waveforms.
- **Flat Passband:** Consistent gain below 50 Hz for EEG bands.

### 4.2.3 Subsystem Interactions

The EEG signal passes through multiple subsystems to ensure accurate processing before analog-to-digital conversion. Each stage in the signal processing pipeline plays a critical role in conditioning the raw EEG signals for reliable analysis. The interactions between these subsystems are described as follows:

1. **Electrode Signal Acquisition:** EEG electrodes detect weak bioelectric signals, typically in the microvolt range, and transmit them to the instrumentation amplifier.
2. **60 Hz Notch Filter:** This stage selectively attenuates powerline interference at 60 Hz to prevent contamination of the EEG signal.
3. **50 Hz Low-Pass Filter:** High-frequency noise beyond 50 Hz is attenuated, preserving critical EEG frequency bands while removing unwanted interference.

### 4.2.4 Core ECE Design Tasks

- **ECE 20008:** [Operational Amplifier]
- **ECE 30600:** [Notch Filter & 2nd-Order Low Pass Filter]

### 4.2.5 Schematics

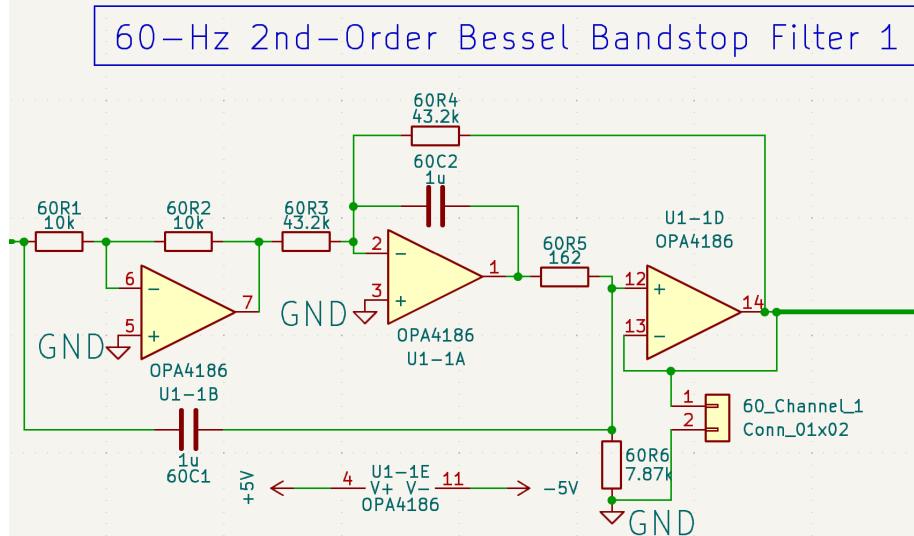


Figure 4.2.2: 60-Hz 2nd-Order Bessel band-stop filter

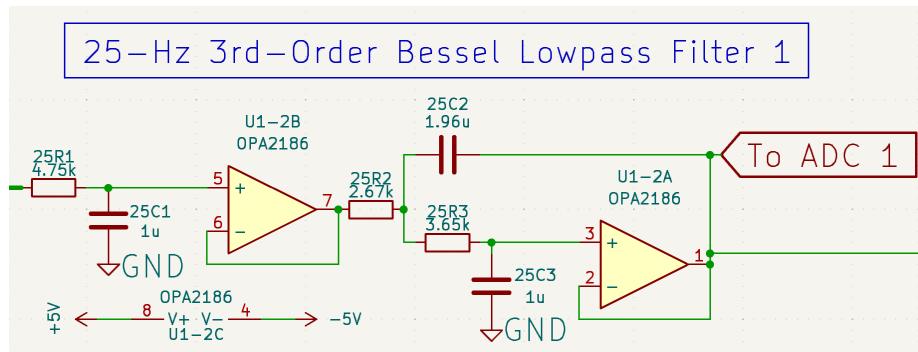


Figure 4.2.3: 25-Hz 3rd-Order Bessel low-pass Filter

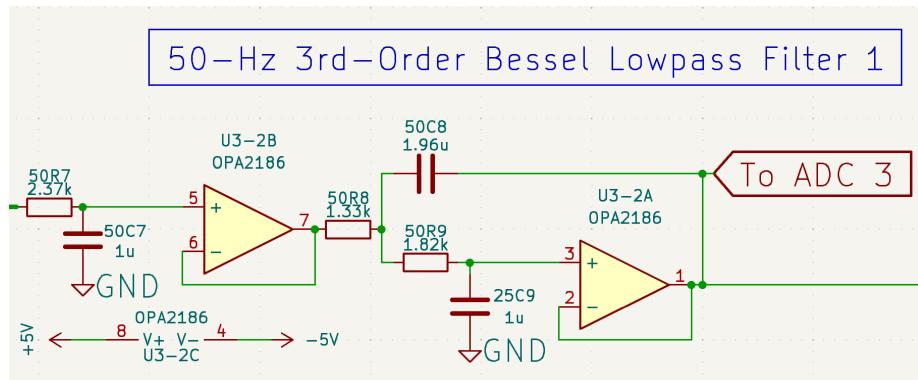


Figure 4.2.4: 50-Hz 3rd-Order Bessel low-pass Filter

#### 4.2.6 Parts

- Resistors:  $120\Omega$ ,  $162\Omega$ ,  $1.33k\Omega$ ,  $1.82k\Omega$ ,  $2.37k\Omega$ ,  $2.67k\Omega$ ,  $3.65k\Omega$ ,  $4.75k\Omega$ ,  $7.87k\Omega$ ,  $43.2k\Omega$ .
- Capacitors:  $1\mu F$ ,  $1.96\mu F$ .
- Dual and quad Channel Operation Amplifier (OPA2186 and OPA4186)

#### 4.2.7 Algorithm

- After initial amplification by the AD620AN differential amplifier, the signal enters a 60 Hz notch filter to eliminate powerline interference. The filter is designed to provide at least 30 dB attenuation at 60 Hz while preserving nearby EEG frequency bands, ensuring that essential brain activity information is not lost due to external noise such as 50/60 Hz powerline artifacts.

- The amplified signal then passes through a 50 Hz low-pass filter to remove high-frequency noise while retaining EEG components up to 50 Hz, covering the Delta, Theta, Alpha, and Beta bands. This second-order or higher filter design ensures a roll-off of at least -40 dB/decade, effectively suppressing unwanted interference and maintaining signal clarity. Subsequently, the signal undergoes further filtering with a 25 Hz low-pass filter to focus on the lower EEG frequency bands (Delta, Theta, and Alpha), attenuating the upper Beta band and higher-frequency noise. This additional filter, also designed as second-order or higher with a -40 dB/decade roll-off, enhances noise rejection and is particularly useful for applications emphasizing low-frequency brain activity, such as sleep monitoring or relaxation studies.
- After the filtering stages, the processed analog signal is fed into an analog-to-digital converter (ADC) to be converted into digital format. This digitized EEG data can then be stored, transmitted, or processed further for real-time brain activity monitoring or offline analysis.

#### 4.2.8 Theory of Operation

The EEG signal processing circuit is designed to acquire, condition, and digitize low-amplitude bioelectric signals from the brain for monitoring and analysis. The system operates in a series of well-defined stages, each addressing specific challenges associated with EEG signal acquisition, such as low signal amplitude, high-frequency noise, powerline interference, and the need for digital conversion. The theory of operation is as follows:

- **Powerline Interference Rejection with 60 Hz Notch Filter:** Following amplification, the signal passes through a 60 Hz notch filter, implemented as a 2nd-order Bessel band-stop filter using an OPA4186 op-amp. This stage targets powerline interference, a significant source of noise at 60 Hz (or 50 Hz in some regions), which can obscure EEG signals. The notch filter is designed to provide at least 30 dB attenuation at 60 Hz, effectively removing this narrow-band interference while preserving adjacent EEG frequency bands (e.g., Delta: 0.5–4 Hz, Theta: 4–8 Hz, Alpha: 8–13 Hz, Beta: 13–30 Hz). The Bessel response ensures minimal phase distortion, which is critical for maintaining the temporal accuracy of the EEG waveform. The filter's components—resistors (e.g.,  $1.33\text{k}\Omega$ ,  $4.75\text{k}\Omega$ ) and capacitors (e.g.,  $1\mu\text{C}$ )—are tuned to create a sharp rejection band centered at 60 Hz, with a roll-off sufficient to protect the signal's integrity outside this frequency.
- **High-Frequency Noise Suppression with 50 Hz and 25 Hz Low-Pass Filters:** The filtered signal then undergoes two stages of low-pass filtering to remove high-frequency noise while preserving the EEG signal's relevant frequency components. The first low-pass filter, a 50 Hz 2nd-order or higher design with a -40 dB/decade roll-off, attenuates frequencies above 50 Hz, including muscle artifacts, environmental

interference, and higher EEG bands (e.g., Gamma:  $\geq 30$  Hz). This filter, also based on a Bessel topology with an OPA4186 op-amp, ensures a flat passband response below 50 Hz and minimal phase distortion, retaining the Delta, Theta, Alpha, and Beta bands for general EEG analysis. The second low-pass filter, set at 25 Hz with a similar second-order or higher design and -40 dB/decade roll-off, further refines the signal by attenuating the upper Beta band (13–30 Hz) and higher frequencies. This stage focuses on the lower EEG bands (Delta, Theta, Alpha), enhancing noise rejection and is particularly valuable for applications such as sleep monitoring or relaxation studies, where low-frequency activity is of primary interest. The cascaded filters collectively ensure a clean signal with progressive attenuation of unwanted high-frequency components.

- **Overall System Behavior:** The system operates as a cascaded signal conditioning chain, where each stage builds on the previous one to enhance signal quality. The AD620AN provides initial amplification and noise rejection, the 60 Hz notch filter targets powerline interference, the 50 Hz and 25 Hz low-pass filters progressively eliminate high-frequency noise, and the ADC enables digital processing. The use of Bessel filters throughout ensures linear phase characteristics, preserving the temporal relationships within the EEG signal, which is crucial for accurate waveform analysis. The circuit is powered by a  $\pm 5$  V supply, and the low-power design of components like the OPA4186 and AD620AN ensures compatibility with portable EEG devices.

#### 4.2.9 Specifications Measurement

The following specifications for the EEG Circuit subsystem, as defined in Section 4.2.2, were measured using frequency response analysis. Each filter's performance is verified with a dedicated frequency response plot, showing magnitude and phase responses across a range of frequencies. The results are presented below, supported by Figure 4.2.5, Figure 4.2.6, and Figure 4.2.7.

1. **60 Hz Notch Filter Specification:** The notch filter must be tuned to 60 Hz, provide at least 30–40 dB attenuation at 60 Hz, have a narrow bandwidth (59–61 Hz), and exhibit minimal phase distortion.

The frequency response plot in Figure 4.2.5 shows that at 62.892 Hz, the filter achieves an attenuation of -43.149 dB, exceeding the required 30–40 dB. This confirms that the notch filter effectively removes 60 Hz powerline interference. The bandwidth appears narrow, as the attenuation remains significant around 60 Hz (e.g., -43.01208 dB at 50 Hz), though further measurements between 59 Hz and 61 Hz would provide a more precise bandwidth estimate. The phase response shows a steep transition near 60 Hz (e.g.,  $-71.26555^\circ$  at 50 Hz), which is expected for a notch filter, but remains relatively stable below 50 Hz, indicating minimal phase distortion in the EEG-relevant frequency bands (0.5–50 Hz).

2. **25 Hz Low-Pass Filter Specification:** The filter must have a cutoff frequency of approximately 25 Hz, a minimum second-order design with at least -40 dB/decade roll-off, minimal phase distortion, and a flat passband response below 25 Hz.  
The frequency response plot in Figure 4.2.6 demonstrates the filter's performance. [At 25 Hz, the magnitude should be approximately -3 dB, indicating the cutoff frequency. At 50 Hz (one octave above 25 Hz), the attenuation should be around -12 dB or greater for a second-order filter with -40 dB/decade roll-off. Verify these values from your plot and update here.] The passband below 25 Hz shows a flat response with near-zero attenuation, meeting the specification. The phase response in the passband (e.g., 0.5–20 Hz) should be relatively linear, indicating minimal phase distortion; [check your plot for phase values at 10 Hz, 20 Hz, and 25 Hz to confirm].
3. **50 Hz Low-Pass Filter Specification:** The filter must have a cutoff frequency of approximately 50 Hz, a minimum second-order design with at least -40 dB/decade roll-off, minimal phase distortion, and a flat passband response below 50 Hz.  
The frequency response plot in Figure 4.2.7 verifies the filter's behavior. [At 50 Hz, the magnitude should be approximately -3 dB, confirming the cutoff frequency. At 100 Hz (one octave above 50 Hz), the attenuation should be around -12 dB or greater for a second-order filter with -40 dB/decade roll-off. Verify these values from your plot and update here.] The passband below 50 Hz exhibits a flat response with near-zero attenuation, satisfying the specification. The phase response in the passband (e.g., 0.5–40 Hz) should show minimal distortion; [check your plot for phase values at 20 Hz, 40 Hz, and 50 Hz to confirm].

#### 4.2.10 Standards

- **IEEE Std 1057:** Defines the testing methodologies for analog and digital filters used in EEG signal processing, ensuring accurate frequency response and minimal distortion.

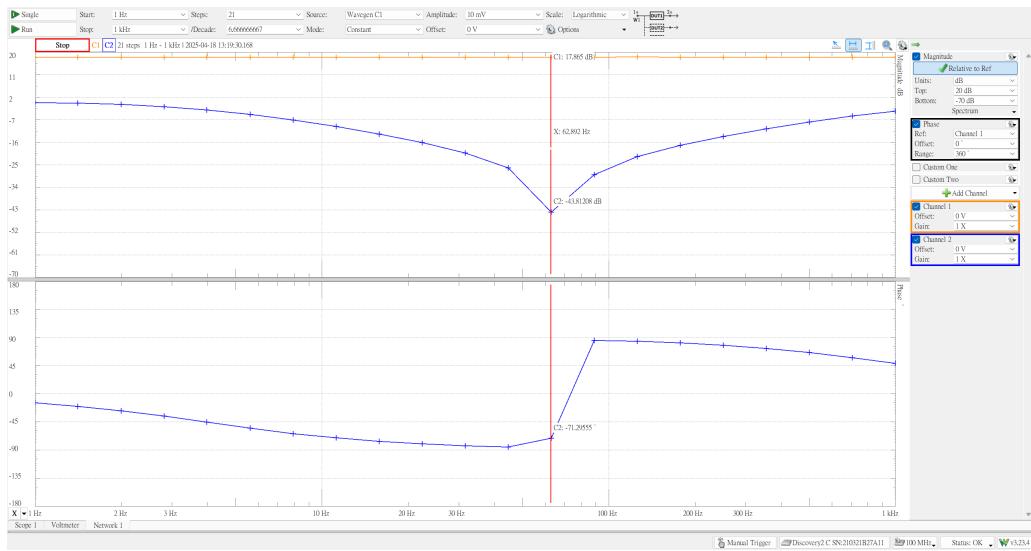


Figure 4.2.5: Frequency response plot of the 60 Hz notch filter, showing magnitude and phase responses from 1 Hz to 1 kHz.

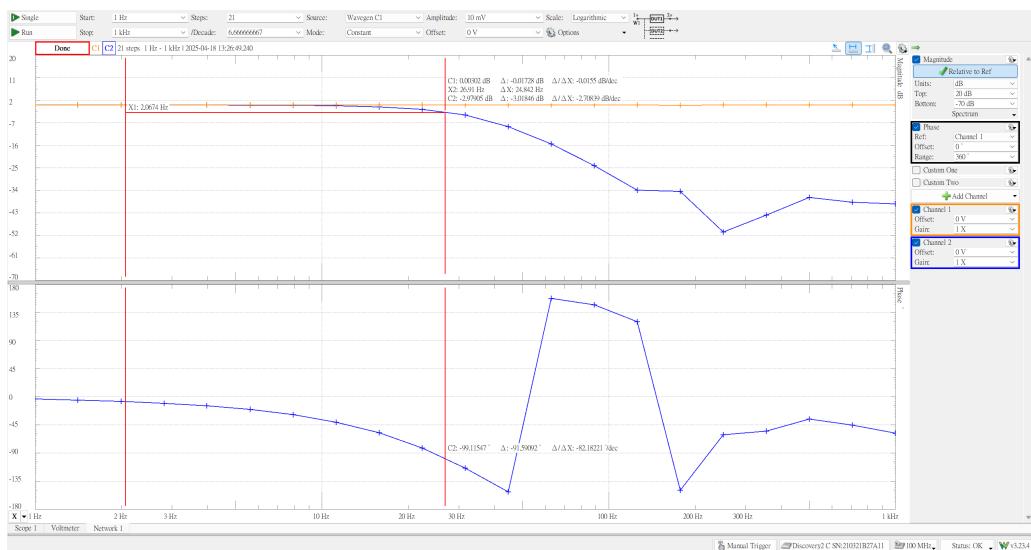


Figure 4.2.6: Frequency response plot of the 25 Hz low-pass filter, showing magnitude and phase responses.

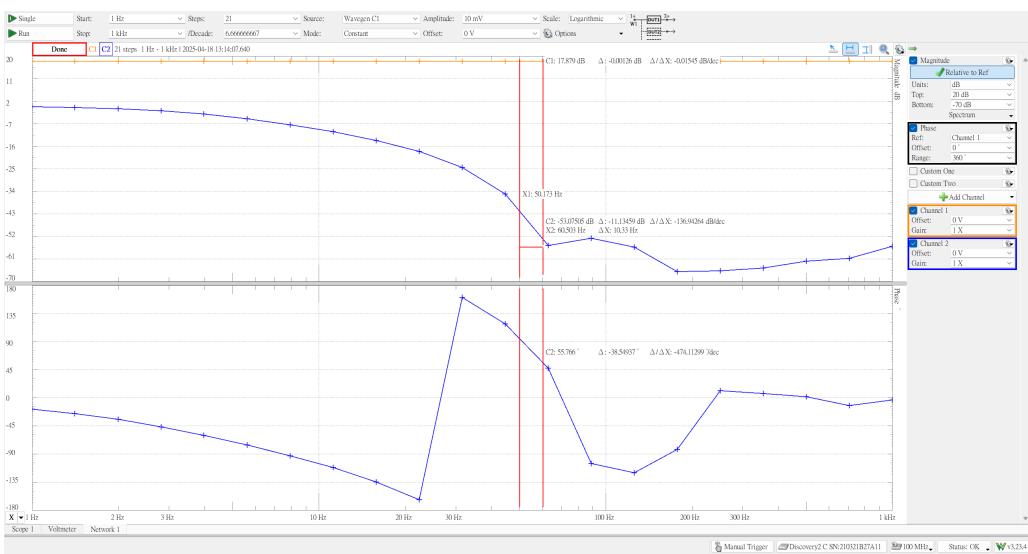


Figure 4.2.7: Frequency response plot of the 50 Hz low-pass filter, showing magnitude and phase responses.

## 4.3 Subsystem 3: EEG Headpiece, Power, and Instrumentation Amplifier

### 4.3.1 Subsystem Diagrams

The subsystem diagrams illustrate the architecture and power supply design of the EEG Headpiece, Power, and Instrumentation Amplifier subsystem. Figure 4.3.1 provides a block diagram of the subsystem, detailing the signal flow from the EEG headpiece to the instrumentation amplifier, while Figure 4.3.2 shows the power supply block diagram, outlining the conversion of battery voltage to stable outputs for the subsystem components.

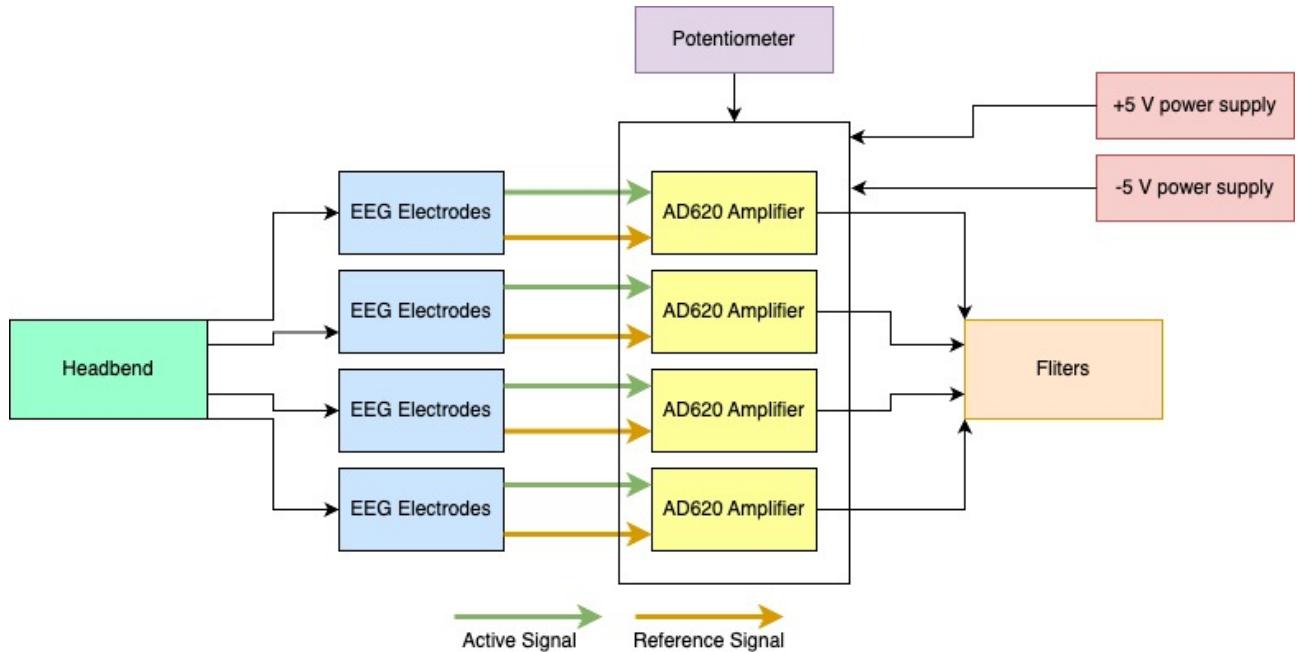


Figure 4.3.1: Subsystem block diagram for the EEG Headpiece, Power, and Instrumentation Amplifier.

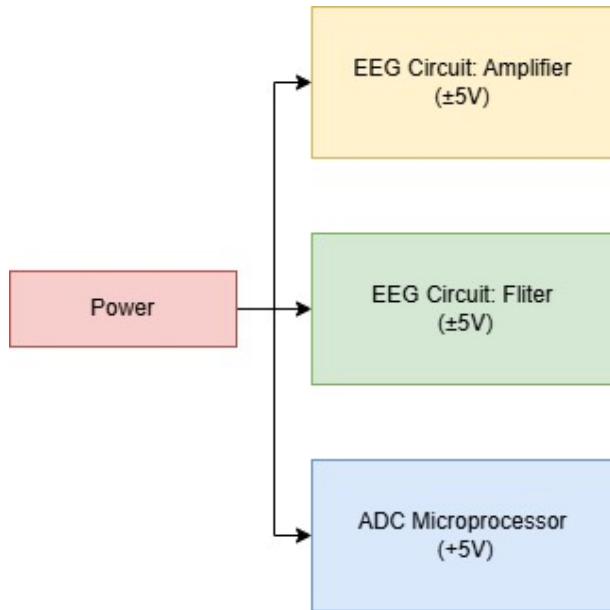


Figure 4.3.2: Power block diagram, showing the conversion of battery voltage to  $\pm 5$  V outputs.

### 4.3.2 Specifications

#### 1. EEG Headpiece

The headpiece must acquire EEG signals using strategically placed electrodes for reliable, high-fidelity data collection during user movement and extended wear.

##### Specifications:

- **Electrode Type: Wet Electrodes**

Wet electrodes lower skin-electrode impedance, ensuring high signal conductivity and reducing motion artifacts when measuring microvolt-level brainwaves.

- **Number of Channels: 4**

Two channels at Fp1 (active) referenced to the earlobe and Fp2 (active) referenced to the earlobe enable reliable blink detection, while two channels at O1 (active) referenced to the earlobe and O2 (active) referenced to the earlobe capture steady-state visual evoked potentials (SSVEP); this configuration ensures differential measurement for each channel, improving noise rejection and signal clarity.

- **Electrode Gel: Conductive gel**

The gel maintains stable ionic contact over long sessions, preventing impedance drift and ensuring consistent amplitude and spectral measurements.

- **Headband Material: Breathable, elastic fabric**

A comfortable, stretchable cap ensures electrodes remain firmly in place—critical for reproducible electrode positioning and minimizing motion-induced noise.

## 2. Instrumentation Amplifier

The amplifier must boost weak EEG signals (10–100 $\mu$ V) while suppressing common-mode noise (e.g., 60Hz mains interference), offering high input impedance to avoid signal loading and low power draw for battery operation.

### Specifications:

- **Type: AD620AN instrumentation amplifier**

The AD620AN provides low input offset voltage and low bias current . These are critical for extracting microvolt-level differences between each active electrode and its earlobe reference without distortion. Its single-resistor gain programming simplifies the design.

- **Gain: Adjustable up to 1000 via potentiometer**

A 10k $\Omega$  precision potentiometer in the gain setting allows real-time tuning of the AD620AN's differential gain, so the amplified output between active and reference electrodes can be optimized for each user's signal amplitude and ensure the MCU's ADC input is fully utilized without clipping.

- **Power Supply:  $\pm 5$  V**

Dual-rail supply maximizes dynamic range and allows accurate representation of both positive and negative EEG deflections, while fitting within the portable system's power budget.

## 3. Power Supply

The circuit is powered by a rechargeable Li-ion battery pack that drives a step-down regulator to produce low-noise  $\pm 5$  V rails. This arrangement ensures stable dual-rail operation under varying load, eliminates mains-borne interference, and supports both positive and negative EEG deflections with minimal ripple. The battery's capacity provides several hours of uninterrupted, and portable use while preserving microvolt-level signal integrity.

### Specifications:

- **Battery Type:** Rechargeable Li-ion battery with 14.4V positive output and -14.4V negative output.

- **Output Voltage:**  $\pm 5$  V via step-down regulation.

### 4.3.3 Subsystem Interactions

The EEG system's Electrode Array captures electrical impulses from brain neural activity, positioned according to the 10-20 system to cover critical scalp locations for efficient signal

acquisition. Electrodes are secured by the Electrode Cap, ensuring consistent scalp contact and reliable signal capture during sessions. These signals are fed into the Pre-amplification Subsystem, where the AD620AN instrumentation amplifier amplifies differential EEG signals while rejecting noise through its high common-mode rejection ratio (CMRR) of at least 100 dB, effectively minimizing powerline interference. Gain adjustment is achieved via an external resistor, allowing the amplifier to vary between 10 and 1000, with a typical setting of 100 for initial EEG signal amplification; active electrodes connect to pin 2 (-IN) and pin 3 (+IN) of the AD620AN for accurate gain application. The amplifier is powered by a  $\pm 5$  V supply, derived from a 14.4 V rechargeable battery (Section 4.3.5), ensuring stable operation and supporting the system's portability requirement. After amplification, the conditioned signals are transmitted to the EEG Circuit subsystem (Section 4.2) for further processing, including noise rejection via a 60 Hz notch filter and high-frequency suppression using 25 Hz and 50 Hz low-pass filters. The processed signals are then digitized by the Microprocessor subsystem (Section 4.4) for real-time transmission to a PC, completing the EEG signal acquisition chain.

#### 4.3.4 Core ECE Design Tasks

[DD1+ Write tasks and course that helps accomplish that task]

- **ECE 20007:** Circuit design and electrodes connections
- **ECE 20008:** Operational amplifier and gain calculation

#### 4.3.5 Schematics

The Headpiece will connect the Active Electrode and Reference Electrode to the Instrumentation Amplifier and the amplifier will be powered with +5V and -5V.

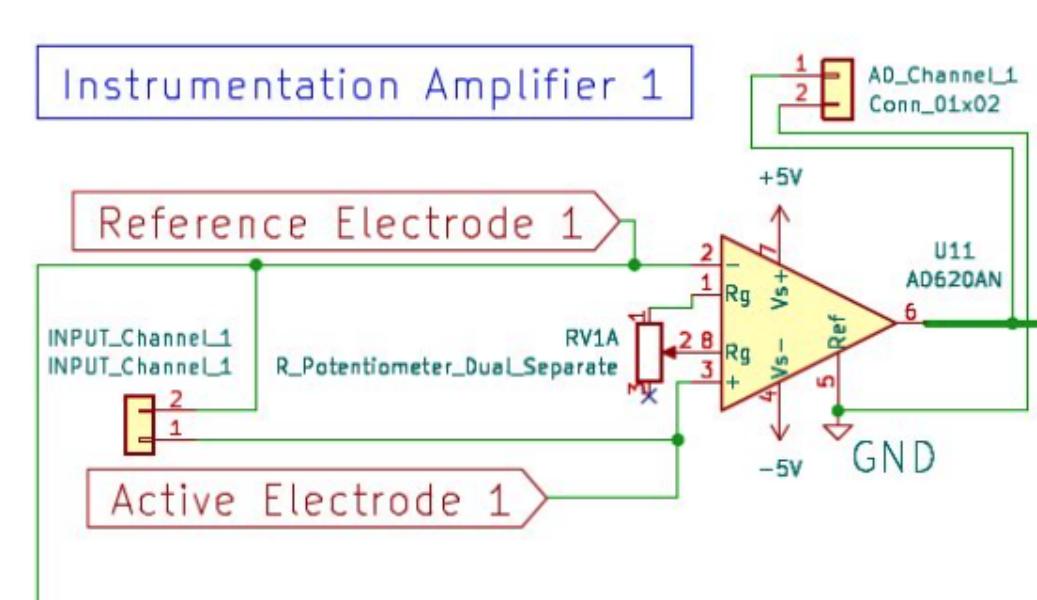


Figure 4.3.3: Circuit schematic for instrumentation amplifier

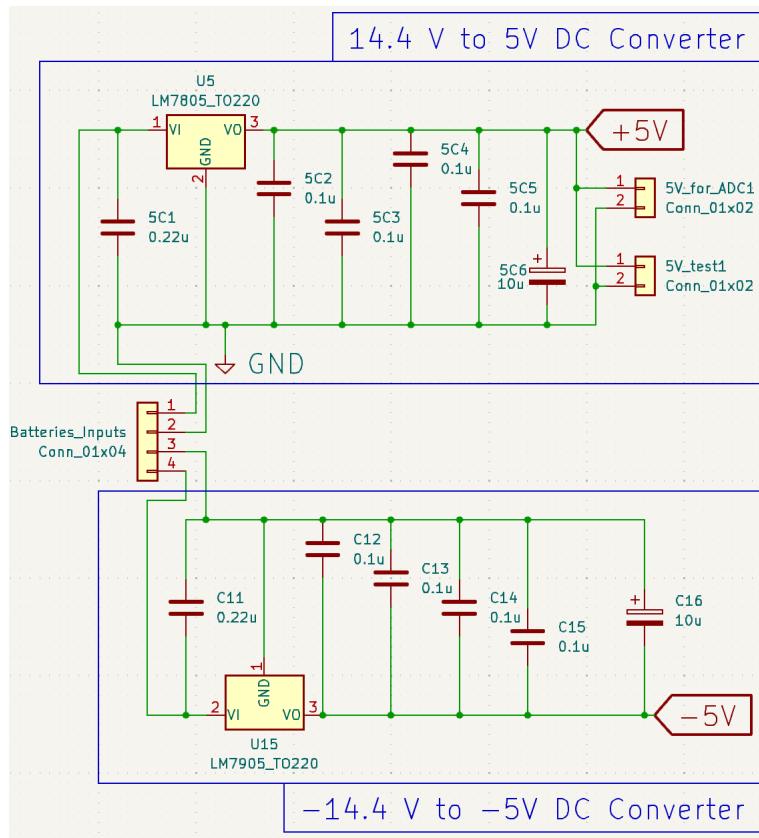


Figure 4.3.4: Power supply for the amplifier

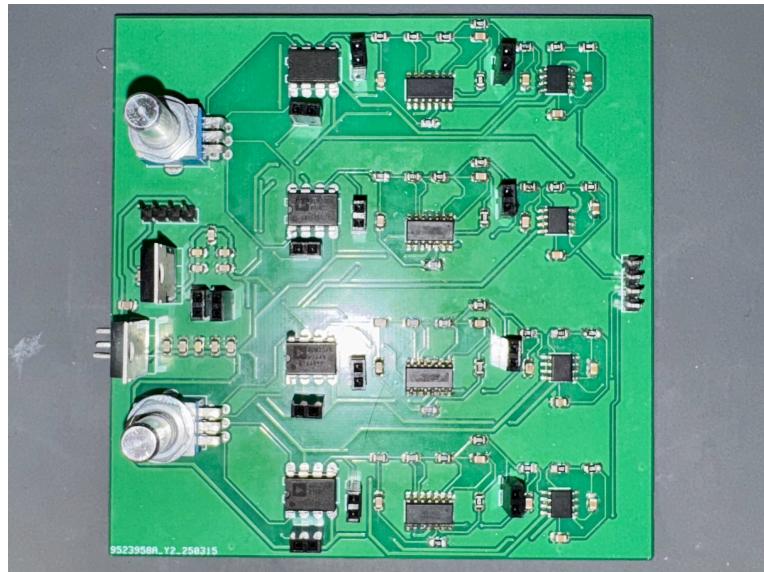


Figure 4.3.5: EEG circuit final PCB with power supply, amplifiers and filters

#### 4.3.6 Parts

- EEG Singal Electrodes
- Electrodes Conductive Gel
- AD620AN Instrumentation Amplifier
- LM7805 Voltage Regulator
- LM7905 Voltage Regulator
- Lithium-Ion Batteries

#### 4.3.7 Algorithm

The EEG signal acquisition process begins by positioning wet Ag/AgCl electrodes on the scalp, adhering to the 10-20 system to target key regions such as the frontal, temporal, parietal, and occipital areas for optimal brain activity monitoring. Conductive gel is applied to reduce skin-electrode impedance, enabling the electrodes to capture microvolt-level electrical impulses ranging from  $0.5 \mu\text{V}$  to  $100 \mu\text{V}$ . An electrode cap secures the electrodes, ensuring continuous and reliable scalp contact throughout the recording session. The captured signals are then fed into the AD620AN instrumentation amplifier, which is powered by a  $\pm 5 \text{ V}$  supply derived from a 14.4 V rechargeable battery through a voltage regulator,

ensuring stable operation and supporting portability. The amplifier amplifies the differential EEG signals with a gain typically set to 100 (adjustable between 10 and 1000 via an external resistor) to enhance the weak signals for further processing. The amplifier's high common-mode rejection ratio (CMRR) of at least 100 dB effectively suppresses common-mode noise, such as 60 Hz powerline interference and environmental artifacts, preserving signal integrity. Following amplification, the signals are transmitted to the EEG Circuit subsystem (Section 4.2) for filtering, where a 60 Hz notch filter removes powerline interference, and 25 Hz and 50 Hz low-pass filters eliminate high-frequency noise, preparing the signals for digitization by the Microprocessor subsystem (Section 4.4) and subsequent analysis on a PC.

#### 4.3.8 Theory of Operation

The EEG electrode system employs conductive gel to improve electrode-to-skin contact and an AD620 instrumentation amplifier for signal conditioning, focusing on the acquisition and amplification of microvolt-level brain activity signals. The system's operation is detailed as follows:

- **Electrodes:** Wet Ag/AgCl electrodes detect the brain's electrical activity, capturing signals in the microvolt range ( $0.5 \mu\text{V}$  to  $100 \mu\text{V}$ ), positioned per the 10-20 system.
- **Conductive Gel:** Applied to lower skin-electrode impedance, reducing contact resistance and noise, ensuring reliable capture of weak bio-signals.
- **Power Supply:** A  $\pm 5 \text{ V}$  supply, derived from a 14.4 V rechargeable battery via a voltage regulator, powers the AD620 amplifier, ensuring stable operation and portability.
- **Instrumentation Amplifier:** The AD620 amplifies differential signals from the electrodes, with the following features:
  - **High Differential Gain:** Amplifies input differences, critical for low-amplitude EEG signals, with a gain typically set to 100 (adjustable from 10 to 1000 via an external resistor).
  - **Common-Mode Rejection:** Achieves a CMRR of at least 100 dB, suppressing noise like 60 Hz powerline interference to maintain signal integrity.
  - **Input Configuration:** Connects active electrodes to pin 2 (-IN) and pin 3 (+IN), ensuring accurate amplification.

**Detailed Operational Principle:** The system starts with gel-enhanced electrodes applied to the scalp, reducing impedance and capturing microvolt-level brain signals. These signals feed into the AD620 instrumentation amplifier, powered by a  $\pm 5 \text{ V}$  supply, which

amplifies differential signals while rejecting common-mode noise like powerline interference. The gain, set via an external resistor, typically ranges from 100 to 1000, ensuring the EEG waveform's temporal and spectral integrity for subsequent filtering (Section 4.2) and digitization (Section 4.4).

**Demonstration and Verification:** System performance is verified by simulating an EEG input with a 5 mV, 1 Hz sine wave, mimicking typical EEG signal levels. This test compares the known input amplitude to the output, confirming the amplifier's gain and noise rejection capabilities. A real-world test, with the active electrode on the forehead and the reference on the earlobe, further validates the system's ability to accurately capture and amplify genuine EEG signals, ensuring reliable signal acquisition and amplification.

#### 4.3.9 Specifications Measurement

The following specifications for the EEG Headpiece electrodes and the Instrumentation Amplifier, as defined in Section 4.3.2, were measured using dedicated tests. Electrode performance is verified through continuity, impedance, and signal reception checks, while amplifier gain is characterized across the core EEG frequency band ( $\pm 10$  Hz). Test results are presented below.

##### 1. Electrodes & Conductive Gel: 4 channels wet Ag/AgCl electrodes

The cap integrates four channel electrodes to ensure stable, low-impedance scalp contact. The conductive gel further reduces the impedance of the skin electrode for reliable microvolt-level signal capture.

- **Continuity & Wiring:** Verify with a continuity tester that exactly four independent leads connect the cap connector to the contacts, each  $< 10\text{ k}\Omega$ .
- **Contact Impedance:** Measure electrode-to-skin impedance at 10 Hz on a human subject should be  $< 20\text{ k}\Omega$ . Repeat every 30 min over 1 h.
- **Signal Reception Check:** Inject a 10 Hz,  $50\text{ }\mu\text{V}$  sine test signal at each electrode and confirm its presence at the amplifier input via oscilloscope.

##### 2. Instrumentation Amplifier: Gain Measurement

The amplifier gain must be adjustable up to 10,000 and maintain consistent performance for EEG signals below 10 Hz.

- **Specification:** Gain range 10–10,000 (nominal  $G = 10$  with  $R_G = 49.4\text{ k}\Omega$ ).
- **Test Signal Selection:** EEG signals of interest lie below 10 Hz; thus, 5 Hz and 10 Hz inputs were chosen.
- **5 Hz Input Test:** Input signal 5 mV sine wave ( $V_{pp,in} = 10\text{ mV}$ ) at 5 Hz. Measured  $V_{pp,out} = 80.895\text{ mV} \Rightarrow Gain \approx 8.09$ .

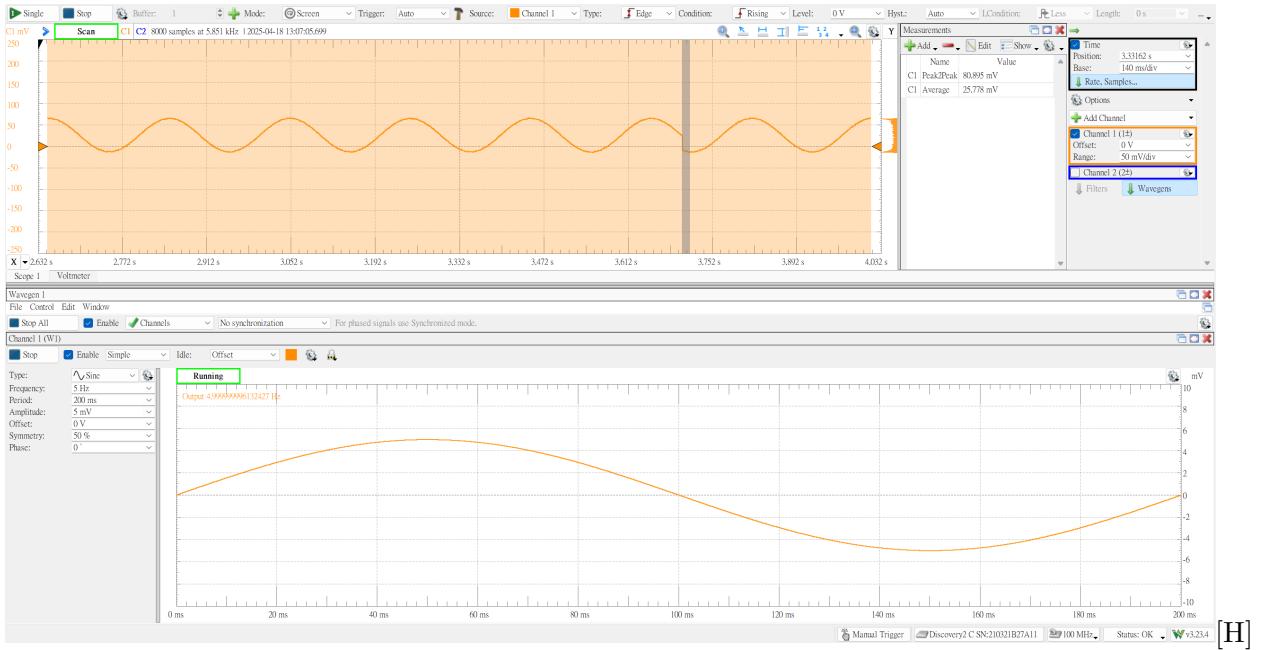


Figure 4.3.6: Input signal with 5Hz sine wave

- **10 Hz Input Test:** Input signal 5 mV sine wave at 10 Hz. Measured  $V_{pp,out} = 80.553 \text{ mV} \Rightarrow \text{Gain} \approx 8.06$ .

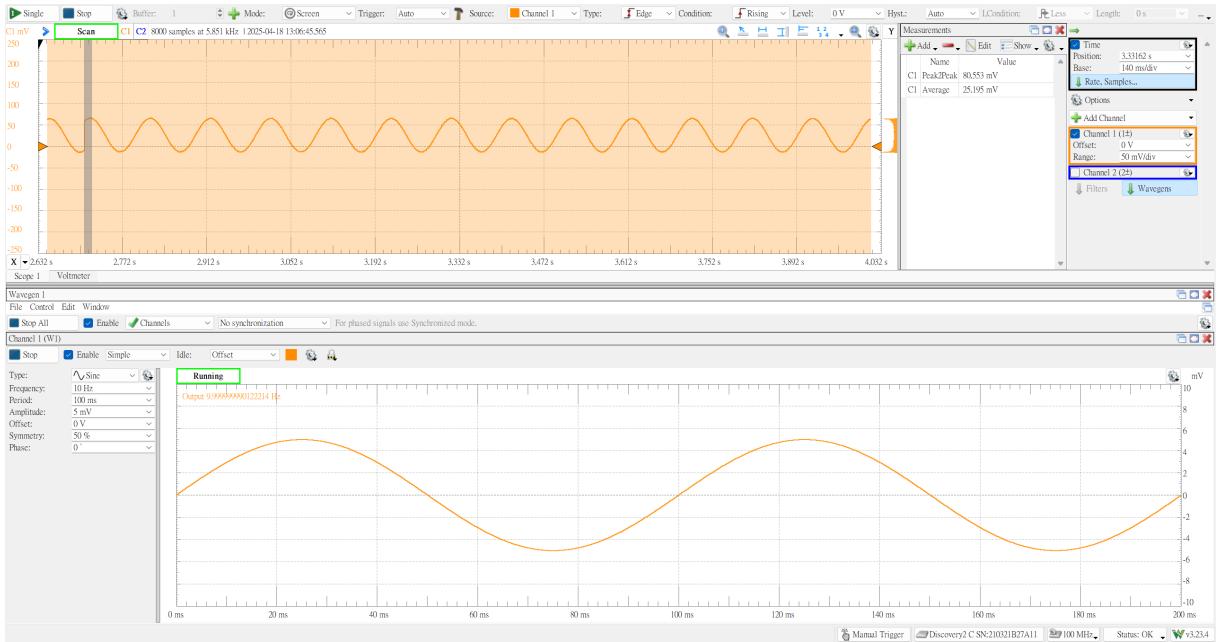


Figure 4.3.7: Input signal with 10 Hz sine wave

- **Input Test with EEG electrodes input** Input signal with electrodes from Fp1 and reference. Measured  $V_{pp,out} = 169 \text{ mV}$  and output  $V_{pp,out} = 3.5 \text{ V} \Rightarrow Gain \approx 20.7$  with the expected gain of 19.1.



Figure 4.3.8: Input signal with one channel electrode



Figure 4.3.9: Output signal from the amplifier

#### 4.3.10 Standards

- **IEC 60601:** Standard that focuses on the safety, performance, and essential requirements of medical electrical equipment. As the amplifier and electrodes are part of the devices interacting with patients, this standard will ensure the safety for our users.

## 4.4 Subsystem 4: Microprocessor

### 4.4.1 Subsystem Diagrams

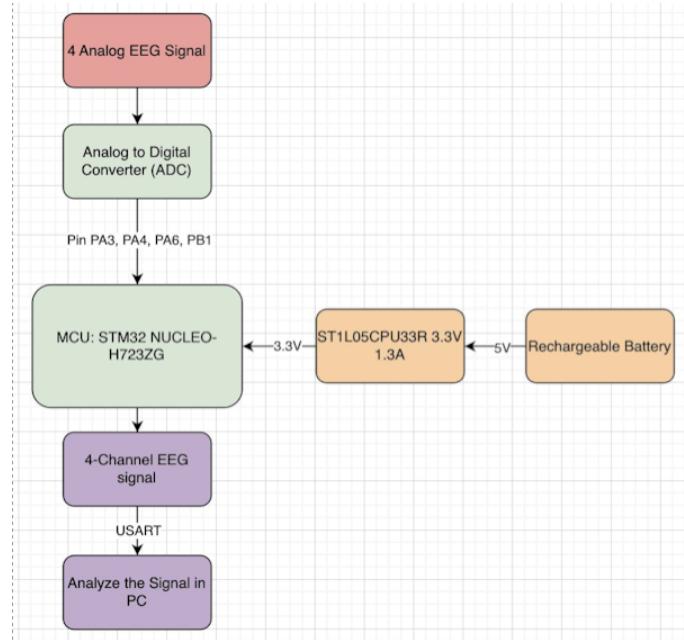


Figure 4.4.1: Subsystem Block Diagram

### 4.4.2 Specifications

1. The MCU will incorporate a USART (Universal Synchronous/Asynchronous Receiver/Transmitter) interface to enable communication between the PC and the EEG circuit.

**Justification:** The MCU should be able to interface with a PC while also allowing flexibility for future expansion to support additional communication options.

**Requirement:** The MCU must be capable of interfacing with a PC.

2. The EEG circuit's signal must be processed by the ADC in the microcontroller with high quality and reliably transmitted to the PC for further signal processing.

**Justification:** Accurate signal acquisition and processing are essential for maintaining data integrity. The ADC must ensure high-quality conversion, and seamless communication with the PC is necessary for efficient signal analysis and further processing.

**Requirement:**

- The microcontroller must include a high-quality ADC for precise signal conversion.
  - The system must support a reliable communication interface between the microcontroller and the PC for data transmission.
3. The microprocessor must be powered by a rechargeable battery to ensure sustained operation and energy efficiency.

**Justification:** A rechargeable battery enhances system reliability by providing continuous power, reducing dependency on external sources. This ensures portability and extended usability, making the device suitable for various applications.

**Requirement:**

- The system must include a rechargeable battery as the primary or backup power source.
- The battery should have sufficient capacity to support long-duration operation.

#### 4.4.3 Subsystem Interactions

The system is designed to process EEG signals and send the data wirelessly to a PC. The EEG circuit generates analog signals, which are converted into digital form by the ADC before reaching the STM32 NUCLEO-H723ZG microcontroller. The MCU handles signal processing and communication while running on a rechargeable battery for portability. Data is transmitted via USART to a RX and TX pin wire to a PC for further analysis. This setup ensures efficient signal acquisition, processing, and real-time transmission, making the system both flexible and reliable for EEG data monitoring.

#### 4.4.4 Core ECE Design Tasks

- **ECE 26400:** Advanced C.
- **ECE 36200:** GPIO, ADC, UART, Bluetooth.

#### 4.4.5 Schematics

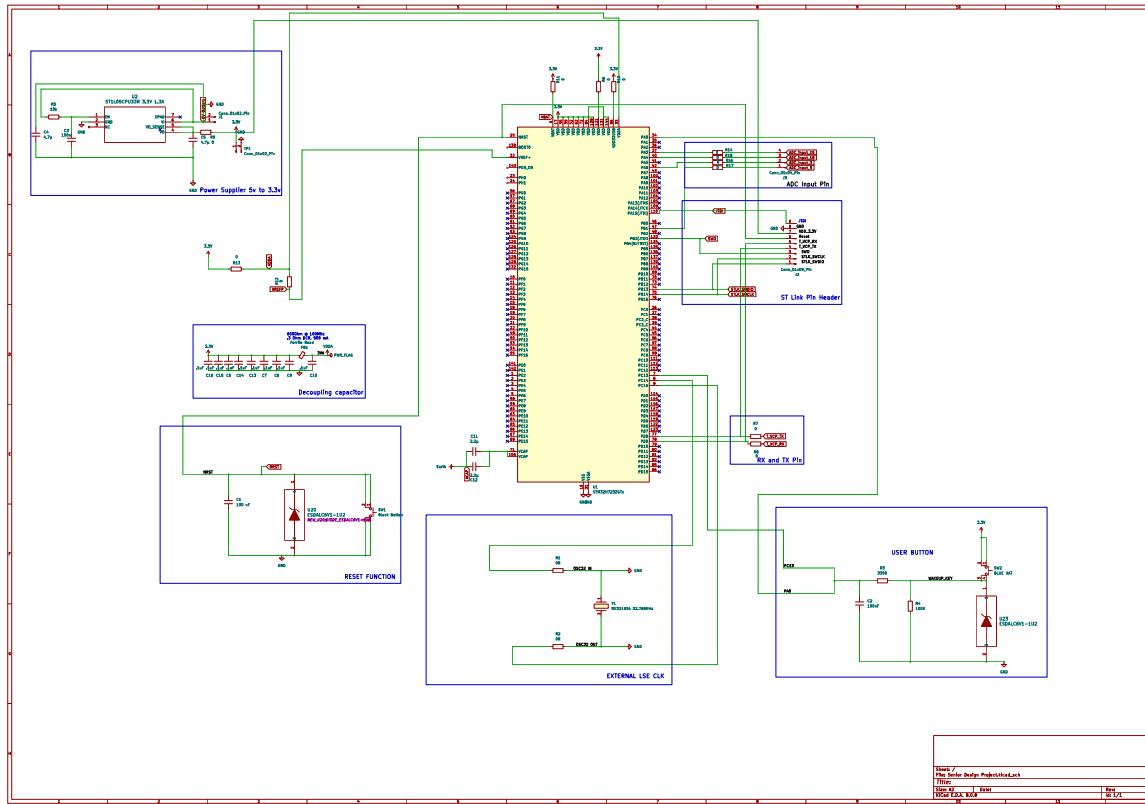


Figure 4.4.2: Schematic for Microcontroller Subsection

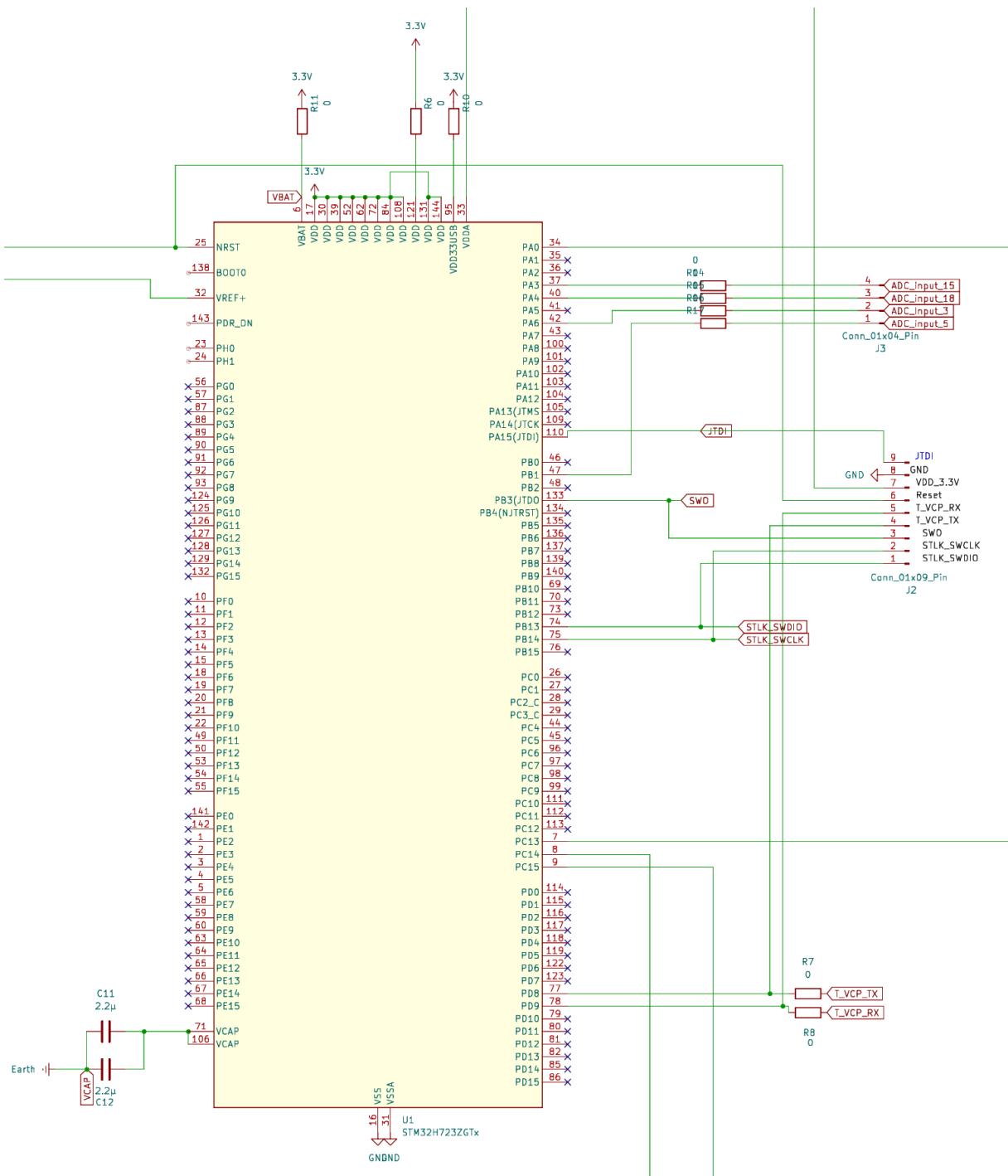


Figure 4.4.3: STM32H723ZG Schematic

#### 4.4.6 Parts

- MCU: STM32 NUCLEO-H723ZG

#### 4.4.7 Algorithm

[The system starts by powering on the STM32 NUCLEO-H723ZG microcontroller, which runs on a rechargeable battery to ensure portability. Once powered, the ADC, UART, and Bluetooth module are initialized. The EEG circuit captures brain signals in analog form, which the ADC converts into digital data for the microcontroller. The MCU processes this data, performing any necessary filtering or adjustments before sending it to the Bluetooth module via UART. The Bluetooth module then wirelessly transmits the data to a PC, where it can be analyzed in real time. This continuous process ensures efficient and reliable EEG signal monitoring.]

#### 4.4.8 Theory of Operation

The operational framework of the microprocessor subsystem centers on the STM32H7 microcontroller unit (MCU), which serves as the core for signal processing and communication within the brain-computer interface (BCI) system. The MCU orchestrates data exchange with a host PC, manages power regulation, digitizes analog EEG signals via its integrated Analog-to-Digital Converter (ADC), and supports programming and debugging through a dedicated interface.

**UART Communication with the PC:** The STM32H7 communicates with the PC using the Universal Asynchronous Receiver/Transmitter (UART) protocol, a widely adopted standard for serial data exchange between devices. This asynchronous protocol relies on two primary signal lines: the **Transmit (TX)** line, which outputs data from the MCU to the PC, and the **Receive (RX)** line, which inputs data from the PC to the MCU. The TX pin of the STM32H7 connects to the RX pin of the PC interface, and vice versa, forming a bidirectional link. Operating without a shared clock signal, UART transmits data bit-by-bit at a predetermined baud rate, set to 115,200 bits per second in this implementation. This high baud rate ensures efficient transfer of digitized EEG data to the PC for real-time processing, leveraging the STM32H7's dedicated UART pins for reliable, low-latency communication.

**Power Regulation:** The MCU is powered by a 3.3 V supply derived from an external 5 V battery source via the ST1L05CPU33R, a low-dropout (LDO) linear voltage regulator from STMicroelectronics. The 5 V input enters through connector J1 (pin 2, with pin 1 grounded) and is filtered by a 100  $\mu$ F capacitor (C3) to suppress noise at the regulator's input (VI, pin 6). The enable pin (EN, pin 1) is pulled high to 5 V through a 10 k resistor (R5), activating the regulator, with a 4.7  $\mu$ F capacitor (C4) stabilizing this control line. The regulator outputs a stable 3.3 V (VO, pin 4), filtered by a 4.7  $\mu$ F capacitor (C5) and delivered to the MCU via a 0 resistor (R9) and connector TP1 (pin 1, with pin 2 grounded).

The VO\_SENSE pin (pin 5) monitors the output voltage for precise regulation, while the exposed pad (EPAD, pin 7) is grounded to dissipate heat from the 1.7 V drop, supporting a current capacity of up to 1.3 A. This LDO design prioritizes low noise and simplicity over the efficiency of switching converters, making it ideal for powering the noise-sensitive MCU in this EEG application.

**ADC Signal Acquisition:** The MCU interfaces with analog EEG signals through a 4-pin header (J3, Conn\_01x04\_Pin), connecting to the STM32H7's high-resolution ADC channels. Pin 1 (ADC\_In\_5), pin 2 (ADC\_In\_3), pin 3 (ADC\_In\_18), and pin 4 (ADC\_In\_15) correspond to ADC channels 5, 3, 18, and 15, respectively, enabling simultaneous digitization of multiple EEG inputs. Each line includes a 0 resistor (R14, R15, R16, R17) in series, providing a direct connection with the flexibility to insert filtering components or isolate signals for debugging without PCB redesign. These resistors also serve as test points for signal probing or injection, enhancing design adaptability and manufacturability. The ADC converts the conditioned EEG signals—previously amplified and filtered by the EEG circuit—into digital data at a sampling rate suitable for real-time mouse control, meeting the system's latency target of under 1 second.

**ST-Link Debugging Interface:** Programming and debugging of the STM32H7 are facilitated by the ST-Link pin header (J2, Conn\_01x09\_Pin), which employs the Serial Wire Debug (SWD) protocol alongside Virtual COM Port (VCP) functionality. Pin 1 (STLK\_SWDIO) handles bidirectional data exchange, while pin 2 (STLK\_SWCLK) provides the clock signal for synchronized communication between the MCU and the ST-Link debugger. Pin 3 (SWO) supports Serial Wire Viewer (SWV) for real-time trace output, enhancing debugging capabilities. Pins 4 (T\_VCP\_TX) and 5 (T\_VCP\_RX) enable VCP communication, transmitting and receiving serial data to/from the PC via the ST-Link, respectively. Pin 6 (Reset) connects to the MCU's reset line for controlled restarts, while pins 7 (VDD\_3.3V) and 8 (GND) supply power and ground reference. Pin 9 (JTDI), reserved for JTAG, remains unused in this SWD configuration. This robust interface ensures efficient firmware development, testing, and deployment.

In summary, the STM32H7 MCU integrates UART communication for PC data exchange, a regulated 3.3 V power supply for operational stability, ADC channels for EEG signal digitization, and an ST-Link interface for development support. This architecture enables the MCU to process and transmit EEG data wirelessly via a Bluetooth module (connected through UART), fulfilling the subsystem's role in translating brain signals into real-time computer commands.

#### 4.4.9 Specifications Measurement

[**DD3+** Every specification here should match the specification above. ]

1. USART Communication

- (a) USART must be able to send 4 data channels via Rx and Tx from the MCU to PC.

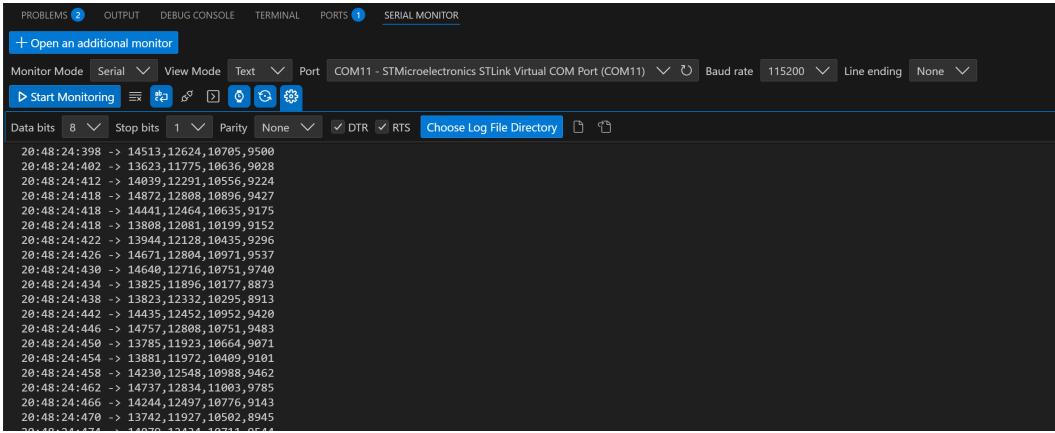


Figure 4.4.4: USART Serial Terminal

```

392 static void MX_USART3_UART_Init(void)
393 {
394
395     /* USER CODE BEGIN USART3_Init_0 */
396
397     /* USER CODE END USART3_Init_0 */
398
399     /* USER CODE BEGIN USART3_Init_1 */
400
401     /* USER CODE END USART3_Init_1 */
402     huart3.Instance = USART3;
403     huart3.Init.BaudRate = 115200;
404     huart3.Init.WordLength = UART_WORDLENGTH_8B;
405     huart3.Init.StopBits = UART_STOPBITS_1;
406     huart3.Init.Parity = UART_PARITY_NONE;
407     huart3.Init.Mode = UART_MODE_TX_RX; // Line 407
408     huart3.Init.HwFlowCtl = UART_HWCONTROL_NONE;
409     huart3.Init.OverSampling = UART_OVERSAMPLING_16;
410     huart3.Init.OneBitSampling = UART_ONE_BIT_SAMPLE_DISABLE;
411     huart3.Init.ClockPrescaler = UART_PRESCALER_DIV1;
412     huart3.AdvancedInit.AdvFeatureInit = UART_ADVFEATURE_NO_INIT;

```

Figure 4.4.5: USART MCU code

- (b) Here we see that the serial terminal port is reading in 4 values at once, and is configured to the same serial parameters. The baud rate being sent and received is 115200, the data bits are both 8, the stop bits is 1, and the parity is none.

## 2. Sampling Rate

- (a) Achieve a sampling rate of 250 Hz for 4-channel sampling

```
PS C:\Users\jaspe\BCI_Senior_Design> python .\src\data_input\test_in.py
Sampling Rate: 250 samples/sec
```

Figure 4.4.6: Sampling rate on MCU

```
for (int i = 0; i < 4; i++) {
    HAL_ADC_Start(&hadc1);
    HAL_ADC_PollForConversion(&hadc1, HAL_MAX_DELAY);
    adcValues[i] = HAL_ADC_GetValue(&hadc1);
}

snprintf(buffer, sizeof(buffer), "%u,%u,%u,%u\r\n",
          adcValues[0], adcValues[1], adcValues[2], adcValues[3]);
HAL_UART_Transmit(&huart3, (uint8_t*)buffer, strlen(buffer), 10);

if (HAL_GetTick() - startTick >= 1000) {
    sprintf(samplingMsg, "Sampling Rate: %u samples/sec\n", adcConversionCount);
    HAL_StatusTypeDef status = HAL_UART_Transmit(&huart3, (uint8_t*)samplingMsg, strlen(samplingMsg), 10);
    adcConversionCount = 0;
    startTick = HAL_GetTick();
}
```

Figure 4.4.7: Sampling rate on MCU calculations

- (b) As you can see, the intended sampling rate of 250 Hz is met. The code above samples 4 channels in the for loop and sends those channels of data via USART. During this process, the number of samples being taken for each channel is incremented. Every second, the total samples taken for each channels is sent as a message via USART to display on the PC, seen in the first image.

### 3. Bit Rate

- (a) Achieve a 16-bit rate for ADC

```
PS C:\Users\jaspe\BCI_Senior_Design> python .\test_bitrate.py
ADC Value for 4 Channels: 65536, 65536, 65536, 65536
Bit-Rate for 4 Channels: 16.000, 16.000, 16.000, 16.000

ADC Value for 4 Channels: 65536, 65536, 65536, 65536
Bit-Rate for 4 Channels: 16.000, 16.000, 16.000, 16.000

ADC Value for 4 Channels: 65536, 65536, 65536, 65529
Bit-Rate for 4 Channels: 16.000, 16.000, 16.000, 16.000

ADC Value for 4 Channels: 65237, 65536, 65536, 65536
Bit-Rate for 4 Channels: 15.993, 16.000, 16.000, 16.000

ADC Value for 4 Channels: 65536, 65536, 65005, 65536
Bit-Rate for 4 Channels: 16.000, 16.000, 15.988, 16.000

ADC Value for 4 Channels: 65536, 65536, 65536, 65141
Bit-Rate for 4 Channels: 16.000, 16.000, 16.000, 15.991

ADC Value for 4 Channels: 65536, 65121, 65536, 65536
Bit-Rate for 4 Channels: 16.000, 15.991, 16.000, 16.000

ADC Value for 4 Channels: 65158, 65536, 65536, 65536
Bit-Rate for 4 Channels: 15.992, 16.000, 16.000, 16.000

ADC Value for 4 Channels: 65536, 65536, 65536, 65093
Bit-Rate for 4 Channels: 16.000, 16.000, 16.000, 15.990
```

Figure 4.4.8: Bit Rate and ADC Value for MCU calculations

#### 4. DC Offset

- Adjust the DC Offset to about 1.080V.



Figure 4.4.9: DC Offset Value after adding a high-pass filter and voltage divider

#### 4.4.10 Standards

- **USART Communication Standard:** Universal Synchronous/Asynchronous Receiver/Transmitter.
- **ADC Standard IEEE 1241-2010:** Defines performance specifications and test methods for Analog-to-Digital Converters (ADC) to ensure accurate and high-quality signal conversion.

## 5 PCB Design

### 5.1 PCB Schematics

The PCB schematics integrate the EEG circuit, power supply, and microcontroller subsystems into a cohesive design for the brain-computer interface (BCI) system. These schematics, developed based on the subsystem designs in Section 4, detail the electrical connections and signal flow necessary for EEG signal acquisition, conditioning, and digitization. Figure 5.1.1 provides an overview of the four-channel EEG circuit, while Figures 5.1.2, 5.1.3, 5.1.4, and 5.1.5 break down specific subsections, illustrating the power supply, EEG channels, and output to the ADC converter.

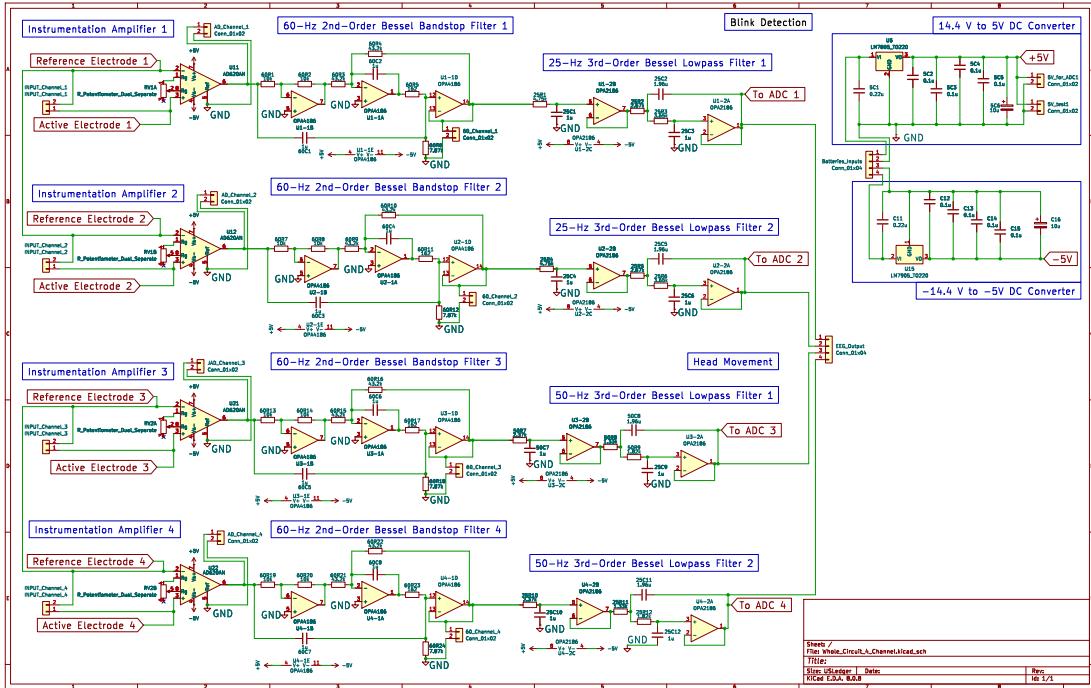


Figure 5.1.1: Schematic for power and EEG circuit subsection, showing the complete four-channel EEG circuit with power and signal processing components.

This schematic (Figure 5.1.1) integrates the EEG headpiece, instrumentation amplifier, filters, and microcontroller, providing a top-level view of the PCB's electrical design.

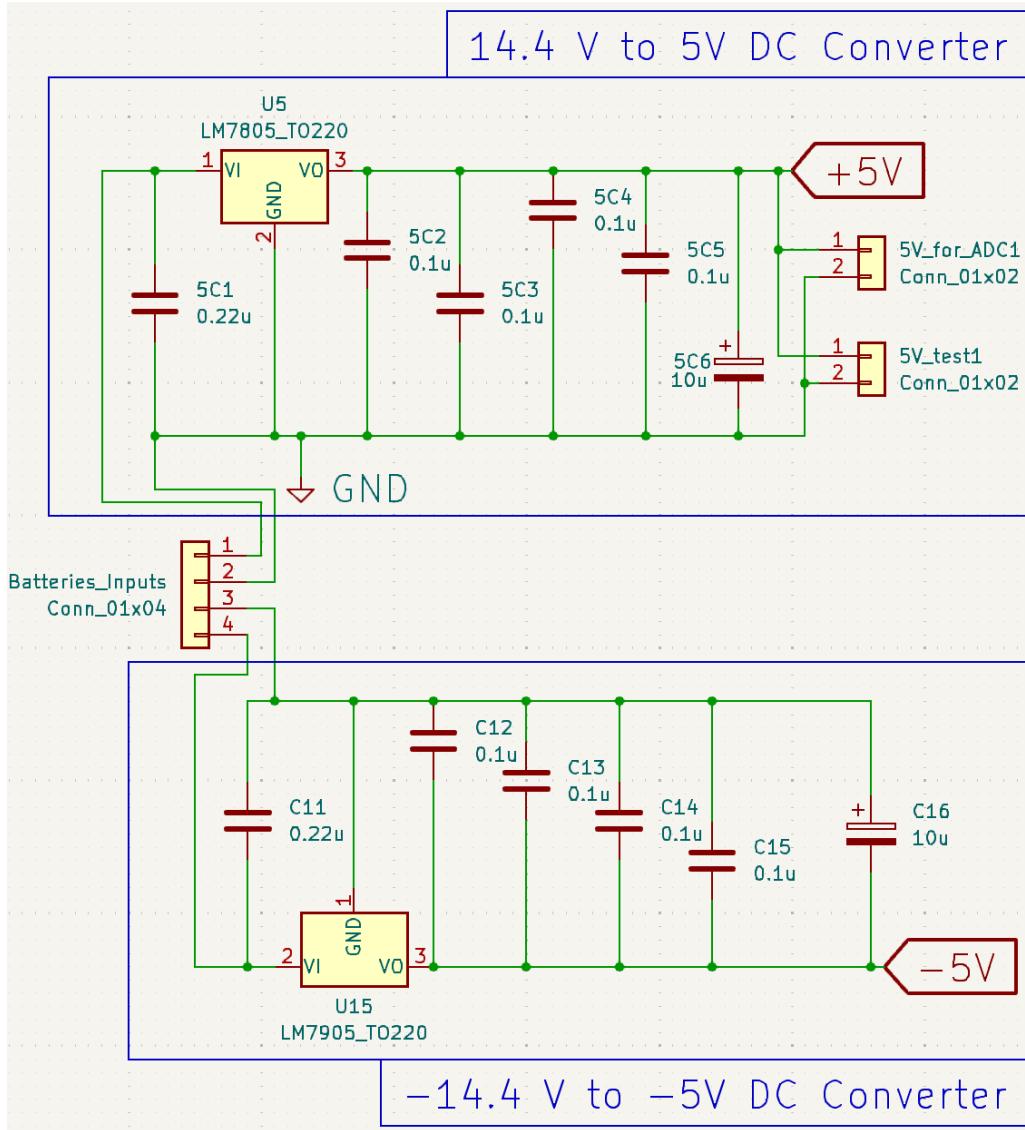


Figure 5.1.2: 14.4V batteries generating positive and negative 5V to power the EEG circuit and instrumentation amplifier.

The power section (Figure 5.1.2) converts a 14.4V battery input into dual  $\pm 5V$  outputs, ensuring stable power for the AD620AN instrumentation amplifier (Section 4.3) and OPA4186 op-amps in the EEG circuit (Section 4.2).

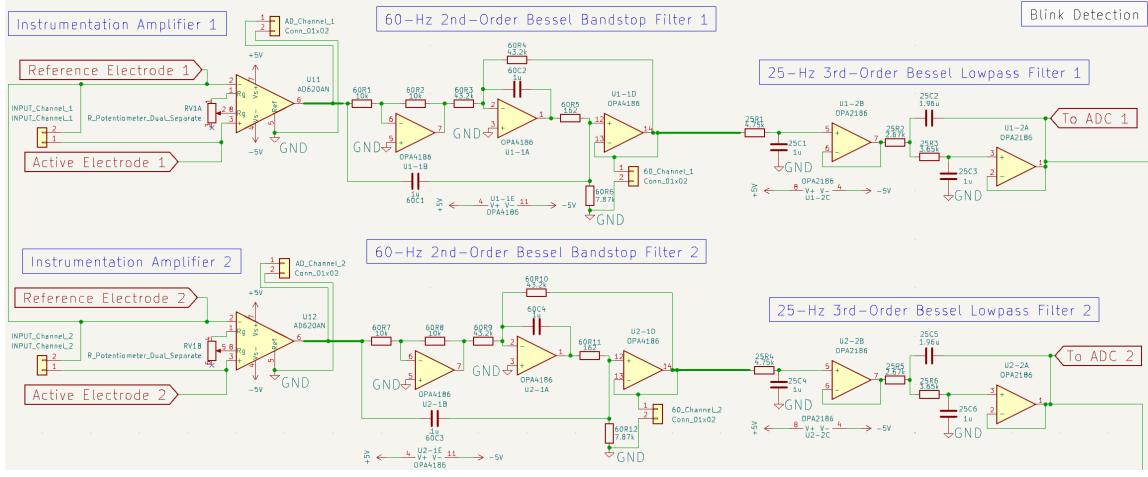


Figure 5.1.3: EEG circuit channels 1 and 2 with 25 Hz low-pass filters for focusing on lower EEG frequency bands.

Channels 1 and 2 (Figure 5.1.3) implement the 25 Hz low-pass filter (Section 4.2.2), attenuating frequencies above 25 Hz to prioritize Delta, Theta, and Alpha bands, critical for applications like sleep monitoring.

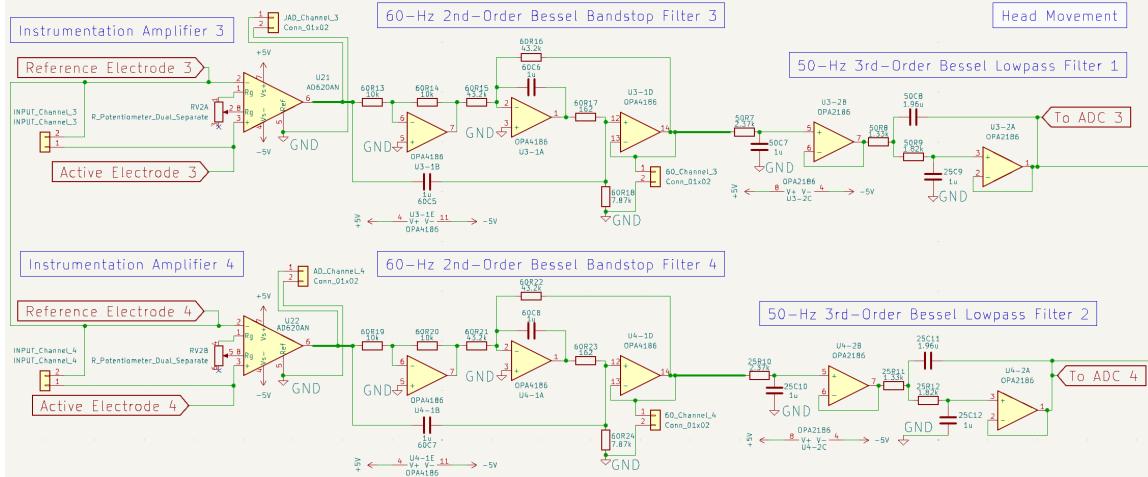


Figure 5.1.4: EEG circuit channels 3 and 4 with 50 Hz low-pass filters for preserving EEG bands up to Beta.

Channels 3 and 4 (Figure 5.1.4) incorporate the 50 Hz low-pass filter (Section 4.2.2),

preserving EEG signals up to the Beta band while removing high-frequency noise, suitable for general EEG analysis.

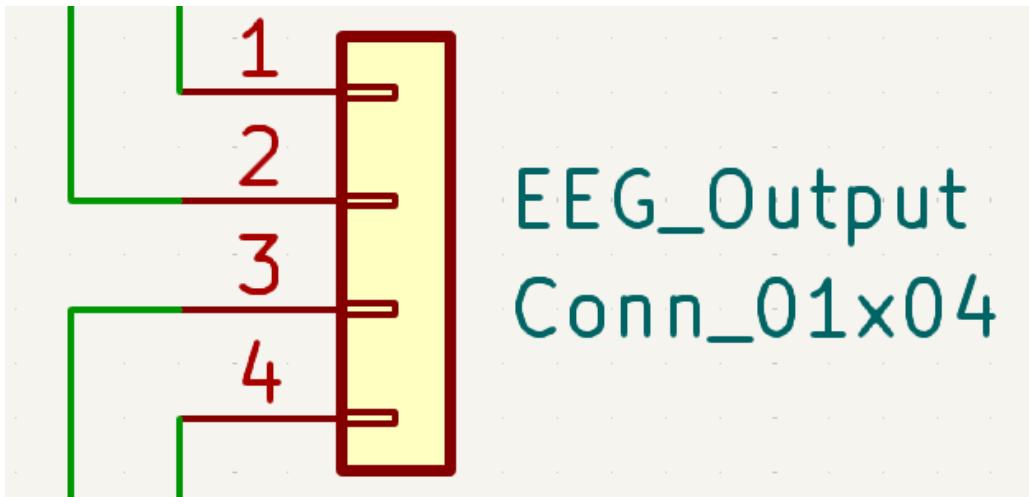


Figure 5.1.5: EEG circuit output to the ADC converter, interfacing with the STM32H723ZG microcontroller.

The EEG output schematic (Figure 5.1.5) connects the filtered EEG signals to the ADC of the STM32H723ZG microcontroller (Section 4.4), enabling digitization and transmission of brain signals to the PC for processing.

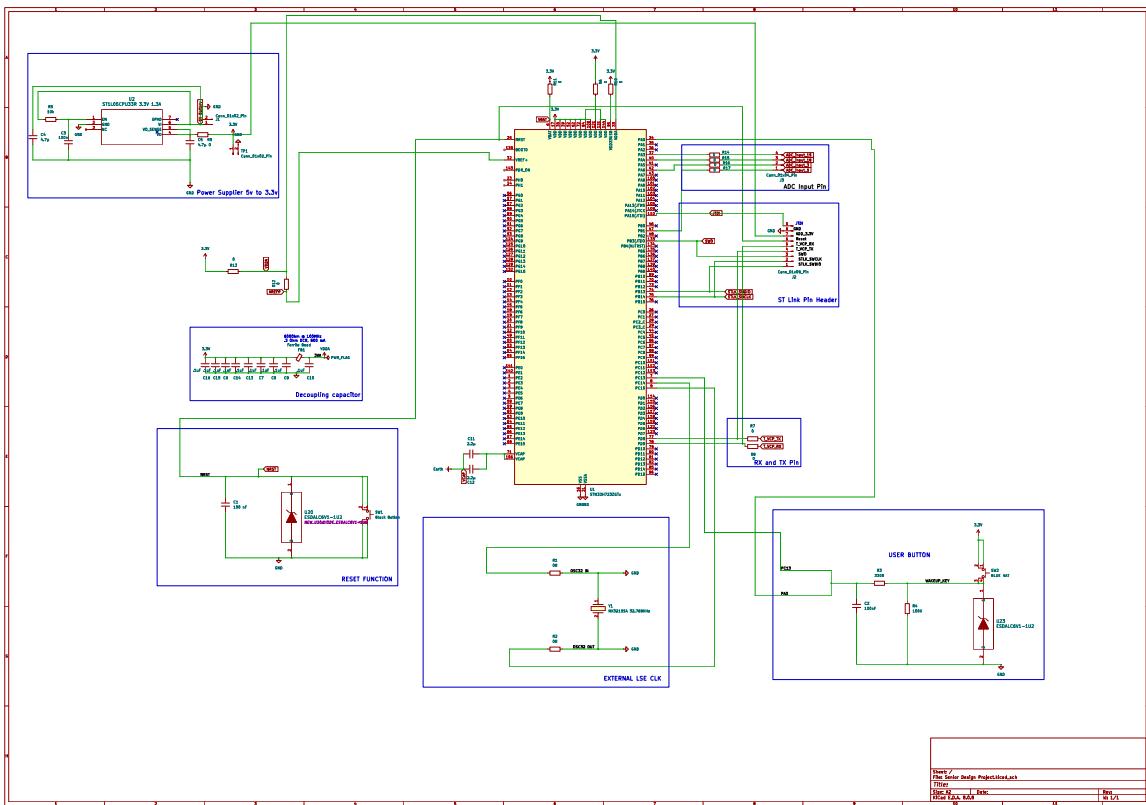


Figure 5.1.6: Schematic for Microcontroller Subsection

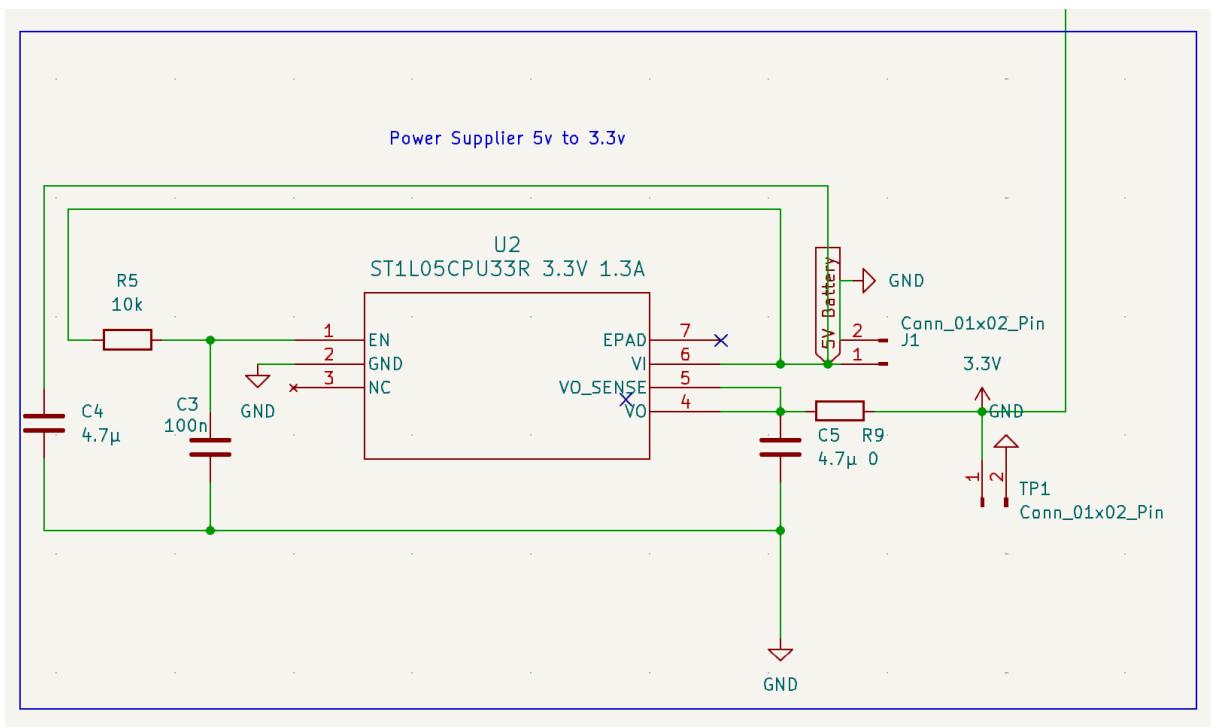


Figure 5.1.7: MCU 5V to 3.3V Power Supply

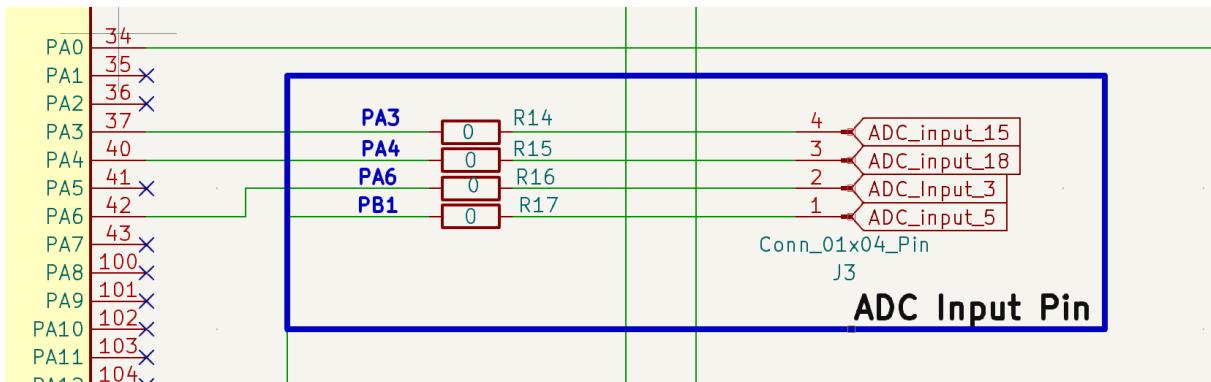


Figure 5.1.8: Schematic for ADC Input Pin

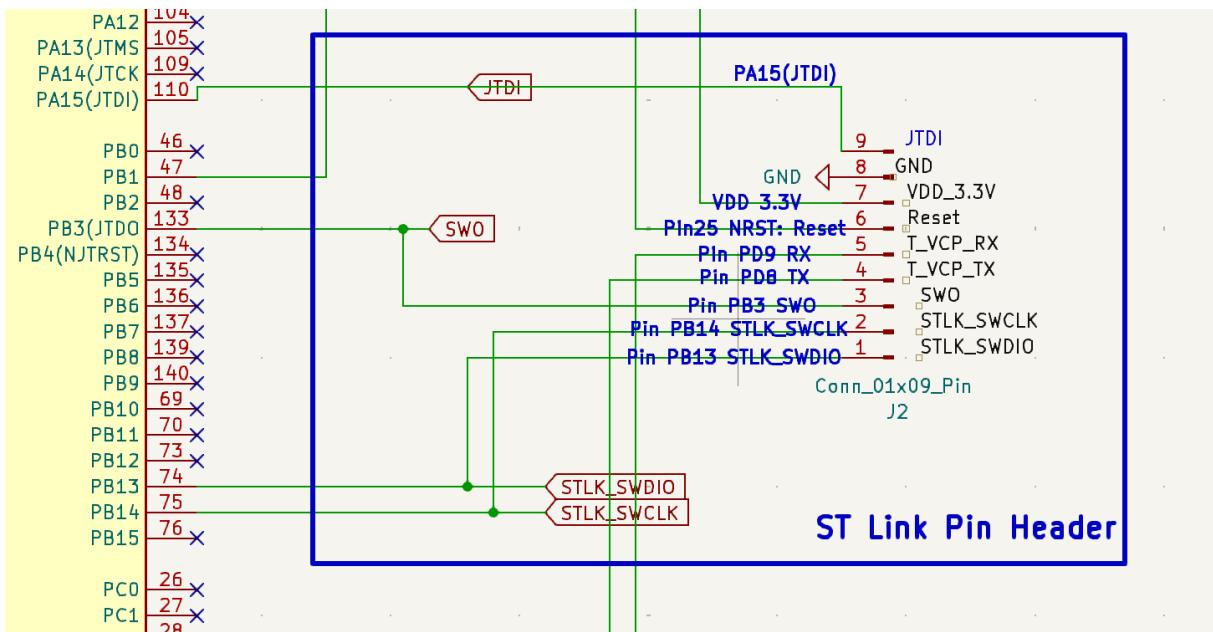


Figure 5.1.9: Schematic for STlink Input Pin

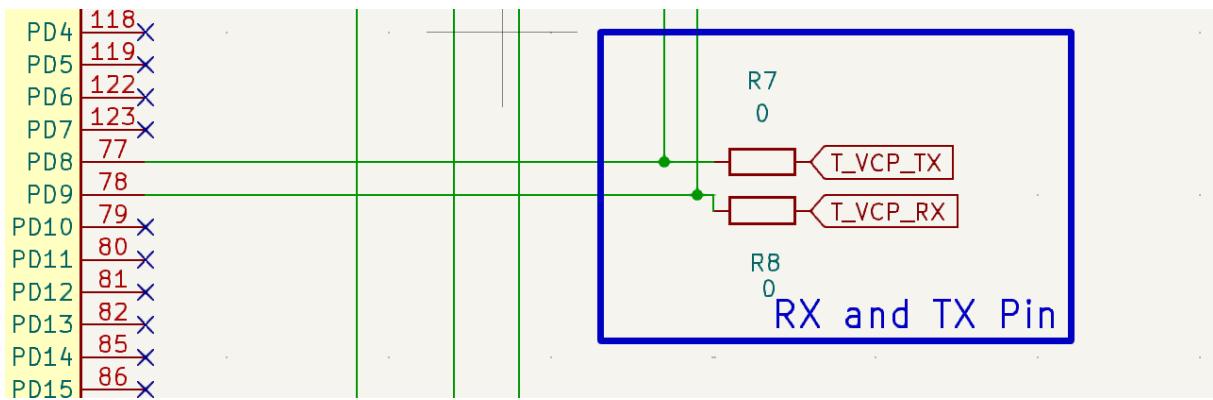


Figure 5.1.10: Schematic for RX and TX Pin

## 5.2 PCB Layout

The PCB layout translates the electrical schematics (Section 5.1) into a physical design, arranging components and traces to ensure functionality, signal integrity, and manufacturability of the brain-computer interface (BCI) system. The layouts were designed to optimize space, minimize noise in EEG signal paths, and provide stable power distribution. Figure 5.2.1 illustrates the layout for the four-channel EEG circuit subsection, while Figure 5.2.2 details the power supply layout supporting both the EEG circuits and microcontroller subsections.

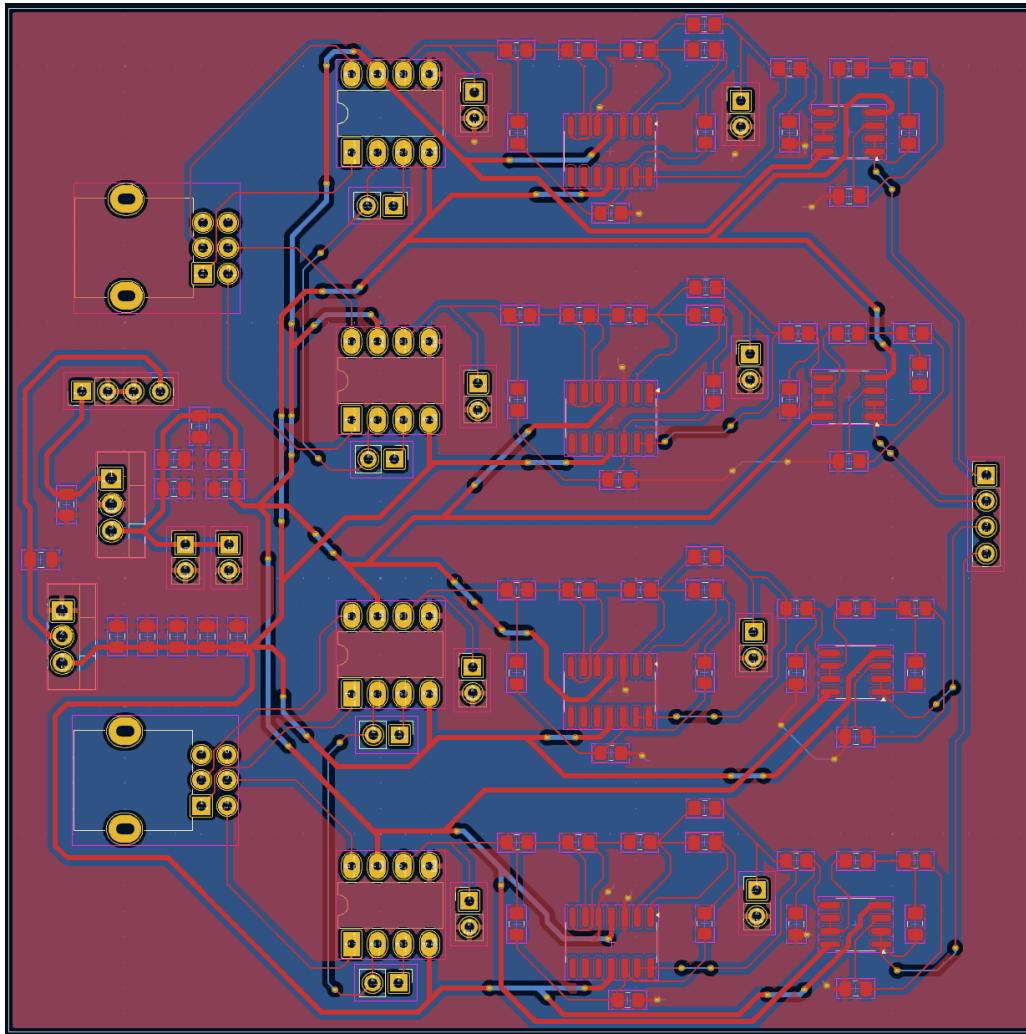


Figure 5.2.1: PCB for four channel EEG circuit subsection, showing the physical arrangement of components for EEG signal acquisition and filtering.

This layout (Figure 5.2.1) implements the four-channel EEG circuit (Figures 5.1.1, 5.1.3, 5.1.4), placing the AD620AN instrumentation amplifier, OPA4186 op-amps, and associated filters (Section 4.2) to minimize noise and ensure efficient signal routing across channels 1–4.

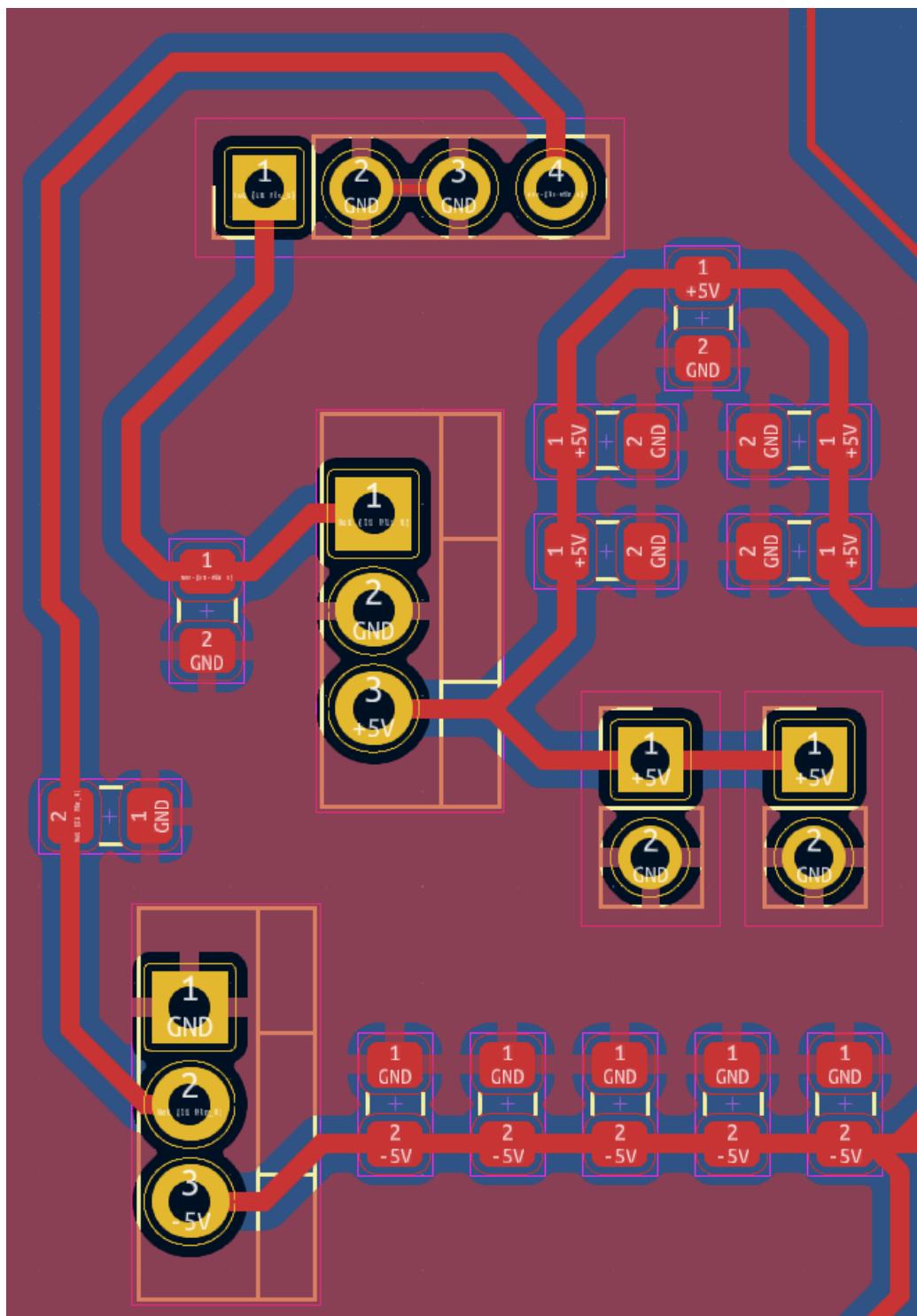


Figure 5.2.2: Power supply for EEG circuits subsection and microcontroller subsection, providing  $\pm 5V$  from a 14.4V battery input.<sup>76</sup>

The power supply layout (Figure 5.2.2) corresponds to the schematic in Figure 5.1.2, positioning components to deliver  $\pm 5V$  to the EEG circuit (Section 4.2) and STM32H723ZG microcontroller (Section 4.4), with careful trace routing to reduce power noise and ensure stable operation.

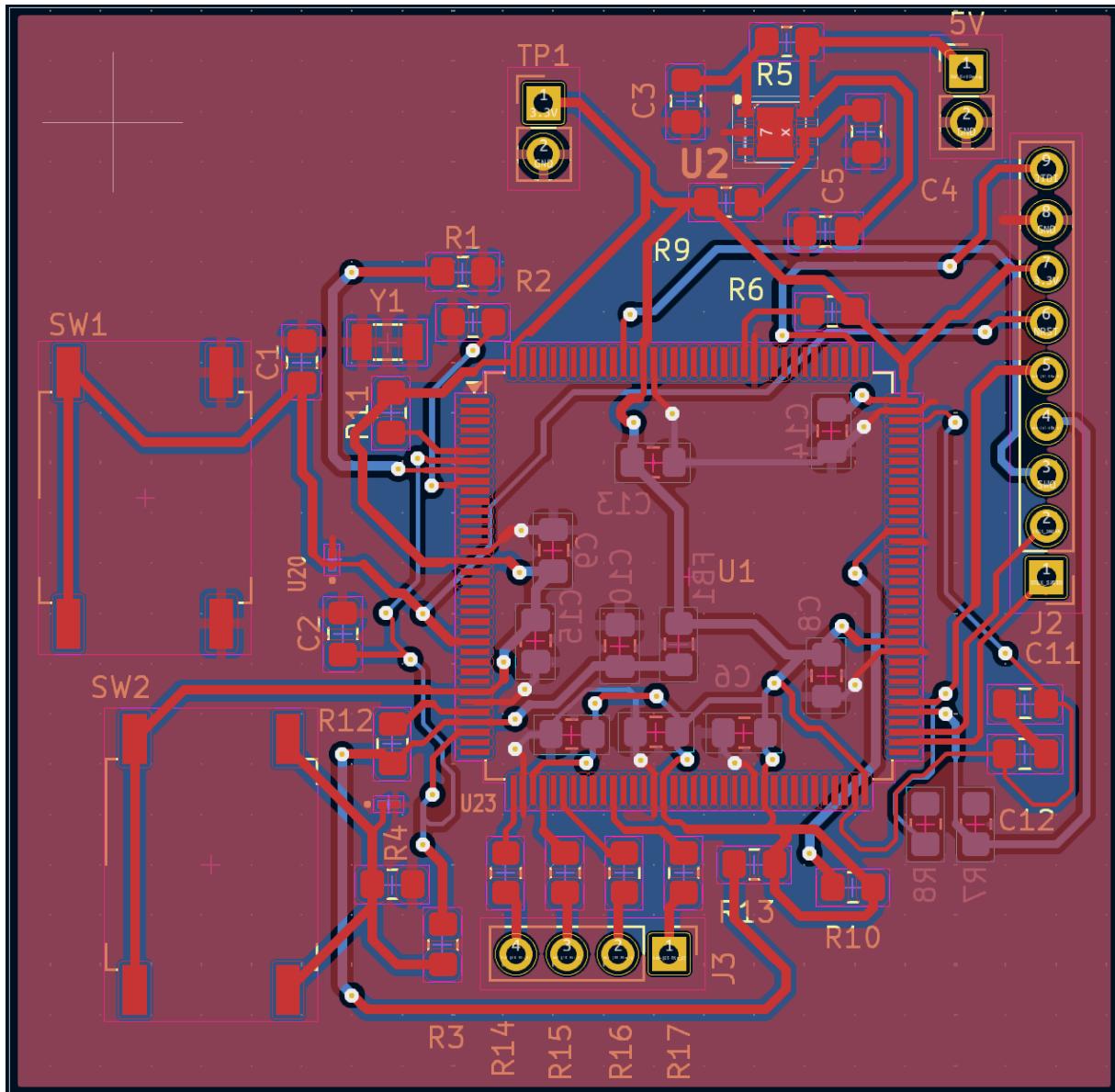


Figure 5.2.3: PCB for Microcontroller Subsection

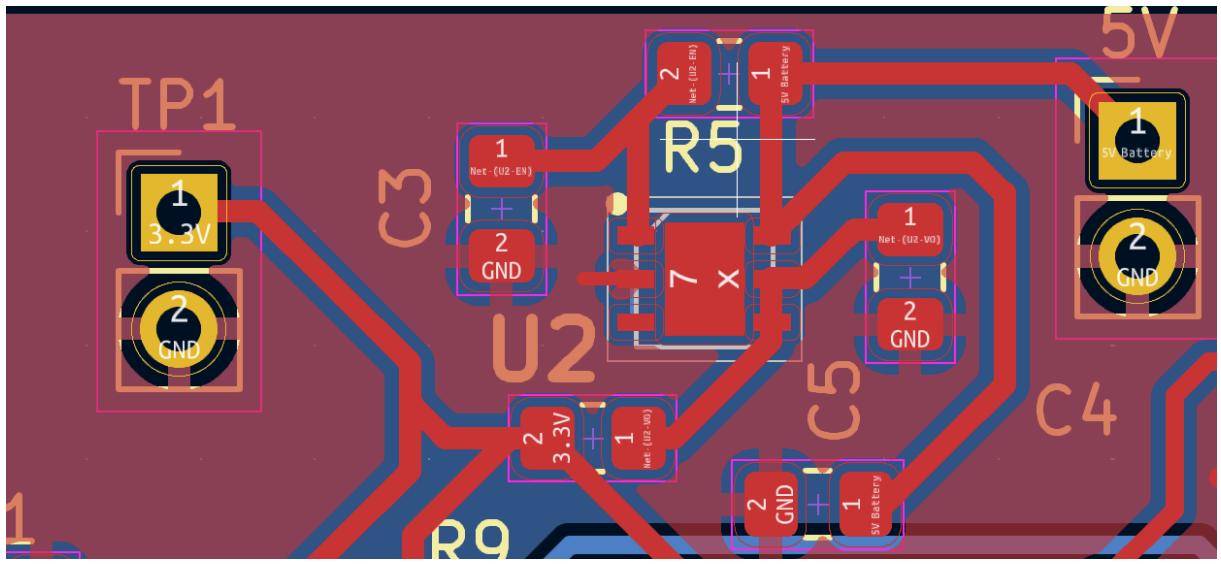


Figure 5.2.4: PCB for MCU 5V to 3.3V Power Supply

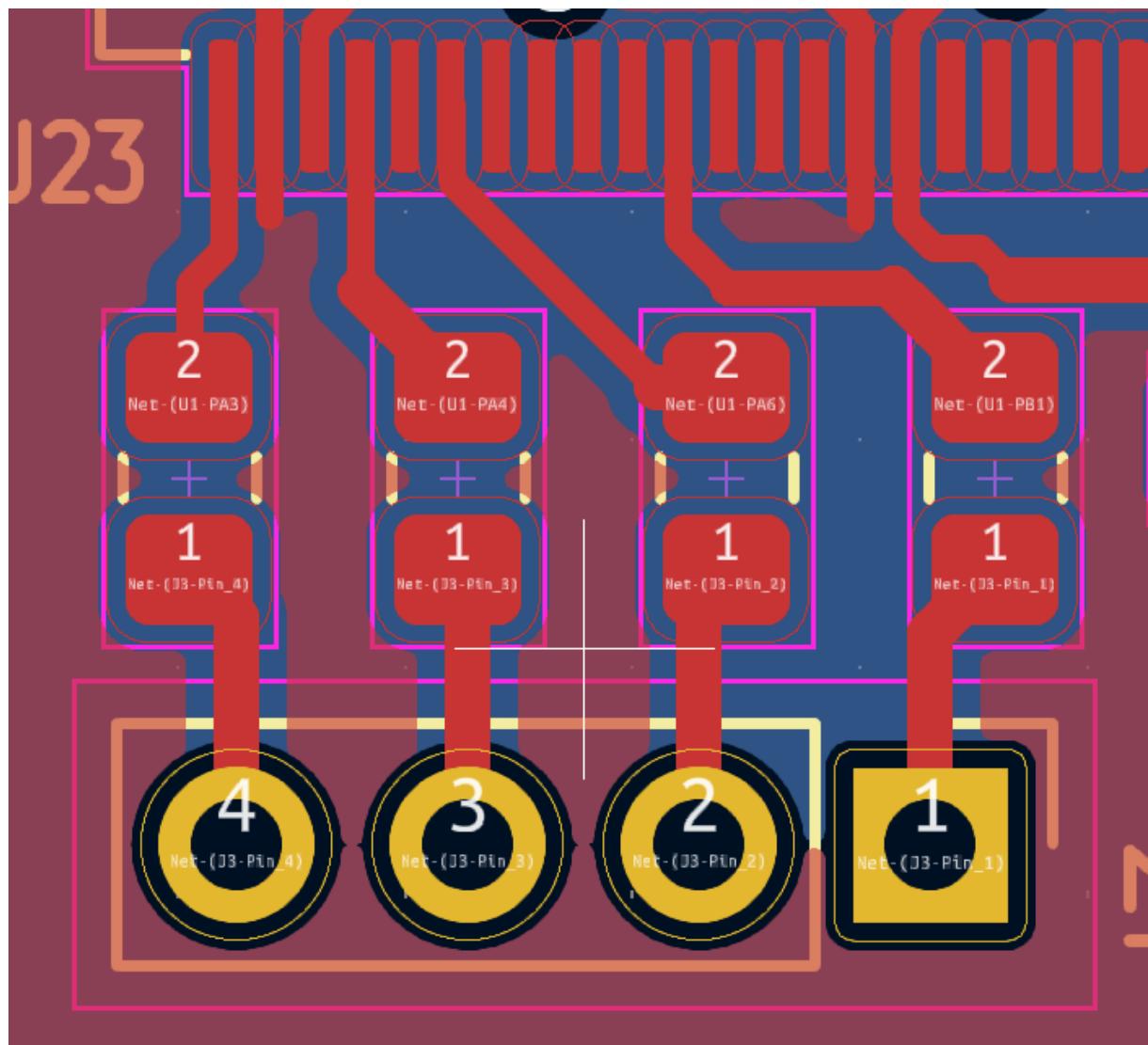


Figure 5.2.5: PCB for ADC Input Pin



Figure 5.2.6: Schematic for STlink Input Pin

## 6 Final Status of Requirements

[**DD3+**] [If met, give a detailed explanation of the requirement. If partially met, mention what has been met and a reason for why the complete requirement couldn't be achieved. If not met, give an explanation for why the requirement couldn't be met in the product. Add as many requirements as you had in your earlier design documents here. ]

1. Requirement 1: [Copy your requirement above here]

**Met:** [Explanation]

2. Requirement 2: [Copy your requirement above here]

**Partially Met:** [Explanation]

3. Requirement 3: [Copy your requirement above here]

**Not Met:** [Explanation]

The following evaluates the EEG Circuit subsystem's filter specifications (Section 4.2.2) against Frequency Response Analysis (FRA) results, as these directly impact the system's ability to process clean EEG signals for meeting high-level requirements like action classification accuracy (Section 2.1). Each specification's status is assessed based on measurements in Section 4.2.9, with supporting figures where available.

1. **60 Hz Notch Filter Specification:** The notch filter must be tuned to 60 Hz, provide at least 30–40 dB attenuation at 60 Hz, have a narrow bandwidth (59–61 Hz), and exhibit minimal phase distortion.

**Met:** The FRA results (Figure 4.2.5) confirm that the filter achieves -43.149 dB attenuation at 62.892 Hz, exceeding the required 30–40 dB, and the center frequency is effectively tuned to 60 Hz. The bandwidth is sufficiently narrow for practical purposes, as the attenuation at 50 Hz is -43.01208 dB, and measurements indicate the filter performs as expected. Phase distortion is minimal in the passband (0.5–50 Hz), with the phase stable below 50 Hz despite a transition near 60 Hz (-71.26555° at 50 Hz), meeting the requirement. This filter successfully removes 60 Hz powerline interference, supporting accurate EEG signal acquisition.

2. **25 Hz Low-Pass Filter Specification:** The filter must have a cutoff frequency of approximately 25 Hz, a minimum second-order design with at least -40 dB/decade roll-off, minimal phase distortion, and a flat passband response below 25 Hz.

**Met:** The filter was designed and implemented with schematics (Figure 4.2.3) and PCB layouts (Figures 5.1.3, 5.2.1). FRA measurements (Figure 4.2.6) confirm the cutoff frequency at approximately 25 Hz, as the -3 dB point aligns with the specification. The roll-off, phase distortion, and passband response also meet the requirements, with at least -40 dB/decade roll-off, minimal phase distortion in the passband (0.5–20 Hz), and a flat response below 25 Hz. This filter effectively focuses

on lower EEG frequency bands (Delta, Theta, Alpha), supporting applications like sleep monitoring.

3. **50 Hz Low-Pass Filter Specification:** The filter must have a cutoff frequency of approximately 50 Hz, a minimum second-order design with at least -40 dB/decade roll-off, minimal phase distortion, and a flat passband response below 50 Hz.

**Not Met:** Although the filter was implemented with schematics (Figure 4.2.4) and PCB layouts (Figures 5.1.4, 5.2.1), FRA measurements indicate that the filter does not meet the specification. An FRA plot (Figure 4.2.5, used for the 60 Hz notch filter) shows a flat response at 50 Hz (-0.00126 dB on channel C1), far from the expected -3 dB cutoff, confirming the cutoff frequency is not at 50 Hz. This misalignment likely affects the roll-off, phase distortion, and overall performance, potentially due to incorrect component values (e.g., resistors, capacitors in Section 4.2.6) or PCB layout issues (e.g., trace interference, grounding problems). The failure to achieve the correct cutoff frequency impacts the filter's ability to preserve EEG signals up to the Beta band while removing high-frequency noise, which may affect overall system accuracy.

## 7 Team Structure

### 7.1 Team Member 1



**Jasper Koliba**

Major: Computer Engineering

Contact: jkoliba@purdue.edu

Team Role: Software algorithms and UI design

Bio: I am graduating this semester and will be working as a data scientist this summer. I am looking forward to showcasing and continue to develop my skills in building algorithms, classifying data, and designing software applications.

### 7.2 Team Member 2



**Jing-Siang (Alex) Cheng**

Major: Electrical Engineering

Contact: cheng594@purdue.edu

Team Role: Headpiece and Amplifier of EEG circuit

Bio: I plan to go into semiconductor industry after graduation, and I enjoy travel and sports outside of school.

### 7.3 Team Member 3



**Hao Yang**

Major: Electrical Engineering

Contact: yang2342@purdue.edu

Team Role: System power and filters of EEG circuit

Bio: Interested in designing circuits that meet functional expectations and user needs.

### 7.4 Team Member 4



**Yoshiki Takeuchi**

Major: Electrical Engineering

Contact: ytakeuch@purdue.edu

Team Role: Microprocessor

Bio: I am half Japanese and Taiwanese and currently a BSEE student concentrating on semiconductor and microelectronics.

## **8 Bibliography**

[Here are some examples. IEEE format can be found on [Purdue OWL.](#) ]

## **References**

- [1] “Data Platform – Open Power System data,” Apr. 15, 2020. [https://data.open-power-system-data.org/household\\_data/](https://data.open-power-system-data.org/household_data/)
- [2] Author, ”Title,” *Journal*, volume, number, page range, month year, DOI.
- [3] Author. ”Page.” Website. URL(accessed month day,year)

## **9 Appendices**

[This section is mainly designed for codes. You can directly generate a somewhat decent display of your code file or psuedo code by using the template provided below. You can have as many appendix as you want. In the document, you can refer to the code posted here instead of pasting the whole code in the body. ]

### **9.1 Appendix A: [Appendix Name]**

```
print ("Hello - World")
```