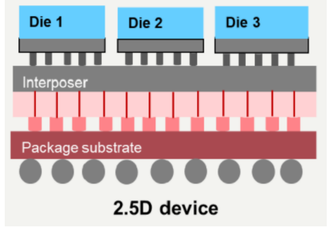
Methods for securing commercial dies in silicon substrates for heterogenous integration

PinChen Su(su363@purdue.edu), Chun-Kang Huang (huan1704@purdue.edu), Takeuchi Yoshiki(ytakeuch@purdue.edu), Aadi Wu (wu2091@purdue.edu), Ying-Wei Lin (lin1990@purdue.edu)
Co-author: Mary Vaughan, Dr. Bermel, Dr. Mohammadi
Birck Nanotechnology Center, Elmore Family School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN, USA

SCALE
SCalable Asymmetric Lifecycle Engagement
Developing the U.S. Defense Microelectronics Workforce

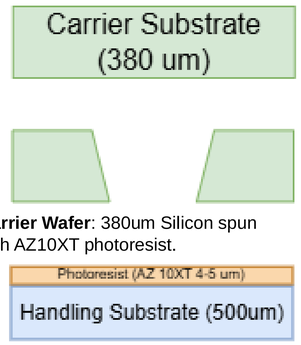
Background

- **Heterogeneous Integration** allows for separately manufactured chips and passive components to be packaged together into a single device, improving performance and scalability.
- **2.5D Heterogeneous Integration** uses a single interposer to combine chips side-by-side.
- **Objects:** Chips are embedded into our silicon interposer and electrically interconnected with aluminum. Copper covers the chips for electromagnetic shielding.
- **Goal:** Implementing improved density, performance, and interconnectivity for applications in low-orbit satellites.



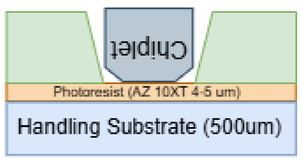
General Heterogeneous Integration [1]

Process

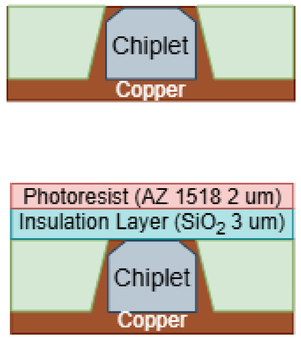


Carrier Wafer: 380um Silicon spun with AZ10XT photoresist.

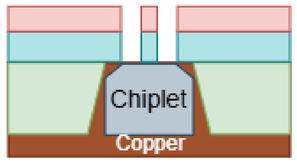
Deposition:
Deposit a 100nm seed layer of Cu



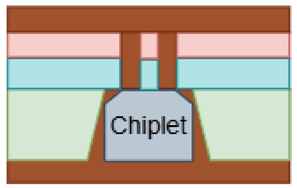
Electroplating:
- The metal seed layer serves as a cathode, enabling the vertical growth of copper, which fills the gap and secures the chiplets in place.



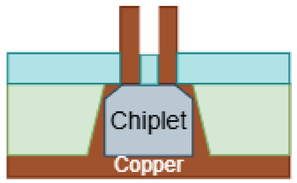
SiO2 Deposition:
- After the handling wafer has been removed, an insulating layer is added to prevent shorting.



SiO2 Etch:
- Patterning and etching through the insulator to expose contacts.



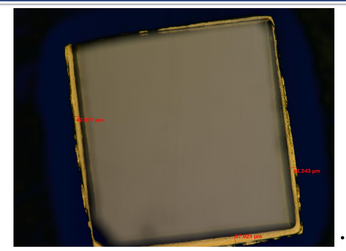
Metallization
- interconnects are created between the dies with aluminum.



Results

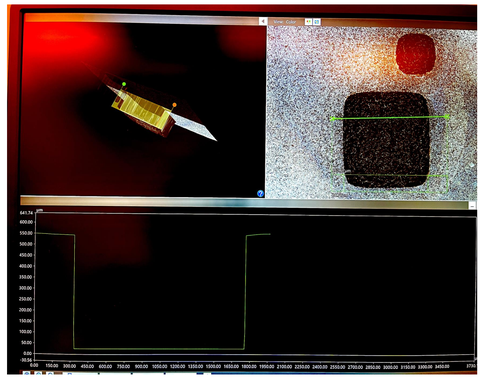
Lithography:

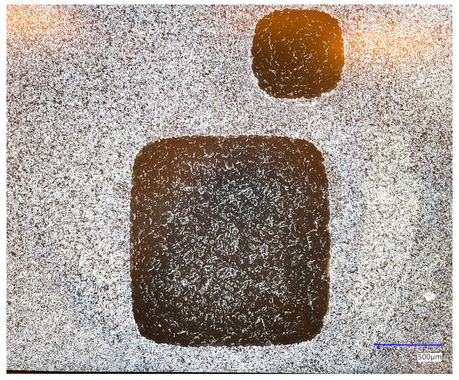
Etching:
- Utilized Tergeo plasma cleaning process to remove photoresist residue, resulting in an improved etch profile on the edges.
- Using DSE etcher successfully etched through a 380 μm thick substrate in Trial 2 and 4 with two different recipes, achieving sidewalls with less than 8° and 4° deviation from vertical, respectively.



Handling wafer
- We utilized physical vapor deposition (PVD) CHA E-beam Evaporator to deposit a 100 nm chromium (Cr) and a 200 nm gold (Au) layer on the silicon substrate.
- Compared to Trail 1 just 100 nm Cr seed layer, the Cr layer on Trail 4 promotes adhesion between the Au and the substrate, while the Au layer prevents the formation of an oxidation layer on top.

- Trial 4 with 100nm of Cr and 200nm of Au handling wafer





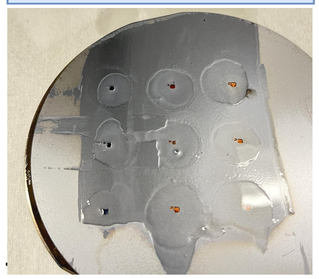
- Trial 2: surface of carrier wafer - no cracking due to high temperature

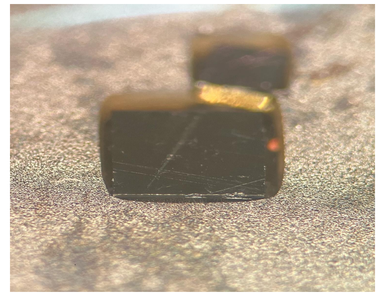
Step	Time(s)	Pressure	C4F8(sccm)	SF6(sccm)	Ar(sccm)	RF2(w)	RF3
Gas Stabilization	20	20		75	30	0	0 - Auto
Ignite	5	20		75	30	100	1500W-4000
Ignite 2	5	25		75	30	100	1500W-Hold
Dep	2	25	150		30	5	2000W-Hold
Etch A	1.9	40		150	30	50	2000W-Hold
Etch B	2	60		150	30	5	2500W-Hold

- This Bosch-process-based recipe alternates C4F8 deposition and SF6 etching, using precise RF power and pressure control to achieve high-aspect-ratio, anisotropic silicon etching with smooth vertical sidewalls.

- Etch recipe with 10um/min etch rate

Etching Recipe improvement:
- AZ1518 -> AZ10XT
- Crystal bond 555 -> 595
- Etching improvement: 10min to 5min cycles, preventing photoresist from cracking.
- Used crystal bond leaks from etched hole.



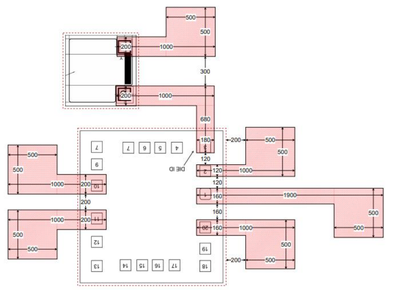


- Trial 1 electroplating result

Electroplating:
- Using the Iko Jr. Electroplater, the applied current setting is critical for balancing speed and quality.

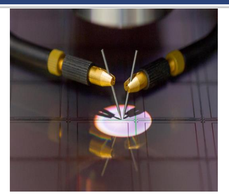
Epoxy Backfilling:
- Spread the epoxy on the wafer as adhesive.
- Removes the need for PVD + electroplating, due to high failure rates of such.

Metallization:
- After handling wafer has been removed, insulating layer is added to prevent shorting.
- Patterning and etching expose contacts and interconnects created between the dies with aluminum.
- Created with KLayout



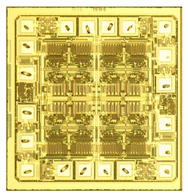
Future Goals

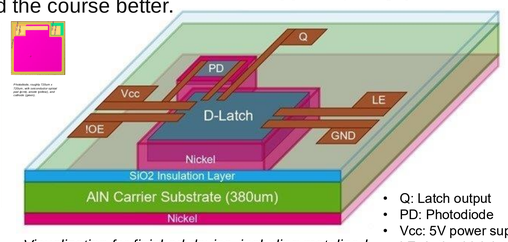
- Experiment with backfilling methods and disussing multi-purposing potentials of material around chiplets.
- Analyze the adhesion characteristics of various materials to identify the most effective option.
- Complete the construction of a course website that accelerates the pre-experiment trainings of new students, and allow faculty and external personnels to understand the course better.



[2] Wafer probing system

Embedded Dies:
- A photodiode is a photovoltaic device that generates a current when its optical component encounters light.
- The D-latch serves as a logic memory-bank to store the value captured by the photodiode





Visualization for finished device, including metalized interconnects and pads.

- Q: Latch output
- PD: Photodiode
- Vcc: 5V power supple
- LE: Active high latch enable
- !OE: Active low output enable

Acknowledgements

Thank you to Dr. Bermel, Dr. Mohammadi, Dr. Chen, Frank, and Birck staff for the continual support of this project. We appreciate the opportunity to use the Birck Nanotechnology Center facilities, including the cleanroom. Also, thank you to Vertically Integrated Projects for providing undergraduates the opportunity to dive deeper into the concepts we learn in class.

[1] Shenzhen QYC CO, LTD
[2] Thermo Fisher Scientific 2023

PURDUE UNIVERSITY