

Jessica

Claire

✉ resumesample@example.com

☎ (555) 432-1000,

Montgomery Street, San Francisco, CA 94105



## Summary

To be part of the Design Group of an innovative "continually growing" company where my expertise and experience as a Senior PCB Layout Engineer can be effectively utilized. 10 years of experience in Printed Circuit board industry with emphasis in PCB Layout of medium to high speed boards for high tech companies such as Intel, Marvell, Philips and LSI Logic using the latest CAD tools. Analytical capabilities and experience in successfully handling multiple projects and meeting tight deadlines. Excellent communication and interpersonal skills with the ability to effectively communicate at all levels.

## Highlights

Cadence OrCAD, Allegro, Mentor Graphics PADs and PADS logic, DxDesigner, Altium Designer. DFM using CAM350. Familiarity with AutoCAD and Solidworks. Proficiency in UNIX, Microsoft Windows, operating systems and Microsoft and Google office tools.

## Education

N.E.D University of Engineering and Technologies , Expected in 1 2001 – B.E : Electrical Engineering - GPA : Electrical Engineering , Expected in – IPC Designer's Council \* 2007 CID+, Certification Altium \* 2007 CAD Training, Altium Designer : - GPA :

## Accomplishments

- 98% on time delivery consistently for the past 3 years.
- Received the "TOP DOG" AWARD" From IPC Designer's Council
- Developed an internal best practices procedure for HDI designs that helped in improving design quClairity and increased product yields by as much as 15%.
- Single handedly developed an accurate component library of more than 1000 parts within a few months.
- Managed and worked on 100+ "ERROR FREE" Medium to Complex Projects during the past 2 years.
- Established good working relationships with customers and vendors.
- – Successfully designed multi-layered Printed Circuit boards comprising of 50+ layers.
- Trained and Spearheaded a team of 5 engineers in-house and 8 engineers overseas in PCB Layout using various CAD tools.
- Successfully laid out a Serdes II Chip Development board for 12Ghz, which was tested at 18Ghz with acceptable results.
- Dramatically improved PCB layout cycle time and accuracy by formulating procedures for similar designs.

## Experience

Cruise Automation - Senior PCB Layout Engineer

, , 02/2010 - Current

- Working as a Senior PCB Layout Engineer and collaborating communications between Customer team, Management, Manufacturing and Project management teams.
- Provided a pre and post engineering support in a fast-paced and deadline oriented environment.
- Developed an internal best practices procedure for HDI designs that helped in improving design quClairity and increased product yields by as much as 10%.
- Lead and work with CAD designers and Engineers and served as a technical Liaison between the Engineers in the US and CAD designers overseas on daily basis and manage their work activities, job assignments, priorities, resolve ongoing quClairity issues, answer questions and clarify specs and design criteria.
- Expertise in Laying out High Speed, Mixed signal and RF circuits along with High Frequency Power supply Board designs with reduced switching noise.
- Performed DFM and DFT analysis and designed for Fabrication, Assembly and Test as per the latest IPC standards on Rigid and Flex PCBs.
- Provided end-to-end support to transfer designs into manufacturing facilities by providing CAD files, Assembly drawings, fabrication guidelines, test packages and BOM generation.
- WEnsured Compliance with ISO standards and company quClairity system and ensure proper procedures and policies ECN, BOM and ECOs.

Amazon.Com, Inc. - PCB Layout Engineer

, , 2005 - 02/2010

- Working as a PCB Layout Engineer/Consultant and collaborating communications between Customer team, Management, Manufacturing and Project management teams.
- Provided a pre and post engineering support in a fast-paced and deadline oriented environment.
- Successfully designed multi-layered Printed Circuit boards (up to 34 layers) using CAD tools such as Cadence OrCad, Cadence Allegro, Mentor Graphics PADs Cadence SPECCTRA, and Altium Designer for top notch companies such as Marvell, LSI Logic, Applied

Materials, Phillips, Cisco systems.

- Developed an internal best practices procedure for HDI designs that helped in improving design quClairity and increased product yields by as much as 10%.
- Lead and work with CAD designers and Engineers and served as a technical Liaison between the Engineers in the US and CAD designers overseas on daily basis and manage their work activities, job assignments, priorities, resolve ongoing quClairity issues, answer questions and clarify specs and design criteria.
- Expertise in Laying out High Speed, Mixed signal and RF circuits along with High Frequency Power supply Board designs with reduced switching noise.
- Performed Impedance Calculations and Matching of Single ended and differential pair and compute and incorporate the design rules in the CAD tools.
- Performed DFM and DFT analysis and designed for Fabrication, Assembly and Test as per the latest IPC standards on Rigid and Flex PCBs.
- Provided end-to-end support to transfer designs into manufacturing facilities by providing CAD files, Assembly drawings, fabrication guidelines, test packages and BOM generation.
- Ensured Compliance with ISO standards and company quClairity system and ensure proper procedures and policies ECN, BOM and ECOs.

Carlisle Interconnect Technologies - PCB Design Engineer

, , 01/2001 - 01/2005

- Served as a PCB Design Engineer and supervised team of 8 engineers for satisfactory completion of time constrained projects.
- Acted as direct liaison between overseas clients and internal design team to interpret design requirements and intricacies during project life cycle.
- Designing of boards originating from engineers schematics or netlist input with design rules built in to the circuits and placing components on the boards using placement routines tailored to suit height restrictions, temperature characteristics, critical circuitry etc.
- Schematic Capture using Cadence OrCad and Pads Logic (formerly Power logic) netlist insertion, part creation and their placement, and routing using SMT and through hole techniques in Cadence Allegro and Pads PowerPCB.
- Standardized design and documentation procedures according to latest IPC standards to streamline design process and improve manufacturing yields on Rigid, Flex and Rigid-Flex Mix PCBs.

Affiliations

Member, IPC Designer's Council and IEEE.

Skills

streamline, Assembly, AutoCAD, CAD, Cadence, Cisco, clarify, Consultant, Council, clients, DFT, Designing, documentation, Engineer, fast, Graphics, ISO, Layout, Logic, Materials, Mentor, office, Microsoft Windows, operating systems, OrCAD, policies, Power supply, Project management, quClairity, routing, schematics, Solidworks, UNIX