Jessica Claire
Montgomery Street, San Francisco, CA 94105 609 Johnson Ave., 49204, Tulsa, OK
Home: (555) 432-1000 - Cell: - resumesample@example.com - -
Professional Summary
Seeking full time job opportunities in the field of computer hardware / software, do not require sponsorship.
Core Qualifications

- C++ (Proficient), C (Proficient), Python (Proficient), PL/SQL (Proficient), Ruby (Beginner)
- Programming APIs: Kernel & Device Driver Programming, MPI, OpenMP, CUDA, STL, PThreads, Selenium
- Hardware Description Languages: Verilog, VHDL (Intermediate)
- Database Technologies: Oracle Database (Proficient), MySQL
- Tools: SST, NI Labview, NI TestStand, Visual Studio, Modelsim, Vivado, NetBeans IDE, Cadence, PyCharm, MATLAB, SQLDbx, SQL Developer, NI MULTISIM, Keil IDE

Accomplishments

- Analysis and Optimization kernels on different Architectures (C, CUDA, Open MP) February 2015 - April 2015 Studied the architecture of Xeon E5, Xeon Phi and Tesla K40 and implemented QR decomposition using OpenMP API in C and CUDA.
- Benchmarked the performance of QR decomposition kernel on the above mentioned processor (CPU), co- processor and Graphics Processing Unit (GPU).
- Implement modified LRU policy for improving second level cache behaviour (C) September 2014 - December 2014 Implemented a modified Least Recently Used replacement algorithm for better victimization on the basis of temporal locality of cache lines and hence increasing the hit rate by about 8%.
- Design and Implement fault tolerant server - client file system (Python) September 2014 - December 2014 Used concept of Data Redundancy for implementing server migration, server replication and load sharing of servers to backup and restore data to prevent loss of data due to server failure.
- 1-D Time Domain Convolution (VHDL, Xilinx Vivado) August 2015 Â December 2015 Implemented 1D FFT convolution on Xilinx Zed board using the processor-data path architecture, while fetching and storing data on external SRAMs across clock domains.
- Design and Implement Low Power ALU (Verilog, Cadence, Xilinx ISE) February 2015 - April 2015 Used Dynamic Voltage Frequency Scaling power reduction technique and achieved a 60% power reduction between highest operating frequency and lowest operating frequency.
- Other Projects: Dictionary Based compression Â decompression technique, Document Classifier using NaÃ¨ve Bayes Algorithm, Touchless Fingerprint Recognition System, 6T Cell SRAM design (Cadence Spectre, Cadence Virtuoso), Microcontroller-8051 Based Text Display.

Experience
06/2016 to Present
Quality Engineer VMware AirWatch â€“ , ,

- Develop automation scripts for browser automation using Cucumber tool, Gherkin and Ruby.

08/2015 to 05/2016
Graduate Research Assistant Children's National Medical Center â€“ , ,

- Developed Parallel Discrete Event Simulator based on behavioural emulation using Python and C++, capable of performing exascale simulations for Novo-G Exascale Emulation (NGEE) project supervised by Dr.
- Herman Lam Developed behavioural emulation objects of future generation processor architectures and hybrid network topologies, by adaptive routing and dynamic scheduling techniques.

05/2015 to 08/2015
Backend Software Developer Â Intern NSF CHREC â€“ , ,

- Created Python scripts for collecting and processing required information from multiple websites using Selenium package.
- Also, handled MySQL database for storing the collected data.

06/2012 to 07/2014
Assistant Systems Engineer Swipe Financial Incorporation â€“ , ,

- Managed the back-end development of critical modules, estimated to generate a revenue of 190 billion INR for client.
- Oracle Database, PL/SQL Increased the performance of the sheet upload and search functionality to speed them up by 60% and 2% respectively Volunteered to visit the client location to interact with users to understand the issues faced in live environment Initial Learning Program: Created and tested user interface while implementing the MVC architecture.
- C++, Unix Won the Certificate of Appreciation for Managing AD-Mad Event in TCS day celebration.

Education
Expected in May 2016 to to
Master of Science: Computer Engineering
University of Florida - Gainesville,

GPA: GPA: 3.58/4.0
Computer Engineering GPA: 3.58/4.0
Expected in to to
Advanced System Programming, Reconfigurable Computing, Principles of Computer System Design, Computer Architecture, Parallel Computer Architecture, VLSI circuits and technology, Advanced VLSI, Image Processing/Computer Vision:
- ,
GPA:
Expected in May 2012 to to
Bachelor's: Electronics and Communication Engineering
Gujarat Technological University - , Gujarat
GPA: GPA: 3.9/4.0
Electronics and Communication Engineering GPA: 3.9/4.0
Professional Affiliations
Skills
AD, automation, C, C++, Cadence, Hardware, client, Database, IDE, Image Processing, Labview, Managing, MATLAB, MVC, MySQL, network, Oracle Database, Developer, PL/SQL, Programming, Python, routing, scheduling, scripts, Scripting, SQL, System Design, Unix, user interface, Verilog, VHDL, Vision, Visual Studio, VLSI, websites