LABC3 – Curiosity Board -- Read Potentiometer (A/D) Count S1 Presses

Goal: Read the potentiometer level (10 bits) and count the number of presses on S1 switch. Light-up LED1 when S1 is pressed. View A/D and number-of-S1-press values with debugger.

Relevant A/D SFRs:

Control and Configuration SFRs: **ANSB** / **AD1CON1** / **AD1CON2** / **AD1CON3**
Channel Select: **AD1CHS**
A/D Result: **ADC1BUF0** (16 bit result storage)

A/D Initialization:

ANSB: Configure potentiometer pin for Analog Input (on ***RB12***)

AD1CON1 Fields:

SSRC, *FORM*, *ASAM, ADSIDL, DMABM, DMAEN* (use 0)
MODE12 – use 10 bits resolution

AD1CON2 (use 0)

AD1CON3 Fields:

ADCS (use 0xFF)
SAMC (use 0x10)
EXTSAM, PUMPEN (use 0)
ADRC (use 0)

Converting A/D (see Fig.1)

Step 1: Select channel (**AD1CHS**, **channel 8** in **CH0SA**); Start A/D converter (*ADON* in **AD1CON1**)

Step 2: **Sample** voltage (use **AD1CON1** *SAMP*) – use short delay (i.e., for loop 1000 cycles)

Step 3: **Hold** sampled voltage (use **AD1CON1** *SAMP*) – Conversion will start automatically

Step 4: Wait for conversion to complete (reference **AD1CON1** *DONE*)

Step 5: Get result (**ADC1BUF0**)

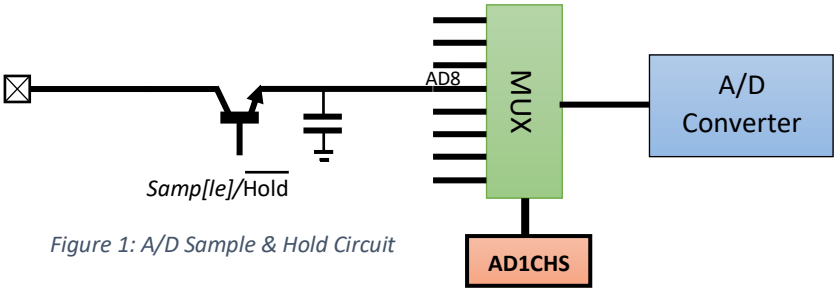
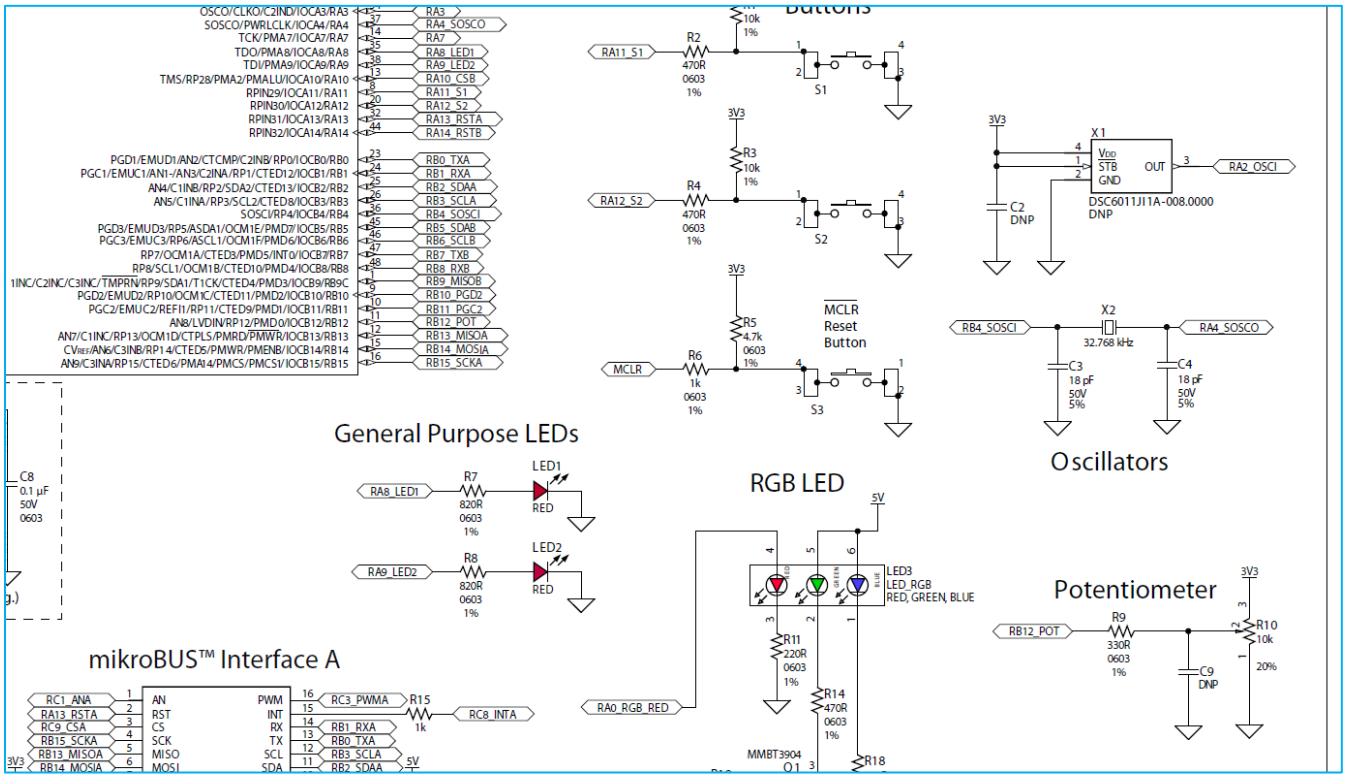


Figure 1: A/D Sample & Hold Circuit

LED and Switch (Configure proper TRIS values)

S1 Switch:	*RA11*	(Read: **PORTA**)
LED1:	*RA8*	(Write: **LATA**)

Curiosity Board Schematic



REGISTER 24-1: AD1CON1: A/D CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADON	—	ADSIDL	DMABM(1)	DMAEN	MODE12	FORM1	FORM0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	HSC/R/W-0	HSC/R/C-0
SSRC3	SSRC2	SSRC1	SSRC0	—	ASAM	SAMP	DONE
bit 7							bit 0

Legend:	C = Clearable bit	U = Unimplemented bit, read as '0'	
R = Readable bit	W = Writable bit	HSC = Hardware Settable/Clearable bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ADON:** A/D Operating Mode bit
1 = A/D Converter is operating
0 = A/D Converter is off

bit 14 **Unimplemented:** Read as '0'

bit 13 **ADSIDL:** A/D Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **DMABM:** Extended DMA Buffer Mode Select bit(1)
1 = Extended Buffer mode: Buffer address is defined by the DMADSTn register
0 = PIA mode: Buffer addresses are defined by the DMA Controller and AD1CON4[2:0]

bit 11 **DMAEN:** Extended DMA/Buffer Enable bit
1 = Extended DMA and buffer features are enabled
0 = Extended features are disabled

bit 10 **MODE12:** A/D 12-Bit Operation Mode bit
1 = 12-bit A/D operation
0 = 10-bit A/D operation

bit 9-8 **FORM[1:0]:** Data Output Format bits (see formats following)
11 = Fractional result, signed, left justified
10 = Absolute fractional result, unsigned, left justified
01 = Decimal result, signed, right justified
00 = Absolute decimal result, unsigned, right justified

bit 7-4 **SSRC[3:0]:** Sample Clock Source Select bits
0000 = SAMP is cleared by software
0001 = INT0
0010 = Timer3
0100 = CTMU trigger
0101 = Timer1 (will not trigger during Sleep mode)
0110 = Timer1 (may trigger during Sleep mode)
0111 = Auto-Convert mode

bit 3 **Unimplemented:** Read as '0'

bit 2 **ASAM:** A/D Sample Auto-Start bit
1 = Sampling begins immediately after last conversion; SAMP bit is auto-set
0 = Sampling begins when SAMP bit is manually set

bit 1 **SAMP:** A/D Sample Enable bit
1 = A/D Sample-and-Hold amplifiers are sampling
0 = A/D Sample-and-Hold amplifiers are holding

bit 0 **DONE:** A/D Conversion Status bit
1 = A/D conversion cycle has completed
0 = A/D conversion cycle has not started or is in progress

Note 1: This bit is only available when Extended DMA and buffer features are available (DMAEN = 1).

REGISTER 24-3: AD1CON3: A/D CONTROL REGISTER 3

R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADRC(1)	EXTSAM	PUMPEN(2)	SAMC4	SAMC3	SAMC2	SAMC1	SAMC0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCS[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ADRC:** A/D Conversion Clock Source bit(1)
1 = Dedicated ADC RC clock generator (4 MHz nominal).
0 = Clock derived from system clock

bit 14 **EXTSAM:** Extended Sampling Time bit
1 = A/D is still sampling after SAMP = 0
0 = A/D is finished sampling

bit 13 **PUMPEN:** Charge Pump Enable bit(2)
1 = Charge pump for switches is enabled
0 = Charge pump for switches is disabled

bit 12-8 **SAMC[4:0]:** Auto-Sample Time Select bits
11111 = 31 TAD
•
•
•
00001 = 1 TAD
00000 = 0 TAD

bit 7-0 **ADCS[7:0]:** A/D Conversion Clock Select bits
11111111 = 256 • TCY = TAD
•
•
•
00000001 = 2 • TCY = TAD
00000000 = TCY = TAD

TABLE 11-1: CONFIGURING ANALOG/DIGITAL FUNCTION OF AN I/O PIN

Pin Function	ANSx Setting	TRISx Setting	Comments
Analog Input	1	1	It is recommended to keep ANSx = 1.
Analog Output	1	1	It is recommended to keep ANSx = 1.
Digital Input	0	1	Firmware must wait at least one instruction cycle after configuring a pin as a digital input before a valid input value can be read.
Digital Output	0	0	Make sure to disable the analog output function on the pin if any is present.

REGISTER 24-6: AD1CHS: A/D SAMPLE SELECT REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NB2	CH0NB1	CH0NB0	CH0SB4	CH0SB3	CH0SB2	CH0SB1	CH0SB0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NA2	CH0NA1	CH0NA0	CH0SA4	CH0SA3	CH0SA2	CH0SA1	CH0SA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **CH0NB[2:0]:** Sample B Channel 0 Negative Input Select bits
1xx = Unimplemented
01x = Unimplemented
001 = Unimplemented
000 = AVss

bit 12-8 **CH0SB[4:0]:** Sample B Channel 0 Positive Input Select bits
11110 = AV_{DD} (1)
11101 = AVss (1)
11100 = Band Gap Reference (V_{BG}) (1)
10000-11011 = Reserved
01111 = No external channels connected (used for CTMU)
01110 = No external channels connected (used for CTMU temperature sensor)
01101 = AN13
01100 = AN12
01011 = AN11
01010 = AN10
01001 = AN9
01000 = AN8
00111 = AN7
00110 = AN6
00101 = AN5
00100 = AN4
00011 = AN3
00010 = AN2
00001 = AN1
00000 = AN0

bit 7-5 **CH0NA[2:0]:** Sample A Channel 0 Negative Input Select bits
Same definitions as for CHONB[2:0].

bit 4-0 **CH0SA[4:0]:** Sample A Channel 0 Positive Input Select bits
Same definitions as for CHOSB[4:0]