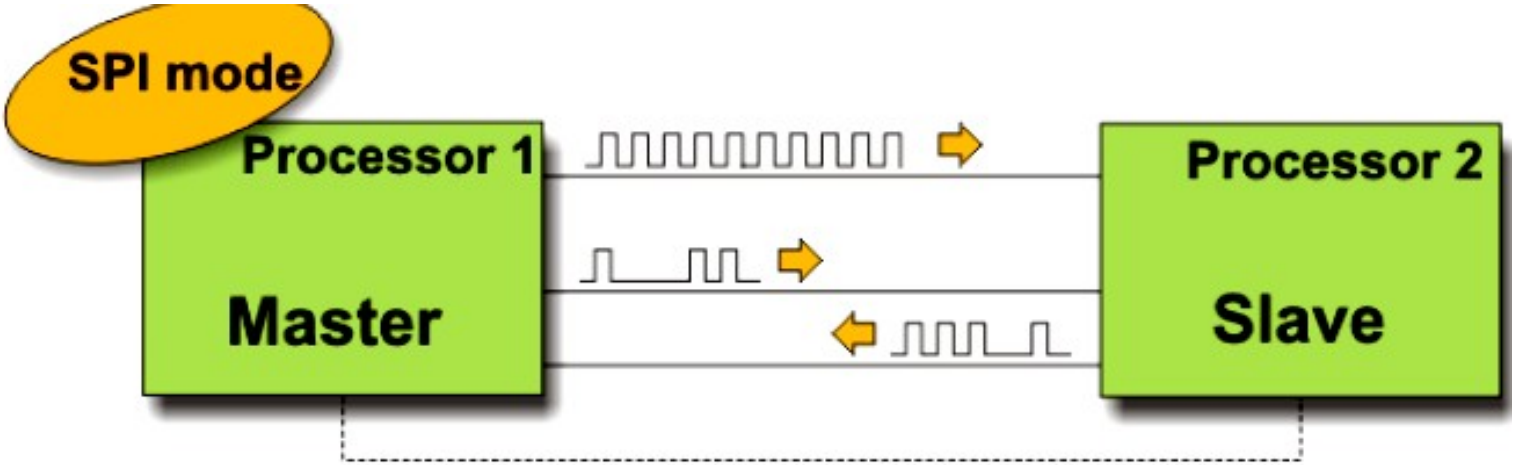
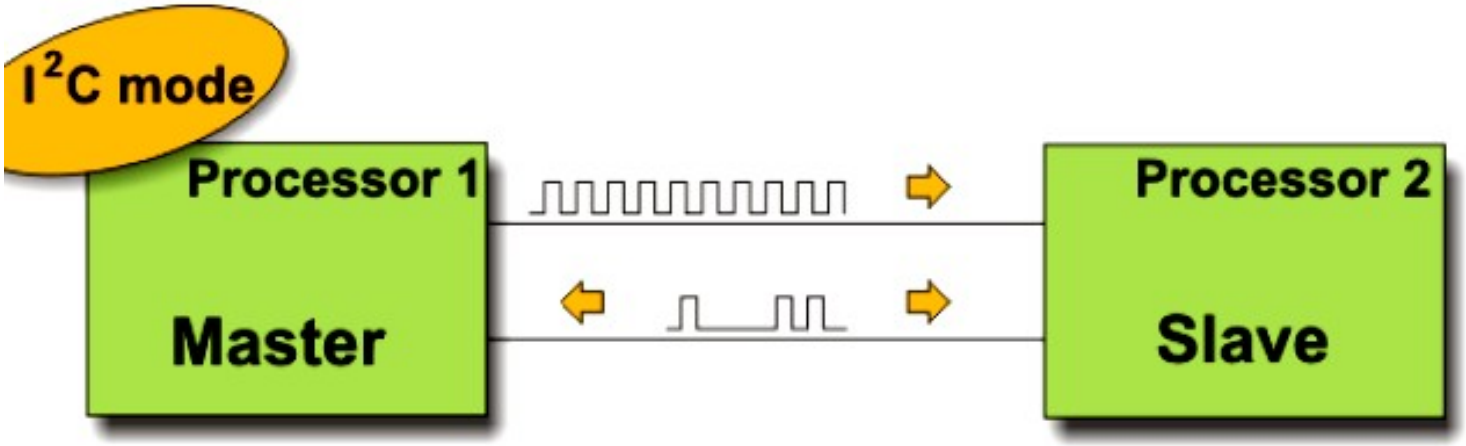
MASTER SYNCHRONOUS SERIAL PORT (MSSP)MODULE

- **The Master Synchronous Serial Port (MSSP) module is a serial interface useful for communicating with other peripheral or micro controller devices.**
- **These peripheral devices may be serial EEPROMs, shift registers, display drivers, A/D converters,SD Cards,USB devices etc.**
- **The MSSP module can operate in one of two modes:**
  - **Serial Peripheral Interface (SPI)**
  - **Inter-Integrated Circuit (I^2C)**


SPI mode
Processor 1
Master
Processor 2
Slave


I2C mode
Processor 1
Master
Processor 2
Slave

Control Registers

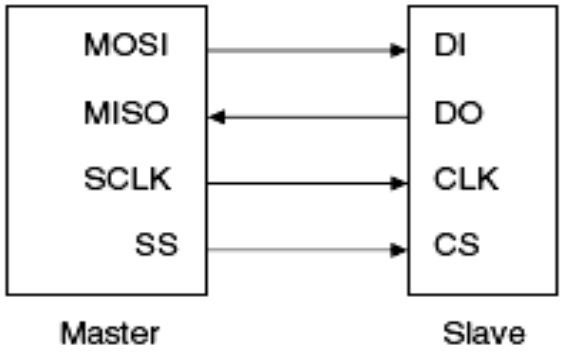
- The MSSP module has three associated registers.
- status register (SSPSTAT) and two control registers (SSPCON1 and SSPCON2).

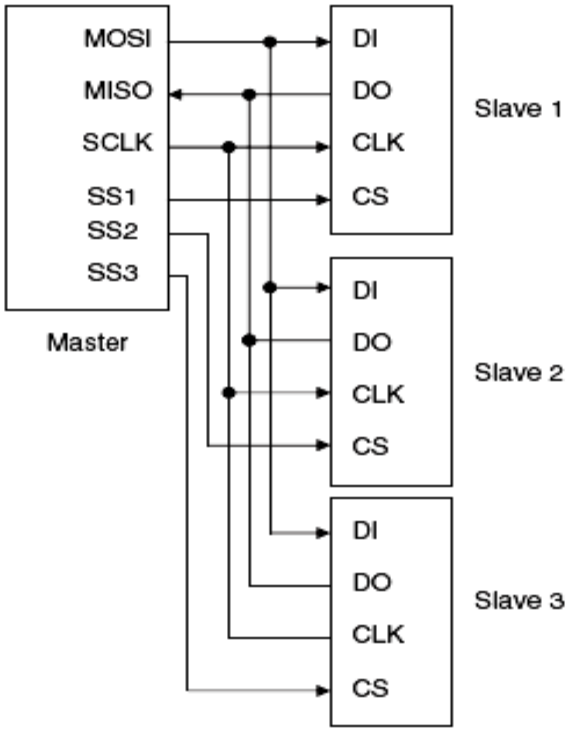
SPI Mode

- SPI bus was started by Motorola Corp
- The SPI mode allows 8-bits of data to be synchronously transmitted and received, simultaneously.
- To accomplish communication, typically three pins are used:
- Serial Data Out (SDO) - RC5/SDO
- Serial Data In (SDI) - RC4/SDI/SDA
- Serial Clock (SCK) - RC3/SCK/SCL/LVDIN
- Additionally, a fourth pin may be used when in a Slave mode of operation:
- Slave Select (SS) - RA5/SS/AN4

SPI Read and Write Protocol

- **In connecting a device with an SPI bus to µC, we use µC as the master while the SPI device acts as slave.**
- **µC generates the SCLK, which is fed to SCLK pin of the SPI device, to synchronize the transfer of data one bit at a time, MSB goes in first.**
- **During transfer, the SS(Slave Select) pin must be HIGH.**
- **To distinguish b/w read and write, D7 bit of address byte(A7) is always 1 for write, and for read this bit is Low.**





Steps for writing data to SPI device

Single byte write

- Make $\overline{SS}$=0 to select the device for writing.
- 8bit address is shifted in one bit at a time, with each edge of SCLK. A7 =1 for the write operation and the A7 bit goes in first.
- After all 8bits of the address are sent in, the SPI device expects to receive the data belonging to address location immediately.
- The 8bit data is shifted in one bit at a time,with each edge of SCLK.
- Make SS =0 to indicate the end of write cycle.

Multi byte burst write

- **SS=0**
- **8bit address of first location is provided and shifted one bit at a time, each edge of SCLK A7=1 for the write operation and A7 bit goes in first.**
- **The 8bit data for the first location is provided and shifted one bit at a time, with each edge of the SCLK.**
- **From then on, we simply provide consecutive bytes of data to be placed in consecutive locations.**
- **During this process SS must Low.**
- **SS=1 to end write cycle.**

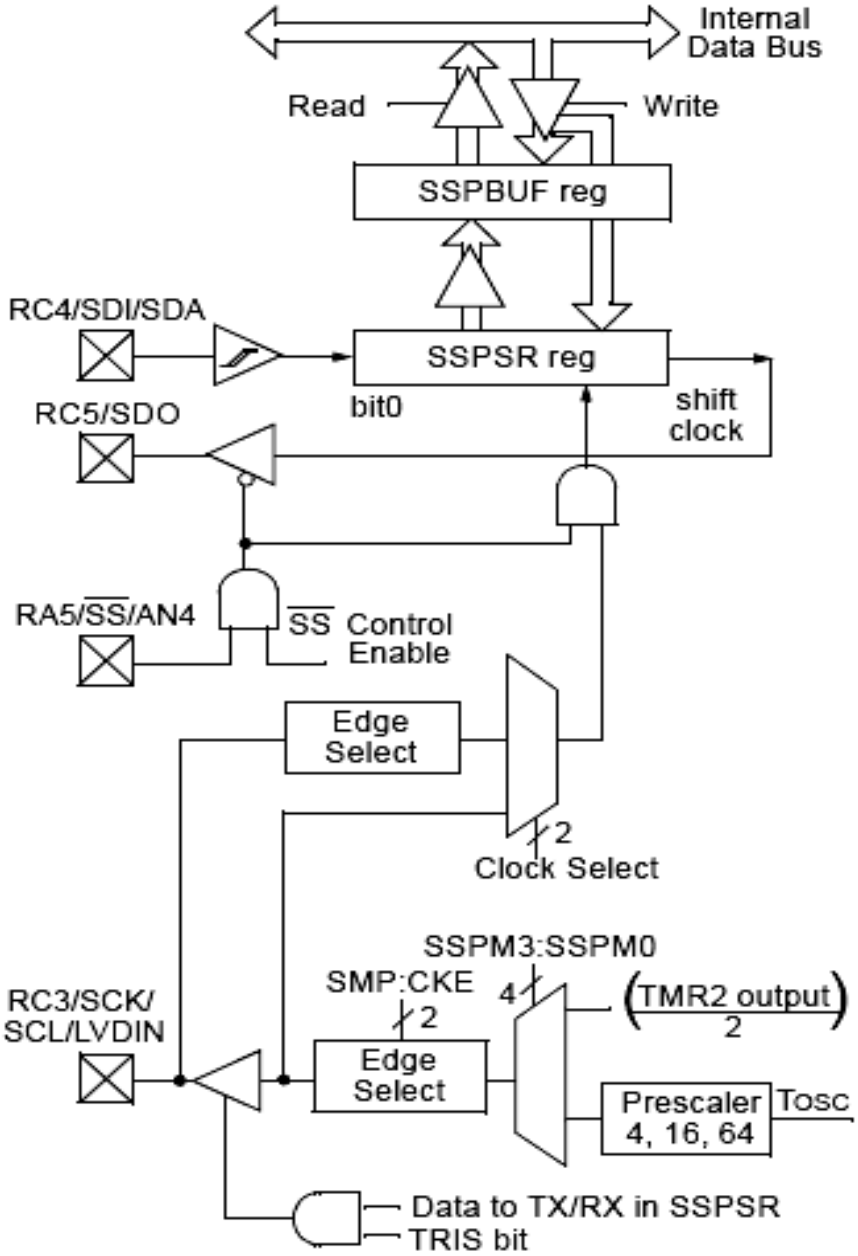
Steps for Reading data from SPI device

Single byte Read

- Make SS=0 to select the device for writing.
- 8bit address is shifted in one bit at a time, with each edge of SCLK. A7 =0 for the write operation and the A7 bit goes in first.
- After all 8bits of the address are sent in, the SPI device sends out the data belonging to address location immediately.
- The 8bit data is shifted out one bit at a time,with each edge of SCLK.
- Make SS =0 to indicate the end of read cycle.

Multi byte burst Read

- **SS=0**
- **8bit address of first location is provided and shifted one bit at a time, each edge of SCLK A7=0 for the write operation and A7 bit goes in first.**
- **The 8bit data for the first location shifted out one bit at a time, with each edge of the SCLK.**
- **From then on, we simply keep getting consecutive bytes of data to be placed in consecutive locations.**
- **During this process SS must Low.**
- **SS=1 to end read cycle.**



REGISTERS

The MSSP module has four registers for SPI mode operation. These are:

- **MSSP Control Register1 (SSPCON1)**
- **MSSP Status Register (SSPSTAT)**
- **Serial Receive/Transmit Buffer (SSPBUF)**
- **MSSP Shift Register (SSPSR) - Not directly accessible**

SSPSTAT: MSSP STATUS REGISTER (SPI MODE)

R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0
SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF
bit 7							bit 0

bit 7 **SMP:** Sample bit

SPI Master mode:

1 = Input data sampled at end of data output time

0 = Input data sampled at middle of data output time

SPI Slave mode:

SMP must be cleared when SPI is used in Slave mode

bit 6 **CKE:** SPI Clock Edge Select

When CKP = 0:

1 = Data transmitted on rising edge of SCK

0 = Data transmitted on falling edge of SCK

When CKP = 1:

1 = Data transmitted on falling edge of SCK

0 = Data transmitted on rising edge of SCK

bit 5 **D/$\overline{A}$:** Data/$\overline{Address}$ bit

Used in I^2C mode only

bit 4 **P:** STOP bit

Used in I^2C mode only. This bit is cleared when the MSSP module is disabled, SSPEN is cleared.

bit 3 **S:** START bit

Used in I^2C mode only

bit 2 **R/$\overline{W}$:** Read/Write bit information

Used in I^2C mode only

bit 1 **UA:** Update Address

Used in I^2C mode only

bit 0 **BF:** Buffer Full Status bit (Receive mode only)

1 = Receive complete, SSPBUF is full

0 = Receive not complete, SSPBUF is empty

SSPCON1: MSSP CONTROL REGISTER1 (SPI MODE)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0
bit 7							bit 0

bit 7 **WCOL:** Write Collision Detect bit (Transmit mode only)

1 = The SSPBUF register is written while it is still transmitting the previous word (must be cleared in software)

0 = No collision

bit 6 **SSPOV:** Receive Overflow Indicator bit

SPI Slave mode:

1 = A new byte is received while the SSPBUF register is still holding the previous data. In case of overflow, the data in SSPSR is lost. Overflow can only occur in Slave mode.The user must read the SSPBUF, even if only transmitting data, to avoid setting overflow (must be cleared in software).

0 = No overflow

Note: In Master mode, the overflow bit is not set since each new reception (and transmission) is initiated by writing to the SSPBUF register.

bit 5 **SSPEN:** Synchronous Serial Port Enable bit

1 = Enables serial port and configures SCK, SDO, SDI, and $\overline{SS}$ as serial port pins

0 = Disables serial port and configures these pins as I/O port pins

Note: When enabled, these pins must be properly configured as input or output.

bit 4 **CKP:** Clock Polarity Select bit

1 = IDLE state for clock is a high level

0 = IDLE state for clock is a low level

bit 3-0 **SSPM3:SSPM0:** Synchronous Serial Port Mode Select bits

0101 = SPI Slave mode, clock = SCK pin, $\overline{SS}$ pin control disabled, $\overline{SS}$ can be used as I/O pin

0100 = SPI Slave mode, clock = SCK pin, $\overline{SS}$ pin control enabled

0011 = SPI Master mode, clock = TMR2 output/2

0010 = SPI Master mode, clock = Fosc/64

0001 = SPI Master mode, clock = Fosc/16

0000 = SPI Master mode, clock = Fosc/4

Note: Bit combinations not specifically listed here are either reserved, or implemented in I^2C mode only.

OPERATION

- When initializing the SPI, several options need to be specified.
- This is done by programming the appropriate control bits (SSPCON1<5:0>) and SSPSTAT<7:6>.
- These control bits allow the following to be specified:
  - Master mode (SCK is the clock output)
  - Slave mode (SCK is the clock input)
  - Clock Polarity (IDLE state of SCK)
  - Data input sample phase (middle or end of data output time)
  - Clock edge (output data on rising/falling edge of SCK)
  - Clock Rate (Master mode only)
  - Slave Select mode (Slave mode only)
- The MSSP consists of a transmit/receive Shift Register (SSPSR) and a buffer register (SSPBUF).
- The SSPSR shifts the data in and out of the device, MSb first.
- The SSPBUF holds the data that was written to the SSPSR, until the received data is ready.
- Once the 8 bits of data have been received, that byte is moved to the SSPBUF register.