IC_Project 2

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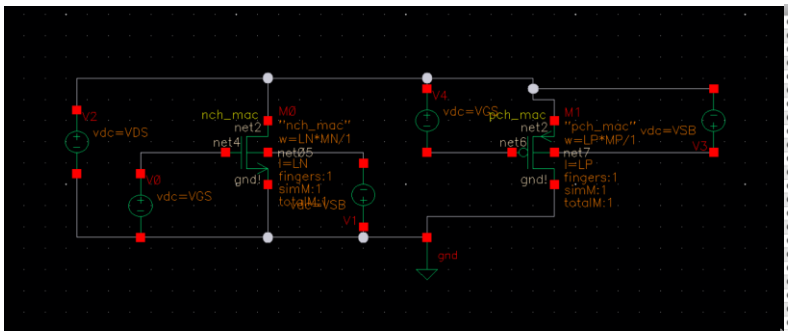
Design Methodology :-

- Devices Used for the amplifier are nch_25od33 and pch_25od33 ,because Vdd = 3.3V which is high for regular nch and pch devices.



Test	Name	Type	Details	EvalType
Gain_Boosted_Cascode:test_bench:1	cgg/id_N	expr	(getData("M0:cgg" ?result "dc") / getData("...	point
Gain_Boosted_Cascode:test_bench:1	cgg_P	expr	getData("M1:cgg" ?result "dc")	point
Gain_Boosted_Cascode:test_bench:1	cdd_P	expr	getData("M1:cdd" ?result "dc")	point
Gain_Boosted_Cascode:test_bench:1	gm_N	expr	getData("M0:gm" ?result "dc")	point
Gain_Boosted_Cascode:test_bench:1	gm_P	expr	getData("M1:gm" ?result "dc")	point
Gain_Boosted_Cascode:test_bench:1	gm/id_N	expr	(getData("M0:gm" ?result "dc") / getData("...	point
Gain_Boosted_Cascode:test_bench:1	gds/id_N	expr	(getData("M0:gds" ?result "dc") / getData("...	point
Gain_Boosted_Cascode:test_bench:1	gm/gds_N	expr	(getData("M0:gm" ?result "dc") / getData("...	point
Gain_Boosted_Cascode:test_bench:1	cdd/id_N	expr	(getData("M0:cdd" ?result "dc") / getData("...	point
Gain_Boosted_Cascode:test_bench:1	ID_N	expr	getData("M0:ids" ?result "dc")	point
Gain_Boosted_Cascode:test_bench:1	vdsat_N	expr	getData("M0:vdsat" ?result "dc")	point
Gain_Boosted_Cascode:test_bench:1	css/id_N	expr	(getData("M0:css" ?result "dc") / getData("...	point
Gain_Boosted_Cascode:test_bench:1	W/ID_N	expr	((VAR("MN") * VAR("LN")) / getData("M0:id...	point
Gain_Boosted_Cascode:test_bench:1	cdd/id_P	expr	abs((getData("M1:cdd" ?result "dc") / getD...	point
Gain_Boosted_Cascode:test_bench:1	cgg/id_P	expr	abs((getData("M1:cgg" ?result "dc") / getD...	point
Gain_Boosted_Cascode:test_bench:1	gm/id_P	expr	abs((getData("M1:gm" ?result "dc") / getD...	point
Gain_Boosted_Cascode:test_bench:1	gds/id_P	expr	abs((getData("M1:gds" ?result "dc") / getD...	point
Gain_Boosted_Cascode:test_bench:1	gm/gds_P	expr	abs((getData("M1:gm" ?result "dc") / getD...	point
Gain_Boosted_Cascode:test_bench:1	vdsat_P	expr	abs(getData("M1:vdsat" ?result "dc"))	point
Gain_Boosted_Cascode:test_bench:1	Vstar_N	expr	((2 * getData("M0:id" ?result "dc")) / getDa...	point
Gain_Boosted_Cascode:test_bench:1	Vstart_P	expr	((2 * getData("M1:id" ?result "dc")) / getDa...	point
Gain_Boosted_Cascode:test_bench:1	css/id_P	expr	abs((getData("M1:css" ?result "dc") / getD...	point
Gain_Boosted_Cascode:test_bench:1	W/ID_P	expr	abs(((VAR("MP") * VAR("LP")) / getData("M...	point

Figure 1: Sizing Test Bench

Folded Cascode Desing:-

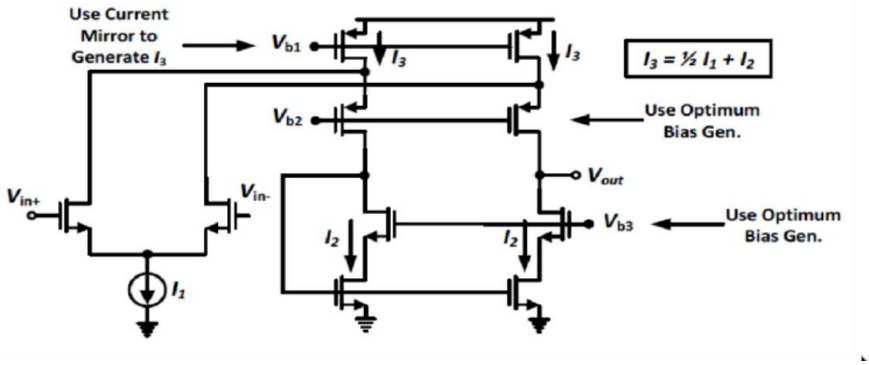


Figure 1. Folded Cascode

The main design Equations for the Folded Cascode Amplifier are the following:
from the Slew Rate $\mathrm{SR} = \frac{I_1}{C_L}$ Spec : form this spec it's follows that the minimum current for , To get the actual $I_1 = 100\mu A$ value of the current from GBW spec.
GBW (Taking Safty factor of 20% for parasitics),
Choose gm/id $= 18$ and $I_D = 65\mu A$, meaning$I_{SS} = 130\mu A > 100\mu A$ $= \frac{\mathrm{gm}}{(C_L + C_{\mathrm{par}})\, 2\pi} \approx \frac{g_{m_{\mathrm{input}}}}{1.2 C_L}$.

Since we are using the 3.3V devices $\boldsymbol{L_{min}}$ is quite high $\boldsymbol{L_{min}}$=500*n* for NMOS and 400n for PMOS, and this achieves all the specs (Gain = 67dB >> 58dB), So we go with $\boldsymbol{L_{min}}$ for all devices except for tail current source (L =1u).

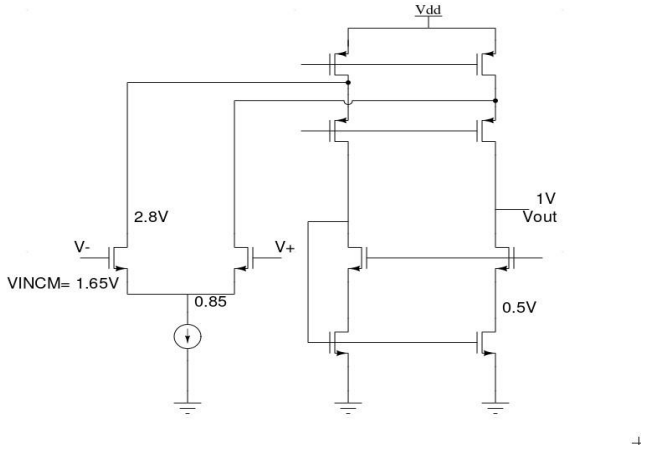


Figure 2. Folded Cascode schematic with voltage assignment

Based ON VINCM spec and output swing , nominal voltages are assigned as in fig-2, For the current I3, it was first chosen to be ¾ I1 (meaning current ratio of 1/2 in the two branches).
Now , given currents, voltages and L , we can determine bias voltages and Widths for each transistor, For Bias Voltages: Vb1 = 2.54V , Vb2 = 1.94V , Vb3 =1.35V and for tail source V_{gs}=0.65V.

1.2 Bias Circuit

Now for the bias circuit:

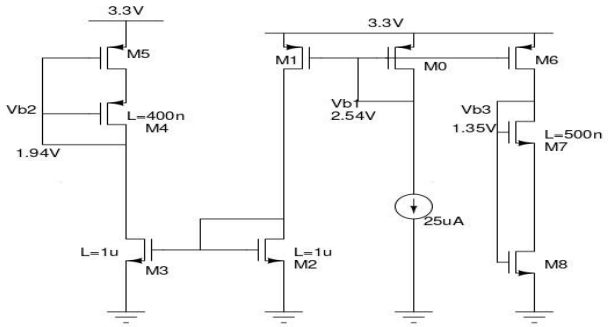


Figure 3. Bias Circuit and Current Mirrors

1 **For the current in each branch** , it was done by experiment to get proper voltages with reasonable sizes of the transistor, it should be noted that for the optimum bias Vb2 , we intentionally chosen it to get a V_{ds} of 0.5V as making Vds = V_{ov} +100mv degrade the performance a lot (Not only the gain but GBW and SR was badly affected) , so we choose to give it a larger marge Vds = 0.5V. **1.3 Final Sizing:**

2 After running simulations, small changes was made to better achieve the specs, here the final sizing.

Device	W	L	Vgs
Input Pair	60u	500n	820mV
PMOS Source	28.36u	400n	760mV
PMOS cascode	10u	400n	860mv
NMOS cascode	10.15u	500n	850mV
NMOS CM	1.25u	500n	1V
NMOS Tail Source	110u	1u	650mV

Table 1. Sizing of Folded Cascode

Device	W	L	Vgs	Device	W	L	Vgs
M0	5.9u	400n	0.76	M1	5.9u	400n	0.76
M2	28.7u	1u	0.65	M3	14.35u	1u	0.65
M4	4.2u	400n	1.36	M5	1.21u	1u	1.36V
M6	7.2u	400n	0.76	M7	13.8u	500n	1.35
M8	740n	1u	1.35V				

Table 2. Sizing of Bias Circuit

2.1.1 DC Operating Points

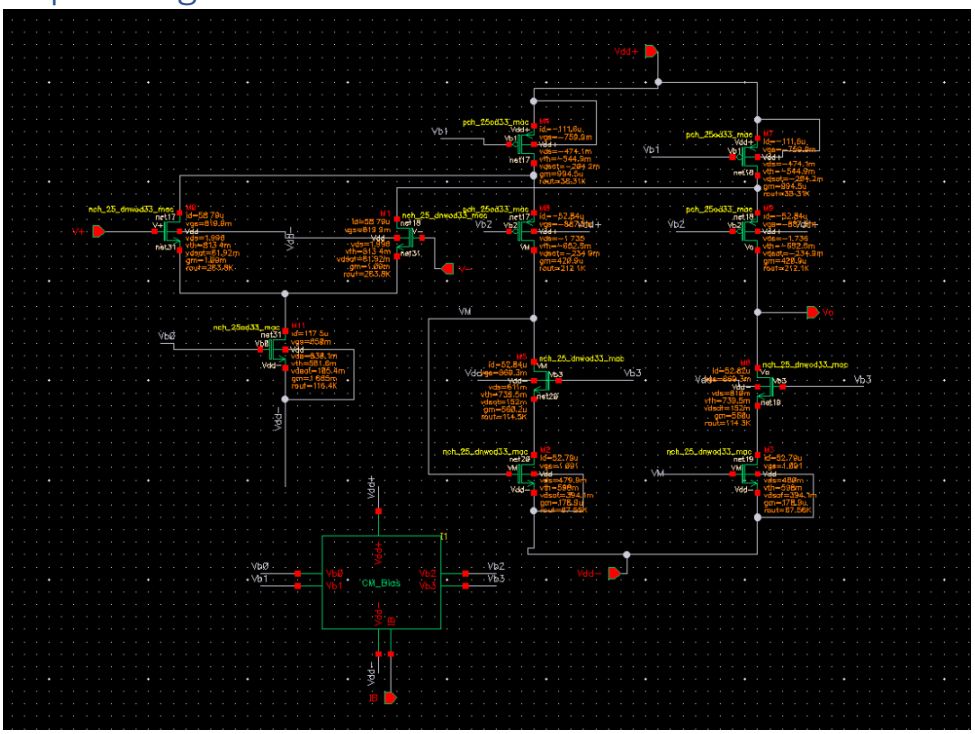


Figure 2: Folded Cascode Operationg Point

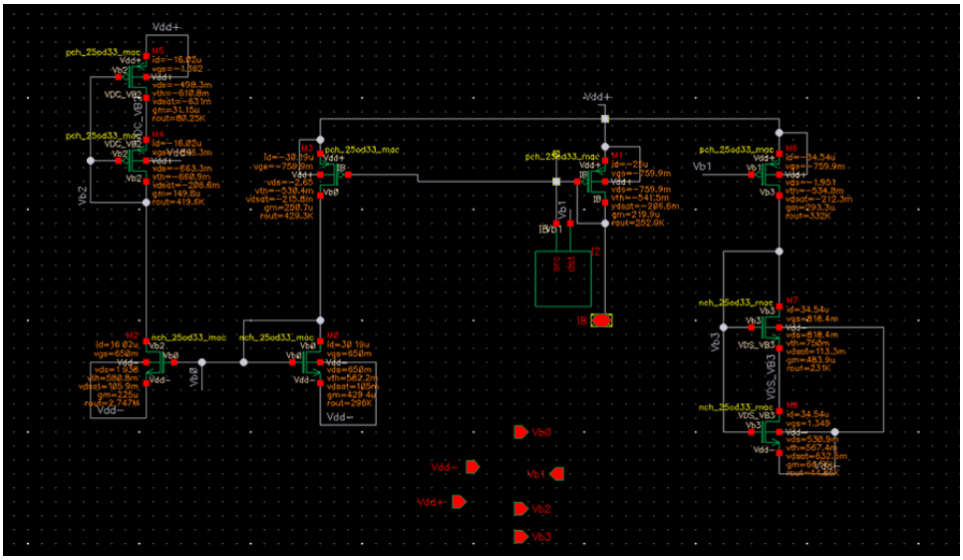


Figure 3: Bias Circuit

3 Simulation Test

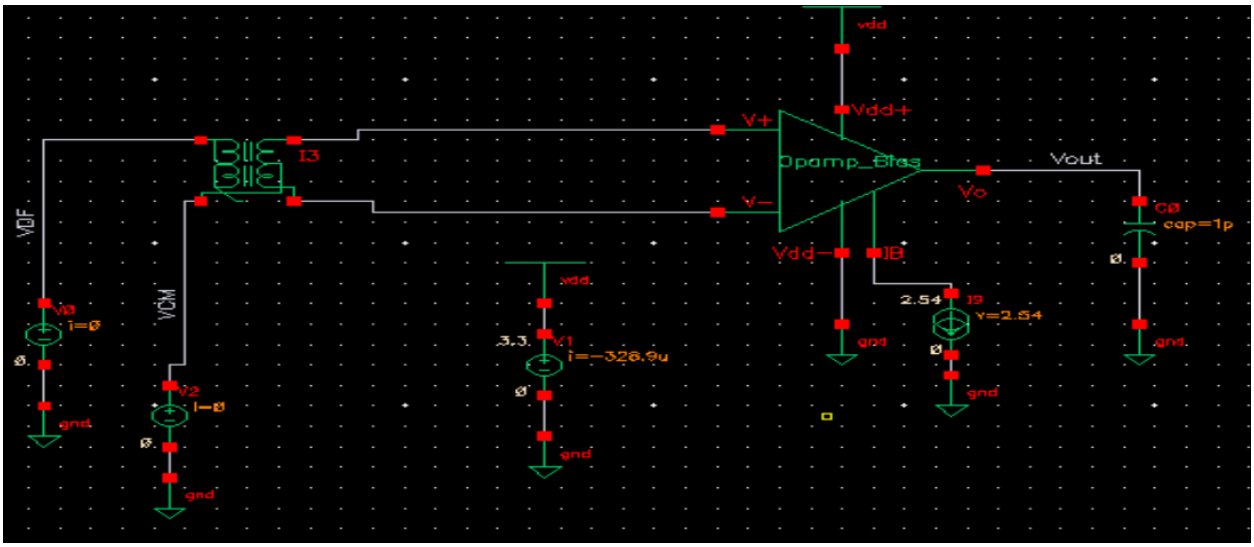


Figure 4 Final Circuit Test

3.1 Open Circuit Analysis:

We used ideal balun

3.1.1 ==> AC test

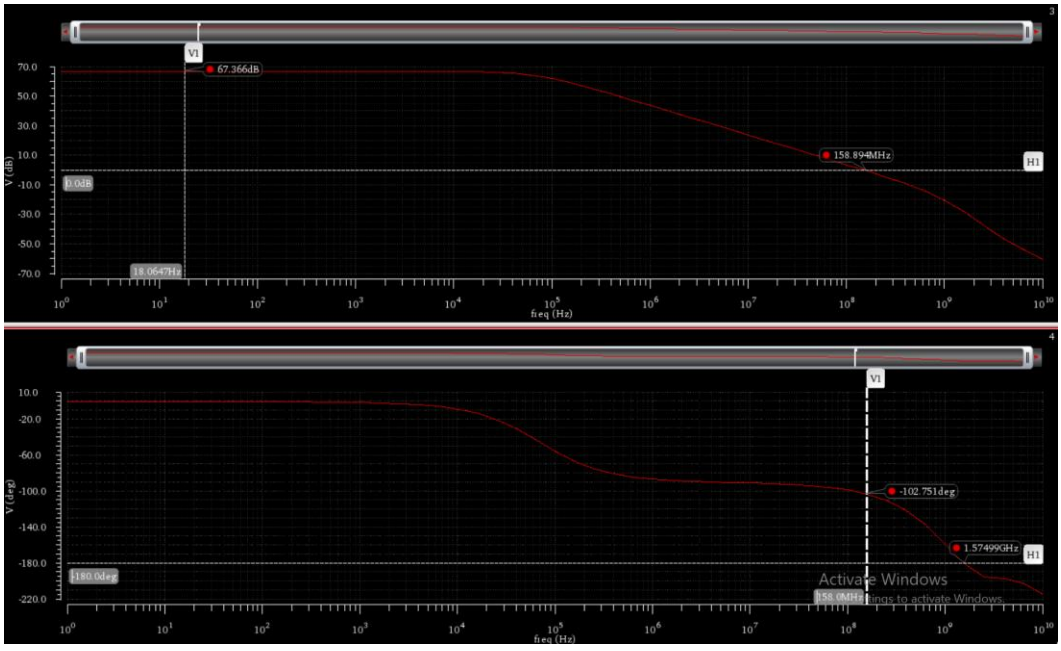


Figure 5 AC-TEST

As shown in figure 5, the Dc gain is 67.3 and the PM is 180-102.8 = 77.2
with Gain Bandwidth = 163.2M

	Expression	Value	Expression	Value
1	phaseMargin(...	77.19	gainBwProd(v(...	163.2E6

Hand analysis:

A_{vd}=gm1,2 * Rout

R_{out}= R_{up}//R_{down}
R_{up}=(ro1,2//ro9,10) *gm7,8*ro7,8 = 3.9Mohm
R_{down}= ro3,4*ro5,6*gm5,6=3.18Mohm
R_{out}=1.75Mohm
AVD=66 dB
G_{BW} ≈ gm1,2/(2pi*CL) = 173M

Comment:

Theoretical GBW **is less than** simulated GBW

3.1.2 ➔ XF test

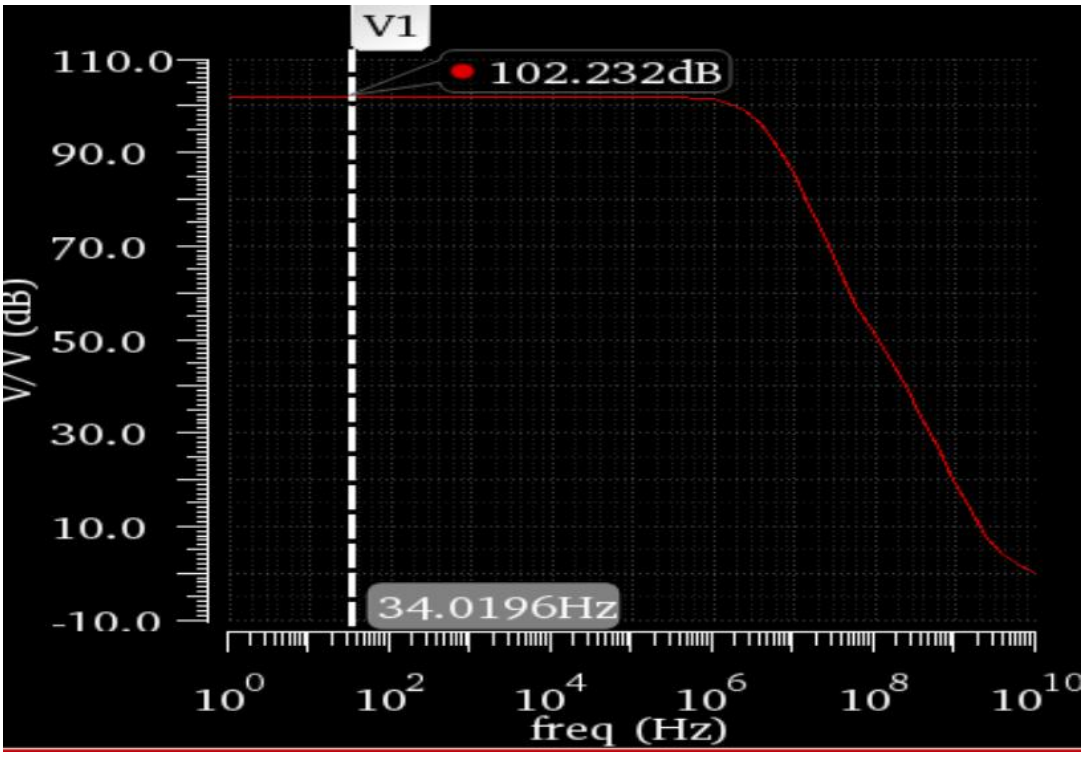


Figure 6 CMMR vs frequency

As shown in figure 6, the CMRR is 102.232 dB

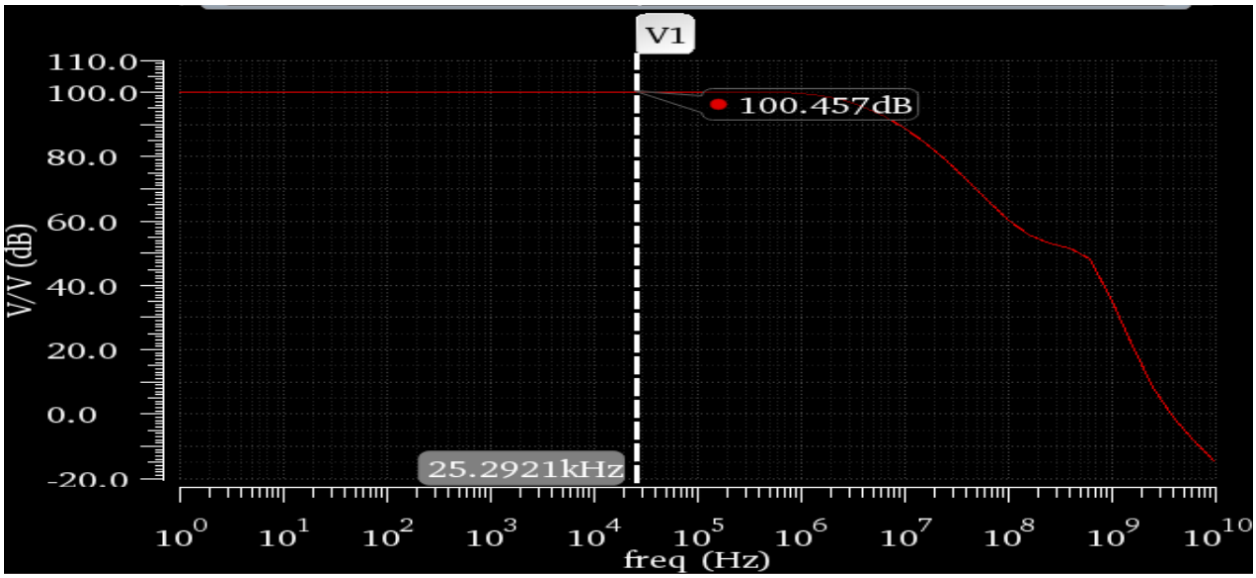


Figure 7 PSRR differential vs frequency

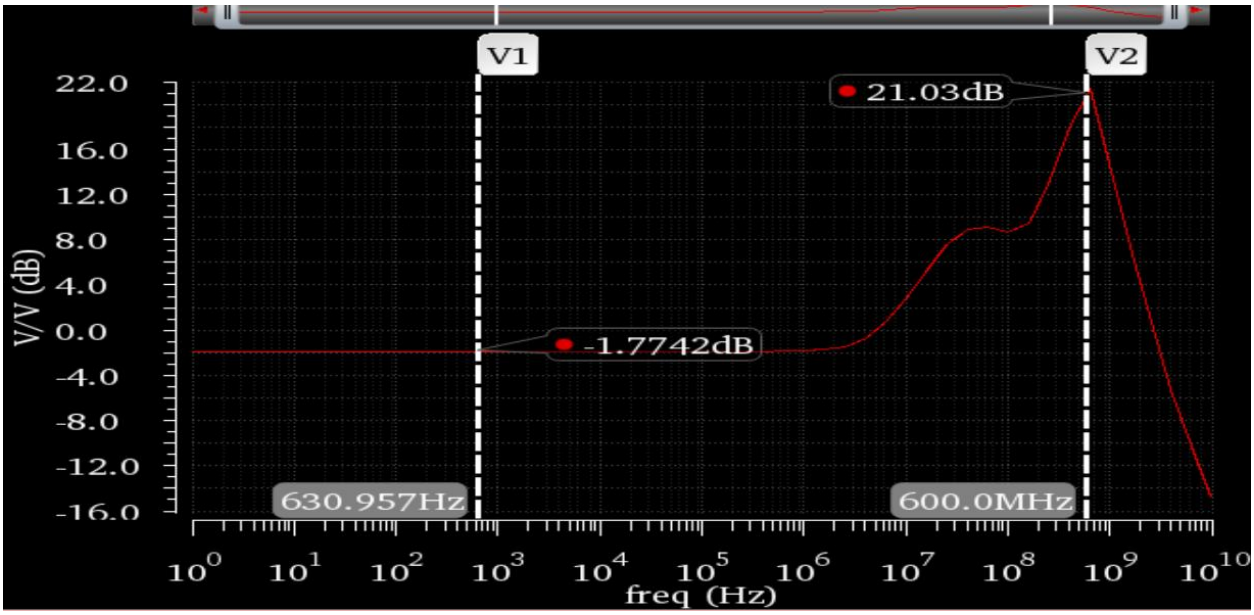


Figure 8 PSRR common vs frequency

As shown in figure 7 and figure 8, the PSRR differential is 100.457 dB while PSRR common is -1.7742 dB.

3.2 ==> Unity Closed loop Analysis:

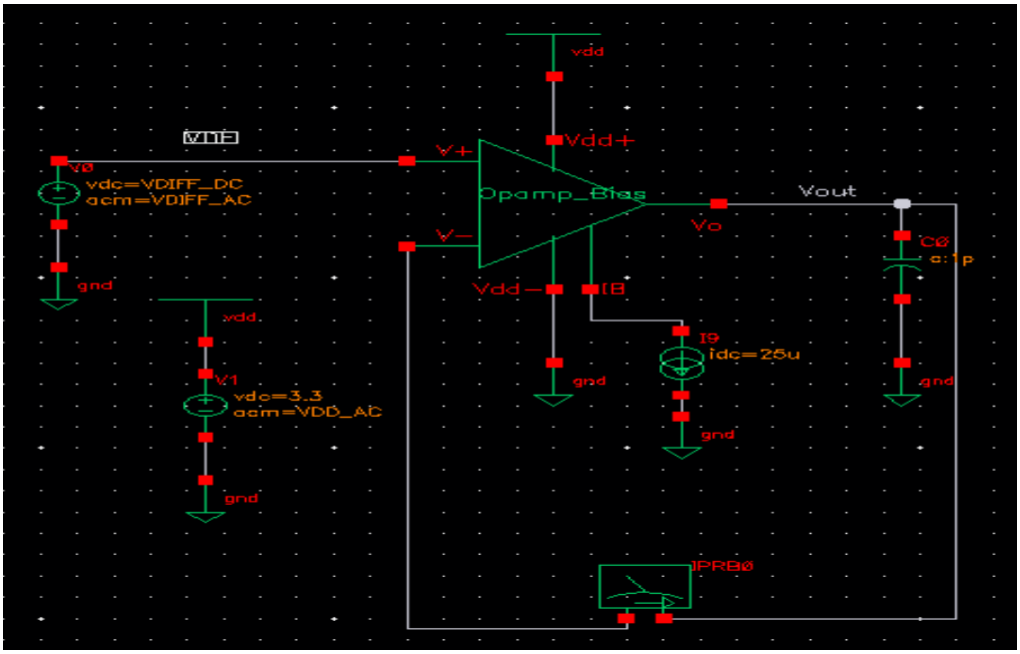


Figure 9 Unity feedback circuit

As shown in figure 10, We used Iprobe in the unity feedback.

3.2.1 ➔ STB test

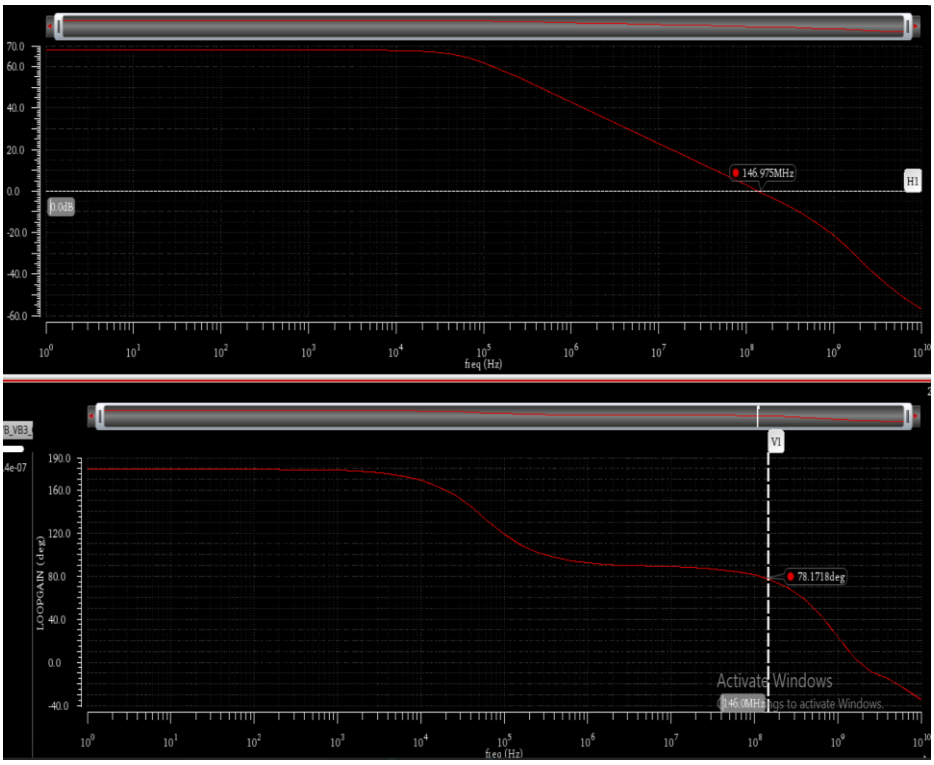


Figure 10 STB TEST

As shown in figure 10, the STB loop gain and phase is the same as the AC analysis.

	WB_VB3_CM	/phaseMargin (Deg)	/gainMargin (dB)	/gainMarginFreq (Hz)	/phase...q (Hz)
1	740.0E-9	78.26	29.70	1.707E9	144.9E6

Figure 11 STB TEST-OUTPUT

As shown in figure 11, the Gain margin is 29.7 dB with Wgc= 1.71G Hz and Phase Margin is 78.26 with Wpm = 144.9 MHz

Comment:

GBW is **less than** the AC open loop simulation as load capacitance is added with the input pair capacitance
In AC Open Loop:
PM = 77.2 with Gain Bandwidth = 163.2M

3.2.2 ==> DC-gain Analysis:

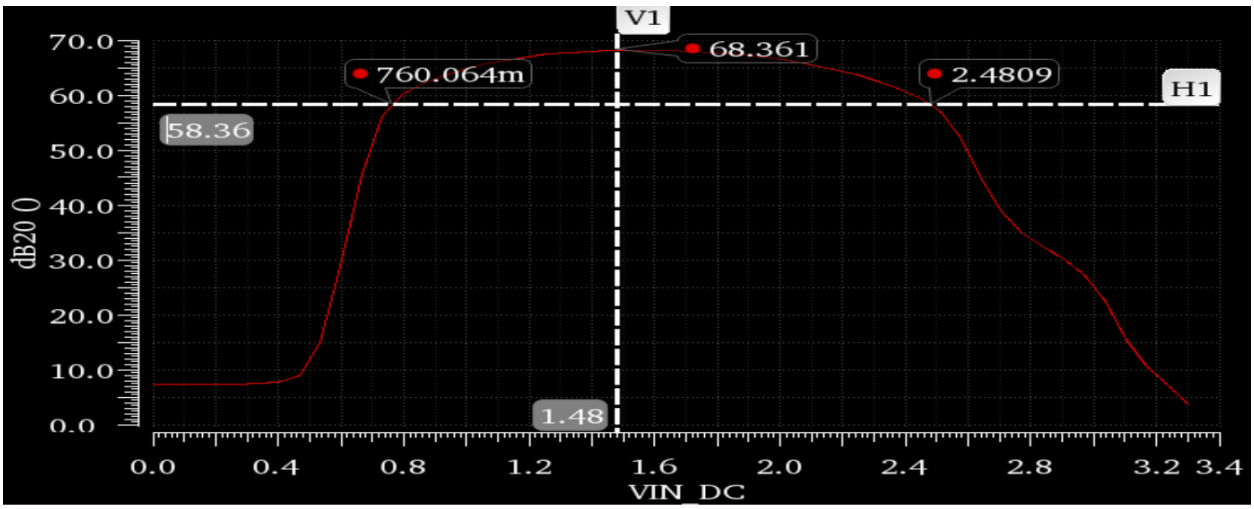


Figure 12 DC gain vs Vin DC

As shown in figure 12, The input range is between 760m and 2.48 which is **bigger than** 1.5 VPP.

3.2.3 AC Analysis:

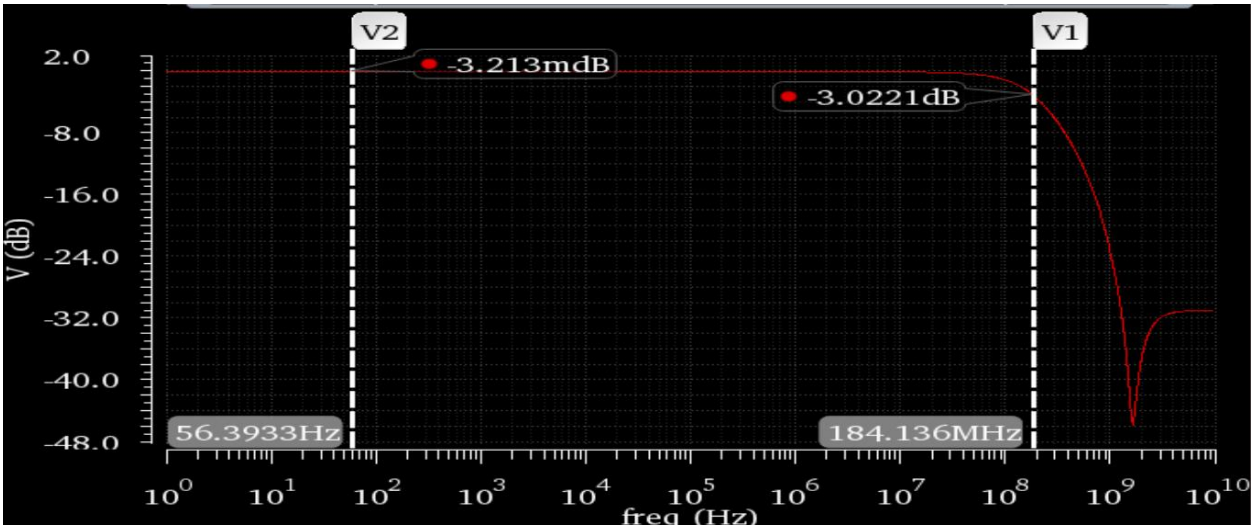


Figure 13 Closed Loop AC analysis

As shown in figure 13, the Acl = -3.23 mdB with BW = 184.1 MHz

Comments:
BW is **larger than** GBW as operating point is different from open loop.
Gain of closed loop is less than 0 dB.
Gain of open loop is finite.

3.2.4 Noise Analysis:

Device	Param	Noise Contribution	% Of Total
/I2/M4	id	3.42435e-09	23.46
/I2/M7	id	3.41726e-09	23.37
/I2/M1	id	3.14741e-09	19.82
/I2/M0	id	3.14407e-09	19.78
/I2/M3	id	1.51658e-09	4.60
/I2/M2	id	1.51626e-09	4.60
/I2/M3	fn	8.04967e-10	1.30
/I2/M2	fn	8.01352e-10	1.28

Spot Noise Summary (in V/sqrt(Hz)) at 10M Hz Sorted By Noise Contributors
Total Summarized Noise = 7.06945e-09
Total Input Referred Noise = 7.08131e-09

Figure 14 *Top* Noise Contributers

As shown in figure 14, the top 4 contributors @10MHz are M4, M7, M1 and M0 with total noise = 7.08 nV/Hz < 10 nV/Hz.

Comment:
Cascode doesn't contribute to the noise as cascode devices see generated gain. Most Noise contributors are input pair and PMOS Current source at folding node.

3.2.5 Transient Analysis:

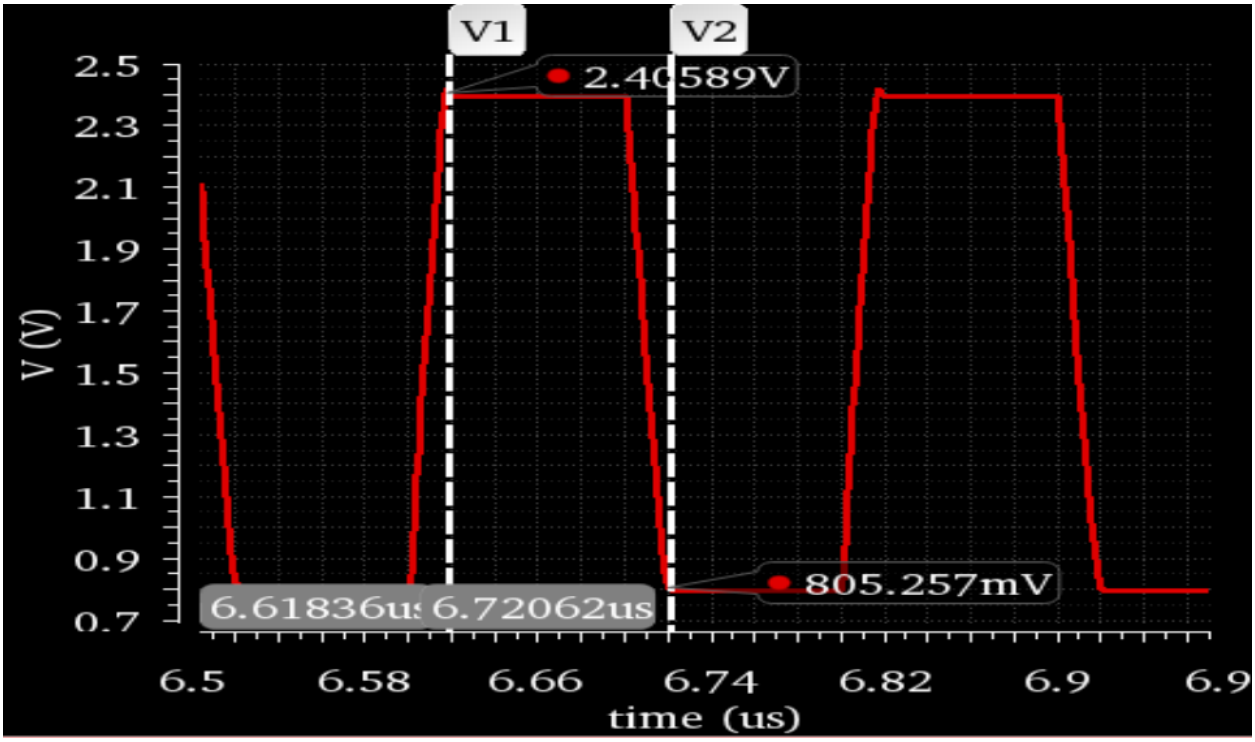


Figure 15 Vout Transient Output

As shown in figure 16, The Slew Rate SR= $\frac{2.405-0.805}{6.7206-6.618} \approx 105M$

3.2.6 ➔Spectrum Analysis:

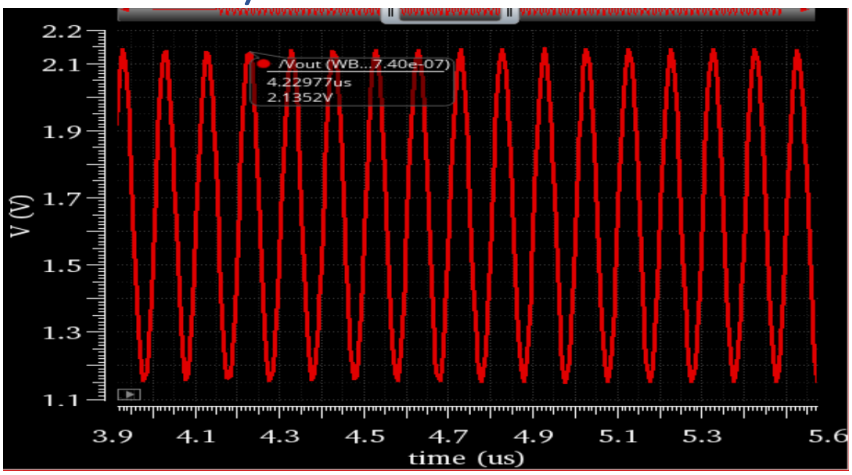


Figure 16 Vout due to sin input

As shown in figure 16, the output is not pure sine wave.

folded_cascode:Closed_Loop_TB:1	SR	102.6M

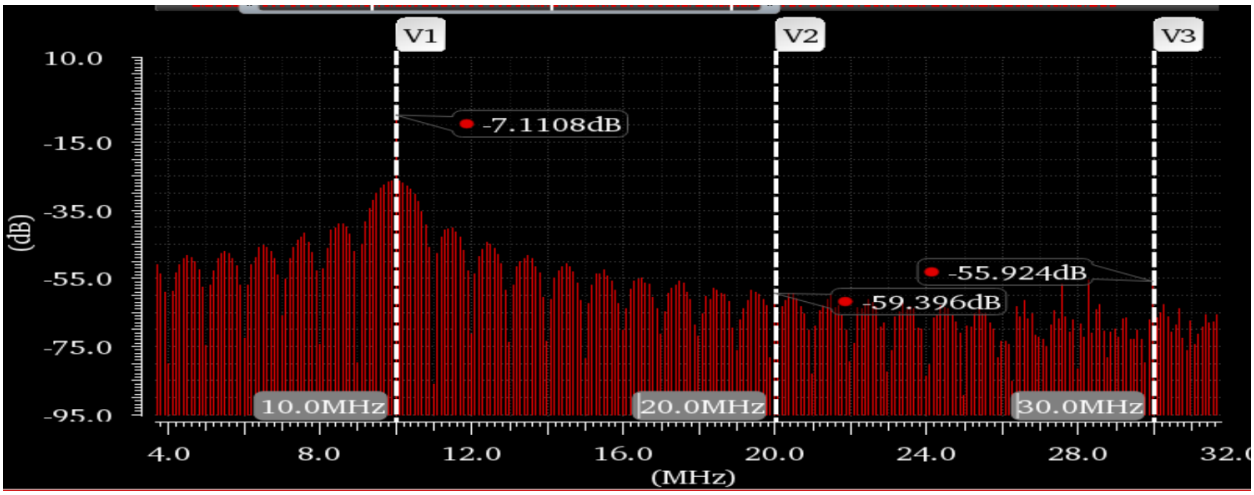


Figure 17 Vout Spectrum

As shown in figure 17, The HD2 = $20 \cdot \log10\left(\frac{V2\omega}{V\omega}\right) = -59.39 + 7.11 = -52.28\ dB$

And HD3 $20 \cdot \log10\left(\frac{V3\omega}{V\omega}\right) = -55.92 + 7.11 = -48.81\ dB$

As for the all harmonics:

folded_cascode:Closed_Loop_TB:1	spectrum_totalharmpower	-52.47
folded_cascode:Closed_Loop_TB:1	spectrum_dcpower	4.352
folded_cascode:Closed_Loop_TB:1	spectrum_thddb	-45.36
folded_cascode:Closed_Loop_TB:1	spectrum_thd	539.4m
folded_cascode:Closed_Loop_TB:1	spectrum_snr	9.469

THD= -45.36 dB = 0.539%

Error Analysis:

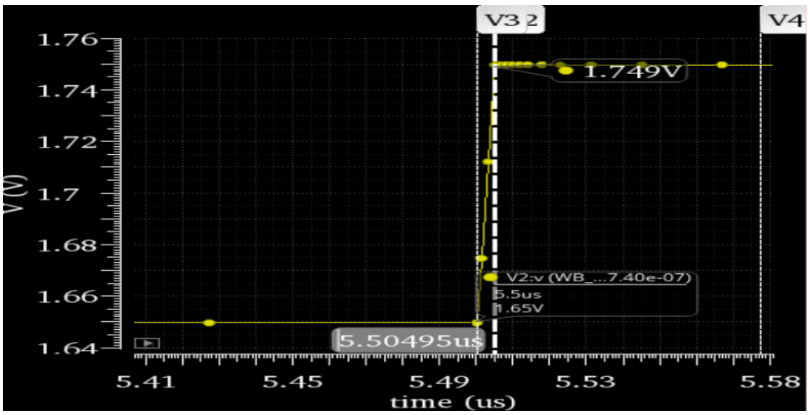


Figure 18 *Vout Impluse Response*

As shown in figure 18, The FGE = $\frac{Vfinal,sim-Vexpected}{Vexpected} = \frac{1.749-1.75}{1.75} = -0.057\%$

And the settling time Ts = 5.50495 – 5.501 = 3.95 ns.

Hand Analysis:

$$FGE = \frac{-1}{LG} = \frac{-1}{10^{\frac{67}{20}}} * 100 = -0.045\%$$

$$1\%\ Settling\ time\ = -ln(0.01)\tau = 3.38ns$$

Summary

Specification	Required	Achieved
DC Gain	58dB	67.3dB
GBW	150M	163M
SR	100 V/ sec	102 V/ sec
Output Swing	1.5 Vpp	1.72 Vpp
Input refered nosie	30nv/$\sqrt{Hz}$	7.08nv/$\sqrt{Hz}$
PM	60	78.26
GM	12	29.70
Power Consumption	min.	328.9uA (1.08mW)
Area	min.	248.45 um^2

Table 3. Achieved Specifications

It's clear that DC gain is over specification that's because the minimum length for the device is
large, making it easy to achieve high gain but the cost of that is the Large Area.