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Embedded head **Plan**

2025-2026

IEEE CAIRO UNIVERSITY STUDENT BRANCH

Personal Information

Youssef Khaled Omar Mahmoud:

- **Education:** Bachelor of Electronics and Electrical Communication Engineering (EECE), Cairo University (Senior-1, 86.93% - Excellent).

- **Core Technical Skills:**
  - **Microcontrollers & Platforms:** STM32 (ARM Cortex-M), ESP32 (IoT), AVR (Arduino Nano/Uno).
  - **Programming:** C/C++, MATLAB, Python.
  - **Tools:** STM32 Cube, Atmel Studio, Proteus, GitHub.

- **Key Achievements:**
  - **Top 15** in the IEEEDuino 2024 Student Hardware Contest (Region 8: Europe, Middle East, Africa) for the "Arduscope" education kit.
  - Strong background in **RTOS essentials** and **Model-Based Design** (MBD) concepts.

- **Leadership Experience:** Founded and led the "Arduscope" project team; Robotics Instructor and Best Member recognition at IEEE CUSB Season 2025.

Objective

To transform the IEEE CUSB Embedded Committee into a **competition-driven platform** focused on building practical, developed projects.

1. **Technical Excellence:** Deliver high-quality, structured workshops (AVR, ARM, MBD, and IoT) that move beyond theory to practical implementation and debugging.
2. **Competition Readiness:** Ensure that every participant who completes a track is prepared to develop a robust, complete project ready for submission to major IEEE contests (like **IEEEDuino** and **IEEE SC Arduino Contest**) or external competitions.
3. **Leadership Development:** Cultivate a technical committee of highly skilled and self-sufficient instructors capable of delivering complex material and mentoring future members.

Big Ideas: Competition & New Technology

My vision is to establish a **structured competition pathway** and integrate a **high-demand technology** into the committee's curriculum.

1. The Competition Track: Project-First Mentality

- **Goal:** Shift the final objective of every workshop from "completing the curriculum" to "**developing a viable competition-ready project.**"
- **Methodology:**
    - **Competition Document (NEW):** Create a mandatory **"IEEE Competition Dossier"** document for all students, detailing rules, submission requirements, and deadlines for key contests (IEEEDuino, IEEE SC, etc.) to ensure all projects are designed with these targets in mind from the start.
    - **Final Project as a Competition Entry:** The final project of each of the four main workshops (AVR, ARM, MBD, IoT) will be designed as a miniature project suitable for entry into a relevant contest (e.g., IEEEDuino, or a simpler internal competition). Students will be encouraged to adapt their project for **any external competition** they wish to target.
    - **Dedicated Final Session:** Reserve the final 1-2 sessions of the academic period for project consolidation, debugging, and presentation/documentation preparation, guided by successful alumni and competition veterans
    - **Showcase Event:** Host a small internal **"Embedded Project Showcase"** event to celebrate and evaluate the best projects before submission deadlines.

2. **New Workshop**: IoT Embedded Systems (using ESP32)
    - **Rationale:** IoT is a high-demand, cross-disciplinary field where embedded systems (ESP32/ESP8266) interface with cloud services and mobile applications. Integrating this workshop will attract a wider pool of students and provide a modern, highly marketable skill set.
    - **Focus:** Practical application of Wi-Fi communication, sensor-to-cloud data transfer (MQTT/HTTP), and the use of low-power, single-chip solutions. This directly builds on the skills needed for complex systems.

Structure

I propose a comprehensive structure led by the **Embedded Head (myself)**, supported by **two Vice Heads**, and four specialized technical teams to manage the new, expanded curriculum.

Leadership and Coordination

- **Embedded Head (1):** Overall strategy, external coordination (FR/PR), budget approval, final content sign-off, and competition mentorship.
- **Vice Head (2):** To assist in organizing and managing the workflow across the four technical workshops.
    - **Vice Head 1 (Curriculum & Training):** Responsible for the quality of content, inter-workshop consistency, and the training pipeline for new instructors.
    - **Vice Head 2 (Logistics & Projects):** Responsible for coordinating hardware acquisition (with FR/Logistics), managing the competition documentation, and overseeing the final project consolidation phase across all tracks.

Technical Teams

Team	Focus Area	Instructors Needed	Core Responsibility
AVR Team	Microcontrollers (AVR)	4-5	Deliver the foundational C and bare-metal AVR workshop.
ARM Team	Microcontrollers (ARM/STM32) & RTOS	4-5	Deliver the advanced ARM architecture and RTOS workshop.
MBD Team	Model-Based Design (MATLAB/Simulink)	3-4	Deliver the control-focused MBD and Embedded Coder workshop.
IoT Team (NEW)	Internet of Things (ESP32/Cloud)	3-4	Develop and deliver the new IoT-focused workshop, managing cloud integration demos.
Mentorship Team (HR)	Emotional & Logistical Support	4-6	Crucial for conducting participant check-ins, managing conflict resolution, and ensuring instructor well-being and tracking engagement.
Total Instructors		**19 - 25 Members**	*This allows for specialized knowledge and reduced load per instructor.*

Continuity Plan

The continuity plan will focus on standardization and knowledge transfer to sustain the new competition-focused vision.

1. **Standardized Content Repository:** Create a highly structured, well-commented **GitHub repository** (or similar platform) for all four workshop tracks. This repository will contain:
   - Final Presentation Slides (Editable).
   - Standardized Code Templates and Labs (Version-controlled).
   - A comprehensive **Feedback Log** from the current season.
2. **Instructor Documentation:** Mandate that all current instructors complete detailed **Lesson Documentation** and a comprehensive **Session Feedback Log**.
3. **Competition Dossier:** Compile a simple, step-by-step **IEEE Competition Submission Guide** (including IEEEDuino and regional contest links, deadlines, and successful project examples from the current season) to hand over to the successor, ensuring the competition momentum is maintained.

Workshops Content Plan

Embedded AVR Workshop (Unchanged - Foundational)

Session Number	Content
0	Intro and setup
1	C Programming- Part 1
2	C Programming- Part 2
3	Embedded Systems Concepts
4	GPIO and Layered Architecture
5	Interrupts
6	Timers & ICU
7	PWM & ADC
8	LCD & Keypad
9	Introduction to Communication Protocols & UART
10	I2C & SPI

Embedded ARM Workshop (Unchanged - Advanced Bare-Metal/RTOS)

Session Number	Content
1	ARM Architecture
2	GPIO Driver
3	SysTick Timer and PLL
4	System Faults and Exceptions
5	NVIC Driver
6	Memory Protection Unit
7	RTOS- Part 1 (Synchronization & Task Management)
8	RTOS- Part 2 (Messaging & Memory Management)
9	Automotive Buses, Intro and LIN Bus
10	Automotive Buses, CAN Bus

Model-Based Design Workshop (Unchanged - Control Focus)

Session Number	Content
1	MDB Concepts & Workflow
2	MATLAB Programming Essentials
3	Simulink Modeling Basics
4	Arduino Simulink Interface- Part 1 (Data Acquisition)
5	Arduino Simulink Interface- Part 2 (Actuator Control)
6	PID Controller Design- Part 1 (Theory & Tuning)
7	PID Controller Design- Part 2 (Simulink Implementation)
8	Stateflow Design & Logic
9	System Modelling (Transfer Functions)
10	Embedded Coder (Code Generation & PIL/SIL Concepts)

Workshops Content Plan

New! IoT Embedded Workshop (ESP32 Focus)

Session Number	Content
1	Introduction to IoT Ecosystem & ESP32 Architecture
2	Bluetooth BLE Basics
3	WiFi/Network Connectivity & TCP/UDP Basics
4	HTTP Protocol (GET/POST requests)
5	Using APIs (Weather/Time/Custom Data)
6	MQTT Protocol: Publish/Subscribe for Reliable Data Transfer
7	Cloud Integration: Connecting ESP32 to a Platform (e.g., Firebase/ThingSpeak)
8	Interfacing with Sensors & Peripherals (BME280, OLED)
9	Over-The-Air (OTA) Updates and Power Management
10	**Project Work Session 1**: Planning & Hardware Integration
11	**Project Work Session 2**: Cloud Logic & Submission Prep

Time Plan (Academic Year 2025/2026)

This timeline is precisely aligned with the Cairo University, Faculty of Engineering, First Semester 2025/2026 dates, ensuring committee activities do not conflict with official exams or holidays.

Date Range	Core Action / Phase	Rationale
24/10/2025 – 25/10/2025	**Recruitment and Interviews (Phase 1 - Rapid Screening)**	**URGENT:** Must finish critical interviews before pre-midterm study week begins.
26/10/2025 – 22/11/2025	**Midterm Study/Exam Break**	**Extended Break:** Includes the study week before Midterms (26/10-1/11) and the Midterm Exams Period (2/11-22/11). Internal work only.
23/11/2025 – 27/12/2025	Learning Phase & Content Preparation	Instructor training, content creation, and participant selection. The time is now condensed into a single phase after midterms.
28/12/2025 – 22/1/2026	**Finals Study/Exam Break**	**Extended Break:** Includes the study week before Finals (28/12-3/1) and the University Final Exams Period (4/1-22/1). No activity.
25/1/2026 – 14/2/2026	Mid-Year Holiday (Relax/Final Content Review)	University Holiday.
15/2/2026 – 28/2/2026	Final Participants Vetting / Logistics Check	Preparation week right before the second semester starts.
1/3/2026 – 7/3/2026	**Session 1** in all workshops	**Start of Workshops** (Start of Second Semester activities).
8/3/2026 – 14/3/2026	Session 2 in all workshops	
15/3/2026 – 21/3/2026	Session 3 in all workshops	
22/3/2026 – 28/3/2026	Session 4 in all workshops	
29/3/2026 – 11/4/2026	**Midterm Study/Exam Break**	**Extended Break:** Includes the week before Midterms (Mar 29-Apr 4) and the Midterm Exam Period (Apr 5-11).
12/4/2026 – 18/4/2026	**Session 5 & 6** in all workshops	**CONDENSED:** Sessions must be combined to finish on time, accommodating the extended break periods.

Time Plan (Academic Year 2025/2026)

Date Range	Core Action / Phase	Rationale
19/4/2026 – 25/4/2026	**Session 7 & 8** in all workshops	**CONDENSED:** Sessions must be combined to finish on time.
26/4/2026 – 2/5/2026	**Session 9 & 10** in all workshops	**CONDENSED:** Final push for content completion before the long Finals Break.
3/5/2026 – 5/6/2026	**Finals Study/Exam Break**	**Extended Break:** Includes the week before Finals (May 3-9) and the University Finals Prep Period (May 10-Jun 5). Sessions must finish before this date.
7/6/2026 – 20/6/2026	Final Project Submission	
21/6/2026 – 30/6/2026	Final Project Evaluation & Showcase	

Risk Plan

We manage technical and logistical risks through redundancy and proactive preparation to protect the quality of delivery and student experience.

Risk Category	Risk Description	Probability	Mitigation Strategy
Curriculum	**Session Time Insufficient:** Sessions run long due to high interaction or complex labs.	Medium	**Pre-recorded Segments & Flexible Labs:** Provide online supplementary videos and schedule dedicated "Debugging/Open Lab" hours.
HR	**Instructor Resignation/Underperformance:** A core team member leaves or fails to deliver quality content.	Medium	**VP Monitoring & Redundancy:** Vice Heads monitor performance weekly. Maintain a **Backup Instructor Pool** (e.g., strong alumni/senior members) to step in.
Logistics	**Hardware Supply Chain Issues:** Key components (STM32/ESP32) are unavailable or too expensive.	High	**Early FR Coordination:** Budget finalization and hardware procurement start in Phase I. **Alternative Simulation:** Increase Proteus/Simulink dependency as a backup.
Project	**Competition Failure:** Projects are technically sound but fail due to poor documentation or not meeting contest rules.	Medium	**Dedicated Final Session:** Use the last sessions specifically for documentation, presentation, and **Competition Dossier** review.

HR Plan

The committee requires specialized technical depth and strong organizational support to execute four complex tracks simultaneously.

Role	Number Needed	Core Tasks	Required Technical Background
Embedded Head (You)	1	Strategy, Budget, External Relations, Final Sign-off, Competition Mentorship.	Advanced C/C++, STM32, RTOS, IoT (ESP32), Project/Team Leadership.
Vice Head 1 (Curriculum)	1	Content Vetting, Inter-track QC, Instructor Training, Documentation Management.	Strong expertise in 2+ tracks (e.g., AVR/ARM), high organizational skills.
Vice Head 2 (Logistics & Projects)	1	Hardware Coordination, Project Follow-up, Showcase Event Organization, Competition Dossier Management.	Technical background (can debug issues), excellent organizational/communication skills.
Technical Instructor (AVR)	4-5	Deliver Foundational C/AVR content, lab assistance, session feedback logs.	Proficiency in **C Programming**, AVR bare-metal, Interrupts, I/O protocols.
Technical Instructor (ARM)	4-5	Deliver Advanced ARM/STM32 content, focus on RTOS concepts.	Strong experience in **STM32/Tiva C**, bare-metal drivers, **RTOS (FreeRTOS)**.
Technical Instructor (MBD)	3-4	Deliver MBD content, focus on Simulink modeling and Embedded Coder.	Expertise in **MATLAB/Simulink**, Control Systems, and Embedded Code Generation.
Technical Instructor (IoT)	3-4	Deliver the new ESP32/Cloud content, manage cloud demos.	Experience with **ESP32** (or similar Wi-Fi microcontrollers), MQTT, HTTP, and Cloud platforms.
Mentorship Team (HR)	**4-6**	Conduct participant check-ins, manage conflict resolution, ensure instructor well-being, and track session engagement/attendance.	Strong communication skills, empathy, and organizational support background.

Quality Control Plan

Quality Control focuses on ensuring content accuracy and instructor effectiveness, directly supporting the goal of generating competition-ready projects.

QC Area	Process and Measure	Responsibility
Content Quality	**Two-Stage Vetting:** Vice Head 1 reviews all presentations and labs 7 days prior to delivery. Final code templates are reviewed and merged on GitHub by the Head.	Vice Head 1 and Embedded Head
Instructional Delivery	**Peer-to-Peer Review:** Instructors observe and provide a short, structured review for at least one colleague's session. **Student Feedback:** Mandatory anonymous online feedback after every 3 sessions to track clarity and engagement.	Vice Head 1 and All Instructors
Project Output	**Standardized Rubric:** The Embedded Project Showcase uses a clear rubric (Technical Complexity, Competition Relevance, Documentation, Presentation).	Vice Head 2 and Project Support Instructor
Knowledge Transfer	**Mandatory Documentation:** Instructors submit detailed lesson plans and feedback logs, which are stored centrally in the Content Repository.	All Instructors

Workshops components/Budget Plan

NOTE: This base budget provides **two core microcontroller board/unit per workshop** for the technical tracks, and a shared lot of general components. If better sponsorship is secured, we will upgrade the offering to full component kits for all students.

Cost Center	Item Description	Estimated Cost Per Unit (EGP)
AVR Track	**Atmega32**	400 EGP
ARM Track	**STM32 F103C8 bluepill**	600 EGP
MBD Track	**Arduino Uno Board**	600 EGP
IoT Track	**ESP32 Dev Kit (Wi-Fi, Bluetooth)**	700 EGP
General Supplies	**Shared Lot of Components for All Tracks** 4x (Includes 10 LEDs, 2 Breadboards, 10 Resistors, 10 Wires M-M, 10 Wires F-M, 10 Wires F-F, 5 Buttons, 2 Potentiometers, 1 OLED per workshop)	2400 EGP
TOTAL ESTIMATED BUDGET		4700 EGP