1. Where is DDR register located?

ATMega32 has 4 ports, and so each port has a DDR:

- Port A: DDRA
- Port B: DDRB
- Port C: DDRC
- Port D: DDRD

**Port A Data Direction Register – DDRA**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| | DDA7 | DDA6 | DDA5 | DDA4 | DDA3 | DDA2 | DDA1 | DDA0 | DDRA |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

**Port B Data Direction Register – DDRB**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| | DDB7 | DDB6 | DDB5 | DDB4 | DDB3 | DDB2 | DDB1 | DDB0 | DDRB |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

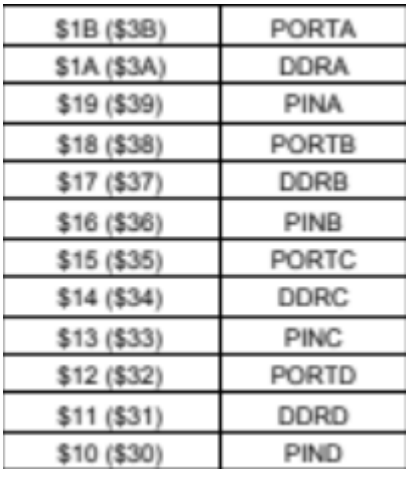
**Port C Data Direction Register – DDRC**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| | DDC7 | DDC6 | DDC5 | DDC4 | DDC3 | DDC2 | DDC1 | DDC0 | DDRC |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

**Port D Data Direction Register – DDRD**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| | DDD7 | DDD6 | DDD5 | DDD4 | DDD3 | DDD2 | DDD1 | DDD0 | DDRD |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

from register summary in page 327 of the ATMega32 datasheet:



| | |
|---|---|
| $1B ($3B) | PORTA |
| $1A ($3A) | DDRA |
| $19 ($39) | PINA |
| $18 ($38) | PORTB |
| $17 ($37) | DDRB |
| $16 ($36) | PINB |
| $15 ($35) | PORTC |
| $14 ($34) | DDRC |
| $13 ($33) | PINC |
| $12 ($32) | PORTD |
| $11 ($31) | DDRD |
| $10 ($30) | PIND |

we find that the memory-mapped locations of each DDR are as shown in the table:

| Register | Memory-mapped address |
|---|---|
| DDRA | 0x3A |
| DDRB | 0x37 |
| DDRC | 0x34 |
| DDRD | 0x31 |

2. SRAM vs Flash:

| Feature | SRAM | Flash |
|---|---|---|
| Volatility | Volatile Memory | Non-volatile Memory |
| Usage | Variables | Program code |
| Speed | Fast | slower |
| Lifetime | Unlimited runtime use | High endurance |
| Modified During Runtime | No | Yes |