Introduction to Digital Design

There are two different ways for the digital design implementation: Application Specific Integrated Circuit (ASIC) flow and Field Programmable Gate Array (FPGA) flow. ASIC flow is a custom design that enables making required system specification using a custom architecture in order to meet frequency, power, and throughput.

FPGA Design Flow

Field-programmable gate arrays (FPGAs) are configurable integrated circuits that you can program to implement arbitrary circuit topologies. Classified as spatial compute architectures, FPGAs differ significantly from fixed Instruction Set Architecture (ISA) devices such as CPUs and GPUs.

In essence, FPGAs consist of programmable logic blocks and configurable interconnects, which can be used to implement complex digital circuits. This allows FPGAs to perform tasks such as digital signal processing, image and video processing, and machine learning, with high efficiency and flexibility.

Typically its architecture has configurable logic blocks (CLBs), input/output blocks (IOBs), memory blocks (BRAM), and digital signal processing (DSP) blocks. CLBs contain configurable logic elements (LEs) that can be programmed to implement a wide range of digital circuits, while IOBs provide input/output interfaces for the FPGA. BRAM and DSP blocks provide specialized memory and signal processing functions.

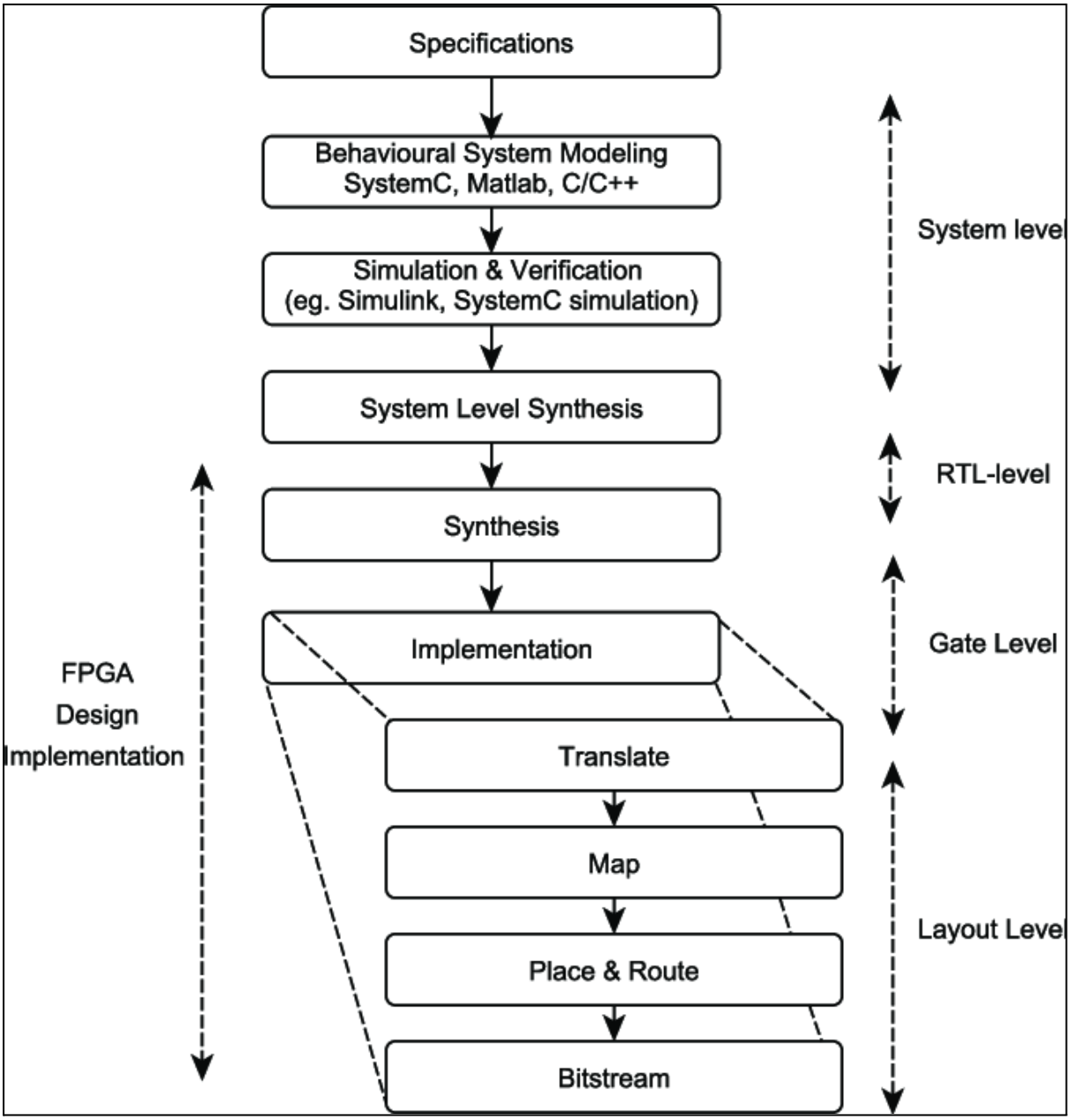

Figure 4. FPGA Design Flow

Designing an FPGA-based system typically involves several stages, including:

1. Specification: Defining the requirements of the system and specifying the functionality that the FPGA must implement.
2. High-Level Design: Developing a high-level design using a hardware description language (HDL) such as Verilog or VHDL.

3. Synthesis: Translating the HDL code into a netlist of logic gates and flip-flops that can be implemented on the FPGA.
4. Place and Route: Mapping the netlist onto the FPGA architecture and routing the connections between logic blocks and I/O pins.
5. Timing Analysis: Verifying that the design meets timing requirements and constraints, such as clock frequency and maximum delay.
6. Bitstream Generation: Generating a bitstream file that can be programmed onto the FPGA to configure its logic blocks and interconnects.
7. Testing and Verification: Testing the FPGA-based system to ensure that it meets functional and performance requirements.

FPGA development typically requires specialized software tools, including HDL editors, synthesis and place-and-route tools, simulation tools, and programming tools for configuring the FPGA. We are going to use Quartus Prime Lite Software provided by Altera and Cyclone IV **EP4CE6E22C8N** FPGA device to perform labs.

Introduction to Cyclone IV EP4CE6E22C8N FPGA Kit

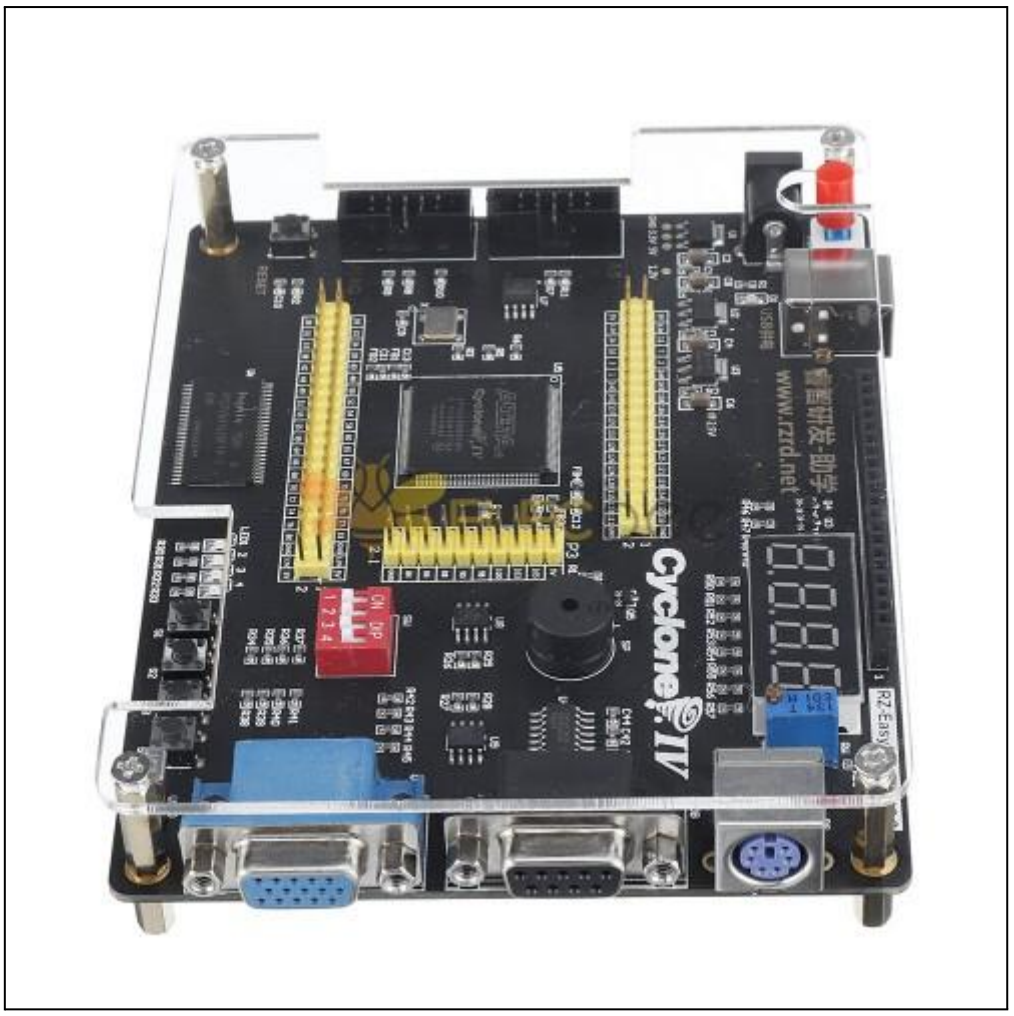

Figure 5. Cyclone IV EP4CE6E22C8N FPGA

General Notes

Power supply

There are two ways to supply power for the development board: USB power supply or 5V power adapter power supply. The red button below is the power switch:

- Press the switch button: USB power supply;
- Lift the switch button: 5V power adapter power supply.

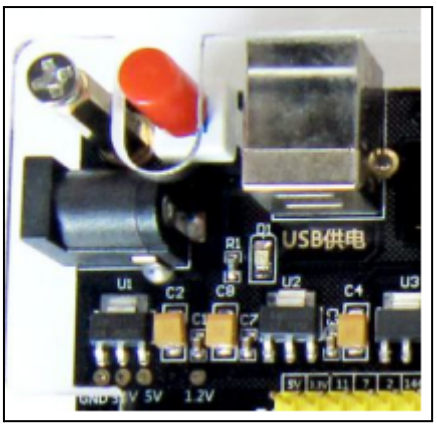

Figure 6. Shows the Power Supply Button in EP4CE6E22C8N FPGA

JTAG

Development board with JTAG Download Interface, don't pull or plug the JTAG cable in charged state, charged pull or plug the JTAG/AS cable may cause fatal damage to the FPGA chip.

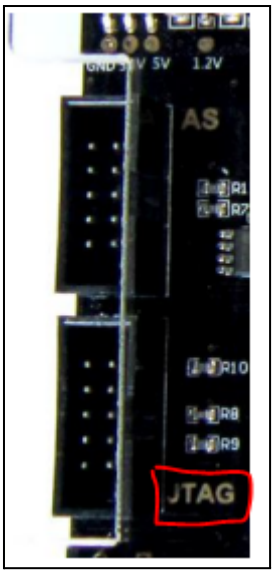

Figure 7. Shows the JTAG interface in EP4CE6E22C8N FPGA

Pinout Numbers

Keys	Pin number
KEY1	88
KEY2	89
KEY3	90
KEY4	91

Figure 8. Dip Switches Pin Numbers of EP4CE6E22C8N FPGA

LED	Pin number
led1	87
led2	86
led3	85
led4	84

Figure 9. Leds Pin Numbers of EP4CE6E22C8N FPGA

Schematic Prints of LEDs and Switches

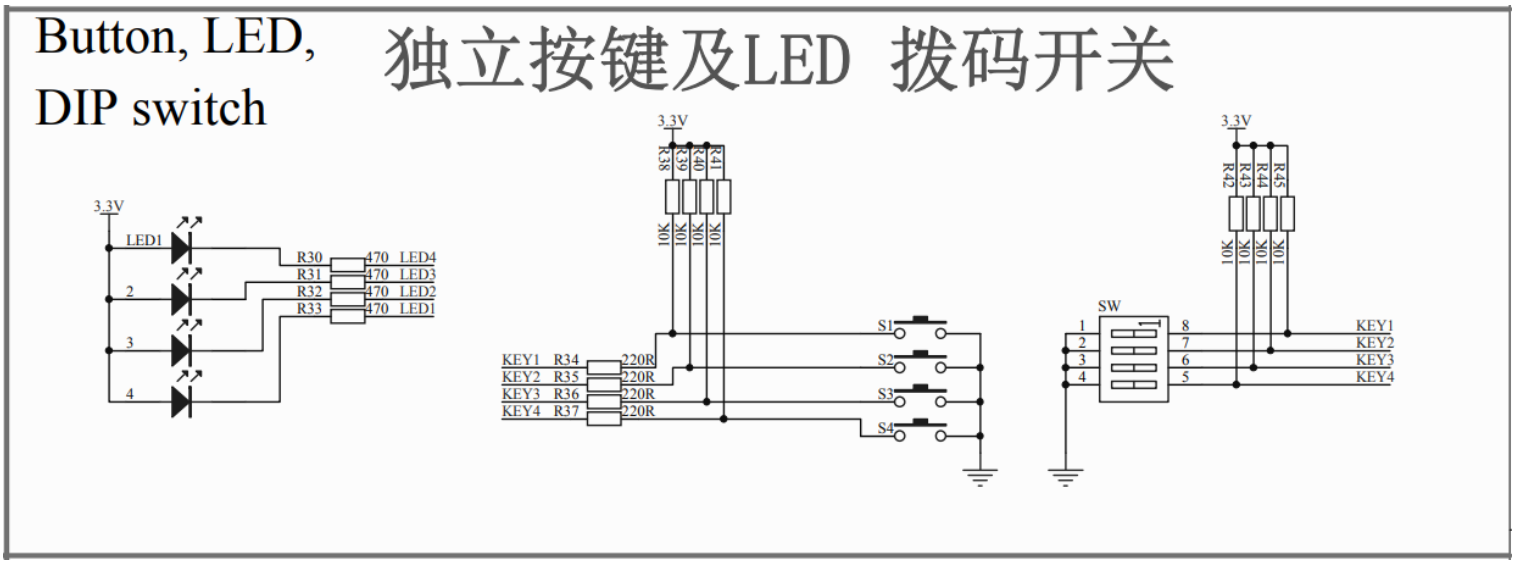

Figure 10. Schematic Diagram for the Circuit Connections of Leds and Switches of EP4CE6E22C8N FPGA

Please note the following:

- Switches are already connected to VDD, and when pressed it will be connected to GND.
- Leds are connected to VDD from the P-side of the PN-junction, and it will be turned on when the N-side is connected to GND. Otherwise will be turned off