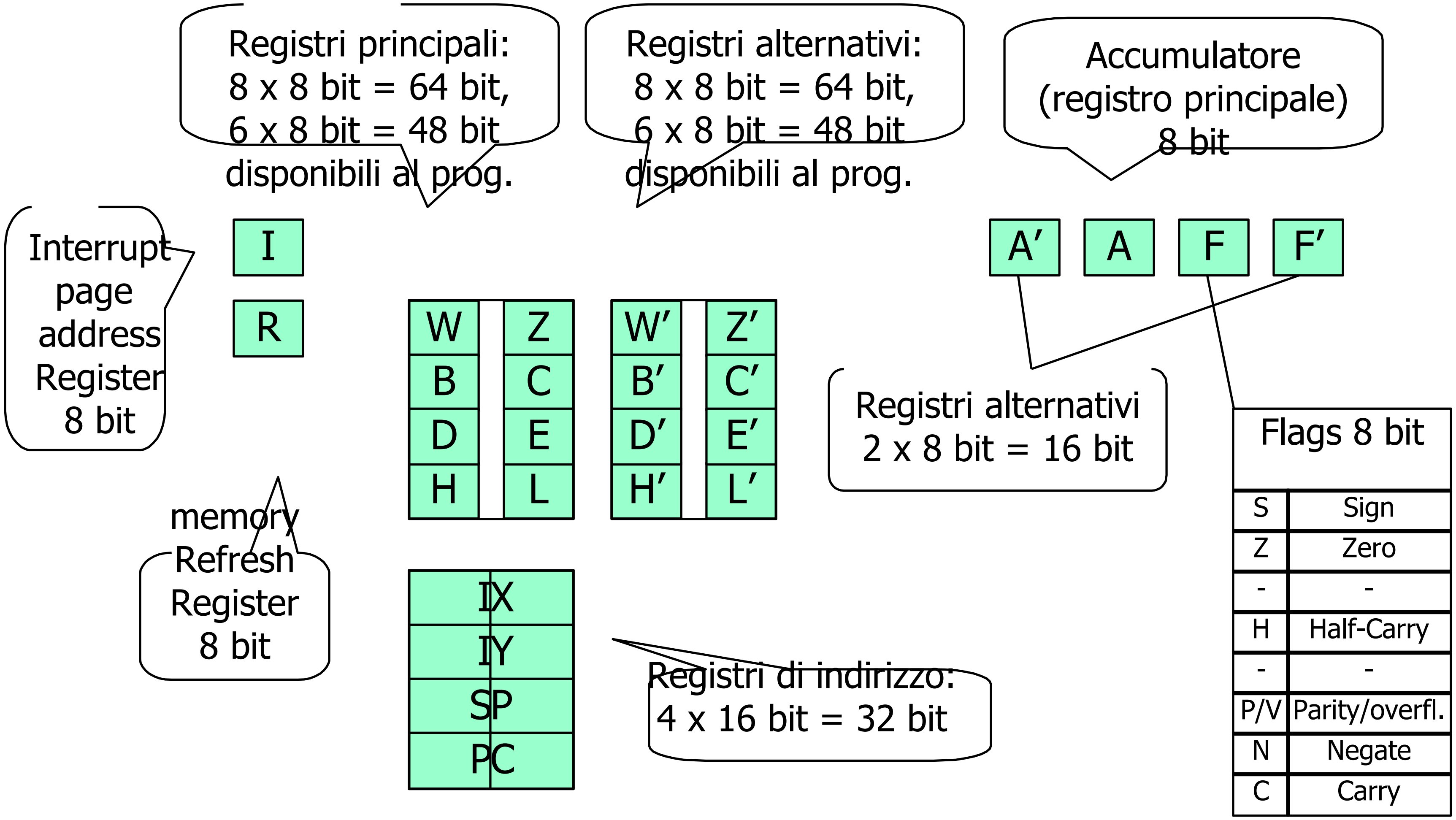
ZiLOG80

Calcolatori Elettronici

Bartolomeo Bajic

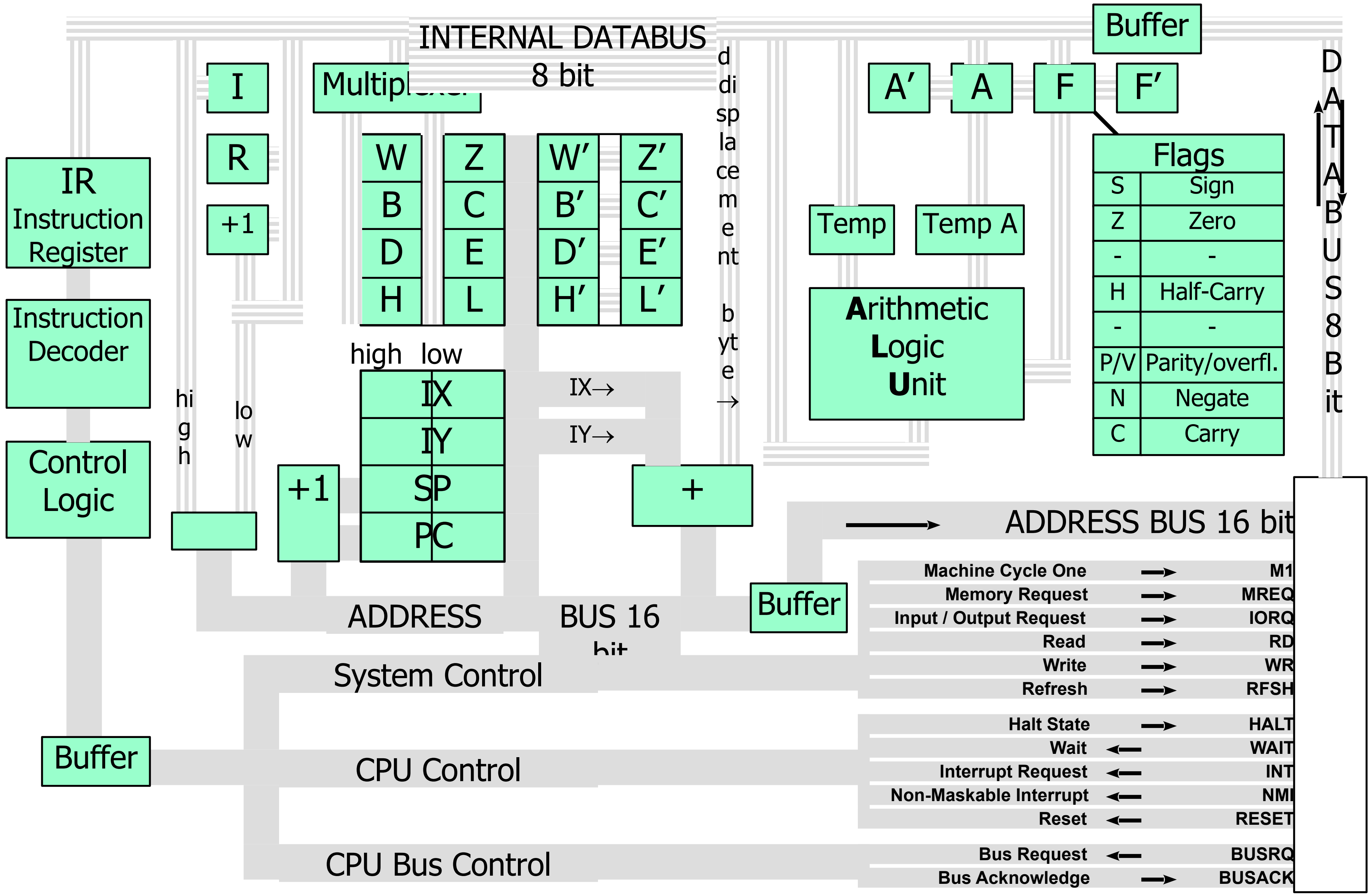

Registri principali: 8 x 8 bit = 64 bit, 6 x 8 bit = 48 bit disponibili al prog.
Registri alternativi: 8 x 8 bit = 64 bit, 6 x 8 bit = 48 bit disponibili al prog.
Accumulatore (registro principale) 8 bit
Interrupt page address Register 8 bit
I
R
W
Z
B
C
D
E
H
L
W'
Z'
B'
C'
D'
E'
H'
L'
A'
A
F
F'
Registri alternativi 2 x 8 bit = 16 bit
memory Refresh Register 8 bit
IX
IY
SP
PC
Registri di indirizzo: 4 x 16 bit = 32 bit
Flags 8 bit

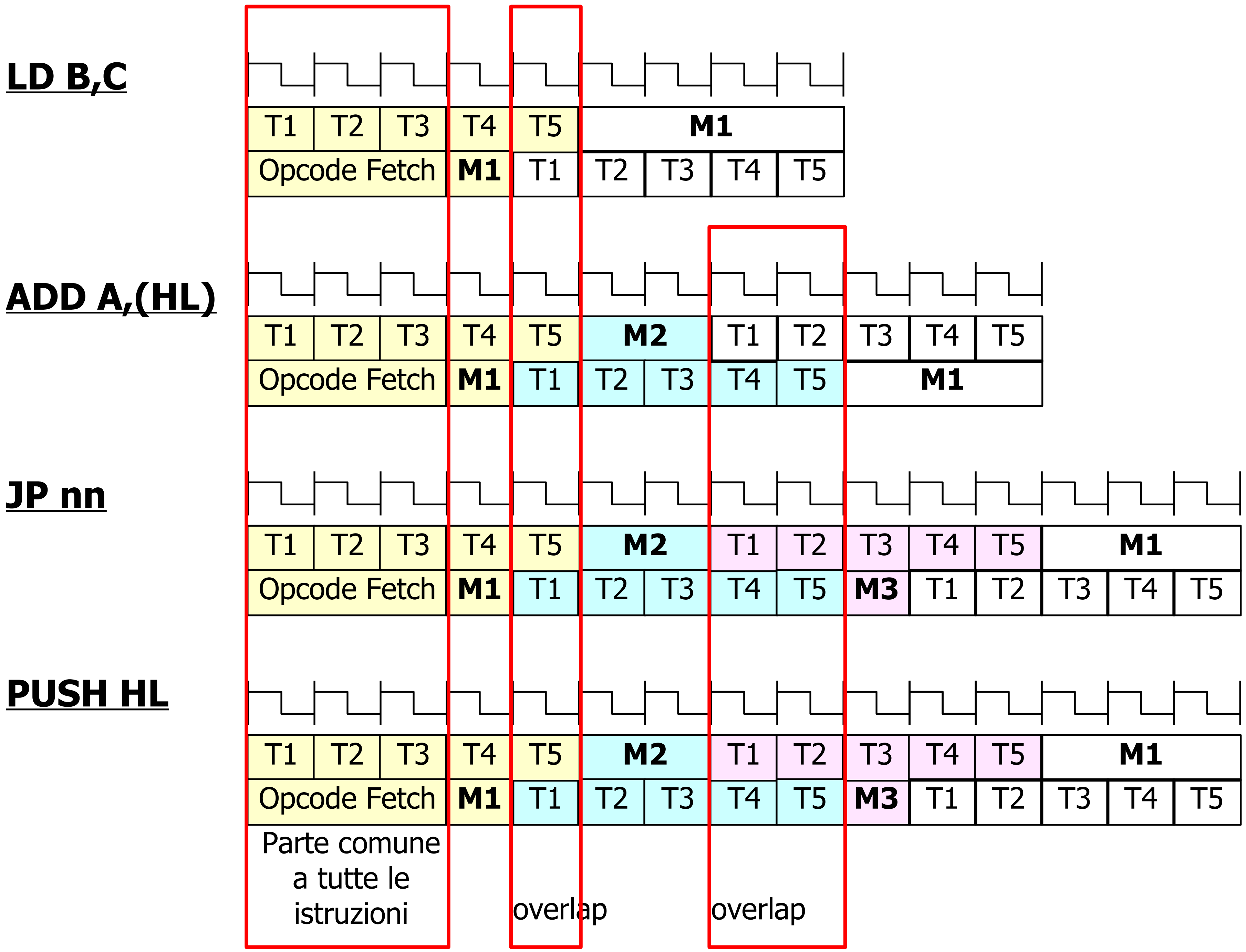
S	Sign
Z	Zero
-	-
H	Half-Carry
-	-
P/V	Parity/overfl.
N	Negate
C	Carry

Memoria Interna allo Z80

Z80

T1	T2	T3	T4	T5	**M2**	T1	T2	T3	T4	T5	**M1**	
Opcode Fetch	**M1**	T1	T2	T3	T4	T5	**M3**	T1	T2	T3	T4	T5

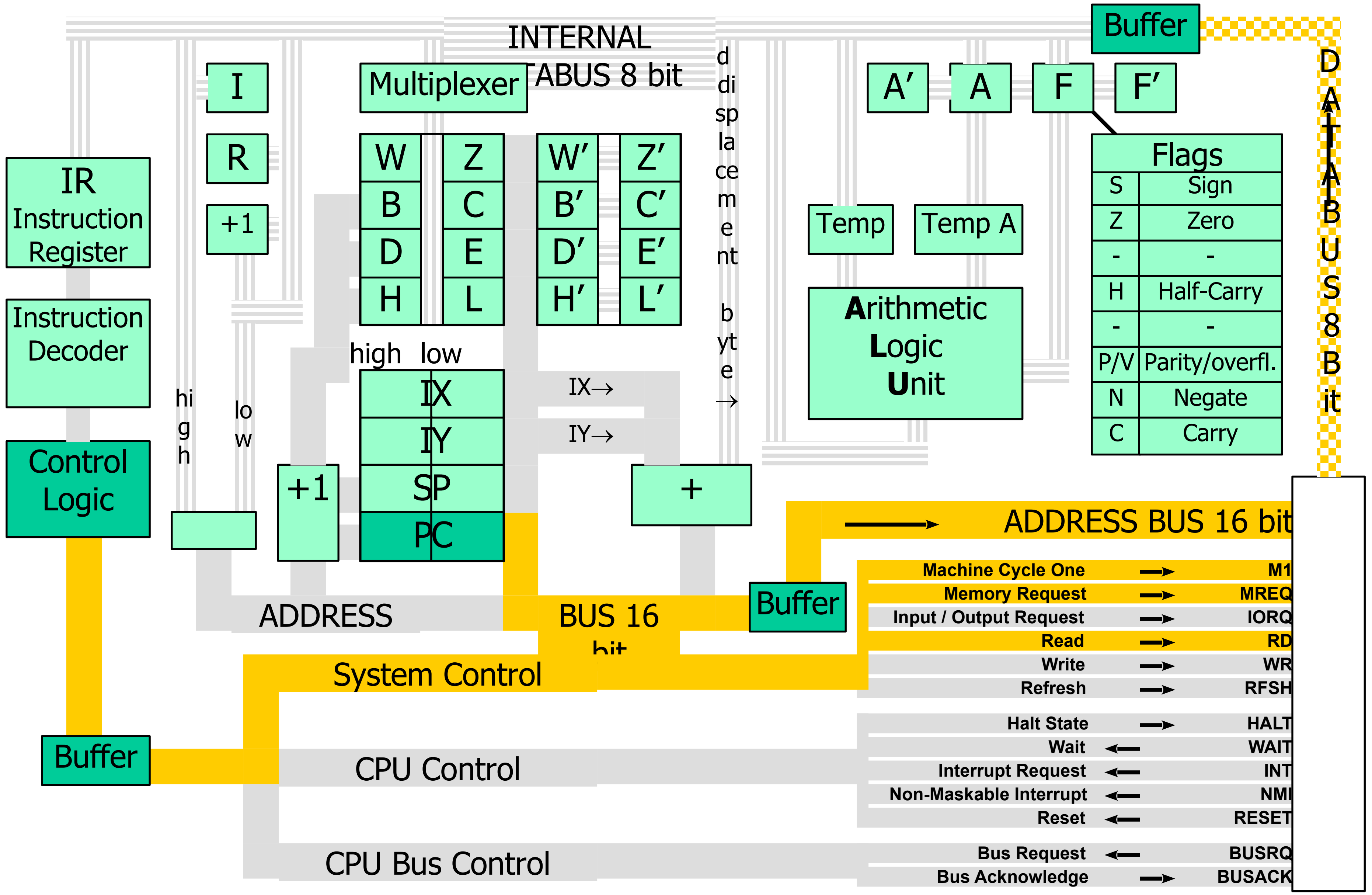



LD B,C
ADD A,(HL)
JP nn
PUSH HL
T1 T2 T3 T4 T5
Opcode Fetch
M1
M2
M3
Parte comune a tutte le istruzioni
overlap
overlap

LD B,C

T1	T2	T3	T4	T5	**M1**				
Opcode Fetch			**M1**		T1	T2	T3	T4	T5

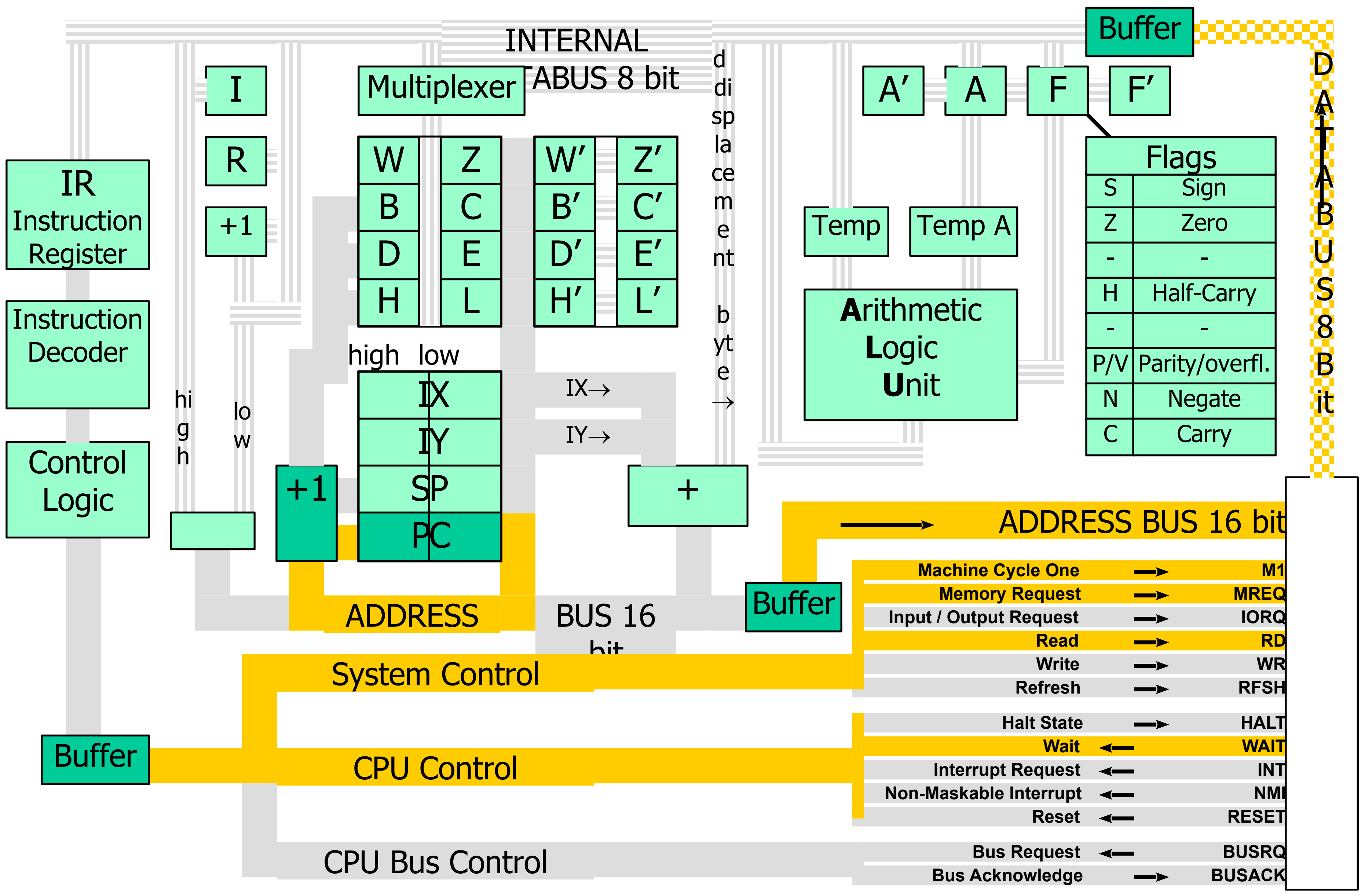
Mp attende byte su DATA BUS alzando impedenza



LD B,C

T1	T2	T3	T4	T5	M1			
Opcode Fetch			M1	T1	T2	T3	T4	T5

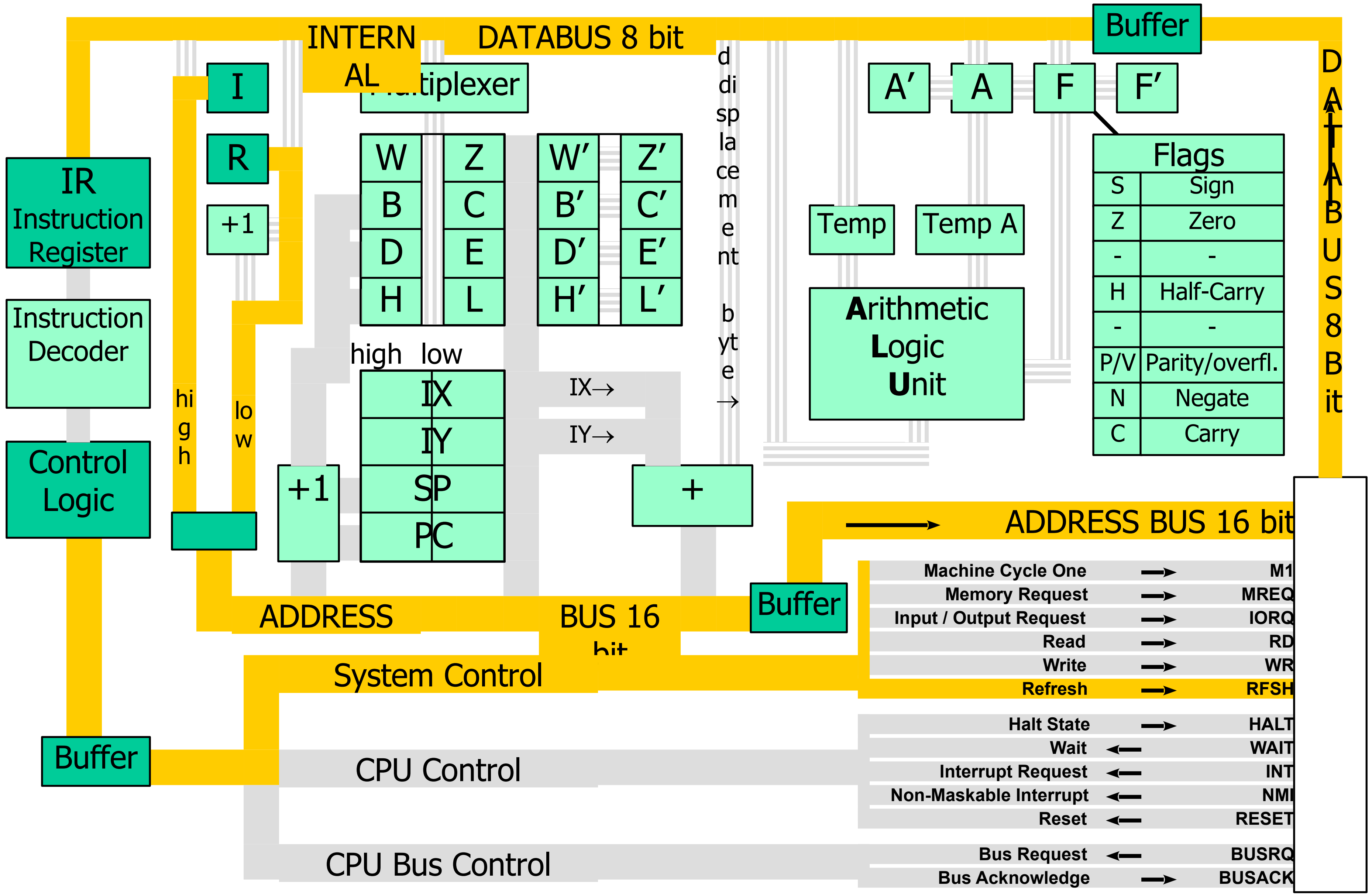
La memoria e' lenta!
...incremento PC...



LD B,C

T1	T2	T3	T4	T5	M1	
Opcode Fetch		M1	T1	T2	T3	T4	T5

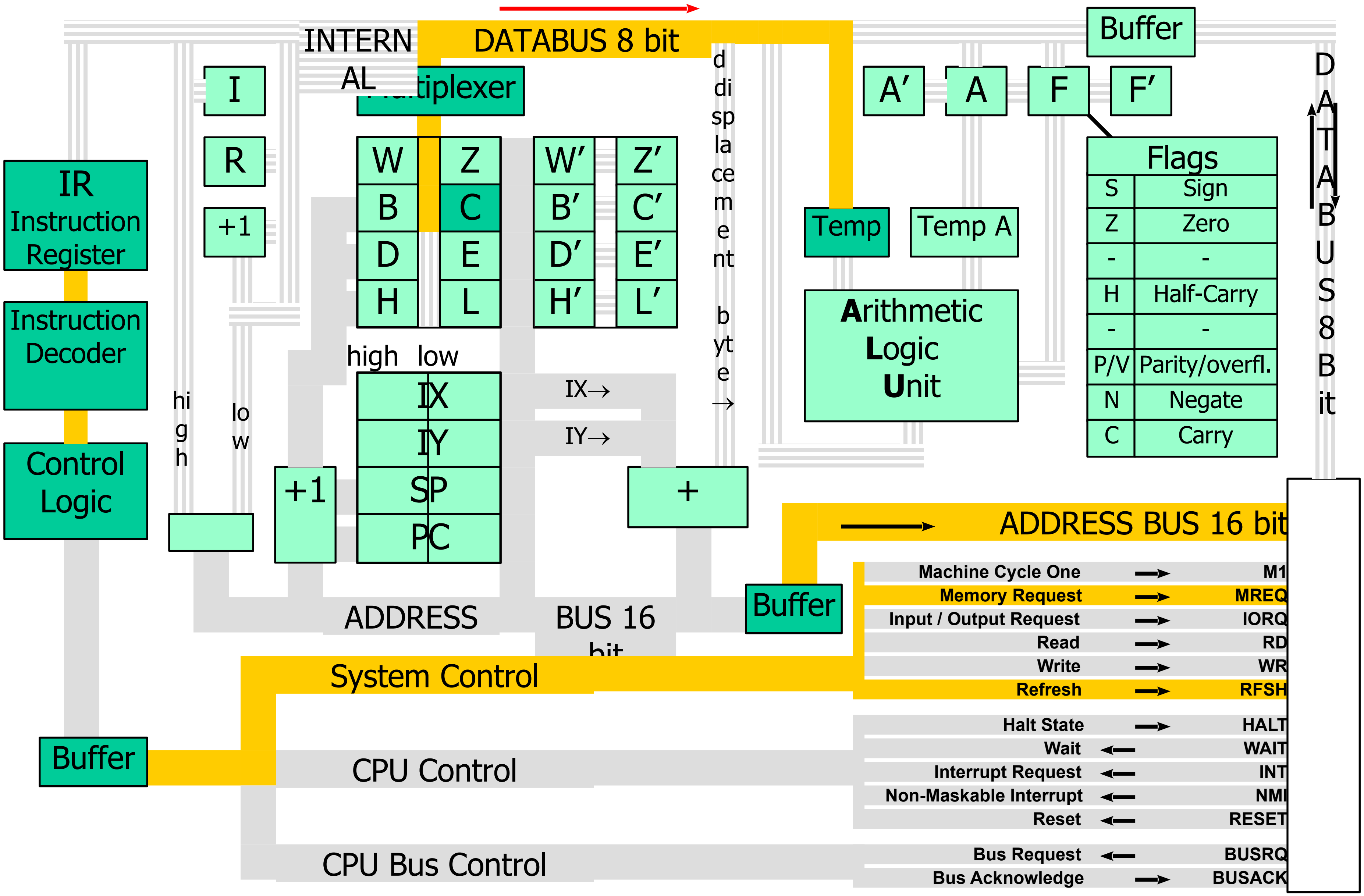
Istruzione da 1 byte in IR,
Refresh memorie dinamiche



LD B,C

T1	T2	T3	T4	T5	M1			
Opcode Fetch			M1	T1	T2	T3	T4	T5

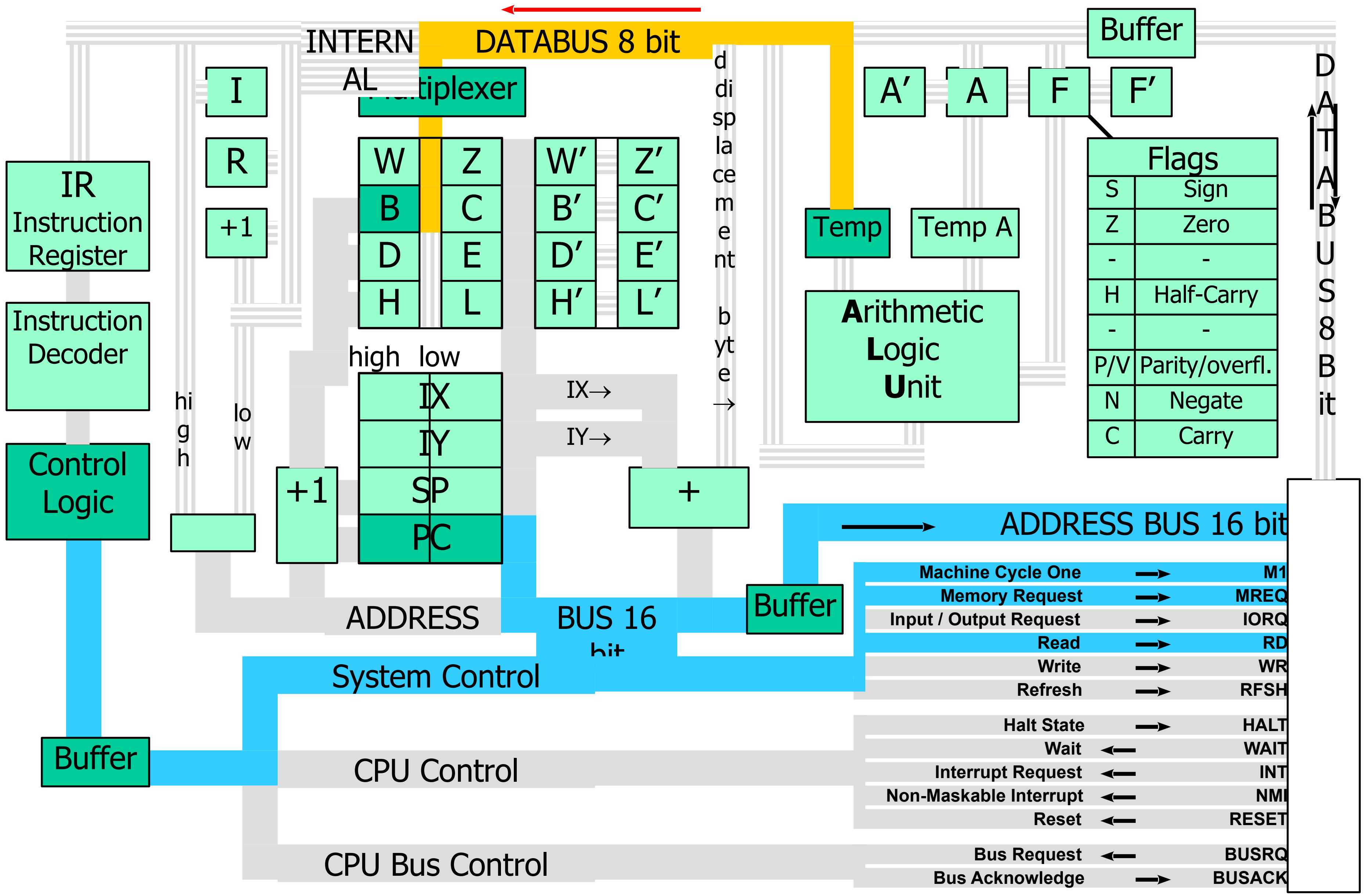
registri B e C non sono in comunicazione diretta



LD B,C

T1	T2	T3	T4	T5	M1				
Opcode Fetch			M1		T1	T2	T3	T4	T5

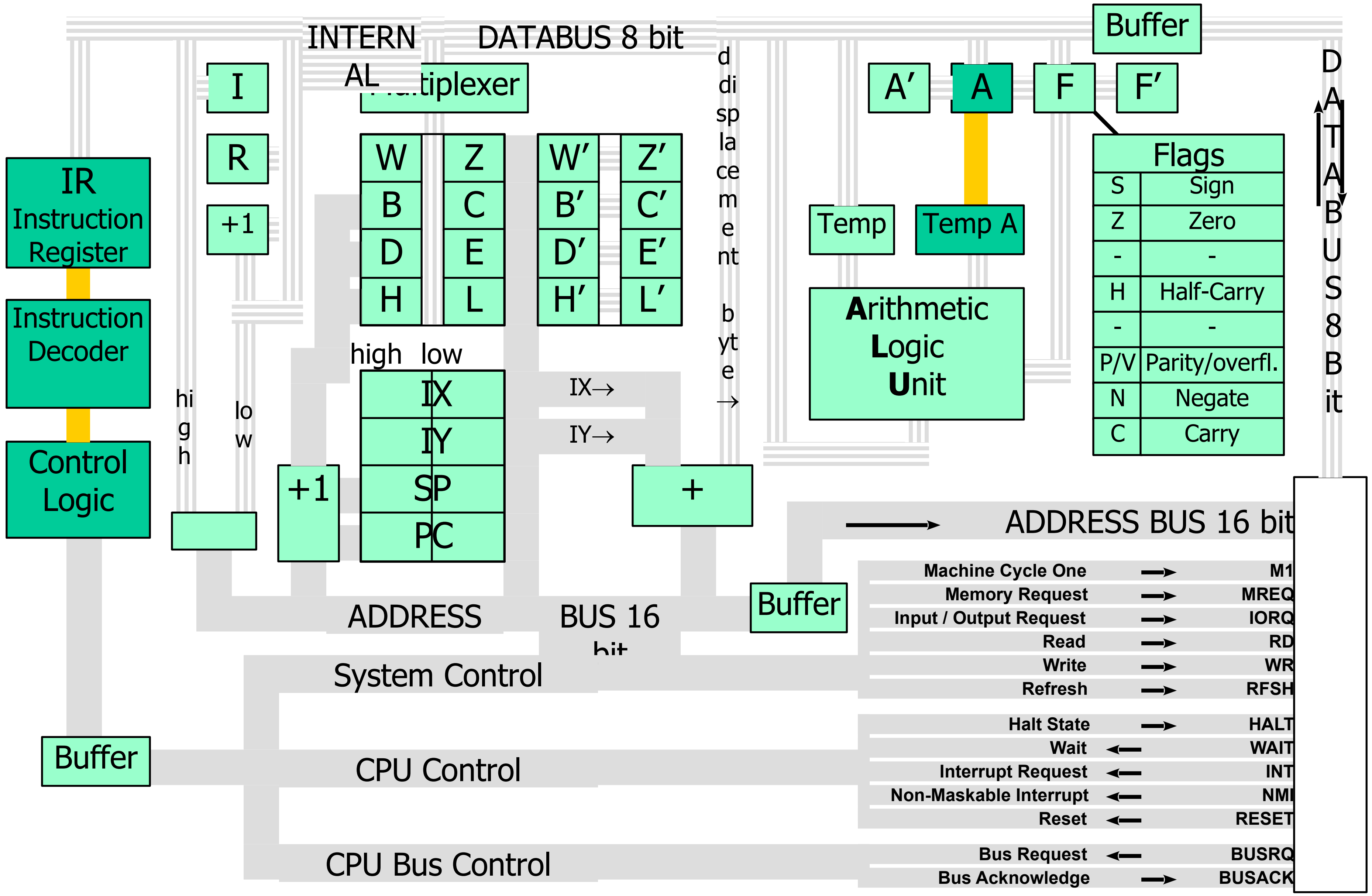
Pipelining! Comincia gia' lettura istruzione successiva



ADD A,(HL)

T1	T2	T3	T4	T5	M2		T1	T2	T3...
Opcode Fetch			M1	T1	T2	T3	T4	T5	M1

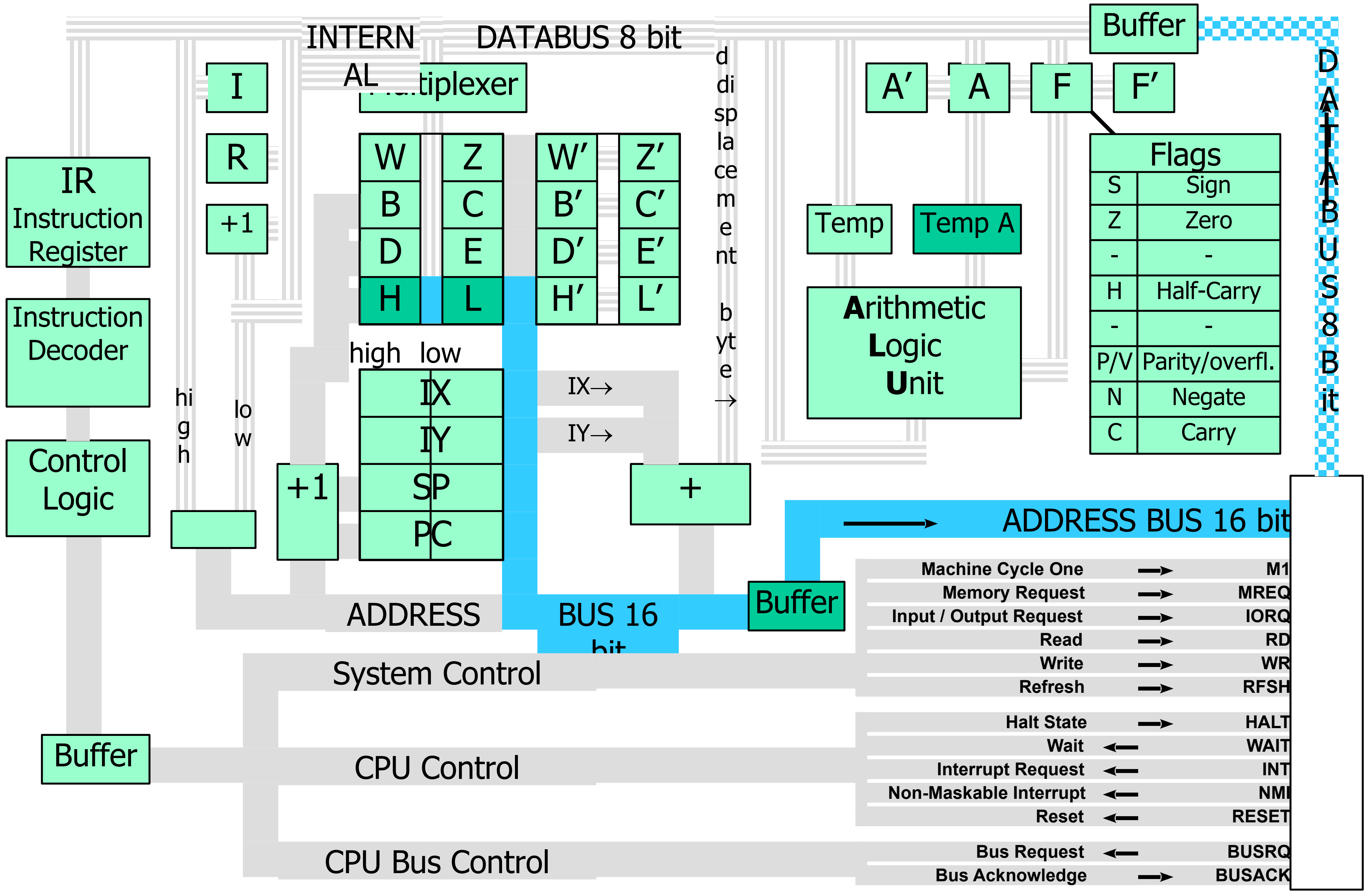
Opcode Fetch come per LD B,C



ADD A,(HL)

T1	T2	T3	T4	T5	M2	T1	T2	T3...
Opcode Fetch			M1	T1	T2	T3	T4	T5	M1

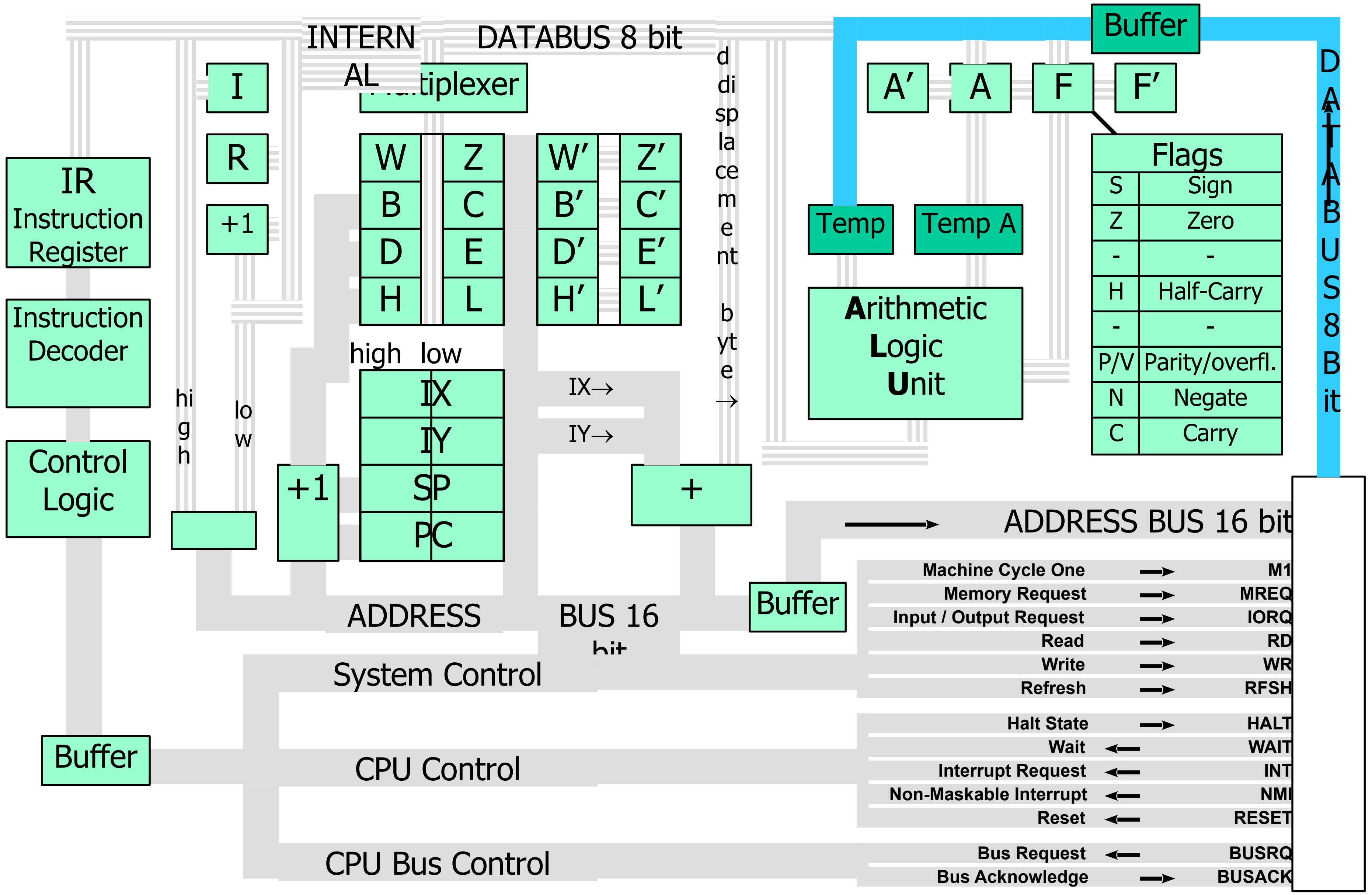
Scarico HL invece di PC sull'ADDRESS BUS



ADD A,(HL)

T1	T2	T3	T4	T5	M2		T1	T2	T3...
Opcode Fetch			M1	T1	T2	T3	T4	T5	M1

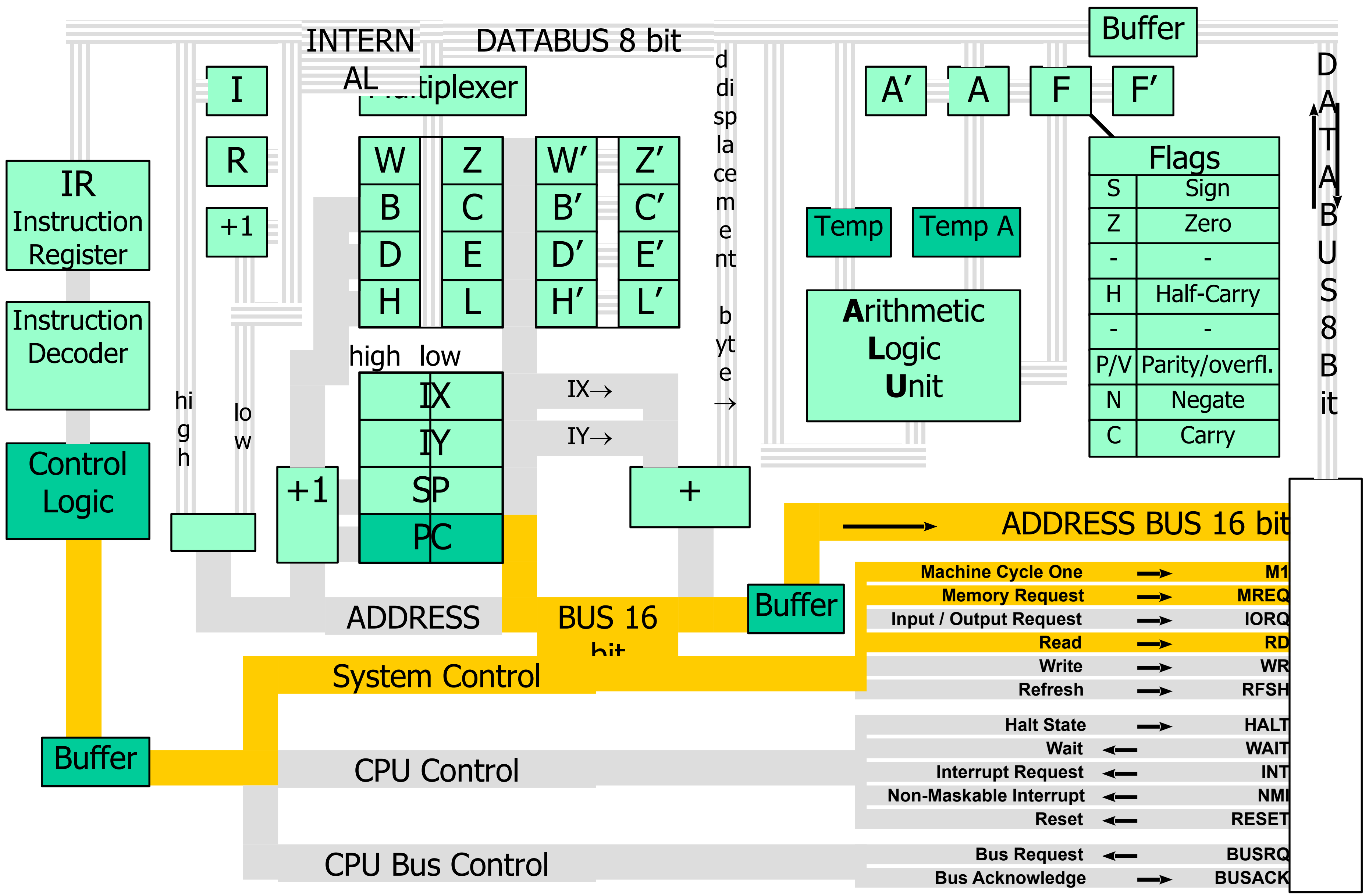
Carico contenuto di (HL) in Temp



ADD A,(HL)

T1	T2	T3	T4	T5	M2		T1	T2	T3...
Opcode Fetch			M1	T1	T2	T3	T4	T5	M1

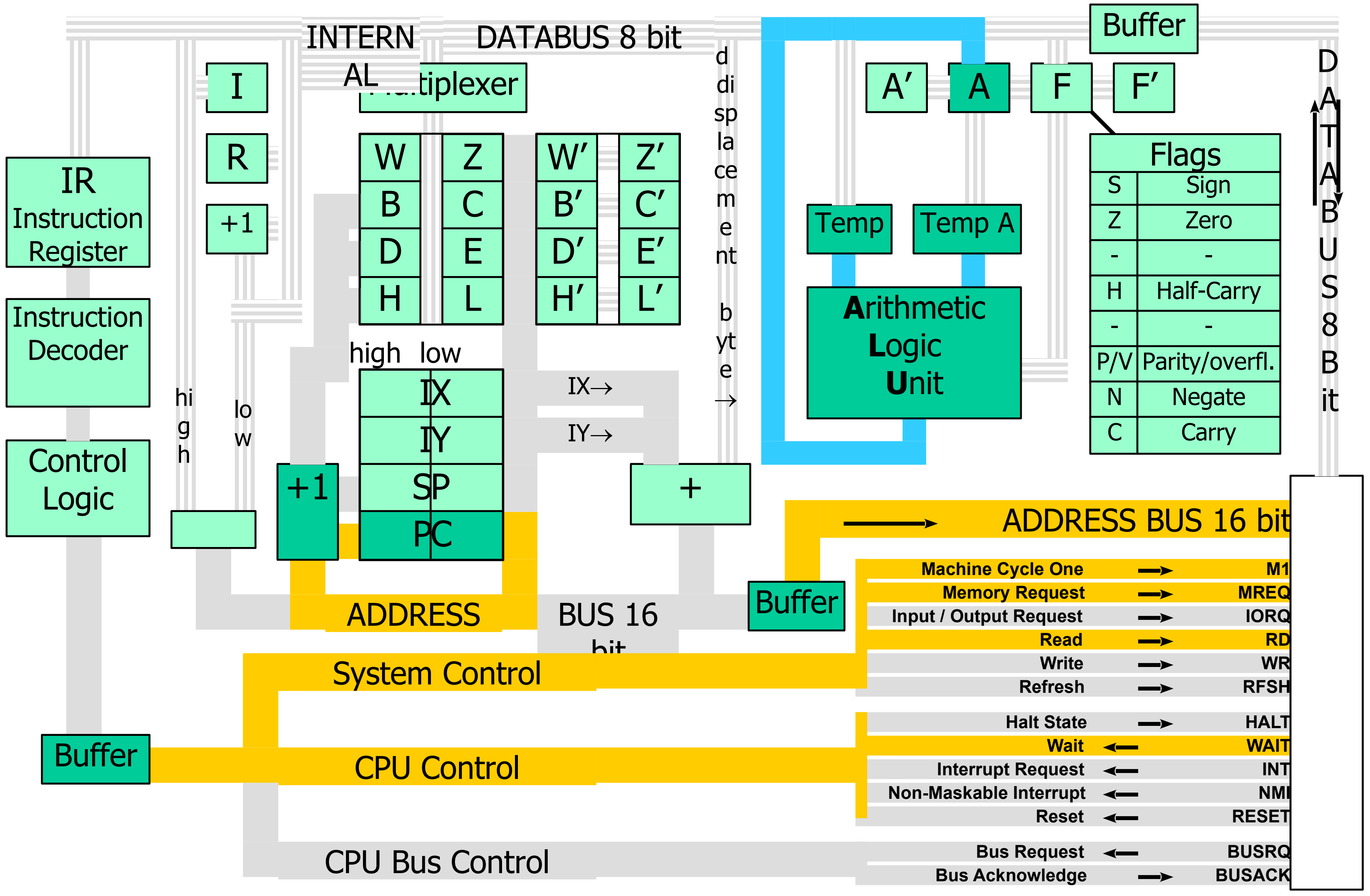
M2 attende, ma parte Opcode F. seguente



ADD A,(HL)

T1	T2	T3	T4	T5	M2		T1	T2	T3...
Opcode Fetch			M1	T1	T2	T3	T4	T5	M1

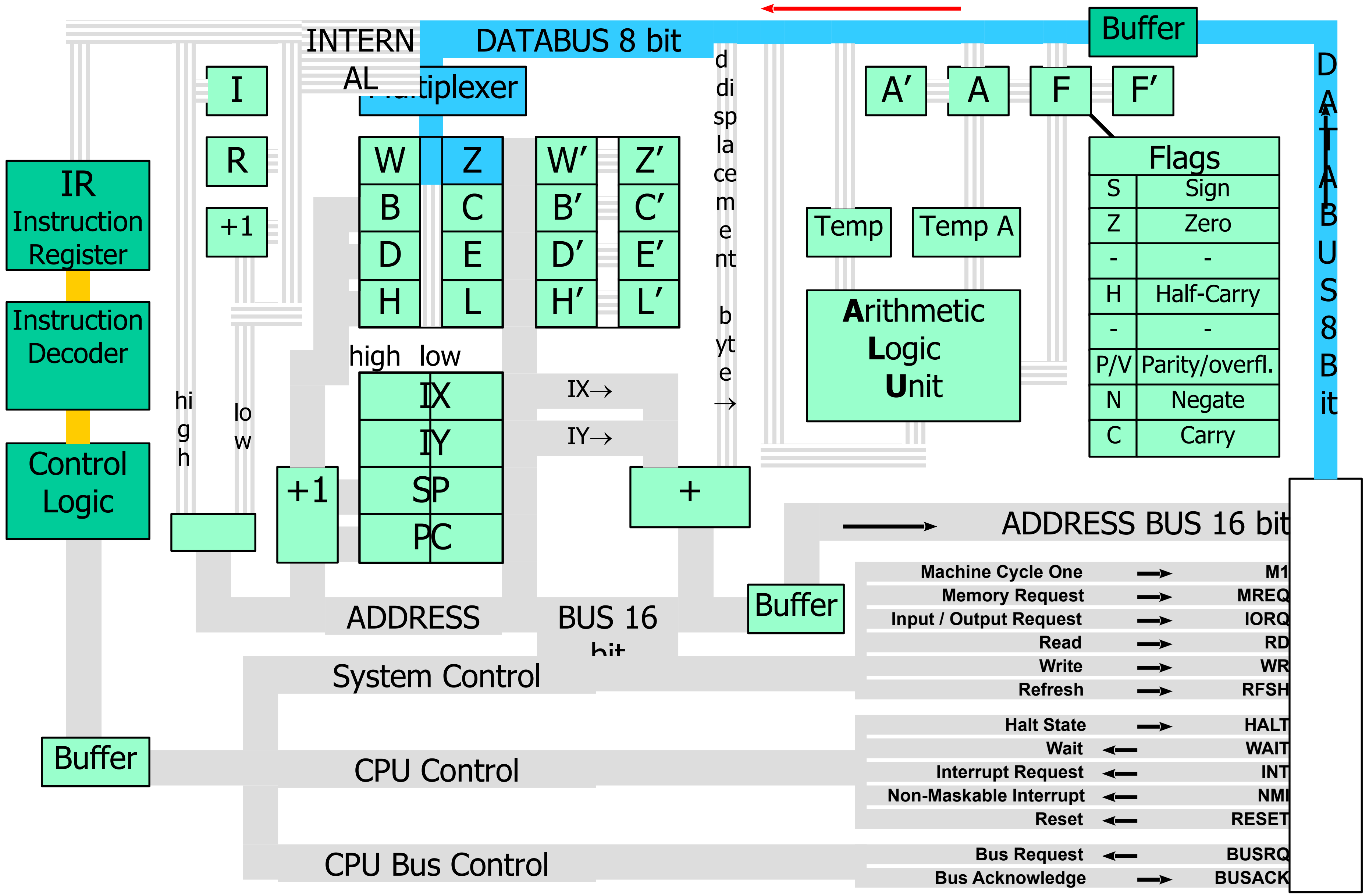
In T5 termina ADD, coincide con M1 T2



JP nn

T1	T2	T3	T4	T5	**M2**		T1	T2	T3	T4	T5	**M1**
Opcode Fetch			**M1**	T1	T2	T3	T4	T5	**M3**	T1	T2	T3...

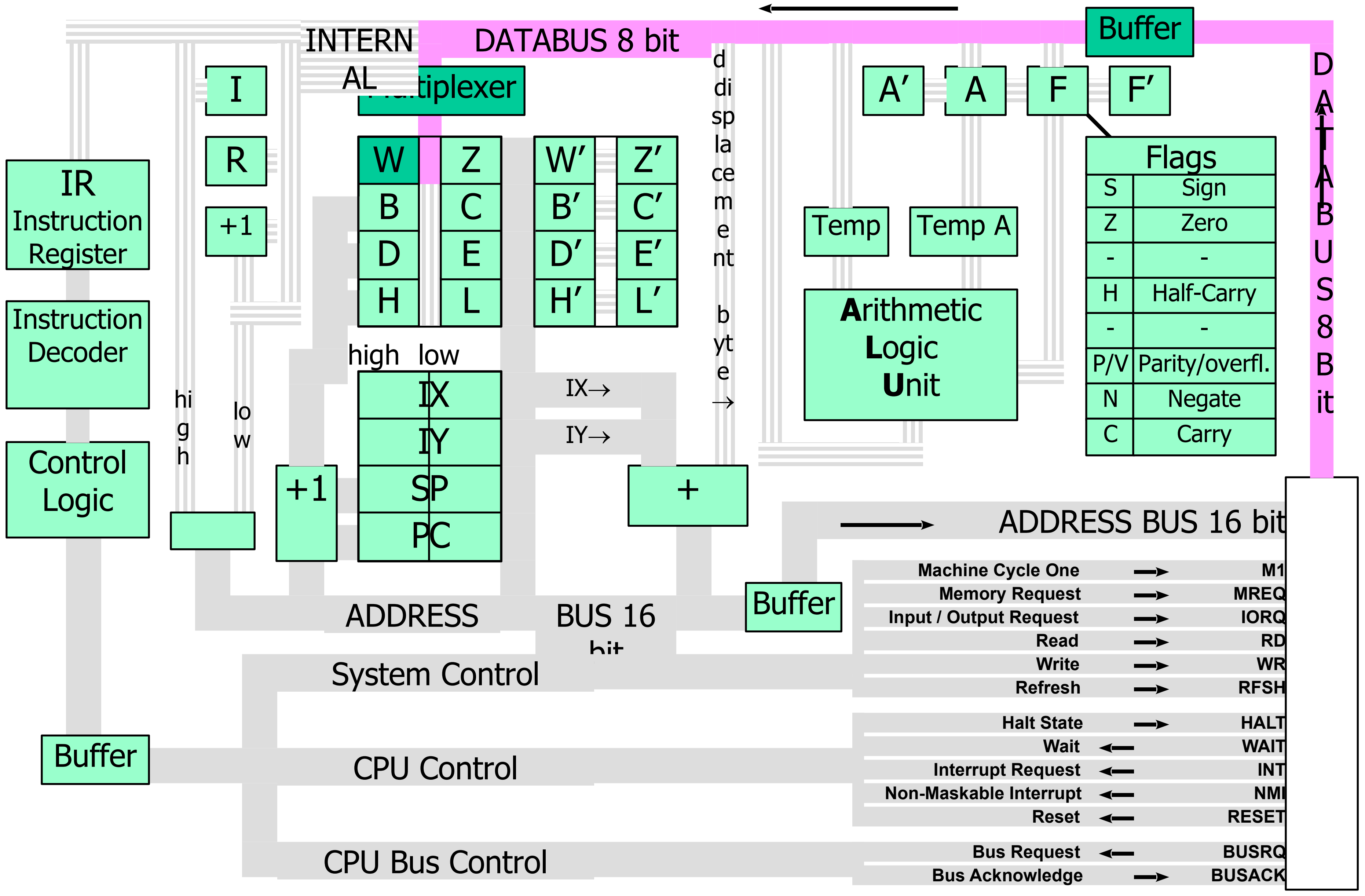
W e Z sono registri ombra



JP nn

T1	T2	T3	T4	T5	**M2**	T1	T2	T3	T4	T5	**M1**
Opcode Fetch			**M1**	T1	T2	T3	T4	T5	**M3**	T1	T2	T3...

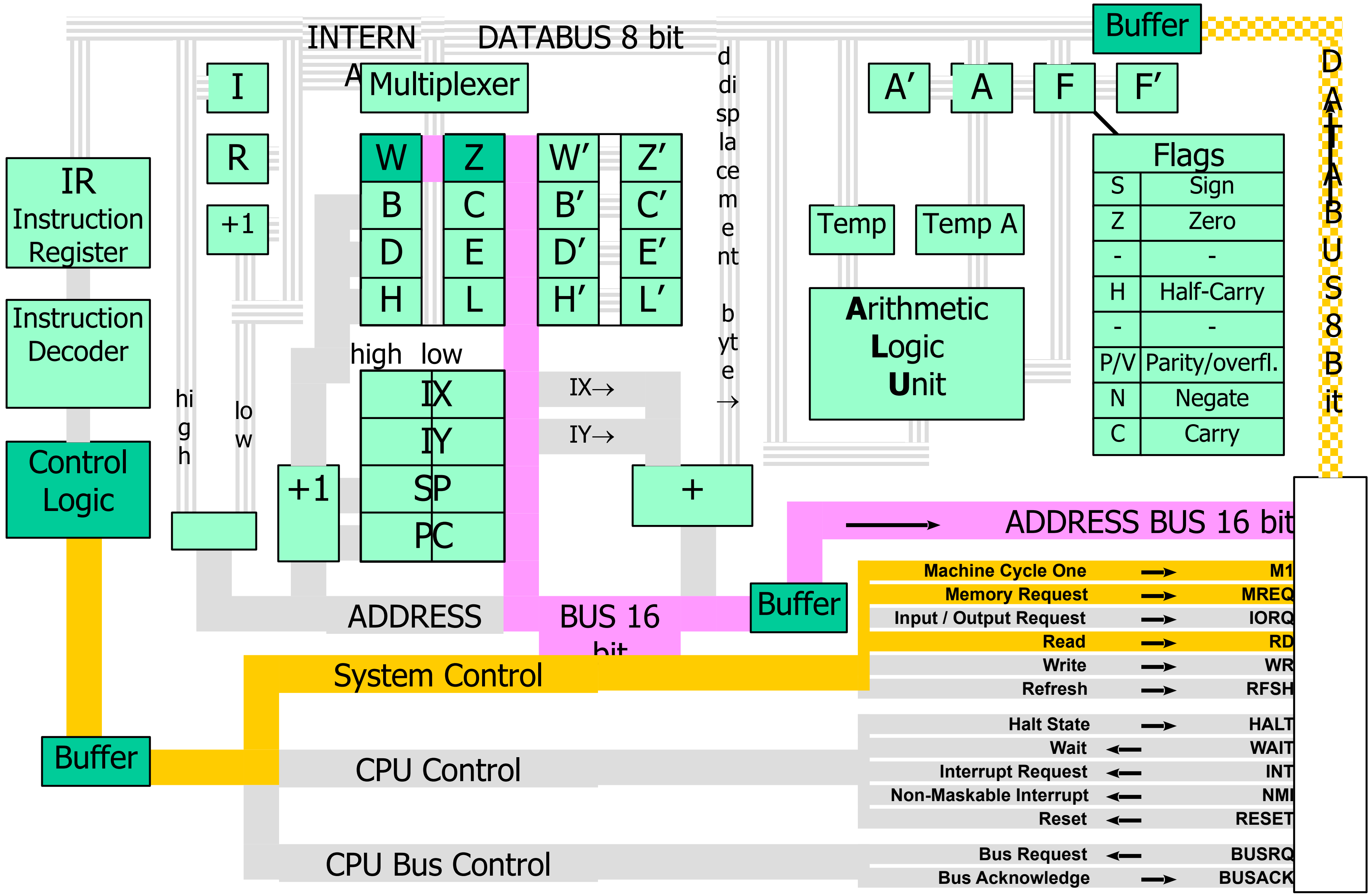
Secondo byte in W



JP nn

T1	T2	T3	T4	T5	**M2**	T1	T2	T3	T4	T5	**M1**
Opcode Fetch			**M1**	T1	T2	T3	T4	T5	**M3**	T1	T2 T3...

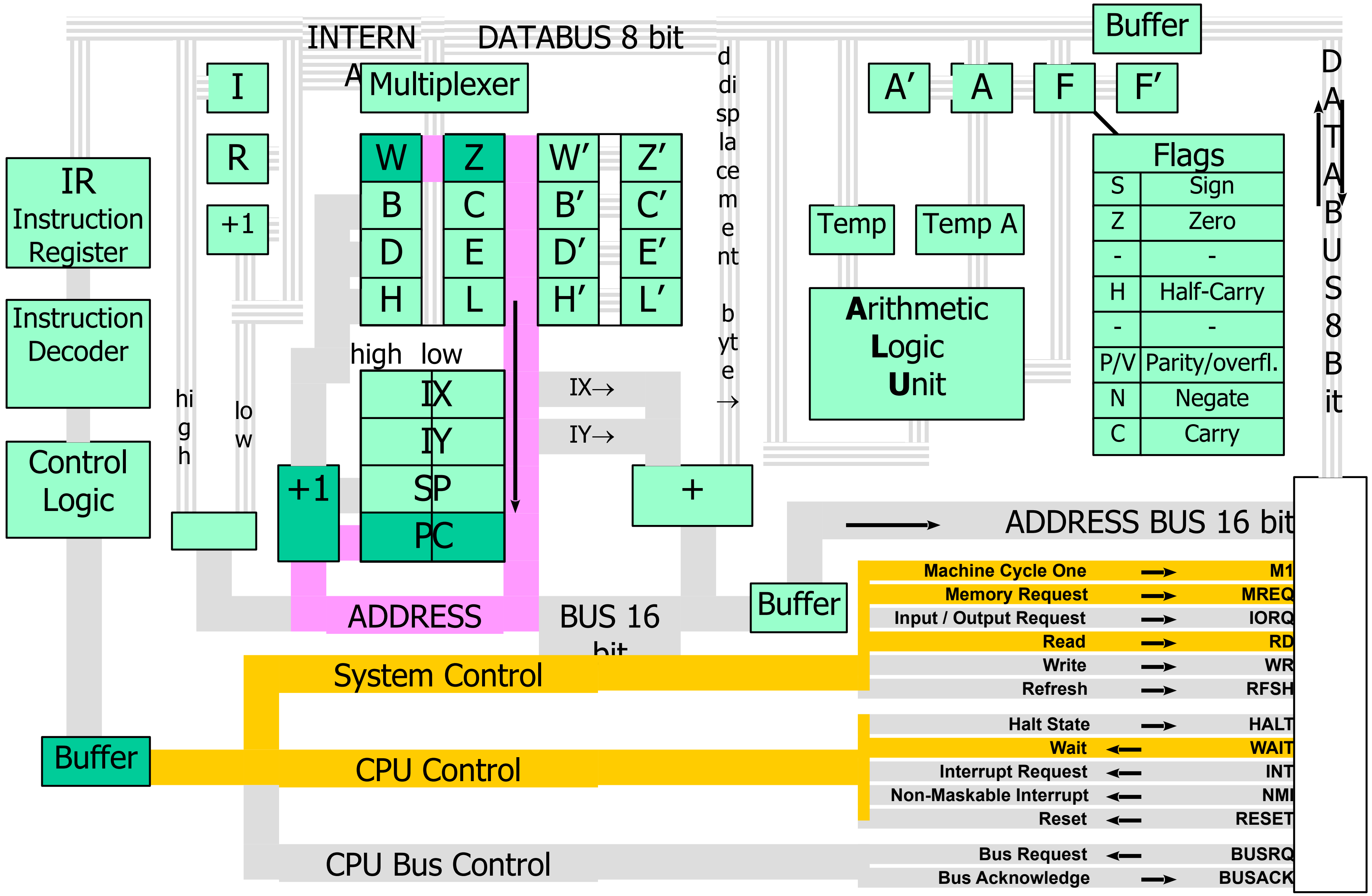
Scarico WZ sull' ADDRESS BUS



JP nn

T1	T2	T3	T4	T5	**M2**	T1	T2	T3	T4	T5	**M1**
Opcode Fetch			**M1**	T1	T2	T3	T4	T5	**M3**	T1	T2	T3...

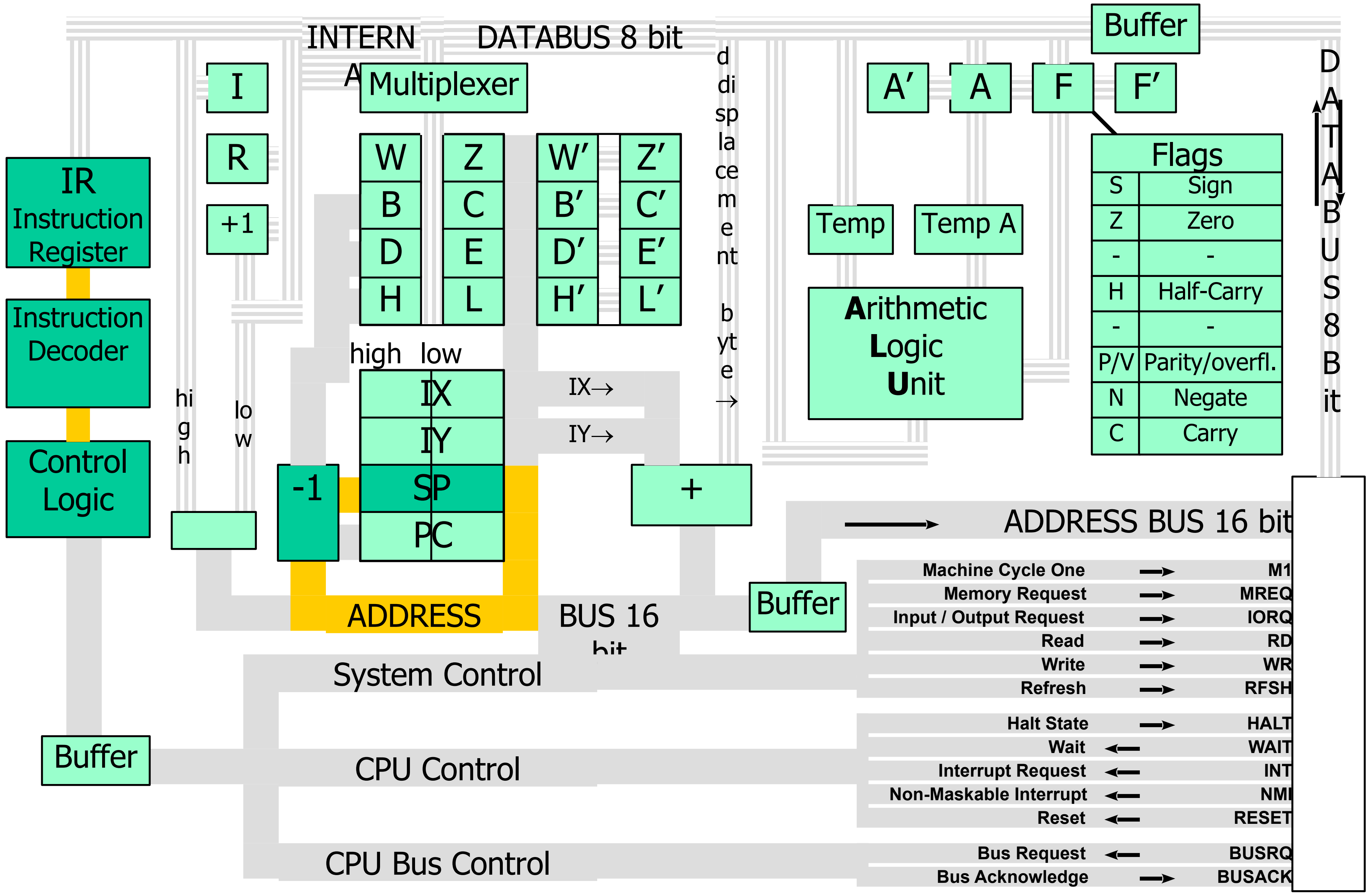
Incremento WZ e carico in PC



PUSH HL

T1	T2	T3	T4	T5	**M2**	T1	T2	T3	T4	T5
Opcode Fetch			**M1**	T1	T2	T3	T4	T5	**M3**	T1	T2...

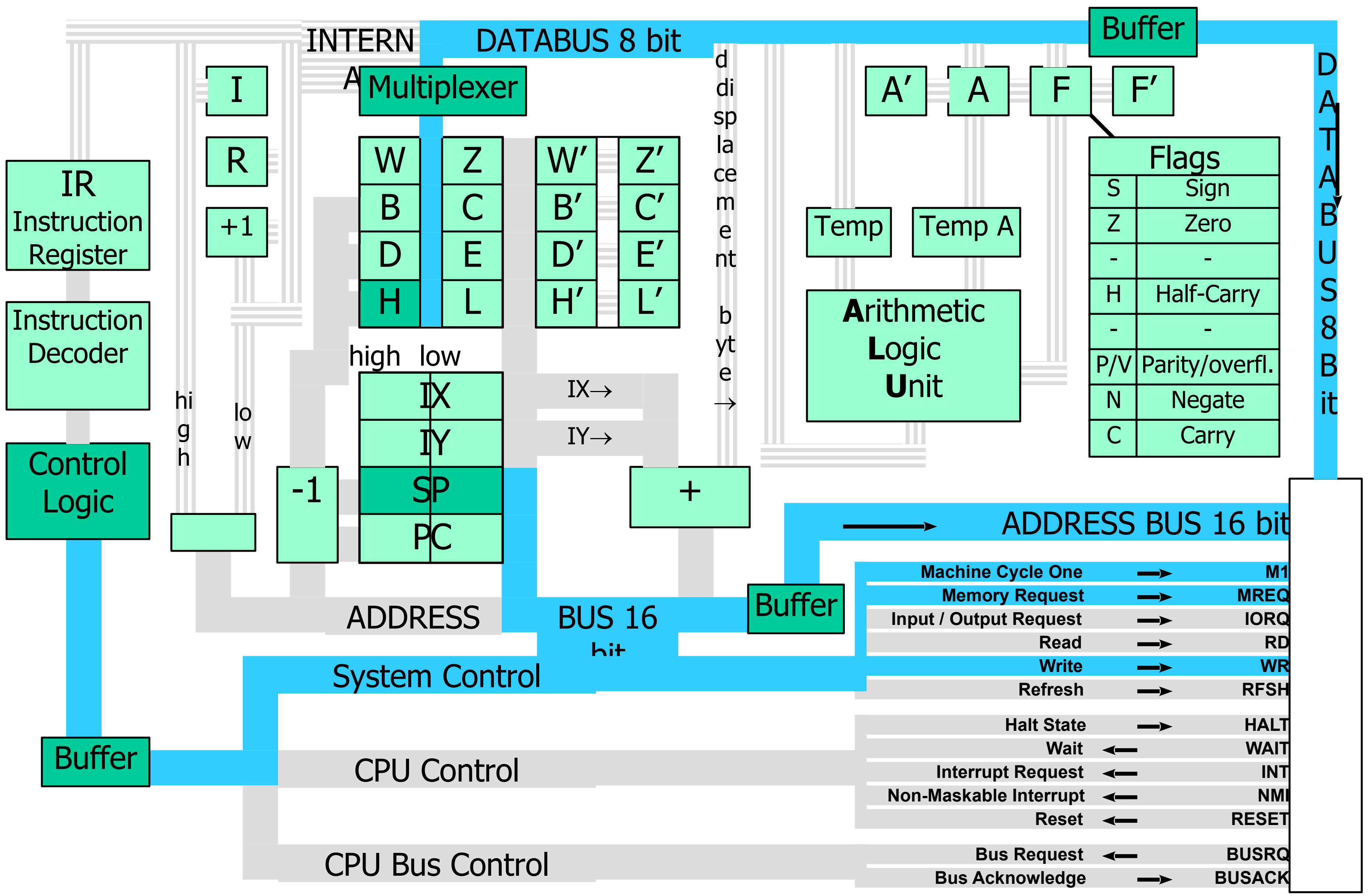
Stack Pointer tipo FIFO



PUSH HL

T1	T2	T3	T4	T5	M2		T1	T2	T3	T4	T5
Opcode Fetch			M1	T1	T2	T3	T4	T5	M3	T1	T2...

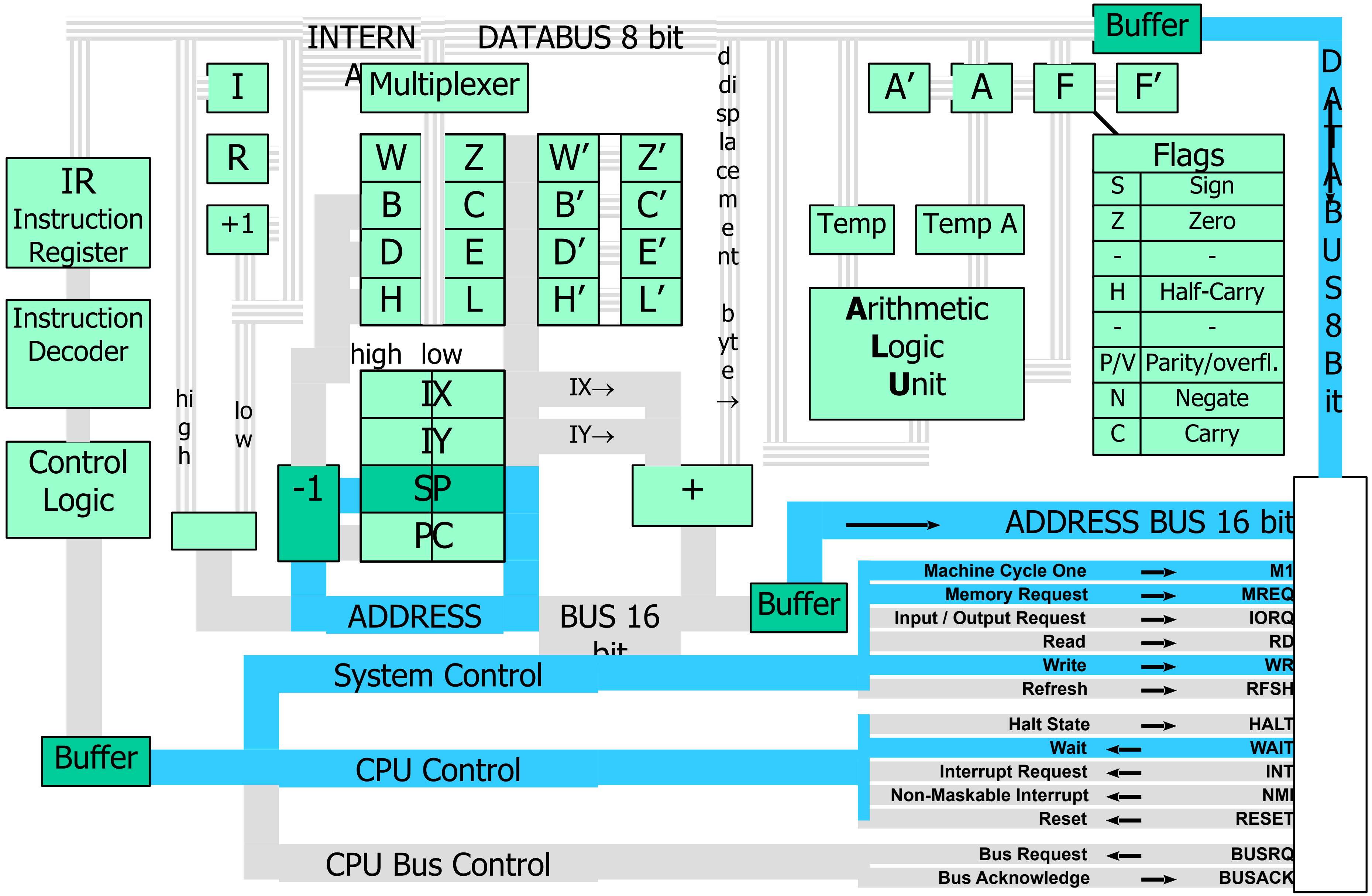
Scrivo High byte in (SP)



PUSH HL

T1	T2	T3	T4	T5	**M2**		T1	T2	T3	T4	T5
Opcode Fetch			**M1**	T1	T2	T3	T4	T5	**M3**	T1	T2...

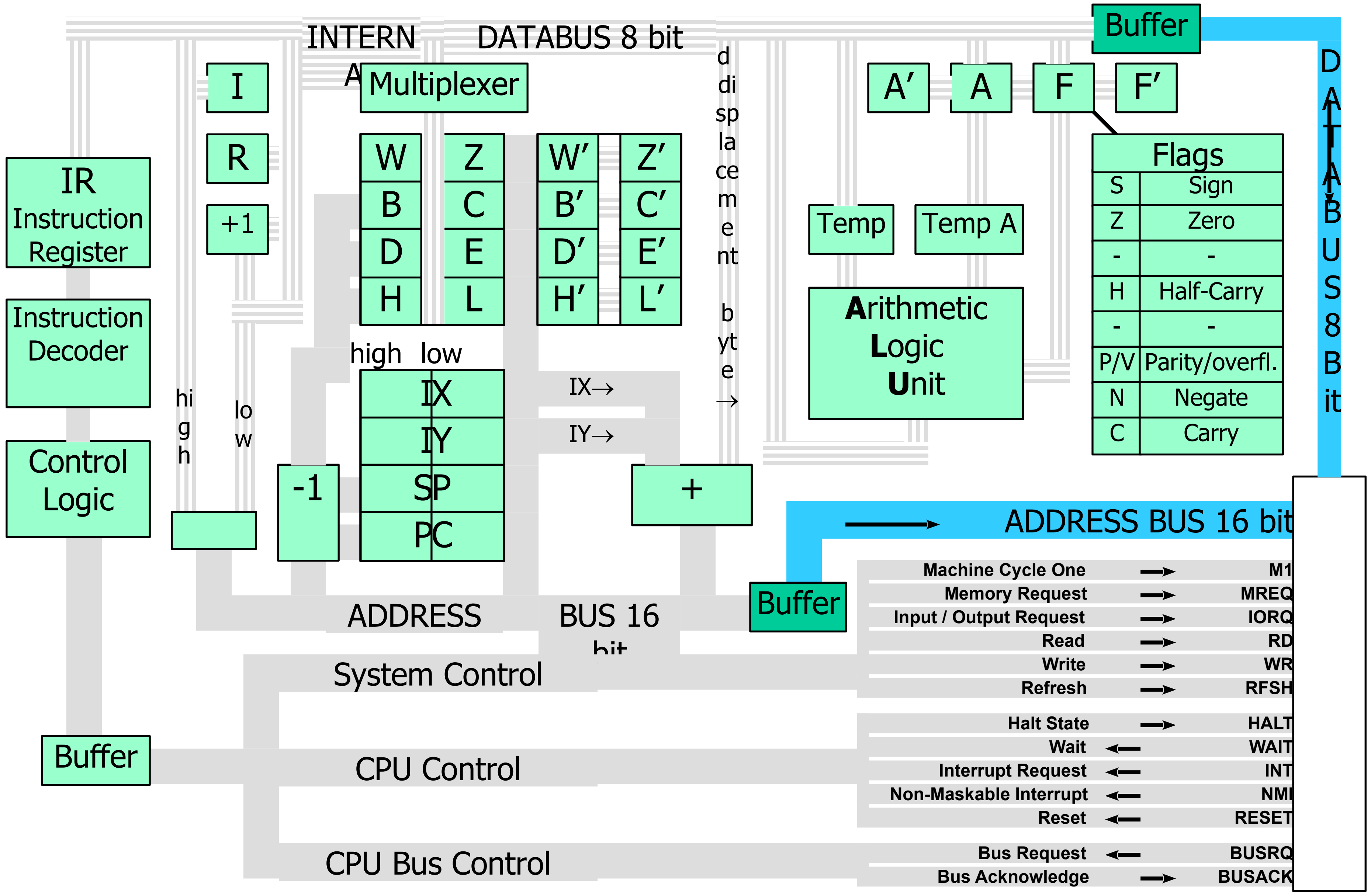
Decremento ancora SP



PUSH HL

T1	T2	T3	T4	T5	**M2**		T1	T2	T3	T4	T5
Opcode Fetch			**M1**	T1	T2	T3	T4	T5	**M3**	T1	T2...

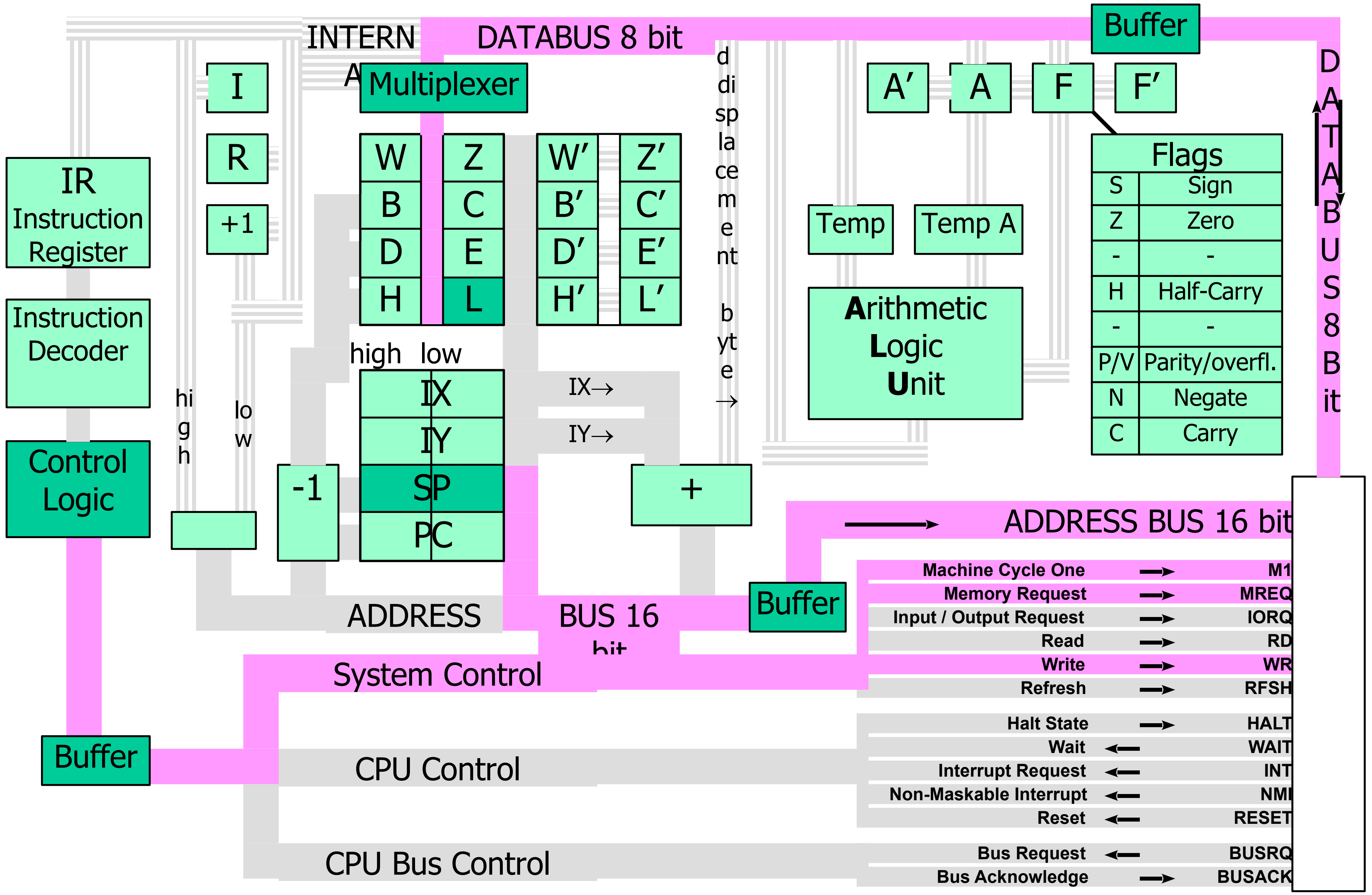
Tengo tutto sui Buffer



PUSH HL

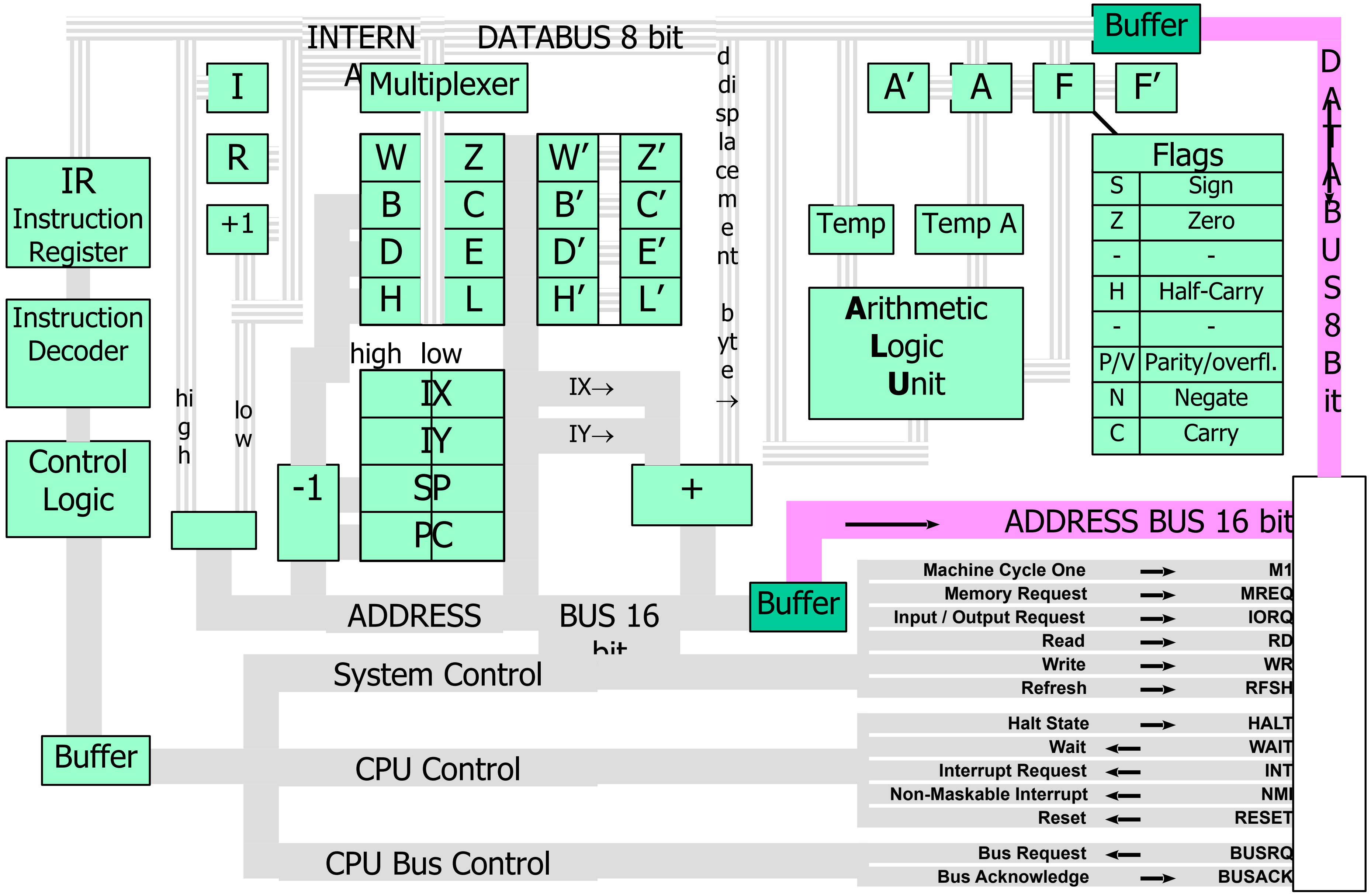
T1	T2	T3	T4	T5	M2		T1	T2	T3	T4	T5
Opcode Fetch			**M1**	T1	T2	T3	T4	T5	**M3**	T1	T2...

Scarico Low byte in (SP)

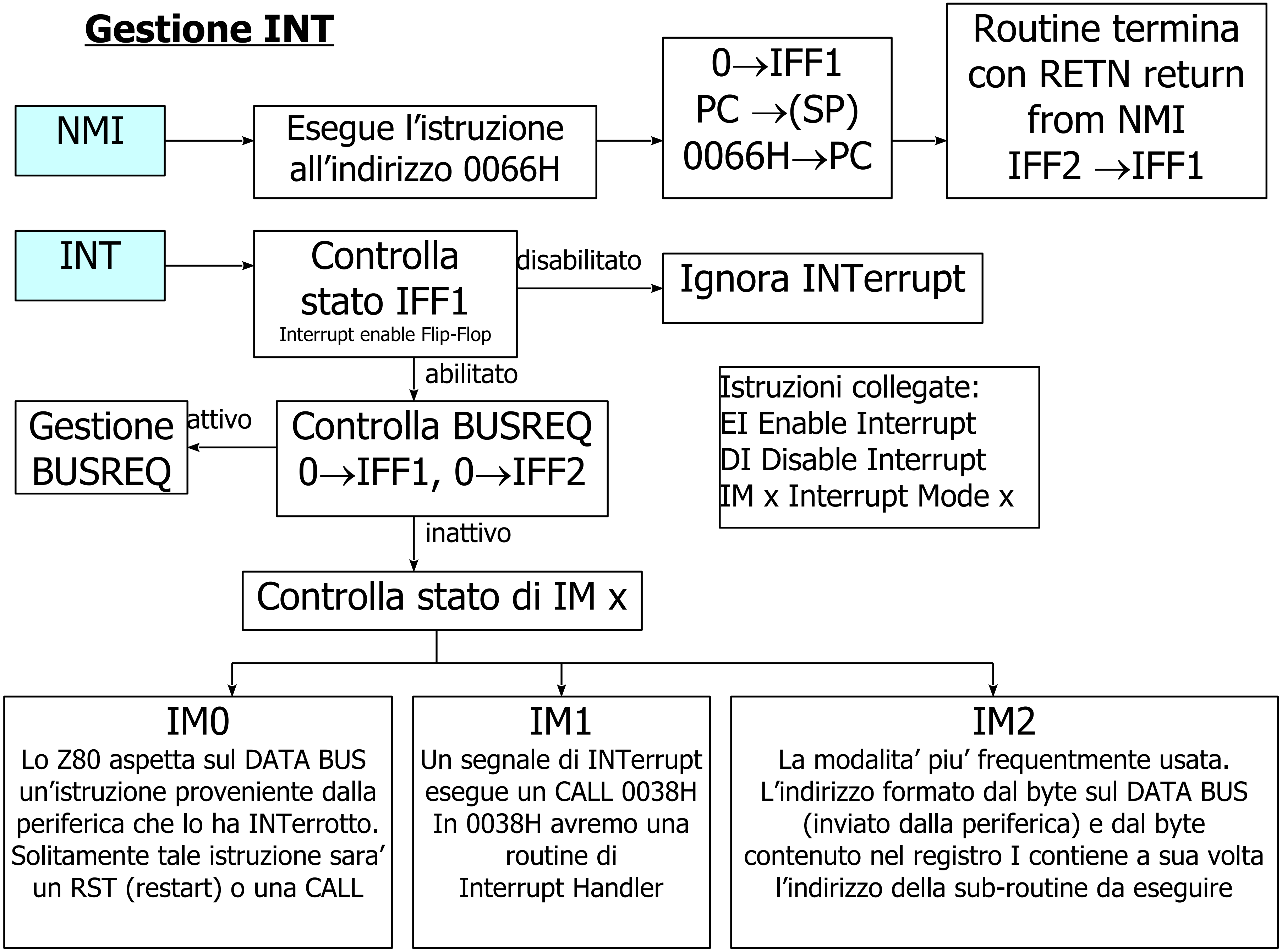


PUSH HL

T1	T2	T3	T4	T5	**M2**		T1	T2	T3	T4	T5
Opcode Fetch			**M1**	T1	T2	T3	T4	T5	**M3**		



Gestione INT



Istruzioni collegate:
EI Enable Interrupt
DI Disable Interrupt
IM x Interrupt Mode x

IM0
Lo Z80 aspetta sul DATA BUS un'istruzione proveniente dalla periferica che lo ha INTerrotto. Solitamente tale istruzione sara' un RST (restart) o una CALL

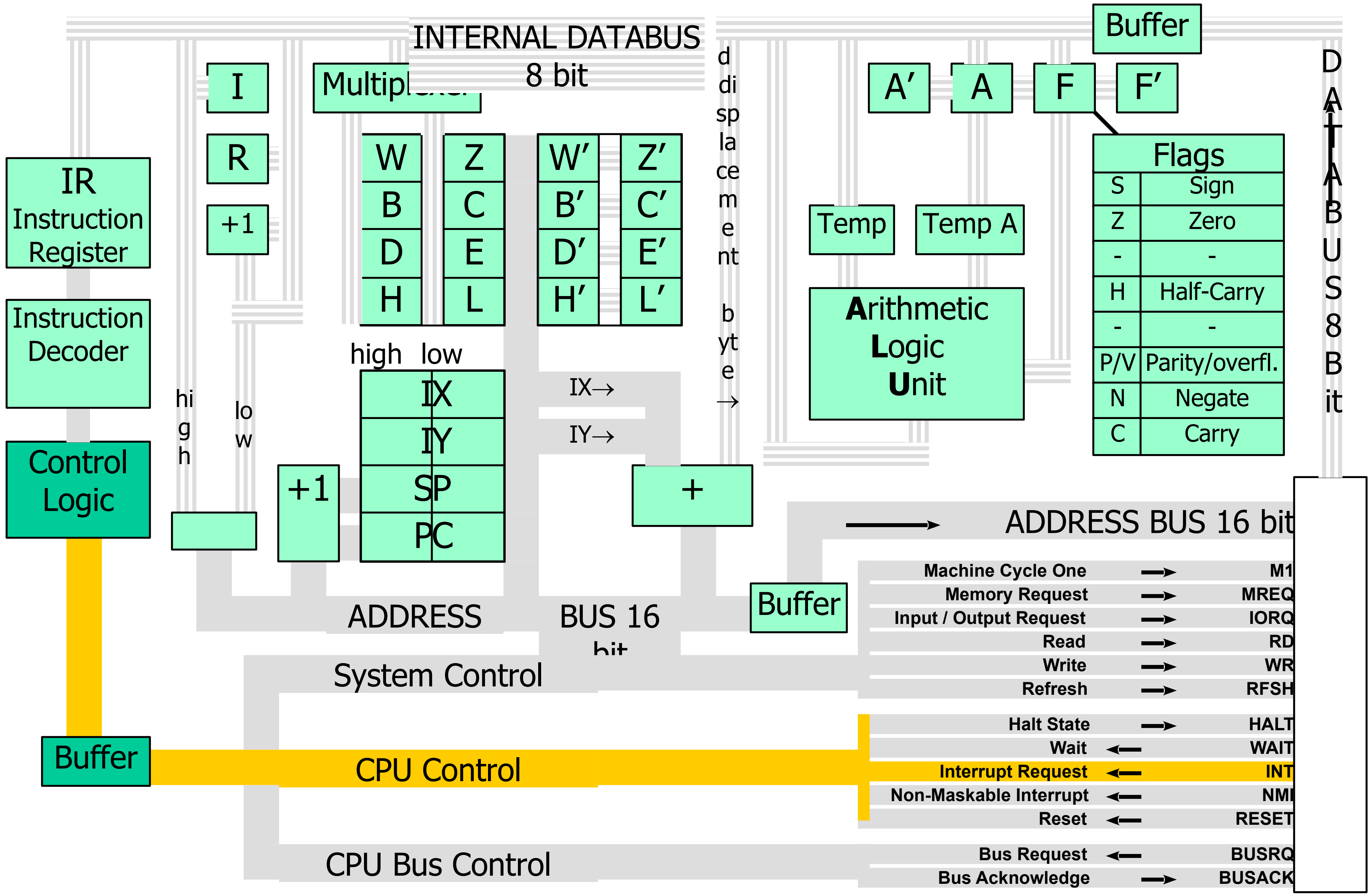
IM1
Un segnale di INTerrupt esegue un CALL 0038H
In 0038H avremo una routine di Interrupt Handler

IM2
La modalita' piu' frequentmente usata.
L'indirizzo formato dal byte sul DATA BUS (inviato dalla periferica) e dal byte contenuto nel registro I contiene a sua volta l'indirizzo della sub-routine da eseguire

INT in IM2

T	T	T1	T2	TW	TW	T3	T4	T1	T2
M		M						M	

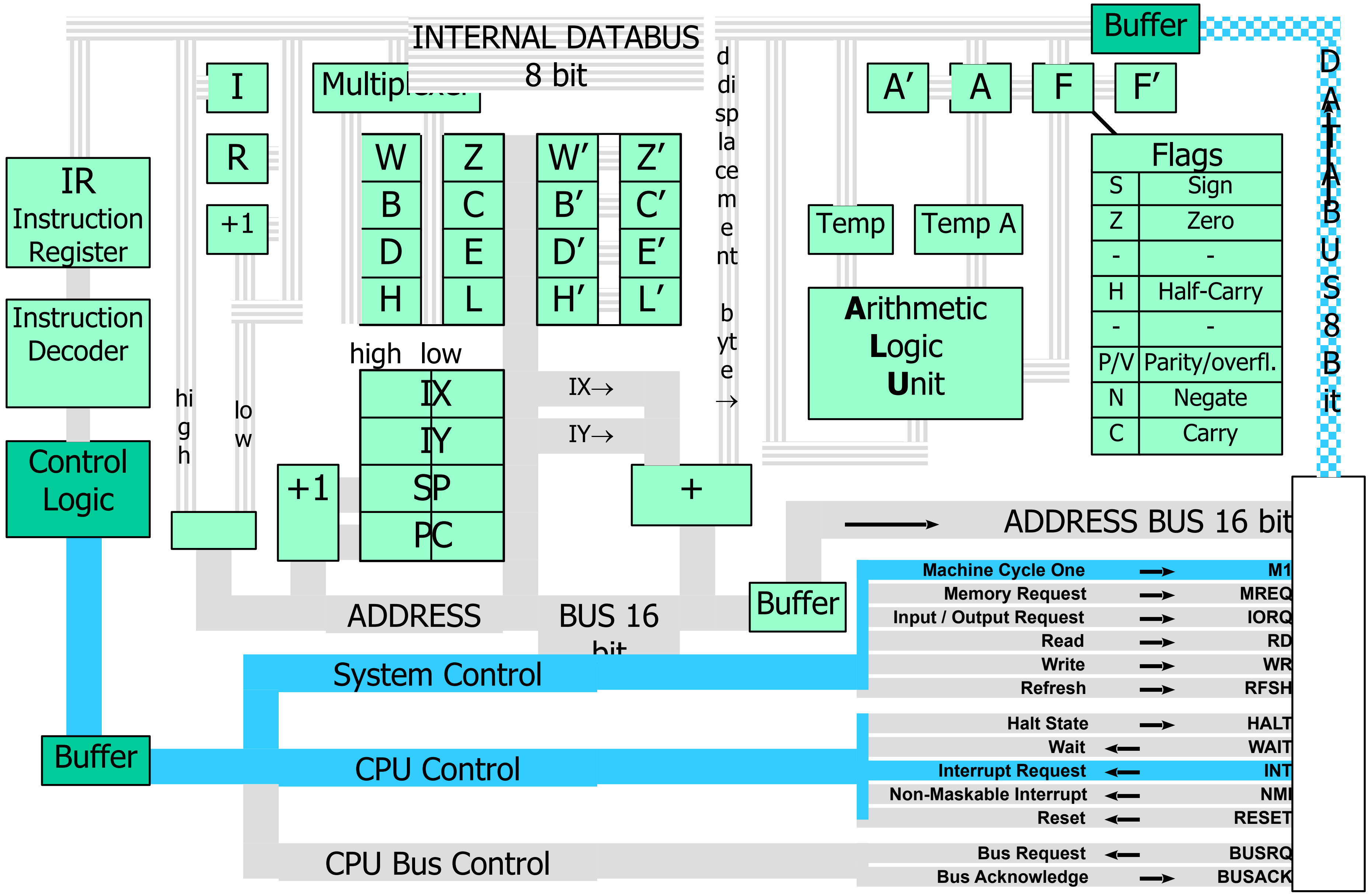
Perriferica invia INTerrupt



INT in IM2

T	T	T1	T2	TW	TW	T3	T4	T1	T2
M		**M**						**M**	

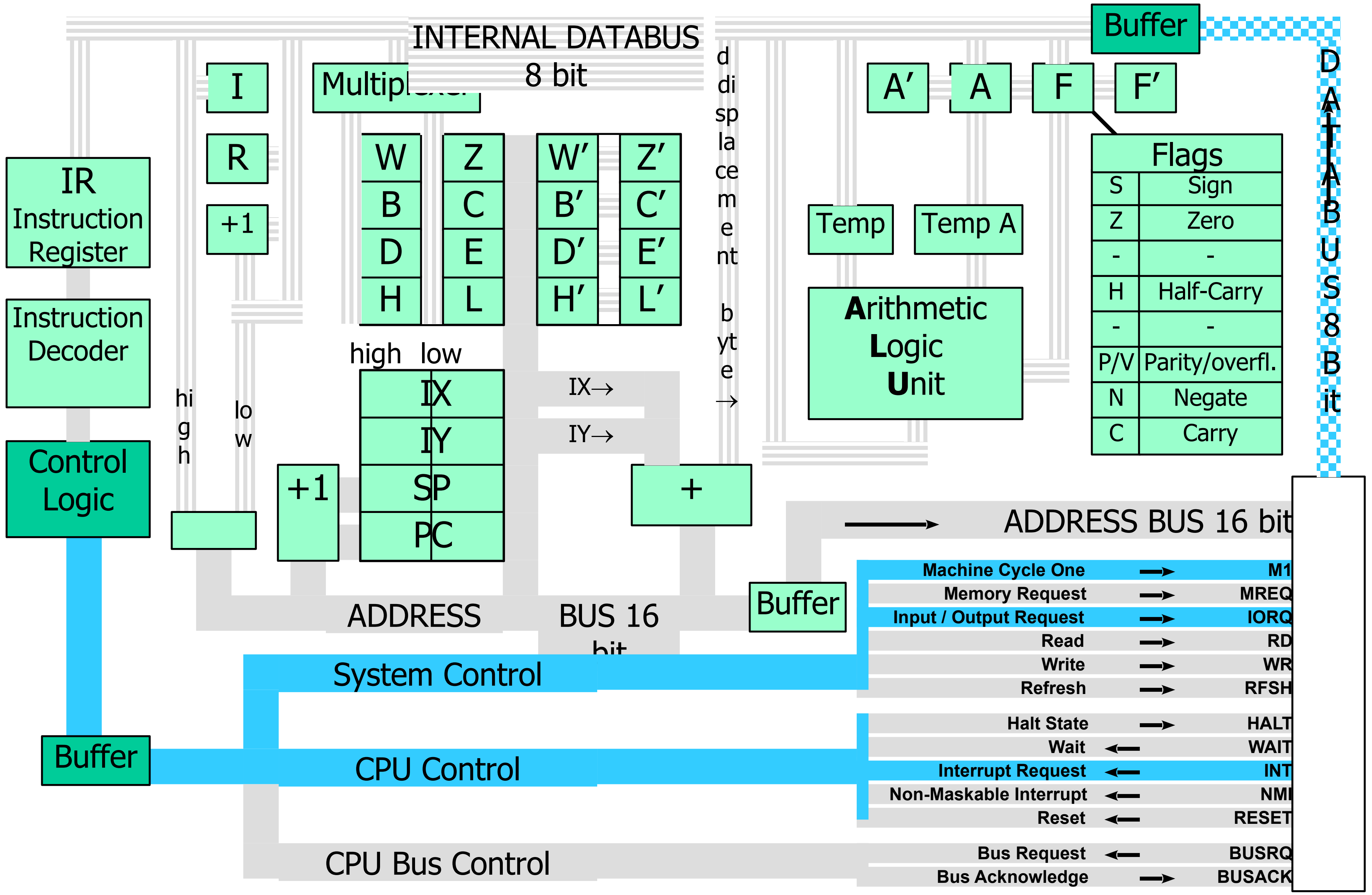
Mp attiva M1 e alza impedenza DATA BUS



INT in IM2

T	T	T1	T2	TW	TW	T3	T4	T1	T2
M		M						M	

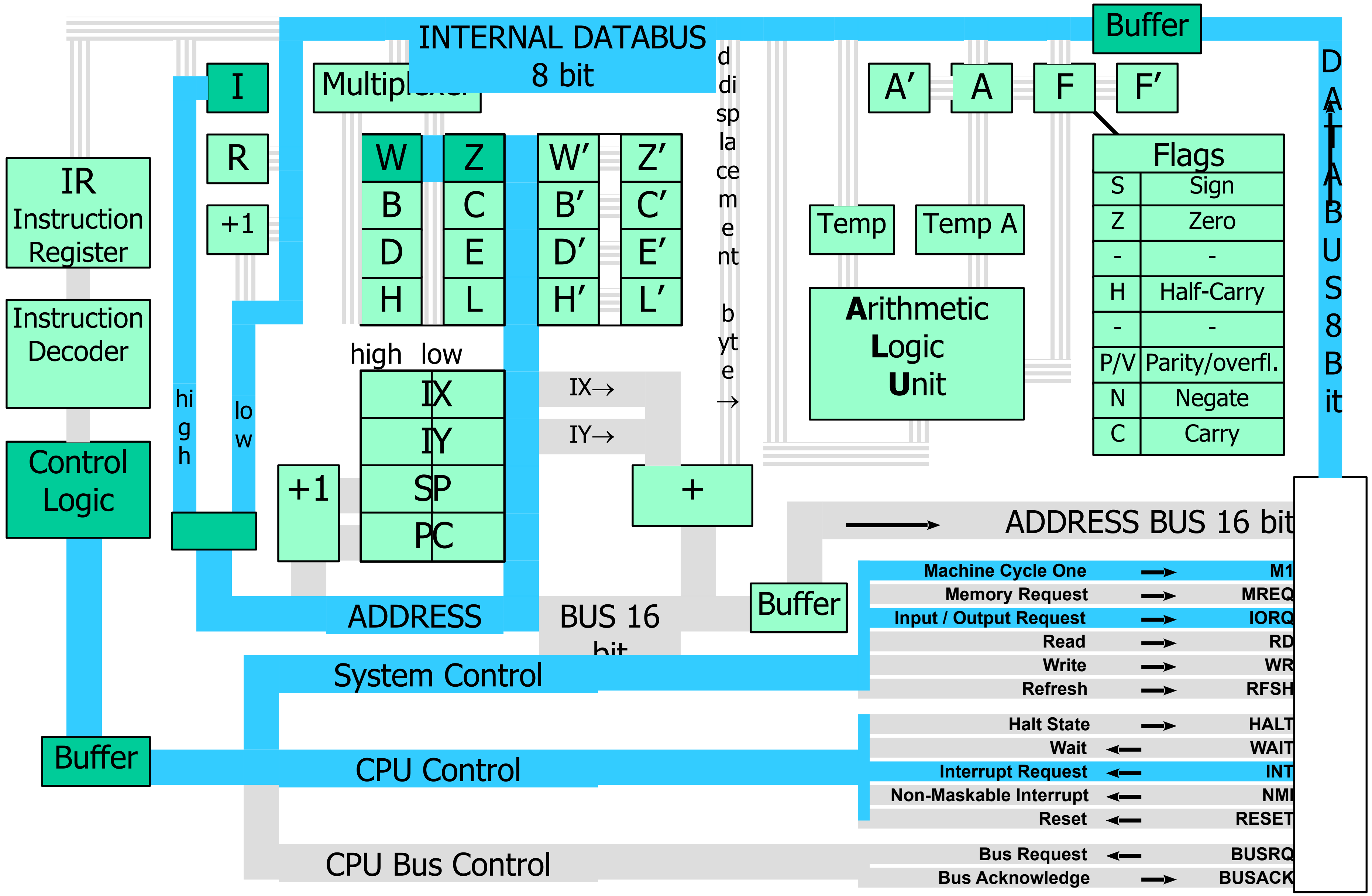
Mp attiva IORQ



INT in IM2

T	T	T1	T2	TW	TW	T3	T4	T1	T2
M		M						M	

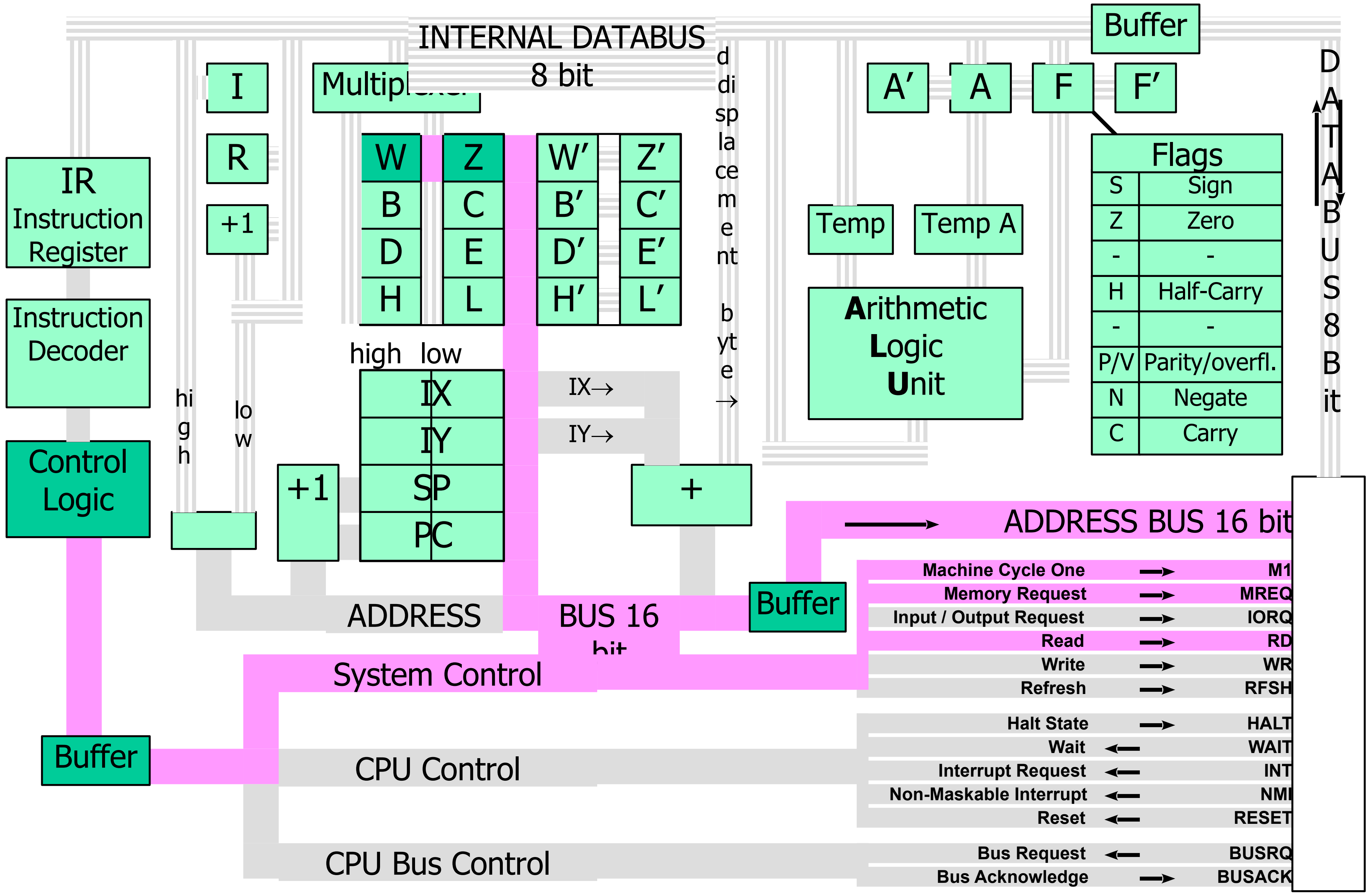
Periferica invia low byte di indirizzo



INT in IM2

T	T	T1	T2	TW	TW	T3	T4	T1	T2
M		M						M	

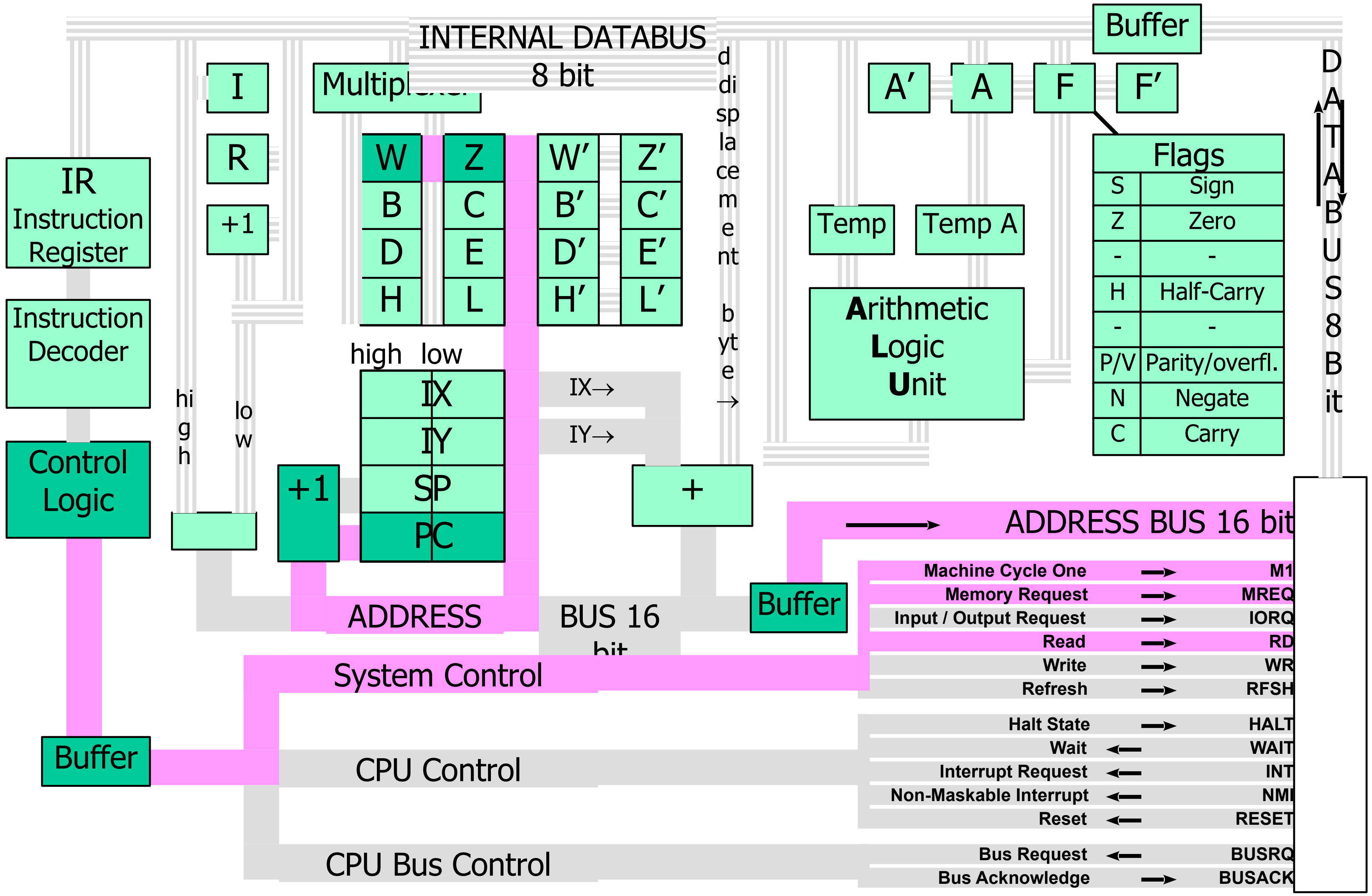
Mp legge routine di gestione INTerrupt



INT in IM2

T	T	T1	T2	TW	TW	T3	T4	T1	T2
M		M						M	

incrementa WZ e salva in PC



INTerrupt handler routine

Interrupt Handler (classico)

```
PUSH AF
PUSH BC
PUSH DE
PUSH HL

;…data acquisition…

POP HL
POP DE
POP BC
POP AF

EI
```

Interrupt Handler (con EXX)

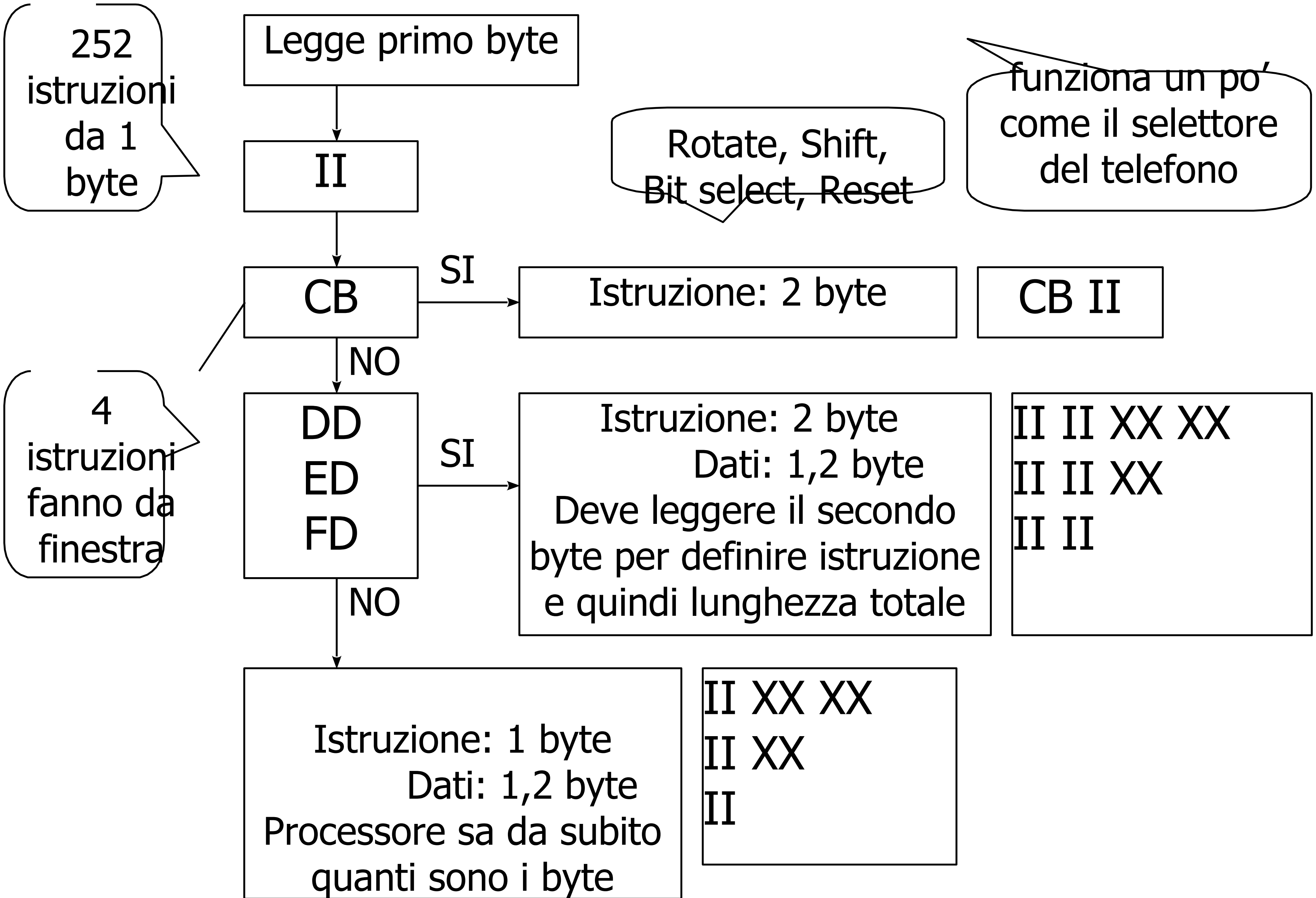
```
EX AF, AF’
EXX

;…data acquisition…

EXX
EX AF, AF’

EI
RETI
```

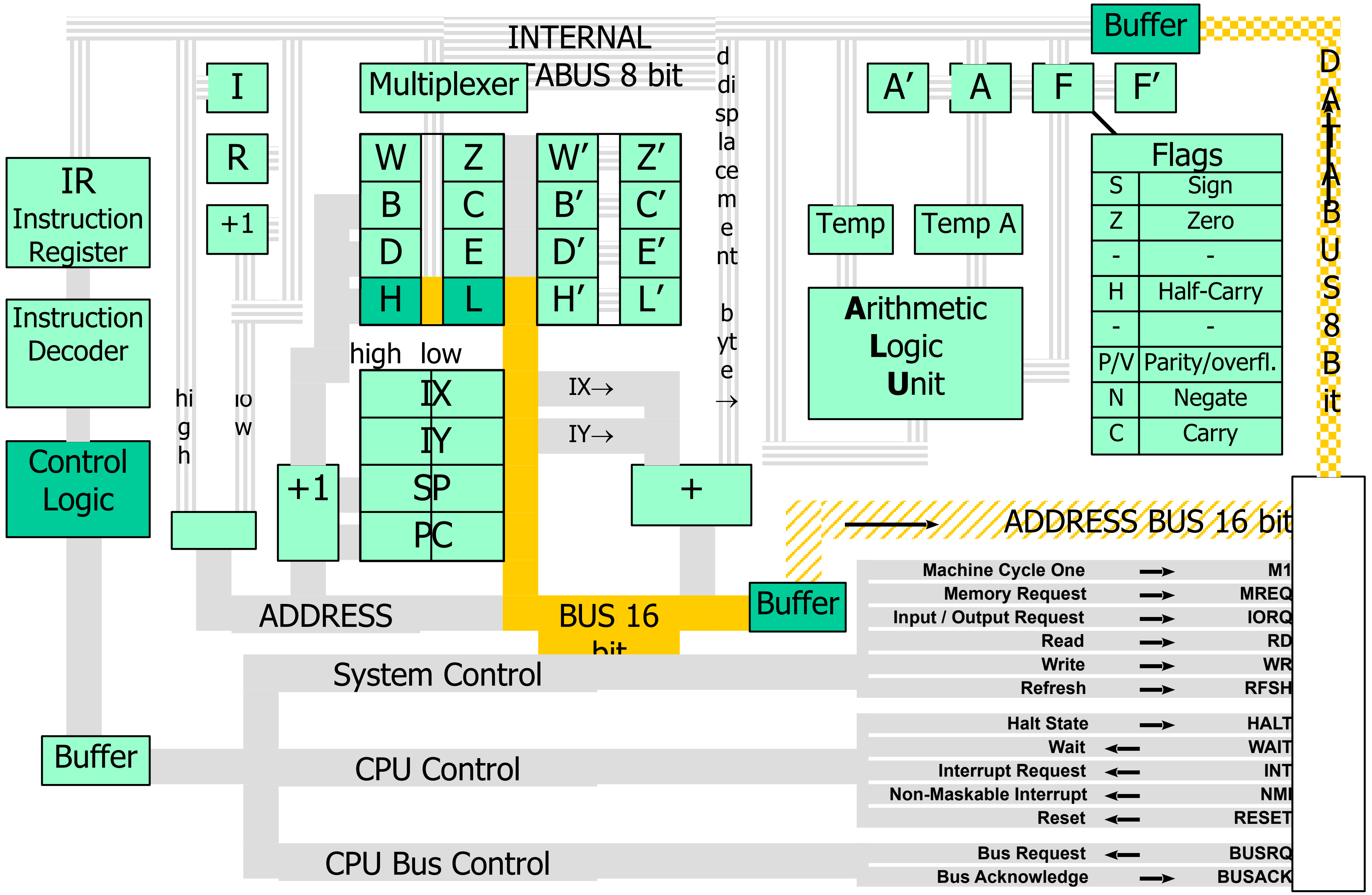
L’assembler Z80 usa istruzioni di lunghezza totale 1,2,3,4 byte


252 istruzioni da 1 byte
Legge primo byte
II
Rotate, Shift, Bit select, Reset
funziona un po’ come il selettore del telefono
CB
SI
Istruzione: 2 byte
CB II
NO
4 istruzioni fanno da finestra
DD ED FD
SI
Istruzione: 2 byte Dati: 1,2 byte Deve leggere il secondo byte per definire istruzione e quindi lunghezza totale
II II XX XX
II II XX
II II
NO
Istruzione: 1 byte Dati: 1,2 byte Processore sa da subito quanti sono i byte
II XX XX
II XX
II

IORQ RD

T1	T2	TW	T3
M			

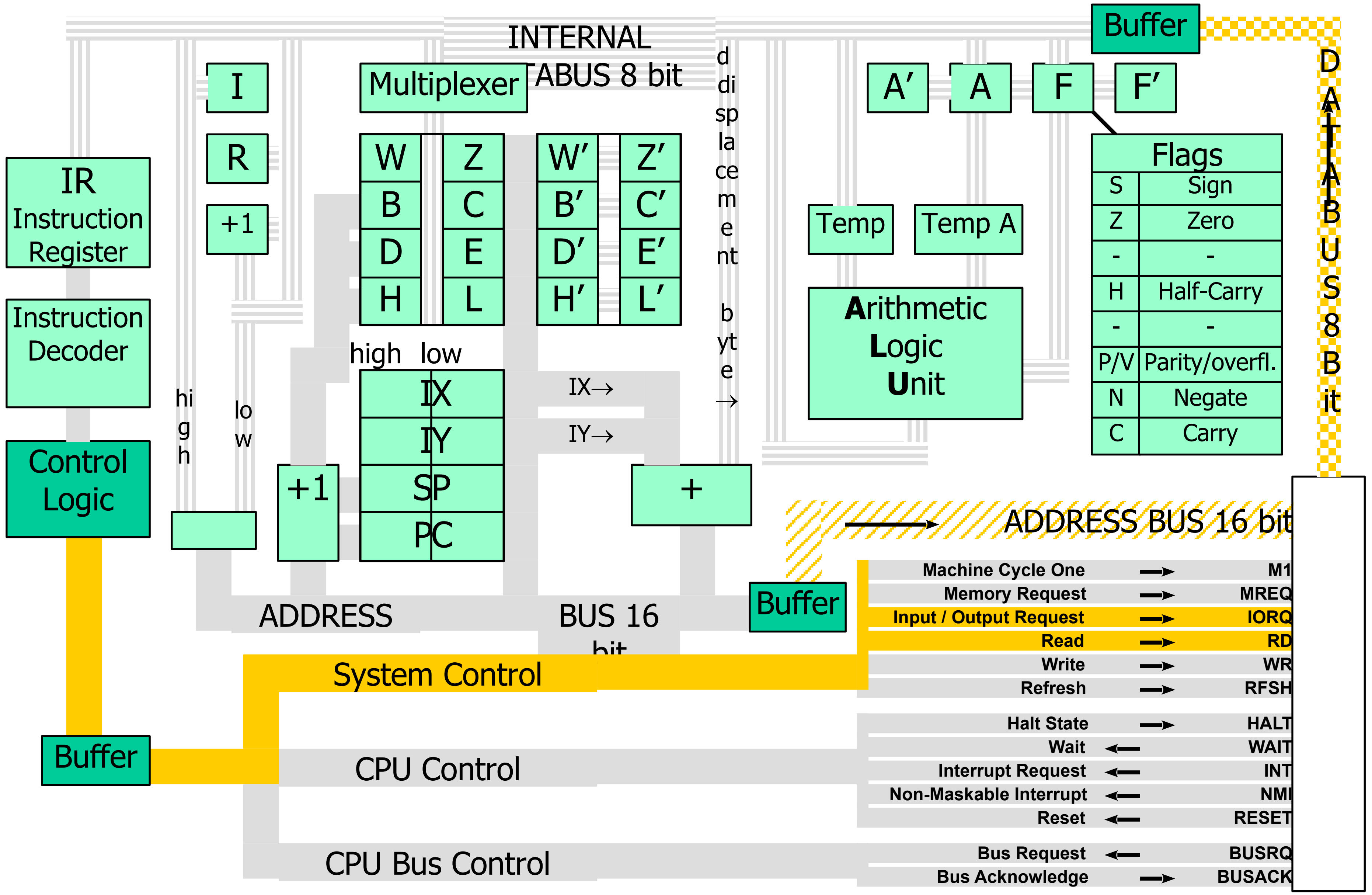
Vengono utilizzate solo le linee A0…A7 dell'ADDRESS BUS (256 dispositivi I/O)



IORQ RD

T1	T2	TW	T3
M			

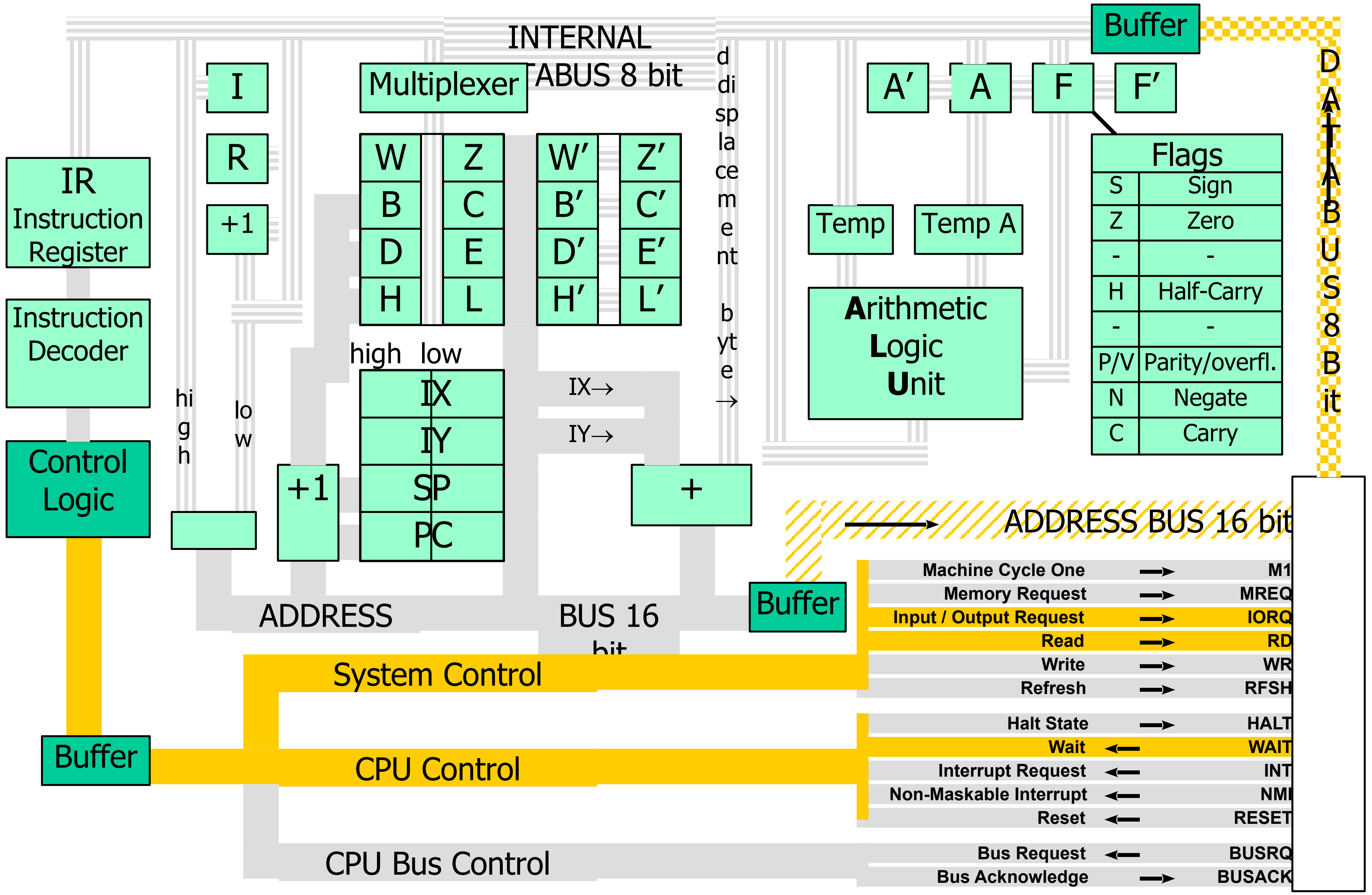
L'IORQ e' simile alla lettura della memoria, ma si attiva IORQ invece di MREQ



IORQ RD

T1	T2	TW	T3
M			

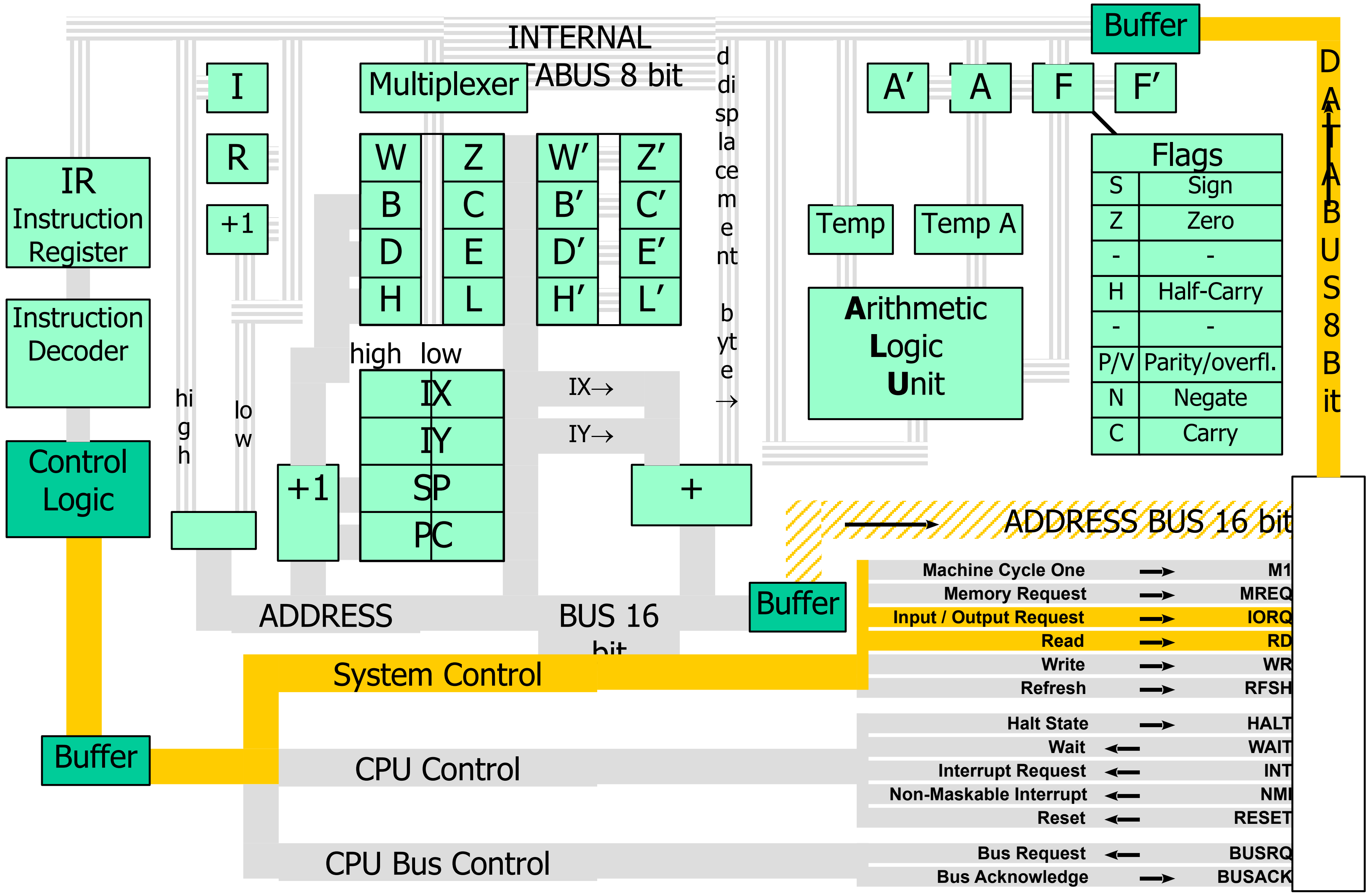
Viene automaticamente inserito uno stato TWait.
Una periferica lenta puo' inserirne altri ancora.



IORQ RD

T1	T2	TW	T3
M			

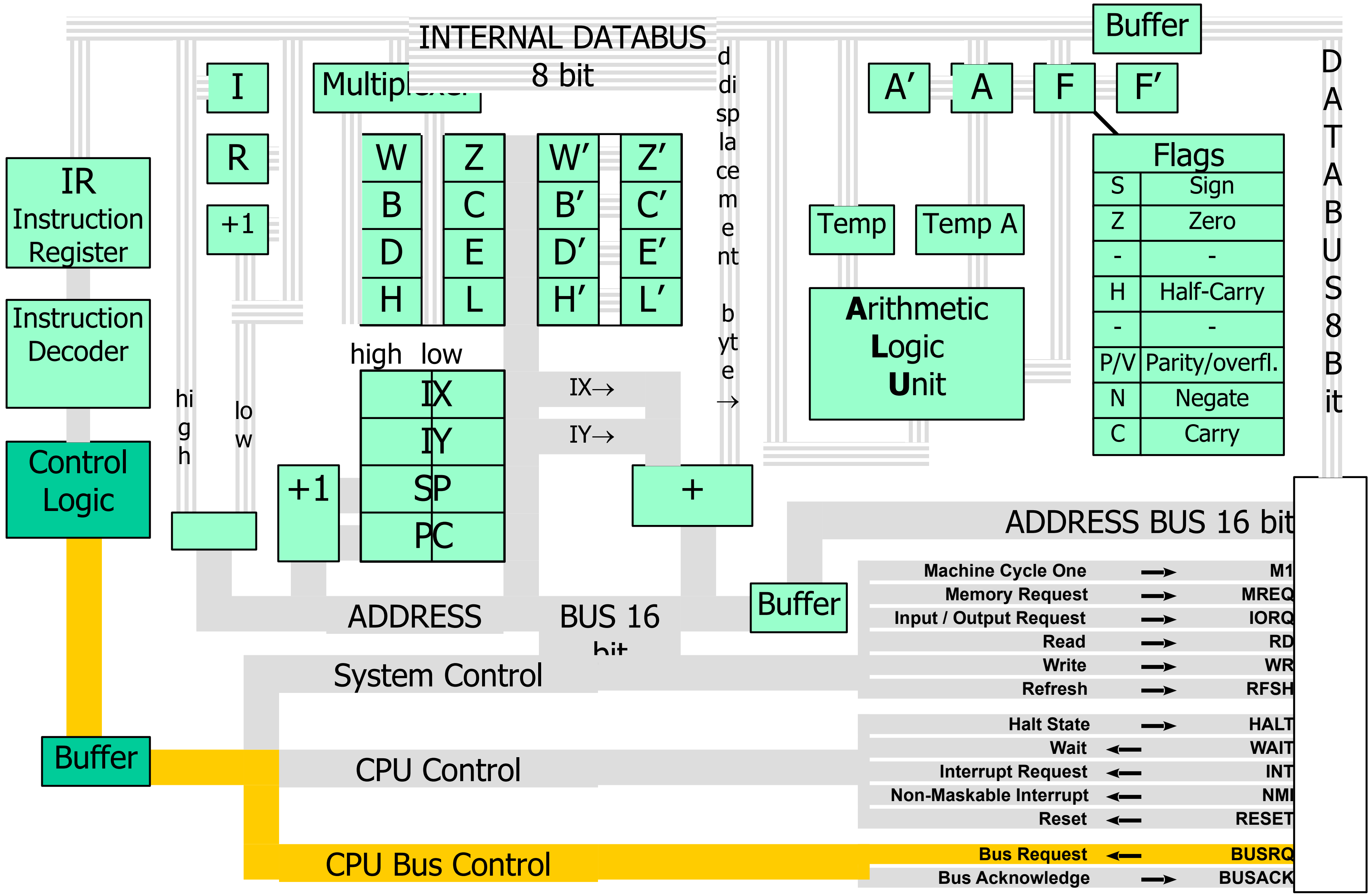
Rilasciato WAIT la periferica scrive



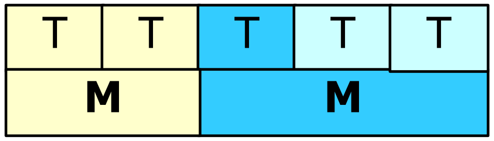
BUSRQ

T	T	T	T	T
M		M		

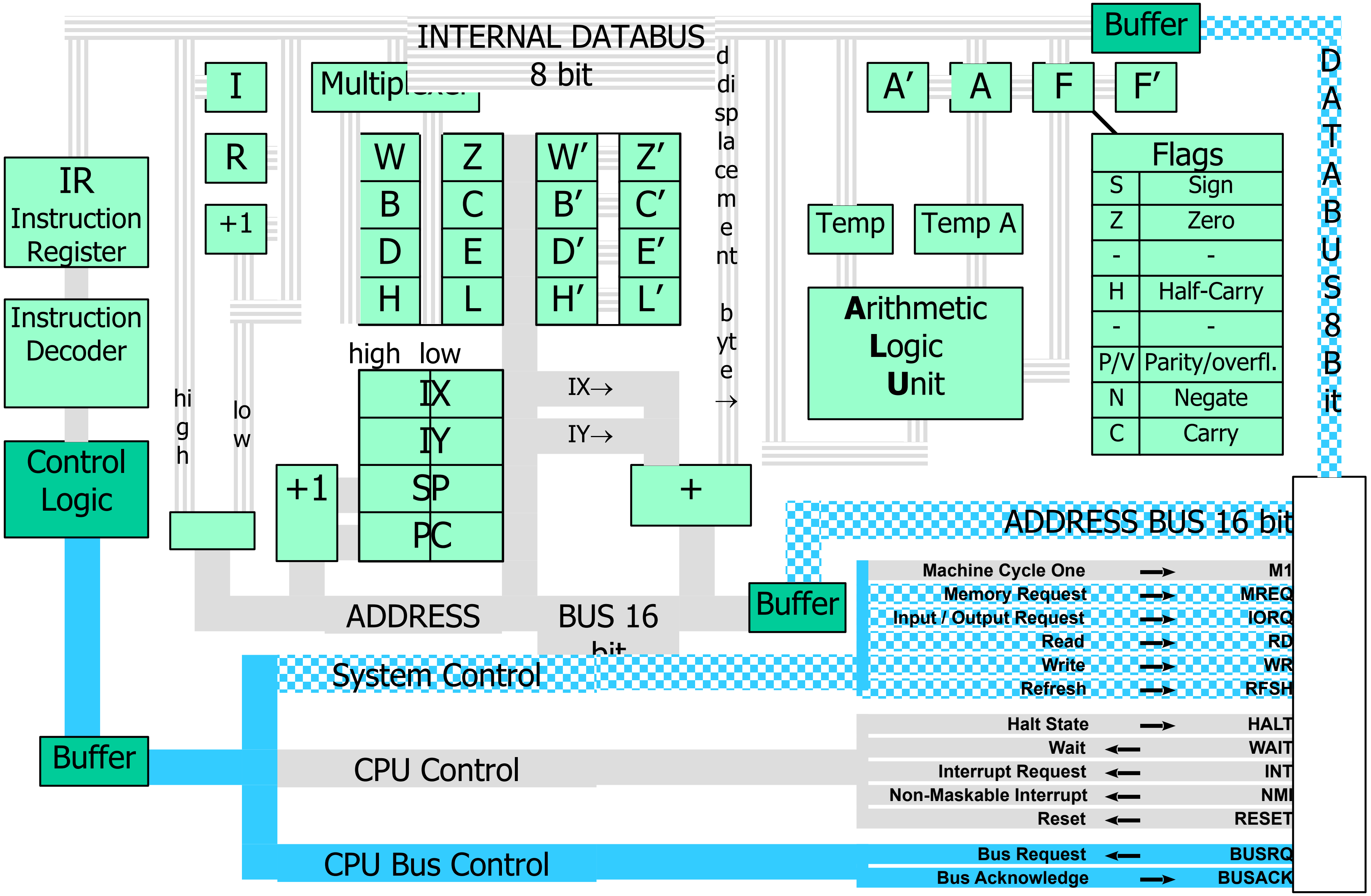
Una periferica molto veloce e’ meglio scriva /legga direttamente in memoria: usa BUSREQ



BUSRQ



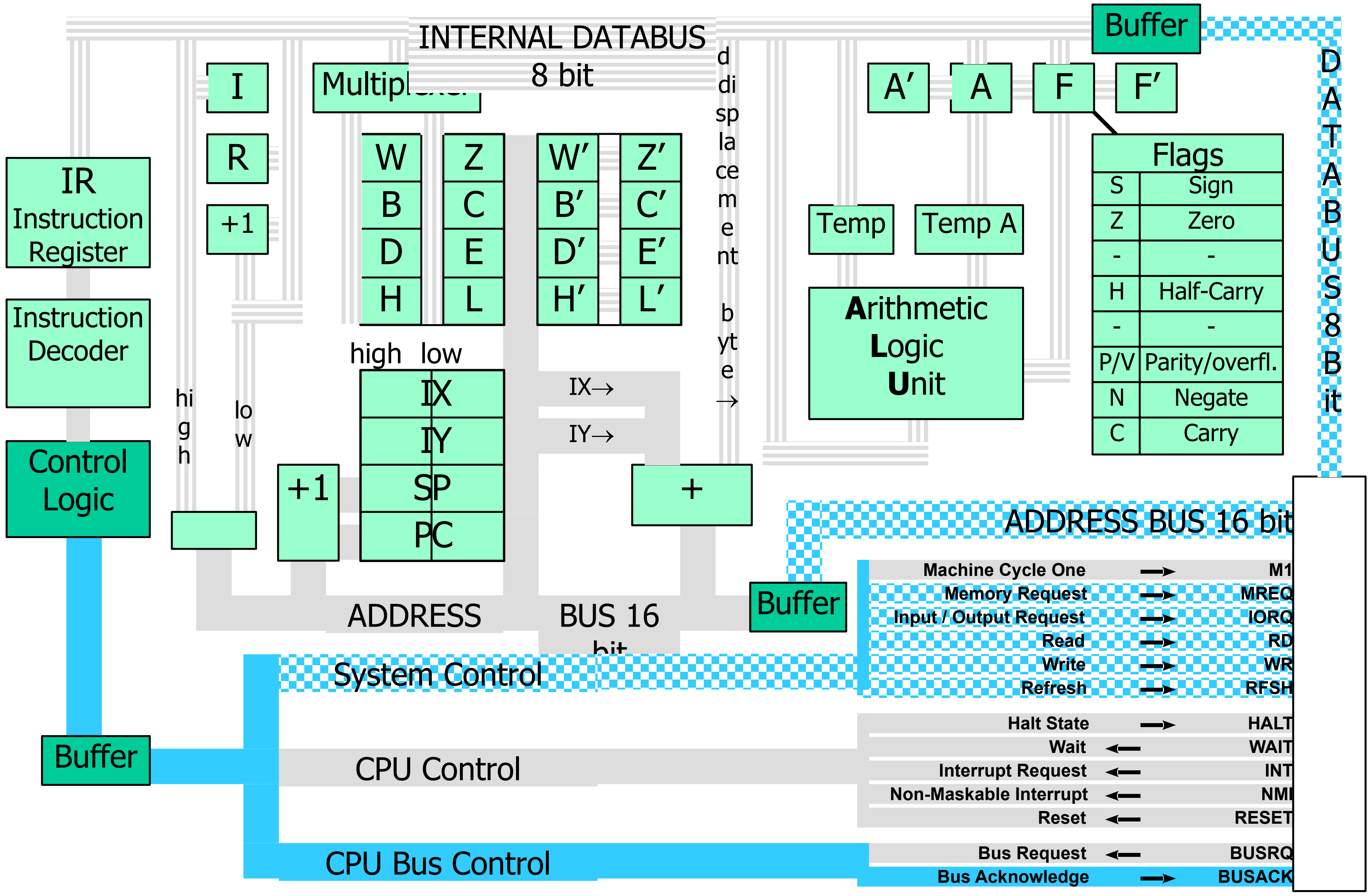
Nell' M seguente, Mp mette alta impedenza: DATA, ADDRESS, CONTROL. Attiva BUSACK



BUSRQ

T	T	T	T	T
M		**M**		

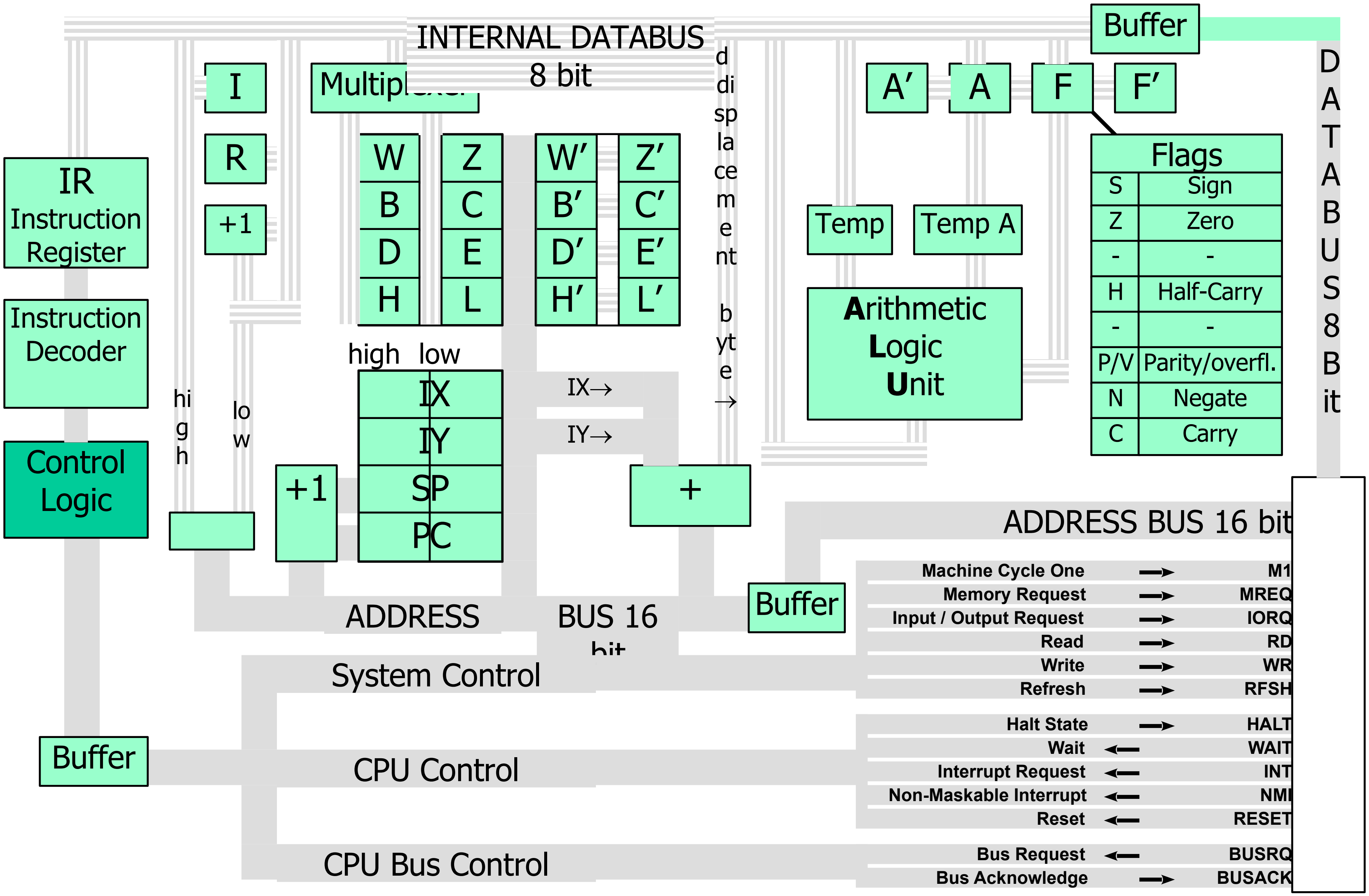
Quando la periferica ha finito rilascia BUSREQ.
Il tutto e' detto DMA-Direct Memory Access



BUSRQ

T	T	T	T	T
M		M		

Mp disattiva BUSACK, riprende controllo BUS
Se DMA lunghi, periferica deve fare Refresh



RESET

Il RESET permette un’accensione ordinata del processore e deve essere tenuto attiva per almeno 3 cicli di clock

Effetti:

PC=0
IFF1=0
IFF2=0
I=0
R=0
IM=0
ADRESS e DATA BUS: alta impedenza
CONTROL LINES: inattive