

Reading Keyboard Scan Codes Through the PS/2 Interface on the DE2-115 board

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1. Reading Keyboard Scan Codes Through the PS/2 Interface on the DE2-115 board

1.1 Background

The PC/AT keyboard transmits data in a clocked serial format consisting of a start bit, 8 data bits (LSB first), an odd parity bit and a stop bit. The clock signal is only active during data transmit. The generated clock frequency is usually in the range 10 - 30 kHz. Each bit should be read on the falling edge of the clock.

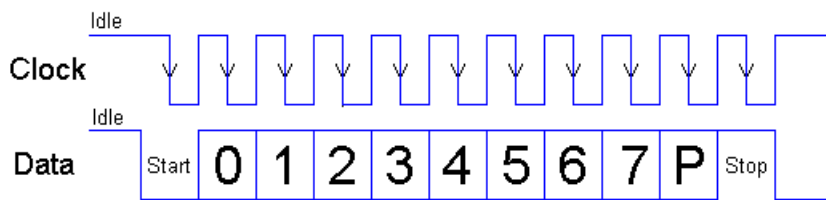


Figure 1. Keyboard transmission waveform

The above waveform represents a one byte transmission from the keyboard. The keyboard generally changes its data line on the rising edge of the clock as shown in the diagram. The data line only has to be valid on the falling edge of the keyboard clock. The Least Significant Bit is always sent first.

When a key is pressed, the keyboard transmits a 'make' code consisting of an 8-bit 'scan' code denoting the key pressed and, when the key is released, a 'break' code. The 'break' code (key released) consists of the same 8-bit scan code preceded by a special code - 'F0'H.

The keyboard handles combinations with control keys as SHIFT, CTRL, ALT, etc as two separate key presses, i.e., SHIFT-MAKE, 'A'-MAKE, SHIFT-BREAK, 'A'-BREAK. The 'A' scan code ('1C'H) is the same for both the shifted and unshifted state. To determine whether the 'A' scan code is interpreted as 'A' or 'a', the PC must keep track of the presence or absence of a prior SHIFT-MAKE.

Read more about the AT keyboard in appendix 1, "PC AT keyboard ref".

1.2 Assignment

Create a circuit that accepts scan codes from a keyboard attached to the PS/2 interface of the DE2-115 Board. The binary pattern of the scan code is displayed on the red LEDs. In addition, if a scan code for one of the '0'-'9' keys arrives, then the numeral will be displayed on the right 7-segment LED display of the DE2-115 Board. The system should be clocked using the 50 MHz oscillator on the DE2-115 board.

The lab group number should be displayed on the two leftmost 7-segment displays of the DE2-115 Board.

Create also a testbench that checks if the keyboard decoder works, testing at least two different key presses. The testbench must report back to the simulation user in plain text if the test worked or not after the simulation stops.

1.3 Problem definition

Here are listed the definitions that is needed to complete the design.

1.3.1 Port definitions

The inputs and outputs of the circuit are defined as follows:

Table 1: Port interface description

Name	Type	Range	Description
kb_data	IN	std_logic	The scan code bits enters through this input.
kb_clk	IN	std_logic	The keyboard clock signal enters through this input.
sys_clk	IN	std_logic	The system clock used to clock the system.
db	OUT	std_logic_vector (9 downto 0)	Drive the red LEDs on the DE2-115 board. Output all bits, except the startbit, received from the PS/2 keyboard
rsb	OUT	std_logic_vector (6 downto 0)	Drive the segments of the rightmost 7-segment digit on the DE2-115 Board.
Hex7	OUT	std_logic_vector (6 downto 0)	Drive the segments of the leftmost 7-segment digit (HEX7)
Hex6	OUT	std_logic_vector (6 downto 0)	Drive the segments of the 2 nd from left 7-segment digit (HEX6)

1.3.2 Process definitions

Within the main body of the architecture section, these processes should be implemented:

sync_keyboard

Synchronize the external inputs (kb_data and kb_clk) to the system clock. Creates an internal copy of the keyboard signals that only changes values on the positive edge of the system clock.

detect_falling_kb_clk

Creates an output (edge_found) which is one during one system clock cycle when a falling edge of the synchronized kb_clk signal has been found. This can be done by comparing the current value of the synchronized kb_clk signal with the old value (stored in the previous clock period) of the synchronized kb_clk signal. Remember that the output signal from this process should not be used as a clock, as this would create a design with multiple clock domains.

convert_scancode

When edge_found is one, this process shifts the data bit on the kb_data input into the most significant bit of a 10-bit shift register. After 11 keyboard clock cycles, the lower 8 bits of the register will contain the scan code, the upper 2 bits will store the stop and parity bits, and the start bit will have been shifted through the entire register and discarded.

The current value in the shift register is applied to the red LEDs. Since the LEDs are active-high, a segment will light for every '1' bit in the shift register. The LED segment will show some flickering as the shift register contents change.

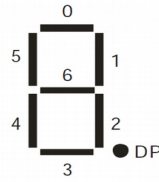


Figure 2: 7-segment display index to segment mapping

Table 2: Scan codes for the alpha numerics 0 to 9

KEY	SCANCODE	rsb
1	00010110	1111001
2	00011110	0100100
3	00100110	0110000
4	00100101	0011001
5	00101110	0010010
6	00110110	0000010
7	00111101	1111000
8	00111110	0000000
9	01000110	0010000
0	01000101	1000000
Else		0000110

If the scan code in the shift register matches the codes for the digits 0-9, then the rightmost 7-segment LED display will be activated to display the corresponding digit. The segments are active-low, and will light whenever the corresponding bit is '0'. If the scan code does not match one of these codes, the letter 'E' is displayed.

1.3.3 Tips and tricks

To avoid a lot of trouble in the design phase a few hints are useful:

- Do not use multiple clock definitions, i.e., `rising_edge()` or the corresponding 'EVENT' definition can only be used on one signal. This signal can in this case only be the system clock signal named `sys_clk`.
- Do not use 'EVENT (except the above), 'LAST_VALUE, `falling_edge` or `rising_edge` (except the case above).

1.4 Interface

The synthesis tool needs to know how the FPGA is connected to the external components. An attribute description included in the VHDL description will be used for this purpose. How to include this into the design will be demonstrated later.

```
type exemplar_string_array is array (natural range <>, natural range <>) of character;
attribute pin_number : string;
attribute array_pin_number : exemplar_string_array;
attribute pin_number of sys_clk : signal is "Y2";
attribute pin_number of kb_clk : signal is "G6";
attribute pin_number of kb_data : signal is "H5";
attribute array_pin_number of db : signal is ("G17","J17","H19","J19","E18","F18",
"F21","E19","F19","G19");
attribute array_pin_number of rsb : signal is
("H22","J22","L25","L26","E17","F22","G18");
attribute array_pin_number of hex6 : signal is
("AC17","AA15","AB15","AB17","AA16","AB16","AA17");
attribute array_pin_number of hex7 : signal is
("AA14","AG18","AF17","AH17","AG17","AE17","AD17");
```

Please note that each string in a pin number attribute list must be of equal length. This is fixed by adding one space at the end of the string before “ if necessary. This is VHDL language requirement. Do not forget this in the project designs!

This attribute description is prepared in a text file and can be copied from

/site/edu/es/TSTE12/material/Lab_Keyboard/keyboard_DE2-115_attributes.txt

1.5 Requirements

Here are the requirements to pass the laboratory:

- Implement the design using hdl_designer.
 - Declare a symbol and corresponding VHDL view.
- Design a test bench to verify the design.
 - The testbench should be built as a structural top level, i.e. block diagram in hdl_designer, and instantiate the keyboard symbol as a component.
 - The testbench should also include a stimuli and a control block in the same block diagram as the keyboard reader. The stimuli block generates the input data to the keyboard. The control block analyzes the design.
 - The testbench has to implement at least two different scancodes. The control block should check the output after each scancode have been generated.
 - The testbench should indicate each test case with correct or wrong behavior in the transcript window of the simulator. Take a look at the the ASSERT statement in VHDL. The user of the testbench should be able to load the testbench, type the command “run -all”, and then see three messages. The simulation should automatically stop when completed. The first two messages should indicate whether the test of a key worked, and the final message stating that the testbench have completed all tests. The messages printed in the modelsim window could for example be

```
Key1 test ok
Key2 test ok.
```

All tests done, stopping simulation

- Synthesize the design and demonstrate the function on the DE2-115 board.
- Summarize a number of key figures for the design.
 - How much of the total available design space is used?
 - What is the maximum clock frequency allowed for the design?

2. Design

It is here assumed that the reader have a basic knowledge of hdl_designer. The experience in the hdl designer intro in this course should be sufficient, available on the exercise page on the web.

On a linux computer platform, there is an important difference is how to start hdl_designer. To enable one group working together on the same design, we prepared the setup. Follow the steps below and the tool start and file permissions are set correctly.

2.1 Introduction

Your designs should preferably be saved in a new library directory. The first two steps differ depending on the computer platform you use. Please work either in the Linux or Windows environment to avoid problems due to possible incompatibilities between the two environments.

Linux

1. Start the hdl designer tool.

Load the course module TSTE12 and start a mentorskal

```
module load TSTE12
mentorskal &
```

Start hdl_designer in the mentorskal window using

```
tste12lab &
```

Once FPGA Advantage have started, do the following:

2. Open the design manager project view by selecting the Project tab at the lower left of the window.
3. Create a new regular library named KEYBOARD by selecting File->New->Library, and set root directory to /site/edu/es/labs/labgroup<nn>/Lab. Replace <nn> with your computer group number.
4. Make the library default and open/explore the library. Continue the work in this library and complete the exercise. Either double click on the library name or use right mouse button to acces the popup menu for the library and choose explore.

2.2 Design entry

Implement the design according to the description and requirements found in section 1. The tutorial material describes how to use the HDL designer tool.

2.3 Adding the pin attributes

The symbol pin attributes are necessary in the synthesis step. Here it is described how to include the prepared pin attributes into the keyboard design.

1. Create the symbol for the design.
2. Open the symbol editor window
3. Locate "User:" under Declarations in the window. Place the mouse pointer over the text. Double-click using left mouse button on the text.
4. Open the pin attributes text file in a text editor.
5. Copy and paste the pin attributes from the text file into the declarations dialog box.
6. Press Ok and the attributes should appear under User declarations.
7. Save the symbol.
8. Finish the design with ports and behavioral view.

The symbol and interface is now complete. Continue to add the behavior of the design and validate the functionality.

2.4 Simulating the design

The created model should be simulated to verify that the design is correct. Modelsim can be executed from within the hdl_designer environment. Stimuli for test of the design can be created using a testbench, which is the preferred way.

During debugging may the repeated change of the testbench code followed by compile and simulate be a bit time consuming. Another approach is therefore to use the interactive debugging in Modelsim. You may then find the following useful:

Add stimulus to kb_clk and kb_data and validate the function. These can either be written into the Modelsim window or put in a macro file. The following example simulate the scancode for the '4' key (remember that the keyboard should only generate a clock when there are bits to send):

```
force -repeat 20 sys_clk 0 0, 1 42
force kb_clk 1 25us, 0 100us, 1 150us, 0 200us, 1 250us, 0 300us, 1 350us, 0 400us, 1
450us, 0 500us, 1 550us, 0 600us, 1 650us, 0 700us, 1 750us, 0 800us, 1 850us, 0
900us, 1 950us, 0 1000us, 1 1050us, 0 1100us, 1 1150us
force kb_data 1 25us, 0 75us, 1 175us, 0 275us, 1 375us, 0 475us, 0 575us, 1 675us, 0
775us, 0 875us, 0 975us, 1 1075us
run 1200 us
```

These commands can also be put in a macro file to simplify repeated tests. Use a text editor to create the file and put the commands to be executed in it. It is important to keep all text on each force command in one single line for each force.

2.5 Creating the testbench

Here we describe briefly the steps to create a testbench. In order to write the testbench, check again the requirements in section 1.5.

1. Create a new symbol for the testbench design.
2. Open the symbol editor window
3. Open it as a new block diagram. This should open a new block diagram window.

4. Instantiate the keyboard reader as a component. Press the green block entry in the toolbars menu, i.e. , "add component".
5. Now a window with available components appear. Drag and drop the keyboard symbol on the testbench block diagram window.
6. Continue and add the stimuli block and control block to the schematic, using blue boxes.
7. Add behavior to the control and stimuli blocks.
8. Validate the testbench design. Important now is to choose generate and compile through components.
9. Validate the design.

1.1 Synthesis flow (using Precision)

1.1.1 Synthesize the Design

The design flow buttons include several steps in one command. There are flows defined for simulation and synthesis. The synthesis assume a validated and compiled design.

Select the keyboard design unit in the design browser.

Start synthesis by choosing the synthesis flow button. You find this next to the compile and generate toolbar buttons.

The Precision Synthesis settings appear. Make sure to change the following in the setup.

Technology:	Altera/Cyclone IV E
Device:	EP4CE115F29C
Speed Grade:	7
Design frequency:	50 MHz
Run Options:	Run Integrated Place and Route should be selected
Implementation options	Single Implementation Mode

Press ok. The synthesis tool is now started.

The synthesis now starts and generates a netlist, various reports including used pins, timing estimates etc., and a sof FPGA configuration file. The synthesis results are located in /site/edu/es/labs/labgroup<nn>/Lab/KEYBOARD/ps.

The sof programming file is located in a subdirectory inside the synthesis folder (ps).

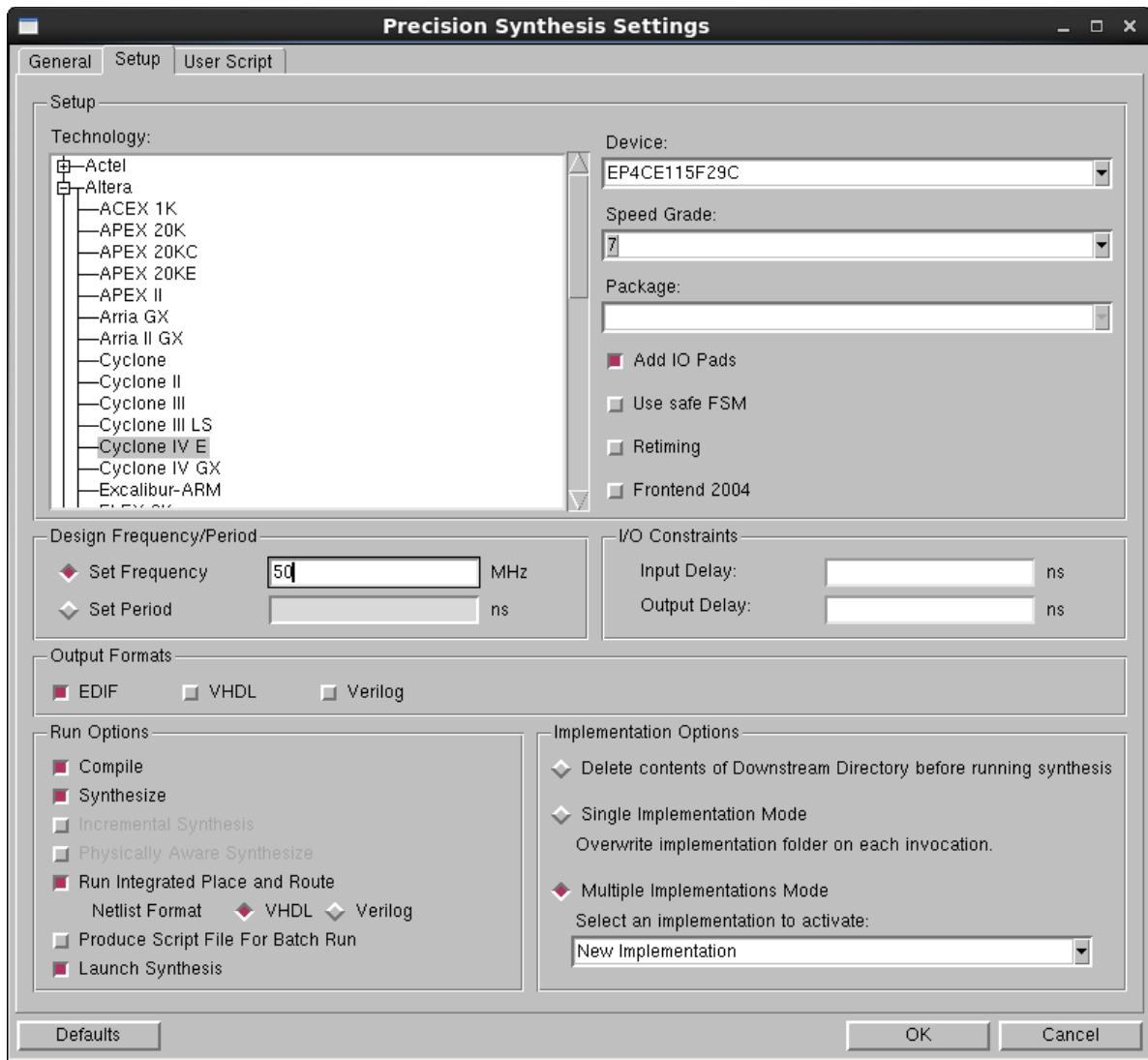


Figure 3: Synthesis settings dialog window

1.1.2 Results

A lot of reports has again been generated. Answer the following questions by looking at the design center tab in the precision tool. Look especially at the area report, the timing report, and the quartus timequest timing analyzer report:

Resource	Used	Available	Utilization
IOs %
LUTs %
Registers %
Memory Bits %
DSP block 9-bit elems %

Clock Name	Min Period [ns]	Max Freq [Mhz]	
sys_clk	Timing report
sys_clk	Quartus II Timequest report, worst case

Note the difference between the timing report and the timequest report. The timing report is a simplified estimate done at synthesis, while the timequest report is a more detailed timing analysis.

1.2 Downloading the Design

The board is always programmed from a computer using an USB connection. The programming is carried out using a special programming software from the FPGA vendor.

One approach to program the board is therefore to login and run the programming software on the computer connected to the FPGA board. This is however not very useful if the board is shared by multiple lab groups.

The board may also be accessed over the network. The programming software is then run on the same computer that is used for development. Instead of selecting the USB port on the development computer is a connection made from within the programming software to the other computer, thereby controlling the board remotely. The only difference is how to select the USB port inside the programming software.

1.2.1 Programming the FPGA

These steps are for programming the DE2-115 FPGA board.

1. Start Quartus II Programmer by entering the following command inside the mentorskal window
quartus_pgmw
2. Press the Add file button. Select your sof programming file.
3. Finally make sure that the USB-blaster and JTAG has been selected as the hardware to use. This is shown close to the the top. If the correct board is shown go to step 7 below.
4. If the wrong board or no board is connected, push the “Hardware Setup” button.
5. If a networked board is used select the JTAG Settings tab. Press Add Server to connect to the computer with the board.
6. Remember to select a board in the “currently selected hardware entry” before closing the Hardware setup window.
7. Select and mark the box Programming/Configure on the right of the file.
8. Then press start button to make the FPGA programmed. The new design will be downloaded within seconds.
9. Try out the hardware. Verify that it is your group number showing on the leftmost 7-segment LEDs.

10. Press keys on the keyboard and observe the results on the LED displays.

1. Appendix: PC AT keyboard ref

A.1 Description of keyboard

The original keyboard design had a single chip microprocessor, but now a customised controller chip is used. This keyboard controller chip takes care of all keyboard matrix scanning, key debouncing and communications with the computer, and has an internal buffer if the keystroke data cannot be sent immediately. The PC motherboard decodes the data received from the keyboard via the PS/2 port using interrupt IRQ1.

The one thing that these keyboards do not generate is ASCII values. With a typical AT keyboard having more than 101 keys, a single byte could not store codes for all the individual keys, plus these keys along with shift, control, or alt, etc. Also for some functions there is no ASCII equivalent, for example 'page up', 'page down', 'insert', 'home', etc.

When the keyboard controller finds that a key is being pressed or released it will send this keystroke information, known as scan codes, to the PIC microcontroller. There are two different types of scan codes - make codes and break codes.

The communications protocol is bi-directional, but here we only discuss the keyboard to host part.

A.1.1 make code

A make code is sent whenever a key is pressed or held down. Each key, including 'shift', 'control' and 'alt', sends a specific code when pressed. Cursor control keys, 'delete', 'page up', 'page down', 'ins', 'home' and 'end', send extended make codes. The make code is preceded by 'E0'h to indicate an extended code. The only exception is the 'pause' key that starts with a unique 'E1'h byte.

A.1.2 break code

A break code is sent when a key is released. The break code is the make

On 08/24/2017 01:21 PM, Thomas Johansson via RT wrote:

> /site/edu/es/labs/labgroup[1-9] /site/edu/es/labs/labgroup[1-3]? code preceded by 'F0'h byte. For extended keys the break code has an 'E0'h preceding the 'F0'h and make code value. The only exception is the 'pause' key as it does not have a break code and does not auto-repeat when held down.

A.1.3 key code

Every key is assigned its own unique code so that the host computer processing the information from the keyboard can determine exactly what happened to which key simply by looking at the scan codes received. There is no direct relationship between the scan code generated by a particular key and the character printed on the key top.

The set of make and break codes for each key comprises a scan code set. There are three standard scan code sets - numbered 1, 2, and 3 - stored within the keyboard controller. Scan code set 1 is retained for compatibility for older IBM XT computers. Scan set 3 is very similar to the set 2 but the extended codes are different. Scan code set 2 is the default for all AT keyboards and all scan codes discussed here are from this set.

A.1.4 scan code

If, for example, you press 'shift' and 'A' then both keys will generate their own scan codes, the 'A' scan code value is not changed if a shift or control key is also pressed. Pressing the letter 'A' generates '1C'h make code and when released the break code is 'F0'h, '1C'h.

Pressing 'shift' and 'A' keys will generate the following scan codes :

The make code for the 'shift' key is sent '12'h.

The make code for the 'A' key is sent '1C'h.

The break code for the 'A' key is sent 'F0'h, '1C'h.

The break code for the 'shift' key is sent 'F0'h, '12'h.

If the right shift was pressed then the make code is '59'h and break code is 'F0'h, '59'h.

By analysing these scan codes the PC software can determine which key was pressed. By looking at the shift keystroke the software can distinguish between upper and lower case.

A.1.5 Keyboard serial data

The AT keyboard transmission protocol is a serial format, with one line providing the data and the other line providing the clock. The data length is 11 bits with one start bit (logic 0), 8 data bits (lsb first), odd parity bit and a stop bit (logic 1). The clock rate is approximately 10 to 30kHz and varies from keyboard to keyboard.

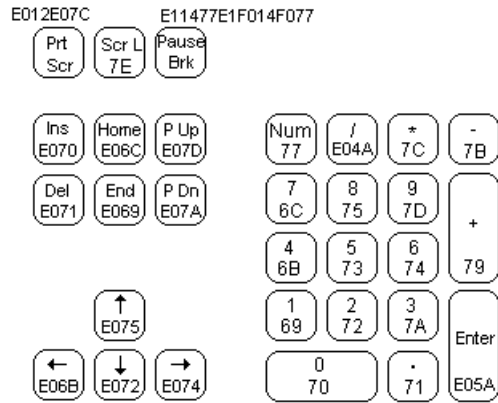
A.2 Scancodes and commands

A.2.1 Keyboard layouts with codes

Scan code tables

Keyboard alpha numeric scan codes

ESC 76	F05 05	F06 06	F04 04	F0C 0C	F03 03	F0B 0B	F83 83	F0A 0A	F01 01	F09 09	F78 78	F07 07		
~ 0E	1! 16	2@ 1E	3# 26	4\$ 25	5% 2E	6^ 36	7& 3D	8* 3E	9(46	0) 45	-_ 4E	+= 55	\ 5D	← 66
TAB 0D	Q 15	W 1D	E 24	R 2D	T 2C	Y 35	U 3C	I 43	O 44	P 4D	[{ 54]} 5B		
Caps 58	A 1C	S 1B	D 23	F 2B	G 34	H 33	J 3B	K 42	L 4B	; 4C	"' 52	↵ 5A		
Shift 12	Z 1A	X 22	C 21	V 2A	B 32	N 31	M 3A	<, 41	>. 49	?/ 4A	Shift 59			
Ctrl 14	Alt 11	SPACE 29						Alt E0 11	Ctrl E0 14					



Key	Make	Break	
A	'lC'h	'F0'h	'1C'h
B	'32'h	'F0'h	'32'h
C	'21'h	'F0'h	'21'h
D	'23'h	'F0'h	'23'h
E	'24'h	'F0'h	'24'h
F	'2B'h	'F0'h	'2B'h
G	'34'h	'F0'h	'34'h
H	'33'h	'F0'h	'33'h
I	'43'h	'F0'h	'43'h
J	'3B'h	'F0'h	'3B'h
K	'42'h	'F0'h	'42'h
L	'4B'h	'F0'h	'4b'h
M	'3A'h	'F0'h	'3A'h
N	'31'h	'F0'h	'31'h
O	'44'h	'F0'h	'44'h
P	'4D'h	'F0'h	'4D'h
Q	'15'h	'F0'h	'15'h
R	'2D'h	'F0'h	'20'h
S	'1B'h	'F0'h	'1B'h
T	'2C'h	'F0'h	'2C'h
U	'3C'h	'F0'h	'3C'h
V	'2A'h	'F0'h	'2A'h
W	'1D'h	'F0'h	'1D'h
X	'22'h	'F0'h	'22'h

Key	Make	Break	
Y	'35'h	'F0'h	'35'h
Z	'1A'h	'F0'h	'1A'h
1	'16'h	'F0'h	'16'h
2	'1E'h	'F0'h	'1E'h
3	'26'h	'F0'h	'26'h
4	'25'h	'F0'h	'25'h
5	'2E'h	'F0'h	'2E'h
6	'36'h	'F0'h	'36'h
7	'3D'h	'F0'h	'3D'h
8	'3E'h	'F0'h	'3E'h
9	'46'h	'F0'h	'46'h
0	'45'h	'F0'h	'45'h

A.3 Further reading

A.3.1 Web references

Interfacing the AT keyboard

<http://retired.beyondlogic.org/keyboard/keybrd.htm>

<http://www.computer-engineering.org/ps2protocol/>