Digital Logic Design
CPCS-211

By

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Lecture No 34

Design Of Synchronous Counters

Today's Topics

In this lecture we will cover the following

- Design of Synchronous Counters

Design of Synchronous Counters

- Synchronous counters are sequential circuits that need clock input to count some sequence of numbers.
- Most counters are devices with no data input that go through a fixed
- sequence of states on successive clocks.
- For example, a 4-bit binary counter cycles through the sequence

  0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 0 1 . . .
- It needs four flip flops because the largest number in this sequence is 15 whose binary is 1111.

Example (4-Bit Binary Counter)

- We want to design a 4-bit binary counter that goes from 0 to 1, 1 to 2, and so on 14 to 15 and then 15 to 0.
- The state table and the truth table for this counter are the same; they have 16 rows (for numbers 0 to 15), 4 input columns (for current number), and 4 output columns (for next number), as shown in the following Table.
- As can be seen, the next state for state 0 (0000) is 1 (0001), for 1 is 2, and so forth, until the next state for 15 (1111) is 0 (0000).
- We shall construct this counter using D-flip flop.
- We know that for D-flip flop, the characteristic equation is

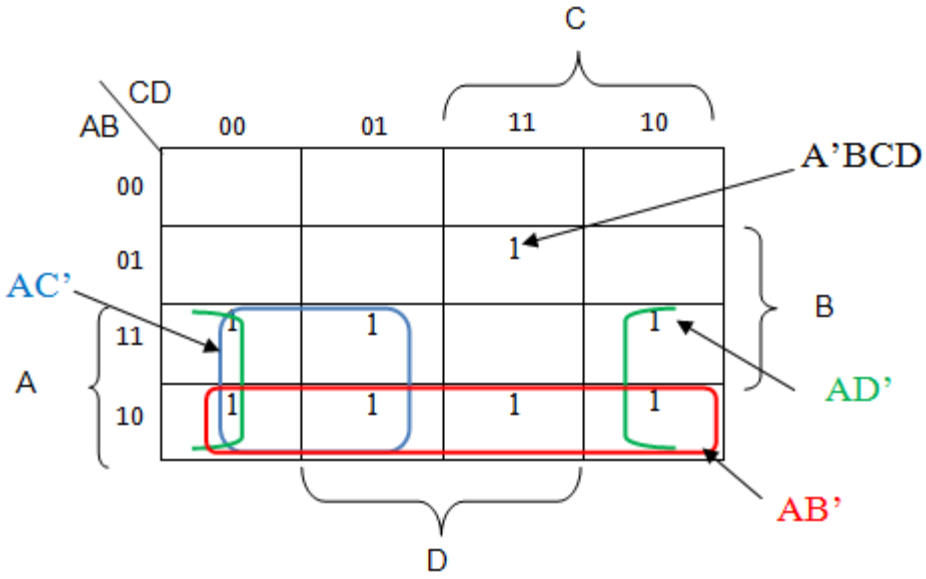
$$D = Q(t+1) = Q^*$$

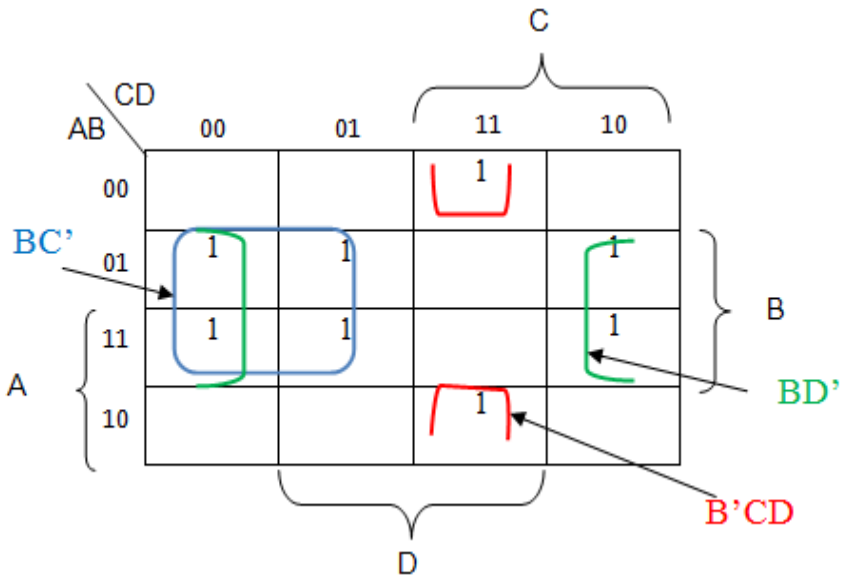
Example (Contd...)

Input				Output			
A	B	C	D	A*	B*	C*	D*
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	1	0	1	0
1	0	1	0	1	0	1	1
1	0	1	1	1	1	0	0
1	1	0	0	1	1	0	1
1	1	0	1	1	1	1	0
1	1	1	0	1	1	1	1
1	1	1	1	0	0	0	0

Example (Contd...)

- Now we shall draw K-maps for next state functions A*, B*, C* and D* as.

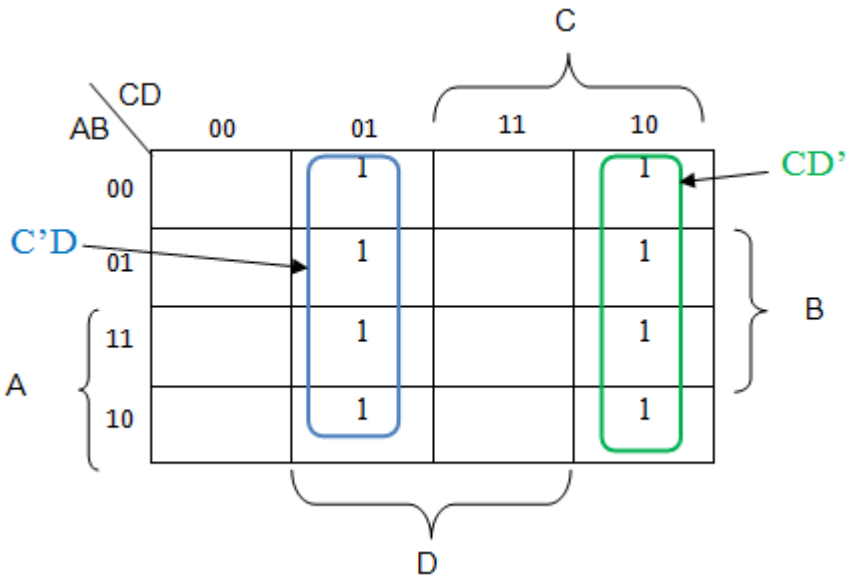


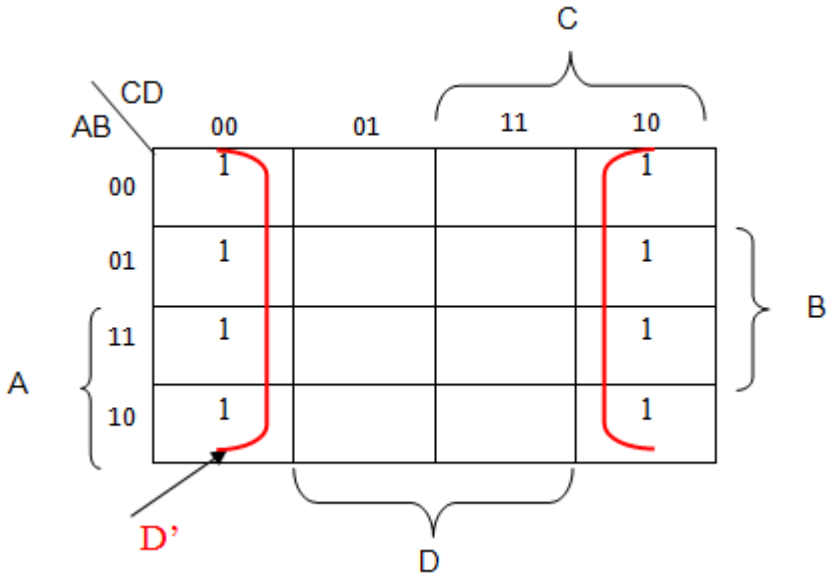


A* = AB' + AC' + AD' + A'BCD

B* = BC' + BD' + B'CD

Example (Contd...)





$C^* = C'D + CD'$

$D^* = D'$

Example (Contd...)

- So, the inputs for all four D-flip flops are:

  $D_A = A^* = AB' + AC' + AD' + A'BCD$

  $D_B = B^* = BC' + BD' + B'CD$

  $D_C = C^* = C'D + CD'$

  $D_D = D^* = D'$

- This solution would require 12 gates (9 AND gates and 3 OR gates) with 30 gate inputs.
- If we have Exclusive-OR gates available, we could simplify the expressions to

$D_A = A^* = A(B' + C' + D') + A'BCD = A(BCD)' + A'(BCD)$
$= A \oplus BCD$

$D_B = B^* = B(C' + D') + B'CD = B(CD)' + B'(CD) = B \oplus CD$

$D_C = C^* = C'D + CD' = C \oplus D$

$D_D = D^* = D'$

- This would only require 2 AND gates and 3 Exclusive-OR gates.

Example (4-Bit Binary Counter)

- We want to design the same 4-bit binary counter that goes from 0 to 1, 1 to 2, and so on 14 to 15 and then 15 to 0.
- As can be seen, the next state for state 0 (0000) is 1 (0001), for 1 is 2, and so forth, until the next state for 15 (1111) is 0 (0000).
- We shall construct this counter using JK-flip flops.
- We know that for JK-flip flop, the excitation table is

Q	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

- Using this excitation table, we construct the following input table (or state table) for the required counter as:

Example (Contd...)

Current States				Next States				Flip Flop Inputs							
A	B	C	D	A*	B*	C*	D*	J_A	K_A	J_B	K_B	J_C	K_C	J_D	K_D
0	0	0	0	0	0	0	1	0	X	0	X	0	X	1	X
0	0	0	1	0	0	1	0	0	X	0	X	1	X	X	1
0	0	1	0	0	0	1	1	0	X	0	X	X	0	1	X
0	0	1	1	0	1	0	0	0	X	1	X	X	1	X	1
0	1	0	0	0	1	0	1	0	X	X	0	0	X	1	X
0	1	0	1	0	1	1	0	0	X	X	0	1	X	X	1
0	1	1	0	0	1	1	1	0	X	X	0	X	0	1	X
0	1	1	1	1	0	0	0	1	X	X	1	X	1	X	1
1	0	0	0	1	0	0	1	X	0	0	X	0	X	1	X
1	0	0	1	1	0	1	0	X	0	0	X	1	X	X	1
1	0	1	0	1	0	1	1	X	0	0	X	X	0	1	X
1	0	1	1	1	1	0	0	X	0	1	X	X	1	X	1
1	1	0	0	1	1	0	1	X	0	X	0	0	X	1	X
1	1	0	1	1	1	1	0	X	0	X	0	1	X	X	1
1	1	1	0	1	1	1	1	X	0	X	0	X	0	1	X
1	1	1	1	0	0	0	0	X	1	X	1	X	1	X	1

Table 7.6

q	$q^\star$
0	0
0	1
1	0
1	1

Example (Contd...)

- Next step is to draw K-maps for J_A , K_A , J_B , K_B , J_C , K_C , J_D and K_D
- In order to save time, we can compare all the columns with one another and conclude that

  $J_A = K_A = BCD$

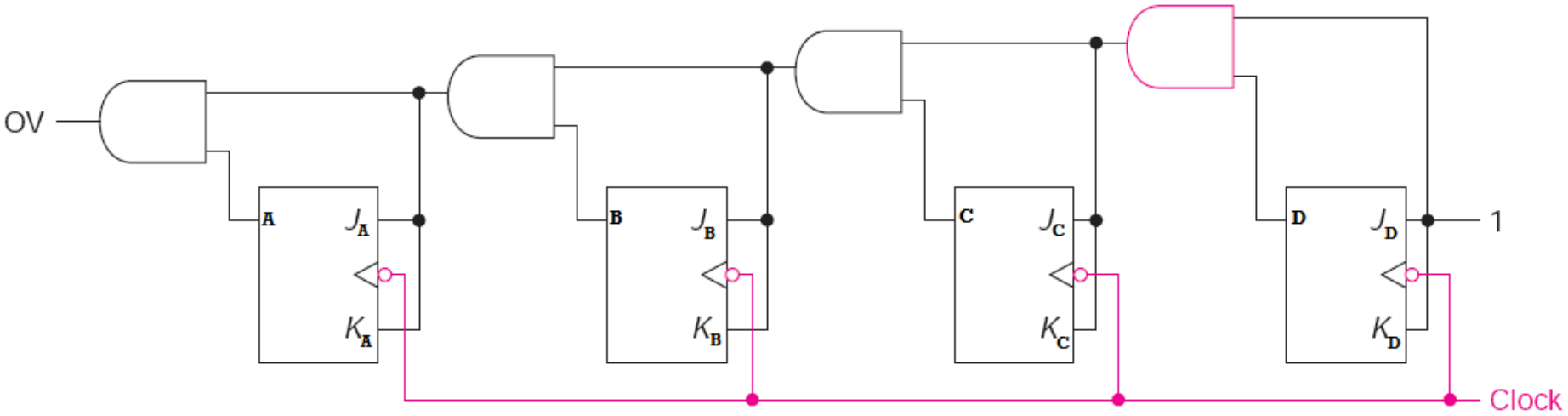
  $J_B = K_B = CD$

  $J_C = K_C = D$

  $J_D = K_D = 1$
- Thus the circuit for the given 4-bit counter, using four JK-flip flops is as follows:

Example (Contd...)

Figure 7.6 A 4-bit counter.*



- The first AND gate is not necessary if this is a stand-alone counter; the output of the "D" flip flop would be connected directly to J_C and K_C.
- The OV output is 1 when the counter is in state 15 (1111). OV could be connected to the JK inputs of another flip flop or, if we built two 4 flip flop circuits like the one above, we could connect the OV output of one to the input where a 1 is now connected to construct an 8-bit counter.

Example (An Up/Down Counter)

- An up/down counter is a one that can count in either direction, depending upon a control input.
- We will label that control input x, such that the counter counts up when x = 0 and counts down when x = 1.
- We shall design this counter by using JK-flip flops.
- The state table for such a counter is shown below:

Example (Contd...)

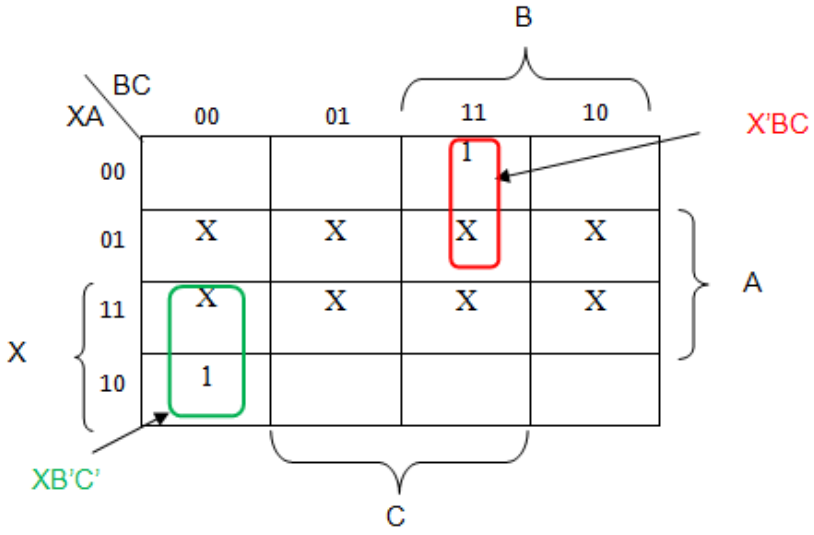
Current State				Next State			Flip Flop Inputs					
X	A	B	C	A*	B*	C*	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	0	1	0	X	0	X	1	X
0	0	0	1	0	1	0	0	X	1	X	X	1
0	0	1	0	0	1	1	0	X	X	0	1	X
0	0	1	1	1	0	0	1	X	X	1	X	1
0	1	0	0	1	0	1	X	0	0	X	1	X
0	1	0	1	1	1	0	X	0	1	X	X	1
0	1	1	0	1	1	1	X	0	X	0	1	X
0	1	1	1	0	0	0	X	1	X	1	X	1
1	0	0	0	1	1	1	1	X	1	X	1	X
1	0	0	1	0	0	0	0	X	0	X	X	1
1	0	1	0	0	0	1	0	X	X	1	1	X
1	0	1	1	0	1	0	0	X	X	0	X	1
1	1	0	0	0	1	1	X	1	1	X	1	X
1	1	0	1	1	0	0	X	0	0	X	X	1
1	1	1	0	1	0	1	X	0	X	1	1	X
1	1	1	1	1	1	0	X	0	X	0	X	1

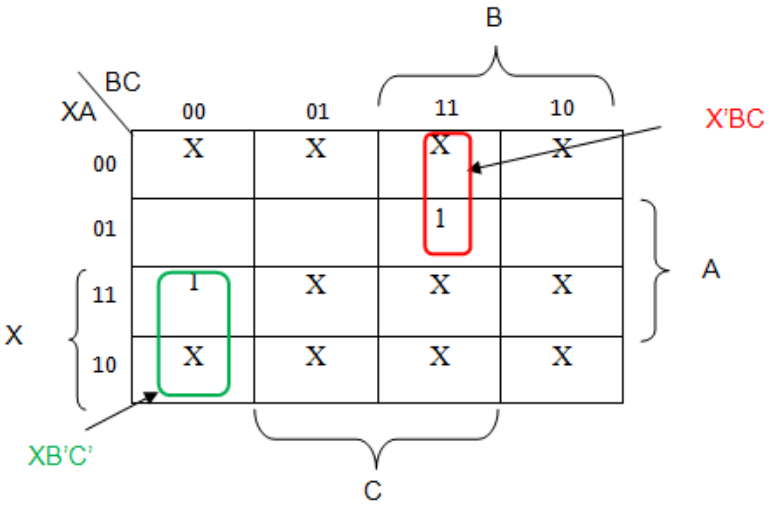
Tabl

q
0
0
1
1

Example (Contd...)

- The K-maps for J_A , K_A , J_B , K_B , J_C and K_C are as follows:

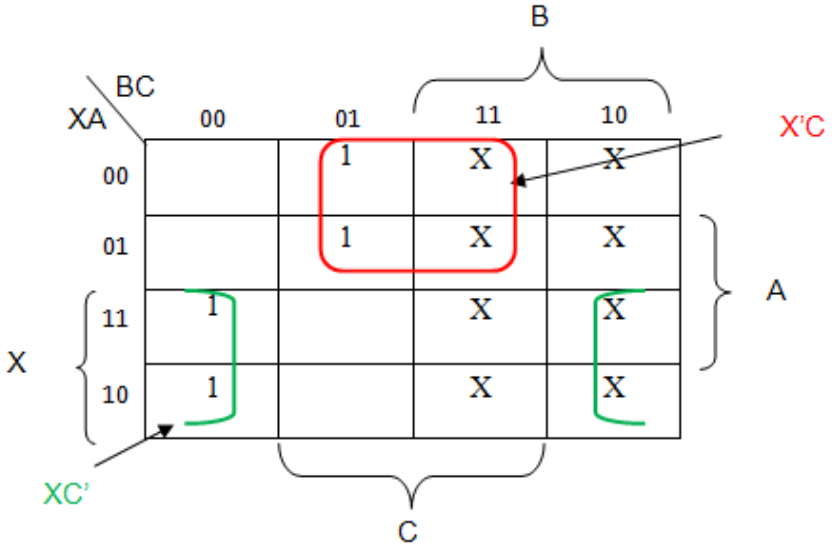


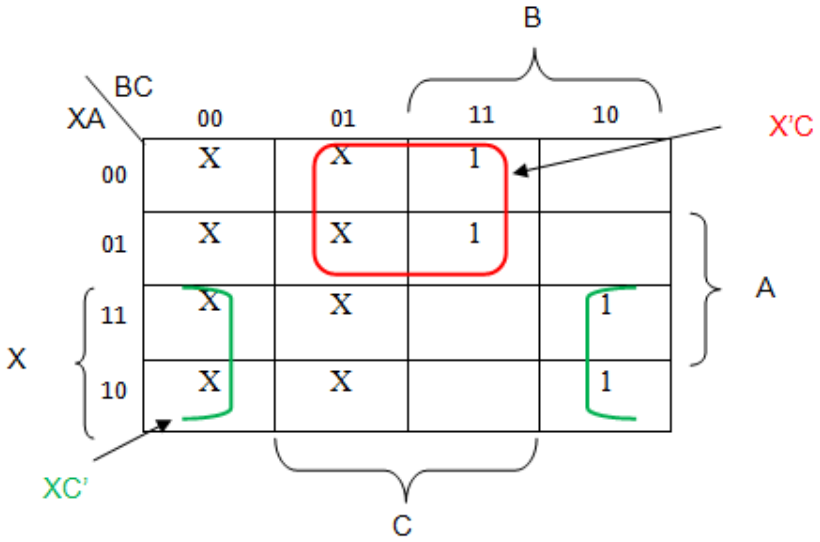


$J_A = X'BC + XB'C'$

$K_A = X'BC + XB'C'$

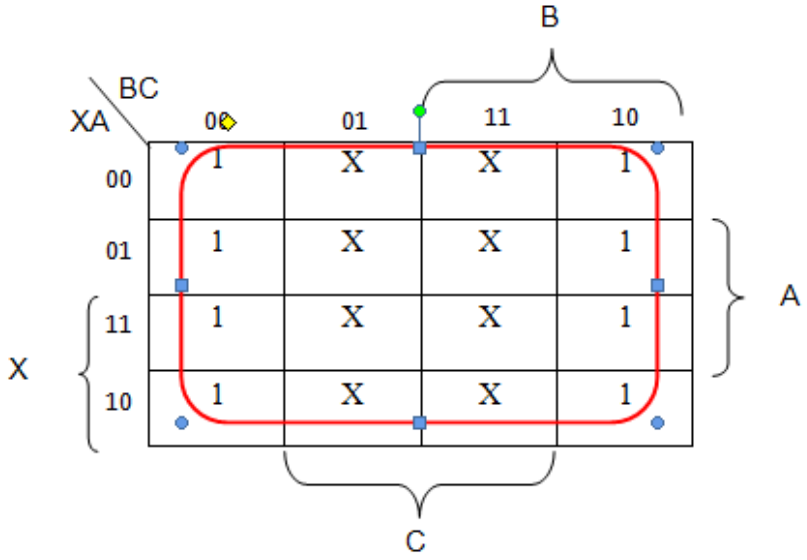
Example (Contd...)



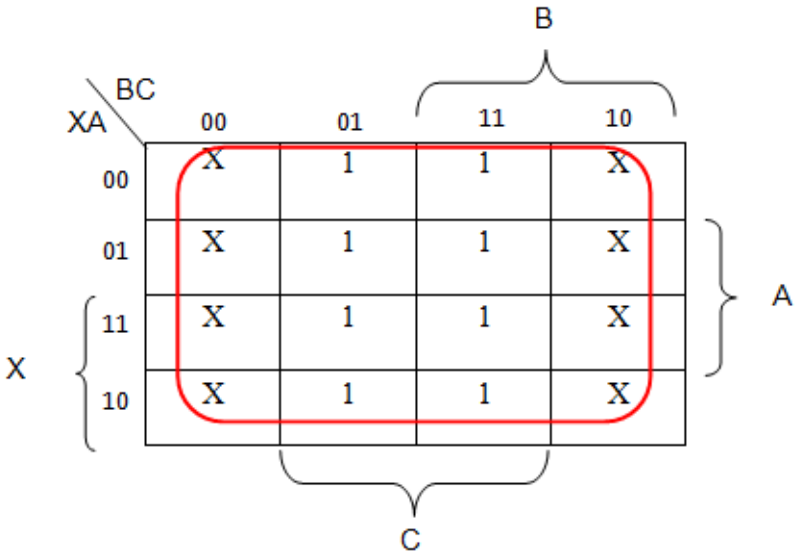


- $J_B = XC' + X'C$ $K_B = XC' + X'C$

Example (Contd...)



$J_C = 1$

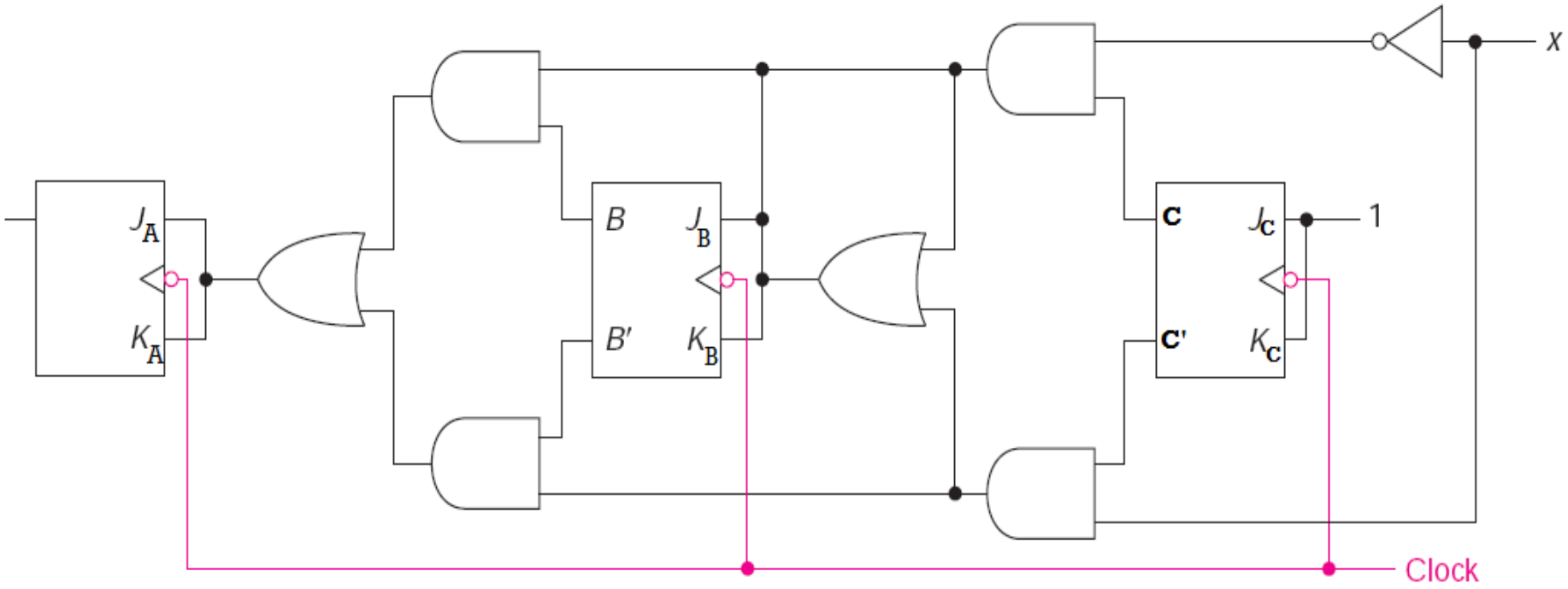


$K_C = 1$

Example (Contd...)

- A block diagram for up/down counter is shown in Figure 7.7.

Figure 7.7 An up/down counter.



Example (Decimal Counter)

- We will look next at a decimal or decade counter, one that goes through the sequence
  0 1 2 3 4 5 6 7 8 9 0 1 . . .
- We shall design this counter using JK-flip flops.
- The state (truth) table is similar to that for the binary counter, as seen below:

Example (Contd...)

Current States				Next States				Flip Flop Inputs							
A	B	C	D	A*	B*	C*	D*	J_A	K_A	J_B	K_B	J_C	K_C	J_D	K_D
0	0	0	0	0	0	0	1	0	X	0	X	0	X	1	X
0	0	0	1	0	0	1	0	0	X	0	X	1	X	X	1
0	0	1	0	0	0	1	1	0	X	0	X	X	0	1	X
0	0	1	1	0	1	0	0	0	X	1	X	X	1	X	1
0	1	0	0	0	1	0	1	0	X	X	0	0	X	1	X
0	1	0	1	0	1	1	0	0	X	X	0	1	X	X	1
0	1	1	0	0	1	1	1	0	X	X	0	X	0	1	X
0	1	1	1	1	0	0	0	1	X	X	1	X	1	X	1
1	0	0	0	1	0	0	1	X	0	0	X	0	X	1	X
1	0	0	1	0	0	0	0	X	0	0	X	0	X	X	1
1	0	1	0	Don't Care				X	X	X	X	X	X	X	X
1	0	1	1	Don't Care				X	X	X	X	X	X	X	X
1	1	0	0	Don't Care				X	X	X	X	X	X	X	X
1	1	0	1	Don't Care				X	X	X	X	X	X	X	X
1	1	1	0	Don't Care				X	X	X	X	X	X	X	X
1	1	1	1	Don't Care				X	X	X	X	X	X	X	X

Table 7.6

q	$q^\star$
0	0
0	1
1	0
1	1

Example (Contd...)

- Next step is to draw K-maps for J_A , K_A , J_B , K_B , J_C , K_C , J_D and K_D
- It is left as an exercise for the students.
- We shall get the following input equations for all four flip flops.

  $J_A = BCD$, $K_A = D$

  $J_B = K_B = CD$

  $J_C = A'D$, $K_C = D$

  $J_D = K_D = 1$
- Thus the circuit for the required decimal counter, using four JK-flip flops is as follows:

Example (Contd...)

- Circuit for the required decimal counter is left as an exercise for the students.

Example

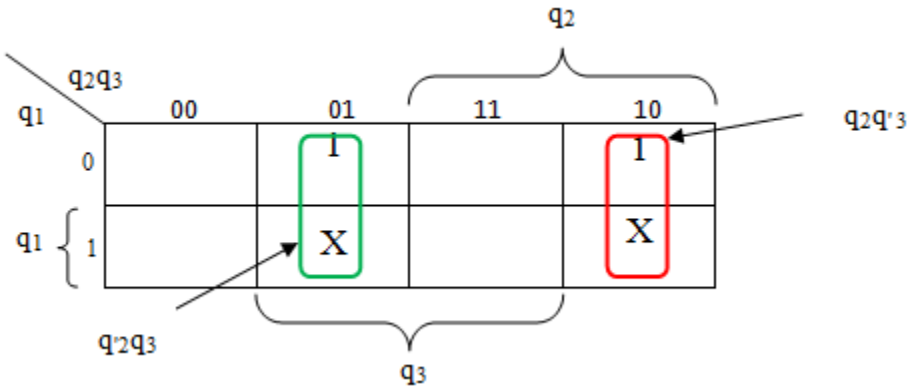
- We will next design a counter that goes through some sequence of states that are not in numeric order
  0 3 2 4 1 5 7 and repeat
- We shall design this counter by using D, SR, T and JK-flip flops.
- Note that the cycle is 7 states; it never goes through state 6 (which will be treated as don't care).
- We can now draw the state table (in any order) or go directly to the truth table, including a row for the unused state.
- The combined state table for SR and T-flip flop inputs for such a counter is shown below:

Example (Contd...)

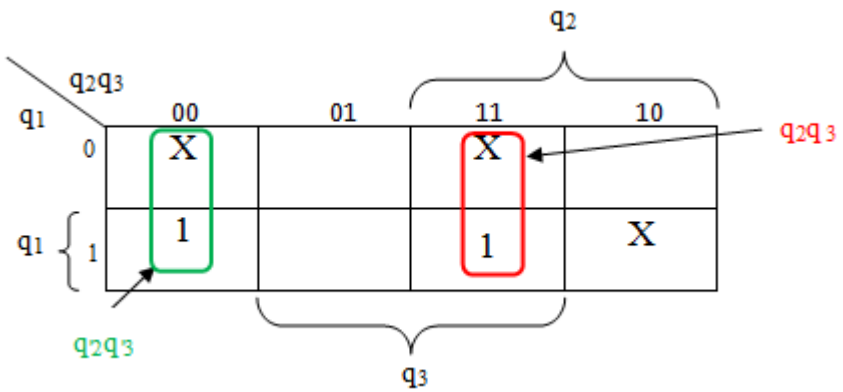
q_1	q_2	q_3	$q_1^\star$	$q_2^\star$	$q_3^\star$	S_1	R_1	S_2	R_2	S_3	R_3	T_1	T_2	T_3
0	0	0	0	1	1	0	X	1	0	1	0	0	1	1
0	0	1	1	0	1	1	0	0	X	X	0	1	0	0
0	1	0	1	0	0	1	0	0	1	0	X	1	1	0
0	1	1	0	1	0	0	X	X	0	0	1	0	0	1
1	0	0	0	0	1	0	1	0	X	1	0	1	0	1
1	0	1	1	1	1	X	0	1	0	X	0	0	1	0
1	1	0	X	X	X	X	X	X	X	X	X	X	X	X
1	1	1	0	0	0	0	1	0	1	0	1	1	1	1

We shall now first construct K-maps for S_1 , R_1 , S_2 , R_2 , S_3 and R_3

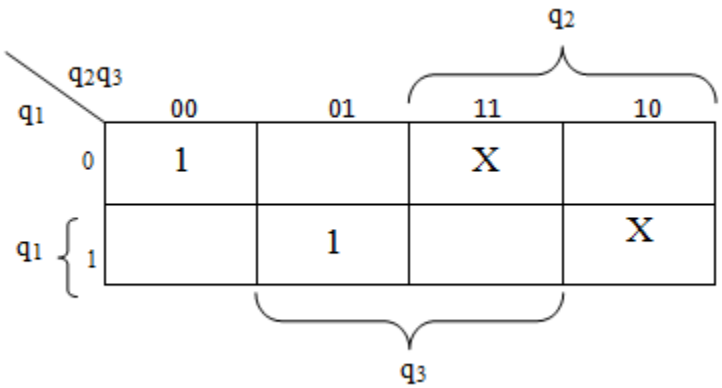
Example (Contd...)



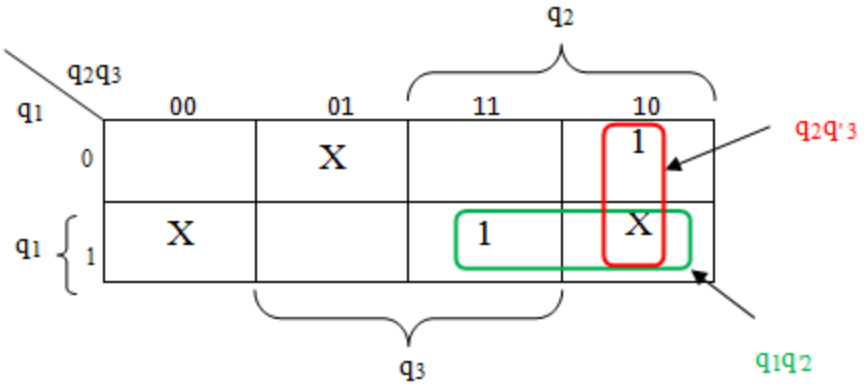
$S_1 = q'_2 q_3 + q_2 q'_3$



$R_1 = q'_2 q'_3 + q_2 q_3$

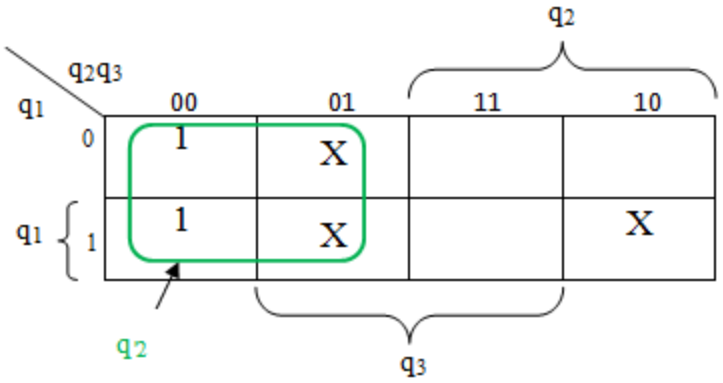


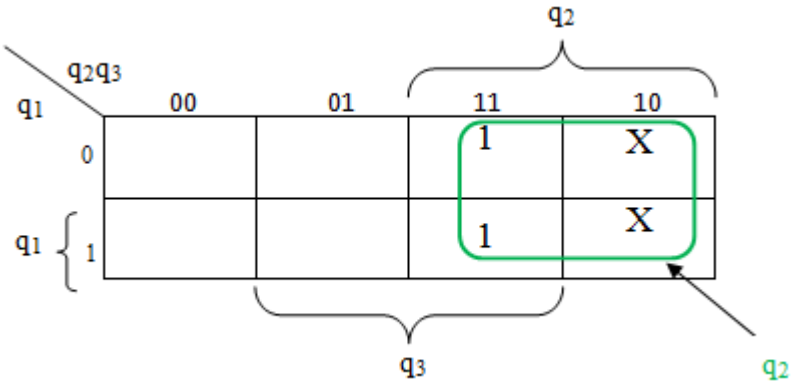
$S_2 = q'_1 q'_2 q'_3 + q_1 q'_2 q_3$



$R_2 = q_1 q_2 + q_2 q'_3$

Example (Contd...)





$S_3 = q'_2$

$R_3 = q_2$

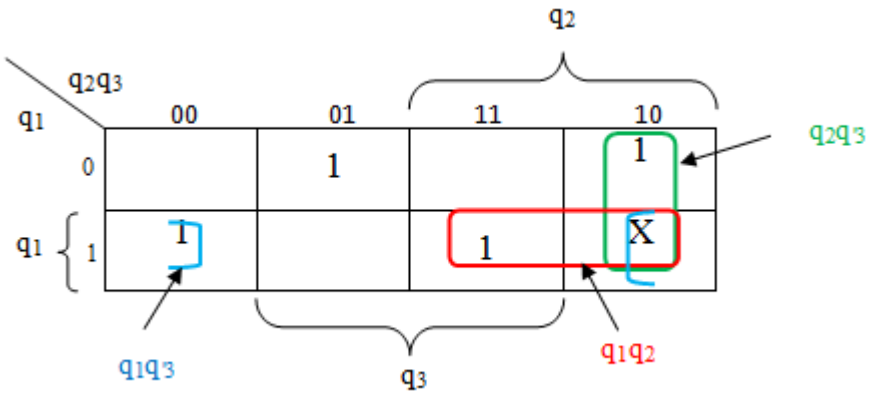
- The circuit for the required counter using SR-flip flops is as follows:

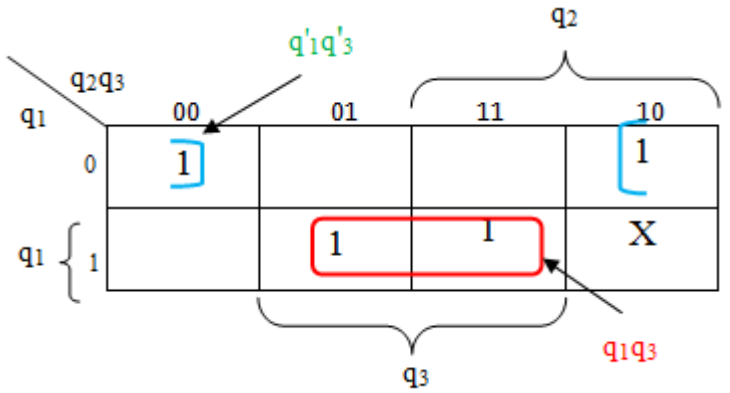
Example (Contd...)

- Left as an exercise for the students:

Example (Contd...)

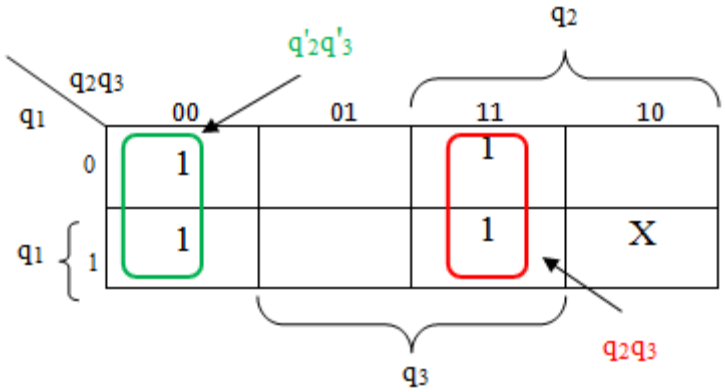
- Now K-maps for T_1 , T_2 and T_3 are as follows:





$T_1 = q'_1 q'_2 q_3 + q_1 q_2 + q_1 q'_3 + q_2 q'_3$

$T_2 = q_1 q_3 + q'_1 q'_3$



$T_3 = q_2 q_3 + q'_2 q'_3$

Example (Contd...)

- The circuit of required counter using T-flip flops is as follows:
- Left as an exercise for the students

Example (Contd...)

- Now finally we shall construct the circuit for the required counter using JK-flip flops.
- For this, the following table gives the JK-flip flop inputs.

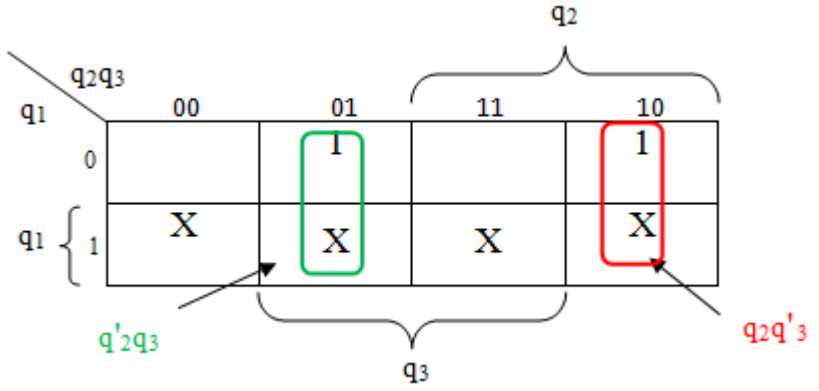
Current State			Next State			Flip Flop Inputs					
q_1	q_2	q_3	$q_1^\star$	$q_2^\star$	$q_3^\star$	J_1	K_1	J_2	K_2	J_3	K_3
0	0	0	0	1	1	0	X	1	X	1	X
0	0	1	1	0	1	1	X	0	X	X	0
0	1	0	1	0	0	1	X	X	1	0	X
0	1	1	0	1	0	0	X	X	0	X	1
1	0	0	0	0	1	X	1	0	X	1	X
1	0	1	1	1	1	X	0	1	X	X	0
1	1	0	X	X	X	X	X	X	X	X	X
1	1	1	0	0	0	X	1	X	1	X	1

Tabl

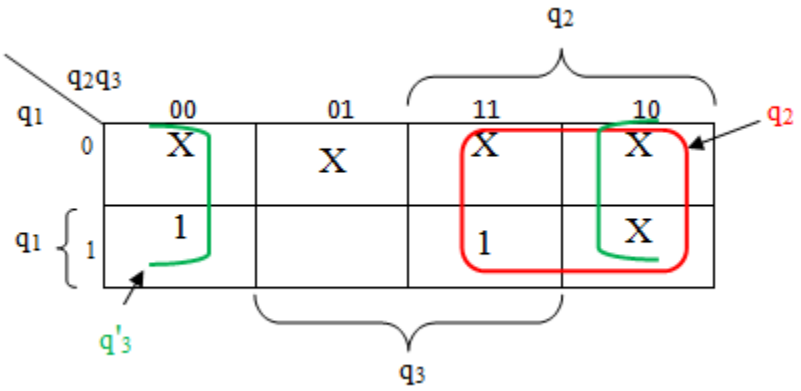
q
0
0
1
1

- The K-maps for J_1 , K_1 , J_2 , K_2 , J_3 and K_3 are as follows:

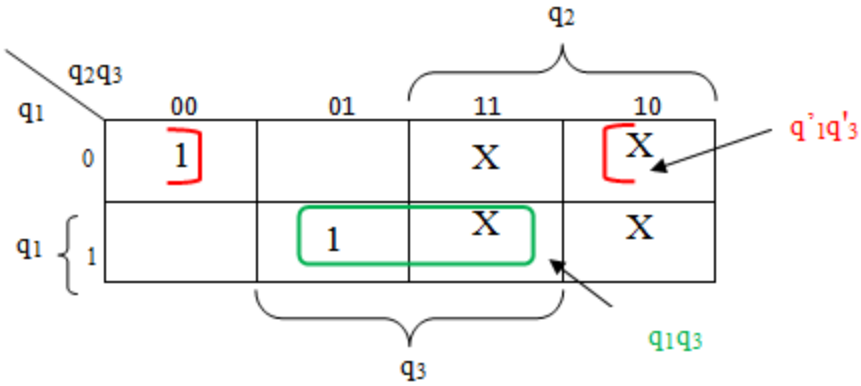
Example (Contd...)



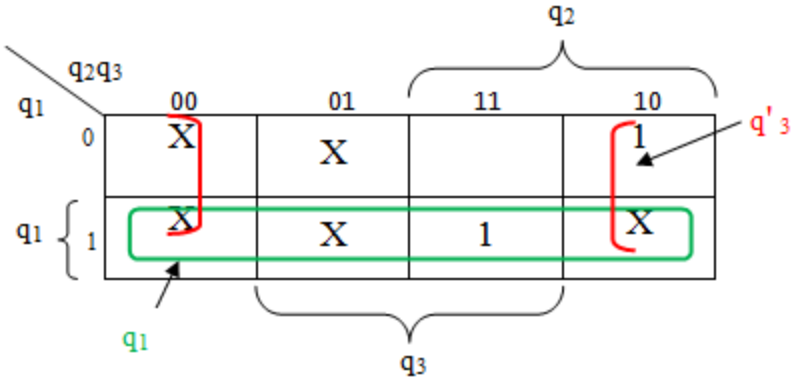
$J_1 = q'_2 q_3 + q_2 q'_3$



$K_1 = q_2 + q'_3$

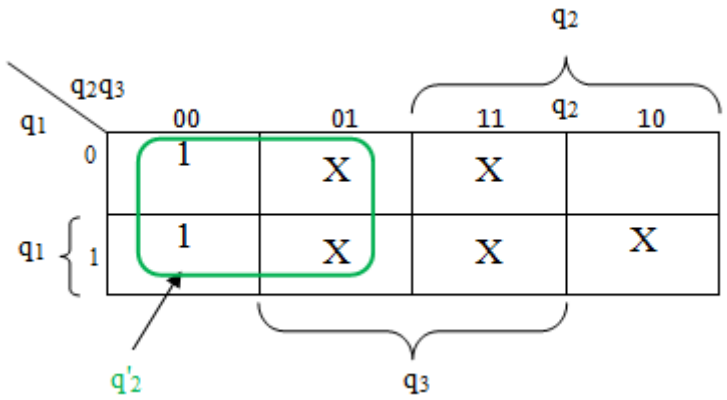


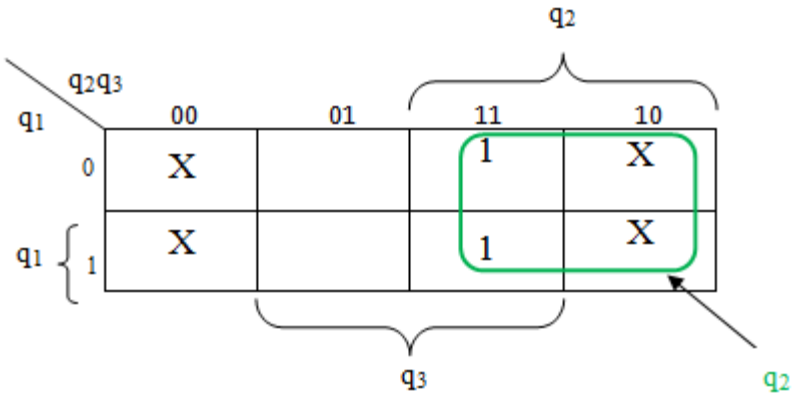
$J_2 = q_1 q_3 + q'_1 q'_3$



$K_2 = q_1 + q'_3$

Example (Contd...)





$J_3 = q'_2$

$K_3 = q_2$

- The circuit for the required counter using JK-flip flops is as follows:

Example (Contd...)

- Left as an exercise for the students

Dealing with Don't Care States

- We can determine what would happen by assuming we are in state 110.
- Thus, we would put $q_1 = 1$, $q_2 = 1$, and $q_3 = 0$ in the equations of flip flop inputs.
- For example, For D-flip flops, we would get

$$D_1 = q_2'q_3 + q_2q_3' = 00 + 11 = 1$$
$$D_2 = q_1'q_2'q_3' + q_1'q_2q_3 + q_1q_2'q_3 = 001 + 011 + 100 = 0$$
$$D_3 = q_2' = 0$$

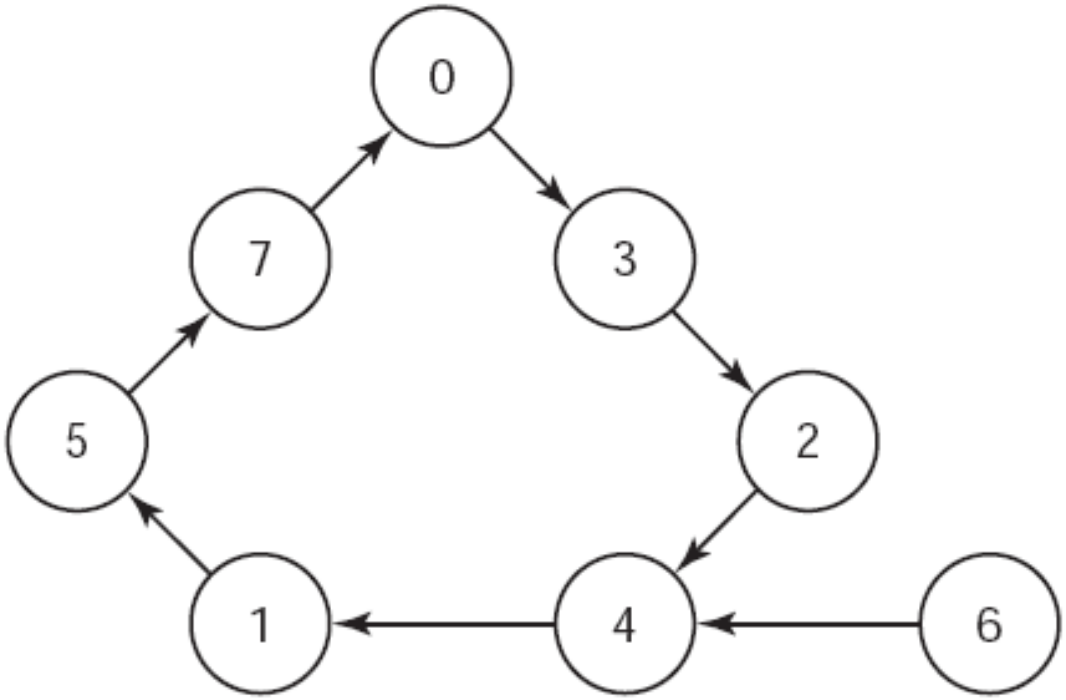
- It means that, the system would go to state 4 (100) on the first clock and continue through the sequence from there.

Note:

- With SR-flip flops, it also goes to state 4, to state 2 with T-flip flops and to state 0 with JK-flip flops.

Dealing with Don’t Care States (Contd...)

- A state diagram, showing the behavior of the system designed with D or SR flip flops, including what happens if the system starts in the unused state, is shown next.



Thanks

Q & A