Makefile

File location:

$VCS_HOME/doc/examples/nativetestbench/systemverilog/vcs_quickstart/Makefile

```
verilog: clean
        vcs +vc -cm line -sverilog fifo_test.v fifo.test_top.v \
           DW_fifo_s1_sf.v DW_fifoctl_s1_sf.v DW_ram_r_w_s_dff.v \
           -debug  \
           +define+ASSERT_ON+COVER_ON \
           -y $(VCS_HOME)/packages/sva/ \
           +libext+.sv \
           +incdir+$(VCS_HOME)/packages/sva
        simv -cm line +NUM+5
        assertCovReport
        vcs -cov_text_report fifo_test.db

vhdl: clean
        mkdir WORK
        vlogan -q -sverilog fifo_test.v
        vlogan -q +vc +define+ASSERT_ON+COVER_ON \
           -sverilog $(VCS_HOME)/packages/sva/assert_fifo.v \
           -y $(VCS_HOME)/packages/sva/ \
           +libext+.v \
           +incdir+$(VCS_HOME)/packages/sva
        vhdlan -q DWpackages.vhd
        vhdlan -q DW_fifo_s1_sf
        vhdlan -q DW_fifo_s1_sf_sim.vhd
        vhdlan -q fifo.test_top.vhd
        scs -cm line tb -debug -mhdl
        scsim -cm line -R -verilog "+NUM+50"
        assertCovReport -cm_assert_dir scsim.db.dir/simv.o.vdb/
        vcs -cov_text_report fifo_test.db

clean:
\rm -rf simv* *.log *.vpd *.dump csrc *.sim *.mra *.log ucli.key session* *.db vcs.key urgRe
```