# README

File location:

$VCS_HOME/doc/examples/nativetestbench/systemverilog/vcs_quickstart/README

```
////////////////////////////////////
//
//  FIFO example for Quickstart VCS2005.06
//
////////////////////////////////////

To run Verilog version: make verilog
To run VHDL version : make vhdl

Please see vcs_quickstart.pdf Guide in $VCS_HOME/doc directory

FILES:

   DW_fifo_s1_sf.v    Verilog FIFO model
        DW_fifoctl_s1_sf.v   Verilog FIFO controller
        DW_ram_r_w_s_dff.v   Verilog memory

        DW_fifo_s1_sf.vhd      VHDL FIFO entity
        DW_fifo_s1_sf_sim.vhd  VHDL FIFO architecture
        DWpackages.vhd         VHDL packages

        synopsys_sim.setup     Setup file


  fifo.test_top.v     Verilog top level instantiating program and testbench
  fifo.test_top.vhd   VHDL top level instantiating program and testbench
        fifo_test.v         program testbench
```