fifo.test_top.v

File location:

$VCS_HOME/doc/examples/nativetestbench/systemverilog/vcs_quickstart/fifo.test_top.v

```
/*************************************************************
 *                        Chronologic VCS (TM)                *
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 *                                                            *
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 *************************************************************/
module fifo_test_top;
  parameter CLOCK_CYCLE = 100 ;
  parameter WIDTH =     16;        // 16 bit data width
  parameter DEPTH =    128;
  parameter ae_level =   3; // words below which almost_empty
  parameter af_level = 120; // words above which almost_full
  parameter err_mode = 0;
  parameter rst_mode = 1;
  reg   clk;
  wire rst_n;
  wire push_req_n;
  wire pop_req_n;
  wire diag_n;
  wire [WIDTH-1 : 0] data_in;
  wire empty;
  wire almost_empty;
  wire half_full;
  wire almost_full;
  wire full;
  wire error;
  wire [WIDTH-1 : 0] data_out;

  //program instantiation
  fifo_test test(.rst_n(rst_n),
                 .clk(clk),
                 .data_in(data_in),
                 .data_out(data_out),
                 .push_req_n(push_req_n),
                 .pop_req_n(pop_req_n),
```

```
                .diag_n(diag_n),
                .full(full),
                .empty(empty),
                .almost_empty(almost_empty),
                .almost_full(almost_full),
                .error(error),
                .half_full(half_full)
                );
  DW_fifo_s1_sf #(WIDTH,  DEPTH,  ae_level,  af_level,  err_mode,  rst_mode)
    dut (.clk(clk),
        .rst_n(rst_n),
        .push_req_n(push_req_n),
        .pop_req_n(pop_req_n),
        .diag_n(diag_n),
        .data_in(data_in),
        .empty(empty),
        .almost_empty(almost_empty),
        .half_full(half_full),
        .almost_full(almost_full),
        .full(full),
        .error(error),
        .data_out(data_out) );
   assert_fifo #(.depth(128), .elem_sz(16), .coverage_level_1(31),
                 .coverage_level_2(0), .coverage_level_3(31) )
     SVA_FIFO_inst (clk, rst_n, !push_req_n, data_in, !pop_req_n, data_out );
  initial begin
    clk = 1'b0;
    forever begin
      #(CLOCK_CYCLE/2)
        clk = ~clk;
    end
  end

endmodule   // fifo_test_top
```