

synopsys_sim.setup

File location:

`$VCS_HOME/doc/examples/nativetestbench/systemverilog/vcs_quickstart/synopsys_sim.setup`

```
WORK      > DEFAULT
DEFAULT   : ./WORK
--DWARE    : ./DWARE

TIMEBASE = NS
CS_ASSERT_STOP_NEXT_WAIT = TRUE
```