YOUNGHUN KIM

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RESEARCH INTERESTS

Memory-Centric Architectures for Accelerator-Rich Systems

- Data Movement, Memory Hierarchy, and Cache Coherence
- Hardware-Software Co-Design for Heterogeneous Systems

EDUCATION

Yonsei University **Seoul, Korea**

B.S., Civil & Environmental Engineering *Mar. 2019 – Feb. 2024*

- CGPA: 4.23/4.30 Major GPA: 4.28/4.30
- Ranked 1/46 Graduated *Summa Cum Laude* (Highest Honors, Top 1% in College of Engineering)

INDEPENDENT PROJECTS

Heterogeneous SoC Memory Contention: Diagnosis & Mitigation **[Github]** *Aug. 2025 – Oct. 2025*

- Established co-run profiling for a heterogeneous SoC (BOOM, Rocket, Gemmini) with a configurable contention stress generator and cycle-accurate, per-tile/per-kernel logging for reproducible interference.
- Diagnosed accelerator slowdowns during co-execution—DRAM bandwidth saturation and L2 bank contention—via sensitivity sweeps across dataflow policies, cache/memory configurations, and contention levels.
- Tuned memory controller parameters (HW) and introduced Phase-Aware Scheduling (SW), boosting system throughput up to 2.7× and improving execution predictability.

Gemmini Offload Thresholds and Memory-Centric Pipeline Co-Design **[Github]** *Jun. 2025 – Aug. 2025*

- Constructed a WS/OS benchmarking framework, sweeping matrix dimensions to compare CPU vs. Gemmini (WS/OS); derived the offload threshold K^* via an automated pipeline.
- Identified two size-dependent bottlenecks: fixed data-movement and launch overheads underutilized the accelerator at small sizes; bandwidth and tiling limits eroded efficiency at large sizes.
- Optimized the memory pipeline: SPM/ACC re-banked/resized, system bus beat-width widening, DMA bus-width alignment, WS/OS auto-selection, lowering K^* and improving reuse/throughput (+58% at M = N = K = 1024).
- Validated analyses/optimizations on FireSim (AWS F1), an FPGA-based HW-accelerated simulation platform.

SHA3 Accelerator Performance Stabilization in Chipyard **[Github]** *Apr. 2025 – Jun. 2025*

- Integrated a SHA3 RoCC accelerator with Rocket core in Chipyard and implemented an automated benchmarking pipeline across 136 B–544 KB inputs.
- Identified single-bank L2 contention using cycle-accurate profiling in Verilator; accelerator speedup over the software-only baseline fell from 206× to 120× as input size increased.
- Redesigned the inclusive L2 into a multi-bank structure, expanding capacity and sub-banking concurrency; achieved +34% throughput at large inputs and stabilized efficiency across scales.

Hardware-Accelerated AES on an FPGA-Based RISC-V SoC *Mar. 2025 – Apr. 2025*

- Engineered a custom AES instruction in VexRiscv and enabled OpenSSL via a Buildroot patch, establishing a Linux-on-FPGA environment for hardware–software co-design.
- Analyzed cache behavior across message sizes and applied cache-line alignment to utilize the hardware AES data-path, achieving 4× throughput over software-only OpenSSL.

RESEARCH EXPERIENCE

Berify, Inc. (bitcoin hardware wallet startup; incorporated Nov. 2024) **Yongin, Korea**
Co-Founder & Systems Architect *May 2024 – Present*

- Developed/implemented secure device software with localization (i18n) stack and custom key/entropy utilities; reproduced and resolved translation regressions to enhance stability.
- Systematized an air-gapped release and installation workflow with offline SHA-256/GPG verification and USB-OTG/UART flashing checklists, ensuring reproducible, audit-ready environments.
- Architected a hardened entropy pipeline, transitioning from software multi-source and SoC HWRNG to external TRNG; achieved ~140× throughput (≈350 kbit/s) and verified via automated NIST SP 800-90B/Dieharder testing.
- Designed bit-for-bit reproducible OS build and release system (Buildroot external in Docker) with CI automation for image builds and SHA-256 hash verification; established an emulator-first integration workflow.
- Engineered a battery-backed power subsystem (TP4056 charger, UPS HAT) with integrated digital power control.

Environmental Hydrodynamics Lab, Yonsei University **Seoul, Korea**
Full-time Researcher (Advisor: Prof. Sung-Uk Choi) *Feb. 2024 – Mar. 2024*

- Developed a MATLAB pipeline for surface-velocity-only discharge estimation using Maximum Entropy Method (MEM), including numerical parameter estimation.
- Reproduced the Shimada Bridge STIV+MEM case end-to-end and validated the pipeline against published results.
- Applied the pipeline to KICT Andong field data (ADV/LSPIV + cross-section), estimating discharge against ADCP ground truth (best MAPE 9.1%, average 21.9%).
- Computed and validated lateral velocity distributions on a Han River cross-section using a depth-integrated, RANS-based Lateral Distribution Method (finite-difference matrix formulation).

Advanced Infrastructure Management Group, Yonsei University **Seoul, Korea**
Undergraduate Intern (Advisor: Prof. Hyoungkwan Kim) *Feb. 2023 – Jul. 2023*

- Labeled 190 scaffolding safety-net images (LabelImg); led discussion on speed-accuracy tradeoffs, mixed-quality train/test splits, and model-assisted pre-labeling (human-in-the-loop).
- Synthesized insights from 8 papers on 3D-to-2D projection and 3D point cloud-2D image fusion into experiment-ready method briefs; reviewed YOLO-based CNNs and simulation-driven robotic construction automation.
- Delivered paper reviews summarizing methods, datasets, and metrics; presented four research briefings synthesizing findings and recommendations.

Department of Civil & Environmental Engineering, Yonsei University **Seoul, Korea**
"High-Rise Piled Raft Foundation Optimization" *Mar. 2023 – Aug. 2023*

- Optimized foundation design for a 50-story tower (56→20 piles), achieving ~67% reduction in concrete volume.
- Presented findings at the 8th Mooyoung CM National Undergraduate Competition.

"Structural Vibration & Earthquake Engineering" *May 2023*

- Implemented MATLAB time-integration solvers and benchmarked stability, accuracy, and runtime trade-offs.

HONORS & SCHOLARSHIPS

Commendation for Academic Excellence, Korean Society of Civil Engineers (KSCE) *Feb. 2024*
Jinri Merit-based Scholarship, Yonsei College of Engineering (6 semesters) *2020 – 2023*
Highest Honors (Top 1%), Yonsei College of Engineering (5 semesters) *2019 – 2023*
High Honors (Top 3%), Yonsei College of Engineering *Aug. 2023*
Honorable Mention, Mooyoung National Undergraduate Construction Management Competition *Aug. 2023*
Honors (Top 10%), Yonsei College of Engineering *Aug. 2020*

WORKSHOPS & ONLINE COURSEWORK

Managing Specialized and Heterogeneous Architectures Workshop, UC Berkeley *Nov. 2025*
MICRO 2025 Workshops & Tutorials *Oct. 2025*
Computer System Design: Advanced Concepts of Modern Microprocessors, Chalmers University (edX) *Oct. 2025*
Algorithmic Foundations for Emerging Computing Technologies Boot Camp, UC Berkeley *Sep. 2025*
Computer Architecture, Princeton University (Coursera) *Sep. 2025*
Hardware Description Languages for FPGA Design, CU Boulder (Coursera) *Sep. 2025*

COMMUNITY ACTIVITIES

Member, Association for Computing Machinery (ACM) *Sep. 2025 – Present*

Social Service Agent, Yongsan-gu District Office, Seoul, Korea *Jun. 2024 – Present*

- Provide administrative support across multiple departments as an alternative military service worker.
- Assisted the Gender Equality Team (Family Policy Division) in planning and executing Gender Equality Week and other public outreach events.
- Supported the Civil Administration/Defense Team during Ulchi exercises and civil defense trainings; recognized with special leave for outstanding contribution.
- Served as team leader during basic training at the Social Service Training Center and received a Certificate of Commendation (Jul. 2024).

Volunteer Math Tutor, Yonsei Red Cross *Mar. 2021 – Dec. 2022*

- Taught weekly two-hour math sessions to 2-3 students at Seongsan Church-affiliated local children's center.
- Improved students' homework completion, test readiness, and academic performance, including an increase of ≈20 points on a 100-point exam after two semesters.

Team Lead & Mentor, Yonsei University Middle-School Mentoring Camp *Sep. 2019 – Nov. 2019*

- Led a 10-mentor team, coordinating a 2-month cycle including scheduling, content design, and activity planning.
- Conducted an 8-hour mentoring camp focusing on career-exploration sessions and campus engagement.

TECHNICAL SKILLS

Programming & Systems: Python, C/C++, MATLAB, Linux, Docker, Git/CI/CD
RISC-V & Accelerator Stacks: Chipyard, RoCC, Gemmini, FireSim, LiteX/VexRiscv, Vortex, FPGA (Xilinx)
RTL/EDA & HW-SW Co-Design: Verilog/SystemVerilog, Scala/Chisel, Vivado, Verilator, Yosys, LLVM/Clang
Embedded & Security Systems: Buildroot, OpenSSL, libsodium, AES, SHA-2/3, GPG, TRNG/HWRNG, NIST SP 800-90B, Dieharder